Keysight D9050LDDC LPDDR5 Test Application



Methods of Implementation

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Contents

1 Overview

LPDDR5 Automated Testing–At a Glance / 10 Required Equipment and Software / 11 Hardware / 11 Software / 12 Licensing information / 12 In This Book / 13 See Also / 13

2 Installing the Test Application and Licenses

Installing the Test Application / 16 Installing the License Key / 17 Using Keysight License Manager 5 / 17 Using Keysight License Manager 6 / 18

3 Preparing to Take Measurements

Calibrating the Oscilloscope / 22 Starting the LPDDR5 Test Application / 23 Configuring Set Up tab for availability of specific tests / 25

4 Electrical Tests

RDQS Detect Method for Read Write Separation / 32 Tests that support the RDQS Detect Burst Identification Method / 33 Method of Implementation for the RDQS Detect Burst Identification Method / 33

Data tests / 34

Overshoot_Amplitude_DQ / 34 Undershoot_Amplitude_DQ / 37 Overshoot_Area_DQ / 39 Undershoot_Area_DQ / 41 SRQseR_DQ / 43 SRQseF_DQ / 44

Command/Address tests / 45 Overshoot_Amplitude_CA / 45 Undershoot_Amplitude_CA / 47 Overshoot_Area_CA / 49 Undershoot_Area_CA / 51 Chip Select tests / 53 Overshoot_Amplitude_CS / 53 Undershoot_Amplitude_CS / 55 Overshoot_Area_CS / 57 Undershoot_Area_CS / 59 Clock (Diff) Tests / 61 Vindiff_CK / 62 Vindiff_CK/2HighPulse / 63 Vindiff_CK/2LowPulse / 64 VIHdiff_CK / 65 VILdiff_CK / 66 SRIdiffR_CK / 67 SRIdiffF_CK / 68 Vinse_CK (Positive Pulse) / 69 Vinse_CK (Negative Pulse) / 71 Write Clock (Diff) Tests / 72 Vindiff_WCK / 73 Vindiff_WCK/2HighPulse / 74 Vindiff_WCK/2LowPulse / 75 VIHdiff_WCK / 76 VILdiff_WCK / 77 SRIdiffR_WCK / 78 SRIdiffF_WCK / 79 Vinse_WCK (Positive Pulse) / 80 Vinse_WCK (Negative Pulse) / 82 Clock (SE Mode) Tests / 84 Vinse_CK_SE / 84 Vinse_CK_SE_High / 86 Vinse_CK_SE_Low / 87 SRIseR_CKSE / 88 SRIseF_CKSE / 90

Write Clock (SE Mode) Tests / 91 Vinse_WCK_SE / 91 Vinse_WCK_SE_High / 93 Vinse_WCK_SE_Low / 94 SRIseR_WCKSE / 95 SRIseF_WCKSE / 97 Clock (SE) CK t (Clock Plus) tests / 98 Overshoot Amplitude CK t / 98 Undershoot_Amplitude_CK_t / 100 Overshoot_Area_CK_t / 102 Undershoot_Area_CK_t / 104 Vinse CK High (CK t) / 106 Vinse_CK_Low (CK_t) / 108 Clock (SE) CK c (Clock Minus) tests / 109 Overshoot_Amplitude_CK_c / 109 Undershoot Amplitude CK c / 111 Overshoot_Area_CK_c / 113 Undershoot_Area_CK_c / 115 Vinse_CK_High (CK_c) / 117 Vinse_CK_Low (CK_c) / 119 Clock (SE) CK t & CK c (Clock Plus & Minus) tests / 120 Vix_CK_ratio / 120 Write Clock (SE) WCK t (Write Clock Plus) tests / 122 Overshoot Amplitude WCK t / 122 Undershoot_Amplitude_WCK_t / 124 Overshoot_Area_WCK_t / 126 Undershoot Area WCK t / 128 Vinse_WCK_High (WCK_t) / 130 Vinse_WCK_Low (WCK_t) / 131 Write Clock (SE) WCK c (Write Clock Minus) tests / 132 Overshoot Amplitude WCK c / 132 Undershoot_Amplitude_WCK_c / 134 Overshoot_Area_WCK_c / 136 Undershoot_Area_WCK_c / 138 Vinse_WCK_High (WCK_c) / 140 Vinse_WCK_Low (WCK_c) / 142 Write Clock (SE) WCK t & WCK c (Write Clock Plus & Minus) tests / 143 Vix_WCK_ratio / 143

Read Data Strobe (Diff) tests / 145 SRQdiffR_RDQS / 145 SRQdiffF_RDQS / 147
Read Data Strobe (SE) RDQS_t (Read Data Strobe Plus) tests / 148 Overshoot_Amplitude_RDQS_t / 148 Undershoot_Amplitude_RDQS_t / 150 Overshoot_Area_RDQS_t / 152 Undershoot_Area_RDQS_t / 154
Read Data Strobe (SE) RDQS_c (Read Data Strobe Minus) tests / 156 Overshoot_Amplitude_RDQS_c / 156 Undershoot_Amplitude_RDQS_c / 158 Overshoot_Area_RDQS_c / 160 Undershoot_Area_RDQS_c / 162

5 Timing Tests

RDQS Detect Method for Read Write Separation / 166 Tests that support the RDQS Detect Burst Identification Method / 167 Method of Implementation for the RDQS Detect Burst Identification Method / 167

Clock (Diff) Tests / 168 tCK(avg) Average Clock Period / 169 tCK(abs) Absolute Clock Period / 170 tCH(avg) Average High pulse width / 171 tCL(avg) Average Low pulse width / 172 tCH(abs) Absolute HIGH Clock pulse width / 173 tCL(abs) Absolute LOW Clock pulse width / 174 tjit(CC) Maximum Clock Jitter between consecutive cycles / 175 tjit(per) Clock period jitter / 176

Clock (SE Mode) Tests / 177 tCKHL / 177

tCKH / 178 tCKL / 179 Write Clock (Diff) tests / 180 tWCK(avg) Average Write Clock period / 181 tWCK(abs) Absolute Write Clock period / 182 tWCKH(avg) Average High pulse width / 183 tWCKL(avg) Average Low pulse width / 184 tWCKH(abs) Absolute HIGH Write Clock pulse width / 185 tWCKL(abs) Absolute LOW Write Clock pulse width / 186 tjit(CC) Maximum Write Clock Jitter between consecutive cycles / 187 tjit(per) Write Clock period jitter / 188 tERR(2per) Write Clock Cumulative error across 2 cycles / 189 tERR(3per) Write Clock Cumulative error across 3 cycles / 190 tERR(4per) Write Clock Cumulative error across 4 cycles / 191 Write Clock (SE Mode) Tests / 192 tWCKHL / 192 tWCKH / 193 tWCKL / 194 Other timing tests / 195

tWCK2CK / 195 tRPRE / 196 tRPST / 197 tDQSQ / 198 tQSH / 199 tQSL / 200

6 Eye Diagram Tests

RDQS Detect Method for Read Write Separation / 202

Tests that support the RDQS Detect Burst Identification Method / 203

Method of Implementation for the RDQS Detect Burst Identification Method / 203

References for DQ Rx Voltage and Timing tests / 204

DQ Rx Voltage and Timing (WRITE) tests / 206

tDIVW1 Margin / 206 tDIVW2 Margin / 207 vDIVW Margin / 209 tDIPW / 210 tDIHL / 211 vDIHL_AC / 212 tWCK2DQI_HF / 213 DQ Rx Voltage and Timing (READ) tests / 216 tQW / 216 tWCK2DQ0_HF / 217 References for CA Rx Voltage and Timing tests / 219 CA Rx Voltage and Timing tests / 221 tCIVW1 Margin / 221 tCIVW2 Margin / 222 vCIVW Margin / 224 tCIPW / 225 vCIHL_AC / 226 tCA2CA / 227 References for CS Rx Voltage and Timing tests / 229 CS Rx Voltage and Timing tests / 231 tCSIVW1 Margin / 231 tCSIVW2 Margin / 232 vCSIVW Margin / 234 tCSIPW / 235 vCSIHL_AC / 236

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

1 Overview

LPDDR5 Automated Testing—At a Glance 10 Required Equipment and Software 11 In This Book 13



LPDDR5 Automated Testing-At a Glance

The Keysight D9050LDDC LPDDR5 Test Application helps you verify compliance of the SDRAM type (LPDDR5) to the respective JEDEC specifications using a supported Keysight Infiniium Oscilloscope. The Keysight D9050LDDC LPDDR5 Test Application:

- · Lets you select individual or multiple tests to run.
- · Lets you identify the device being tested and its configuration.
- · Shows you how to make oscilloscope connections to the device under test.
- · Automatically checks for proper oscilloscope configuration.
- · Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- · Creates a printable HTML report of the tests that have been run.

NOTE

The tests performed by the Keysight D9050LDDC LPDDR5 Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

For each SDRAM type being tested, you may refer to the following specification documents for compliance testing measurements. For more information, see the JEDEC website: https://www.jedec.org/.

SDRAM Type	Reference Documents
LPDDR5	JEDEC Standard, LPDDR5, JESD209-5, February 2019

Required Equipment and Software

In order to run the LPDDR5 automated tests, you need the following equipment and software:

Hardware

- Use one of the following Oscilloscope models. Refer to www.keysight.com for the respective bandwidth ranges.
 - Keysight DSO9000A-Series, DSO90000A-Series and DSOX90000A/Q/Z/V-Series Oscilloscopes with a minimum bandwidth of 8GHz (recommended) for accurate measurements. For faster speed grade devices, a minimum bandwidth of 13GHz bandwidth is recommended.
 - Keysight UXR Oscilloscopes
- Target Device Under Test (DUT)
- InfiniiMax probe amplifiers:
 - N1169A 12GHz InfiniiMax II probe amplifier
 - · N2803A 30GHz InfiniiMax III probe amplifier
 - N2802A 25GHz InfiniiMax III probe amplifier
 - · N2801A 20GHz InfiniiMax III probe amplifier
 - N2800A 16GHz InfiniiMax III probe amplifier
 - N2831A 8GHz InfiniiMax III probe amplifier
 - · N2832A 12GHz InfiniiMax III probe amplifier
- InfiniiMax probe heads InfiniiMax I/II probe heads and accessories (compatible with 9000 Series and 90000 Series, use N5442A precision BNC adapter with 90000X/Q Series):
 - N5381A InfiniiMax II 12GHz differential solder-in probe head and accessories
 - N5382A InfiniiMax II 12GHz differential browser
 - E2677A InfiniiMax II 12GHz differential solder-in probe head and accessories
 - · N5425A InfiniiMax II 12GHz ZIF probe head
 - N5426A InfiniiMax II ZIF tips (×10)
- · InfiniiMax III probe heads and accessories:
 - N5451A Long Wire tips (×10)
 - N5439A ZIF probe head
 - N5445A Browser (hand held) probe head
 - N5441A Solder-in probe head
 - N2838A 450 Ω PCB ZIF tips (set of 5)
 - · N2848A InfiniiMax III QuickTip head
 - · N2849A InfiniiMax III Quick tips (4 per kit)
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, gty = 1, (provided with the Keysight Infinitum oscilloscope)
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2 (provided with the Keysight 54855A and 80000B series oscilloscopes)
- 50-ohm Coax Cable with SMA Male Connectors 24-inch or less RG-316/U or similar, qty = 2, matched length
- Keysight also recommends using a second monitor to view the test application.

Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight D9050LDDC LPDDR5 Test Application Release Notes)
- Keysight D9050LDDC LPDDR5 Test Application software
- Keysight E2688A Serial Data Analysis and Clock Recovery software (for clock recovery)

Licensing information

Refer to the *Data Sheet* pertaining to LPDDR5 Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9050LDDC" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 17 to see the difference in installing a license key using either of the applications on your machine.

In This Book

This manual describes the tests that are performed by the Keysight D9050LDDC LPDDR5 Test Application in more detail; it contains information from (and refers to) the LPDDR5 specification and it describes how the tests are performed.

- Chapter 1, "Overview" gives an overview of the automated test application and the required equipment and software.
- Chapter 2, "Installing the Test Application and Licenses" explains how to obtain the installer for
 the automated test application and install the associated licenses (if it was purchased separately).
- Chapter 3, "Preparing to Take Measurements" describes how to launch the Keysight D9050LDDC LPDDR5 Test Application and gives a brief overview of how it is used.
- Chapter 4, "Electrical Tests" describes the methods of implementation for WRITE and READ cycle electrical tests performed on LPDDR5 devices.
- Chapter 5, "Timing Tests" describes the methods of implementation for timing tests performed on LPDDR5 devices.
- Chapter 6, "Eye Diagram Tests" describes the methods of implementation for eye diagram tests
 performed on LPDDR5 devices.

See Also

The Keysight D9050LDDC LPDDR5 Test Application's Online Help, which describes:

- Starting the LPDDR5 Test Application
- · Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- · Additional Settings in the Test App

1 Overview

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

2 Installing the Test Application and Licenses

Installing the Test Application 16 Installing the License Key 17

If you purchased the D9050LDDC LPDDR5 Test Application separate from your Infiniium oscilloscope, you must install the software and license key.



Installing the Test Application

- 1 Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9050LDDC release notes). To ensure that you have the minimum version, select Help > About Infiniium... from the main menu.
- 2 To obtain the LPDDR5 Test Application, go to Keysight website: "http://www.keysight.com/find/D9050LDDC".
- 3 In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

- 1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.
- 2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

-	Keysig	nt License <mark>Manage</mark> r	
		Licenses on	(localhost) 🔿
Conn		Full computer name:	.msr.is.keysight.com
ectio		Host ID:	PCSERNO, JBXXXXXXX
ns			

Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

- 1 Save the license files on the machine, where you wish to run the Test Application and its features.
- 2 Launch Keysight License Manager.
- 3 From the configuration menu, use one of the options to install each license file.

3 2 - □ ×	
Why do I need these tools?	
Install License File	Ctrl+I
Install License from Text	Ctrl+T
View License Alerts Ctrl+L	
Explore Transport URLs	
About Keysight License Manager	

Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

- 1 Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
- 2 Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

Keysight License	Manager 6	
Home	Licensing Version	= Keysight License Manager Ver: 6.0.3 Date: Nov 9 2018
	Copyright	= © Keysight Technologies 2000-2018
Environment	AGILEESOFD SERVER CONFIG	_
	AGILEESOFD SERVER LOGFILE	= C:\ProgramData\Keysight\Licensing\Log\
View licenses		
	SERVER_LICENSE_FILE	
License usage	AGILEESOFD_LICENSE_FILE	= <u>C:\ProgramData\Keysight\Licensing\Licenses\Other</u> C:\ProgramData\Keysight
	FLO_LICENSE_FILE	= <u>C:\ProgramData\Keysight\Licensing\Licenses\Other;C:\ProgramData\Keysight</u>
Borrow license	KAL_LICENSE_FILE	= C:\ProgramData\Keysight\Licensing\Licenses\Other;C:\ProgramData\Keysight
	AGILEESOFD_DEBUG_MODE FLEXLM TIMEOUT	=
	THERE IN THE OUT	
	Default Hostid	= XXXXadXXXXbe XXbaXeaceXee
	Ethernet Address	= XXXXadXXXXbe XXbaXeaceXee
	DID	
	Physical MAC Address	= XXXXadXXXXbe PHY_ETHER=XXbaXeaceXee
	IP Address Computer/Hostname	= 127.0.0.1
	Computer/Hostname Username	
	0 SELMANE	
	PATH	= C:\Program Files (x86)\Common Files\Intel\Shared Libraries\redist\intel6
		1.
	💟 Compact View	
		<u>R</u> efresh <u>Close</u> <u>H</u> elp

Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

- 1 Save the license files on the machine, where you wish to run the Test Application and its features.
- 2 Launch Keysight License Manager 6.
- 3 From the Home tab, use one of the options to install each license file.

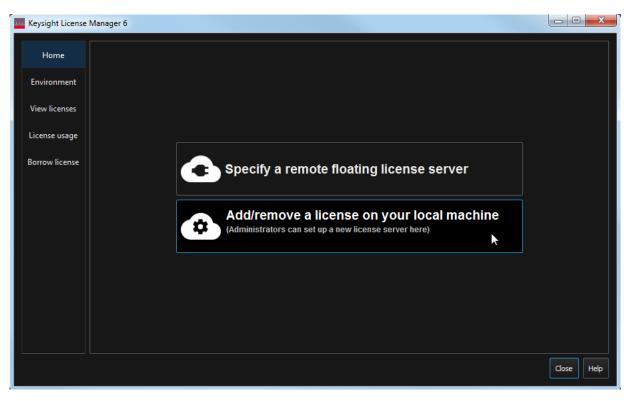


Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

2 Installing the Test Application and Licenses

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

3

Preparing to Take Measurements

Calibrating the Oscilloscope 22 Starting the LPDDR5 Test Application 23

Before running the automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the LPDDR5 Test Application and perform the measurements.



Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.



If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.



If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the LPDDR5 Test Application

1 Ensure that the LPDDR5 Device Under Test (DUT) is operating and set to desired test modes. To start the LPDDR5 Test Application: From the Infiniium Oscilloscope's main menu, select Analyze > Automated Test Apps > D9050LDDC LPDDR5 Test App.

₹	LPDDR5 Test LPDDR5 Device 1												
Fi	File View Tools Help												
S	Set Up Select Tests Configure Connect Run Automate Results HTML Report												
				LPDD	R5 Tes	st Envi	ronm	ent Setup					
	Gen	eral Settings -					Sign	al Source	Setting	js ——			
		t Mode						Diff) (Live))				
	Liv	/e Signal					Cha	annel1					
	Dat	a Rate [MT/s]	WCK	Frequency	[MHz]		WC	(Diff) (Liv	re)				
	32	00	160	0			Cha	annel2					
	wc	K:CK Ratio	Cloc	k Frequency	[MHz]		DQ	(Live)					
	2:	1	800				Cha	annel3					
SE	Ava	ilable Signal Sou	rce				CA (Live)					
Ξ	Ck	((Diff), WCK (Dif	f), DQ, CA				Cha	annel4					
υp													
Р													
Settings Source			e)	Thresho	lds								
	lest	Report Comm	ents (Optioi	nal) ——									
					_	_	_				_		
	lessag				_	_		D-1-11-	_		_		
S		aries (click for -07-19 09:01:0			ort Dof	reched	_	Details Application	on initia	alized ar	nd read	dy for us	
≻		-07-19 09:01:0 -07-19 09:01:0		<u> </u>	JTL REI	esneu		Application			ia real	ay tor us	
GE							V						
	0 Test	ts											

Figure 5 LPDDR5 Test Application Main Window

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9050LDDC LPDDR5 Test Application Online Help* available in the Help menu.

Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

NOTE

In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application. Configuring Set Up tab for availability of specific tests

The **Set Up** tab consists of configuration options that correspond to the LPDDR5 device under test (DUT). Select the appropriate options for the relevant tests to appear.

The configuration options specified in the previous table can be set in specific areas of the LPDDR5 Test Application:

• LPDDR5 General Setup—Configure parameters specific to the DUT. To access this window, click Settings... under the Set Up tab.

LPDDR5 General Setup)	? (=)×)		
Test Mode				
🔵 Live Signal 🌔	Offline			
Data Rate				
3200 🔽 МТ	T/s JEDEC standard values			
WCK : CK Ratio 2:	1 VCK Frequency : 1600 MHz Clock Frequency : 800 MHz			
Signal Source				
CK (Diff), WCK (Dif	f), DQ, RDQS (Diff)			
Single-Ended N	lode			
Signal Operation Mod	de			
CK (Diff) Burst				
WCK (Diff) Burst	Burst WCK optio	ns		
RDQS Preamble/Post	amble Length			
RDQS Preamble	Static: 4 tWCK, Toggle: 0 tWCK			
RDQS Postamble	0.5 tWCK			
RDQS Postamble Mode Toggle				
WCK Postamble Length				
WCK Postamble 2.5 tWCK				
Show Hints OK Close				

Figure 6 General Settings under Set Up tab

- **Test Mode**—select whether to run tests on a live signal (with DUT connected) or on offline signal (saved waveforms).
- **Data Rate**—select the speed grade for test signal transmission and the frequency ratio for Write Clock (WCK) and Clock (CK) signal.
- **Signal Source**—Select the combination of signals for the corresponding LPDDR5 tests to appear in the Select Tests tab.
- **Signal Operation Mode**—select whether the differential clock and differential write clock signals will be transmitted in either continuous or burst modes. For WCK bursts, you may select the read/write separation technique.

- **RDQS Preamble/Postamble Length**—Select the length of RDQS preamble and postamble when RDQS (Diff) is selected as one of the test signals.
- WCK Postamble Length—Select the length of WCK postamble when WCK (Diff) is selected as one of the test signals.

- Signal Source Setup-To access this window, click Source... under the Set Up tab.
 - For Live Signal Test Mode, assign Oscilloscope Channels to each signal selected under Signal Source.

Signal Source Setup		? X
Available Live Signal(s	;) ——	
CK (Diff)	Channel1	$\mathbf{\overline{v}}$
WCK (Diff)	Channel2	\mathbf{Y}
DQ	Channel3	\mathbf{v}
СА	Channel4	\mathbf{v}
Show Hints	(OK Close

Figure 7 Signal Source Settings under Set Up tab

• For **Offline** Test Mode, click **Browse...** against each signal type and select the offline waveform file in *wfm* format.

	Signal Source	e Setup	? _ X
	Available O	ffline Signal(s)	
I	CK (Diff)	NA	Browse
I	WCK (Diff)	NA	Browse
I	DQ	NA	Browse
I	CA	NA	Browse
I			
I			
I			
	Show H	ints	OK Close

Figure 8

Signal Source Settings under Set Up tab

- Threshold Setup–To access this window, click Thresholds... under the Set Up tab.
 - Under **Signal Thresholds** tab, verify or modify the upper, middle and lower threshold values for each selected **Signal Source** type.

Threshold Setup	?
Signal Thresholds Measurement Thresholds	
Rud Burk High Ingedance Midde With Burk CK (Diff) Upper Threshold Upper Threshold (V) DQ Upper Threshold (V) 0.145 CA Widde Threshold (V) 0 Lower Threshold (V) 0.145 Upper Threshold (V) 0 V 0 Lower Threshold (V) 0.145 V	Read Bure High Inpuddinio Vinza Buret Meda Antifa Antifa A
Show Hints	OK Close

Figure 9 Signal threshold settings

Under Measurement Thresholds tab, verify or modify the corresponding threshold values required for measurements to be performed on each selected Signal Source type.

Threshold Setup		? - X
Signal Thresholds	Measurement Thresholds	
	VDD VDDQ VH4	llff
CK (Diff)	οφ (V)	
Show Hints		OK Close



Click **OK** to apply and save any changes made to each window for the settings to take effect.

NOTE

The prerequisite Test IDs indicate all such tests that must be run prior to the corresponding tests. It is possible that one or more of the prerequisite tests may not have been selected prior to running the related test. However, the LPDDR5 Test Application automatically runs such tests and displays the resulting values.

3 Preparing to Take Measurements

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

4 Electrical Tests

RDQS Detect Method for Read Write Separation 32 Data tests 34 Command/Address tests 45 Chip Select tests 53 Clock (Diff) Tests 61 Write Clock (Diff) Tests 72 Clock (SE Mode) Tests 84 Write Clock (SE Mode) Tests 91 Clock (SE) CK_t (Clock Plus) tests 98 Clock (SE) CK_c (Clock Minus) tests 109 Clock (SE) CK_t & CK_c (Clock Plus & Minus) tests 120 Write Clock (SE) WCK_t (Write Clock Plus) tests 122 Write Clock (SE) WCK_c (Write Clock Minus) tests 132 Write Clock (SE) WCK_t & WCK_c (Write Clock Plus & Minus) tests 143 Read Data Strobe (Diff) tests 145 Read Data Strobe (SE) RDQS_t (Read Data Strobe Plus) tests 148 Read Data Strobe (SE) RDQS_c (Read Data Strobe Minus) tests 156



RDQS Detect Method for Read Write Separation

RDQS Detect is a read write separation method. This method works when the signal source contains at least an RDQS signal and a WCK signal. In this method, the Read/Write burst data is identified based on the presence of RDQS burst. If WCK burst contains an RDQS burst, then it is a Read burst. If the WCK burst does not contain an RDQS burst, then it is a Write burst.

If you select the RDQS Detect mode as the burst identification method, you must select the length of the WCK Postamble in the WCK Postamble Length section of the LPDDR5 General Setup dialog box.

LPDDR5 General Setup	? 🗆 🗙			
Cat the data rate of the l	A			
3200 🔽 MT,	3200 Y MT/s JEDEC standard values			
WCK : CK Ratio 2:1	WCK : CK Ratio 2:1 VCK Frequency : 1600 MHz Clock Frequency : 800 MHz			
Signal Source	and accurate in such that the state to be the state of the			
	nal source input for the current test trial. This option will test measurements. When the value for this option change, it will be reset.			
WCK_t (SE), WCK_c	(SE), RDQS_t (SE), RDQS_c (SE)			
Single-Ended M				
Signal Operation Mod	e			
	ode of the signal source.			
CK (Diff) Continuou	ntinuous 💉			
WCK (Diff) Burst	Burst WCK options			
RDQS Preamble/Posta	amble Length			
	QS Preamble and Postamble.			
RDQS Preamble	Static: 4 tWCK, Toggle: 0 tWCK			
RDQS Postamble	0.5 tWCK			
RDQS Postamble Mode	RDQS Postamble Mode Toggle			
WCK Postamble Length				
Identify the length of WCK Postamble.				
WCK Postamble	2.5 tWCK			
	2.5 tWCK			
🖌 Show Hints	4.5 tWCK OK Cancel			
	6.5 tWCK			





Figure 12 WCK Burst Options Setup Dialog

Tests that support the RDQS Detect Burst Identification Method

The following Electrical tests support the RDQS Burst Identification method:

WRITE Tests

- Vindiff_WCK
- Vindiff_WCK/2HighPulse
- Vindiff_WCK/2LowPulse
- Vinse_WCK (Positive Pulse)
- Vinse_WCK (Negative Pulse)
- Vinse_WCK_High (WCK_t)
- Vinse_WCK_High (WCK_c)
- Vinse_WCK_Low (WCK_t)
- Vinse_WCK_Low (WCK_c)
- VIHdiff_WCK
- VILdiff_WCK
- SRIdiffR_WCK
- SRIdiffF_WCK
- Vix_WCK_Ratio
- Vinse_WCK_SE
- Vinse_WCK_SE_High
- Vinse_WCK_SE_Low
- SRIseR_WCKSE
- SRIseF_WCKSE

READ Tests

- SRQseR_DQ
- SRQseF_DQ
- SRQdiffR_RDQS
- SRQdiffF_RDQS

Method of Implementation for the RDQS Detect Burst Identification Method

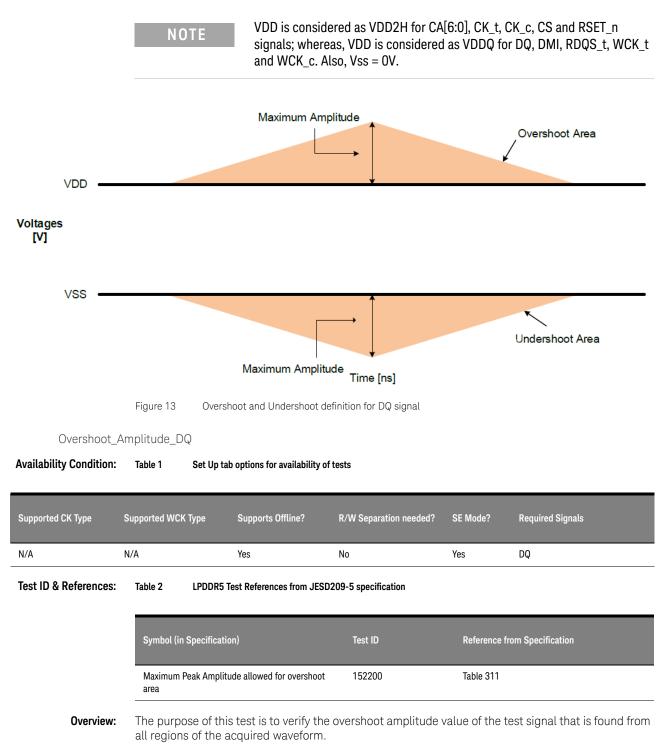
The following are the steps for the method of implementation for the RDQS Detect burst identification method:

- 1 Populate the burst from WCK signal.
- 2 Locate FirstWCKRising for the burst.
- 3 Compute TimeA = FirstWCKRising + tWCKPRE_Toggle_RD * ClockCycleWidth.
- 4 Compute TimeB = Start of WCK postamble. For example, if tWCKPST=2.5nWCK then TimeB = time of second last rising edge of WCK burst. If tWCKPST=4.5nWCK then TimeB = time of fourth last rising edge of WCK burst.
- 5 Compute TimeC = 0.5*(TimeA+TimeB)
- 6 Compute VmaxTimeCWithinUI = Vmax range from (TimeC 1*UI) to (TimeC + 1*UI)
- 7 Compute VminTimeCWithinUI = Vmin range from (TimeC 1*UI) to (TimeC + 1*UI)
- 8 If [(VmaxTimeCWithinUI > VOHDiff_RDQS) AND (VminTimeCWithinUI < VOLDiff_RDQS)] then the burst will be recognized as a READ burst. Otherwise, the burst will be recognized as a WRITE burst.
- 9 Repeat steps 2 to 8 for the rest of burst.

4 Electrical Tests

Data tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 13.



In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},$ V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

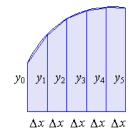
Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_ V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 14 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

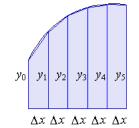
- e To find the worst case, save the following calculated results for later use:
 - · Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Amplitude_DQ

Availability Condition: Table 3 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A	Yes	No	Yes	DQ		
Test ID & References:	Table 4 LPDDF	R5 Test References from JE	SD209-5 specification				
	Symbol (in Specific	ation)	Test ID	Reference	from Specification		
	Maximum Peak Am area	plitude allowed for undersh	oot 152201	Table 311			
Overview:	The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.						
	In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.						
Procedure:	1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).						
	2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.						
	3 Within UndershootRegion # 1:						
	a Evaluate	a Evaluate Undershoot Amplitude by:					
		i Using T _{MIN} , V _{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.					
	ii Calc	ii Calculating Undershoot Amplitude using the equation:					
		Un	dershoot Amplitude = Vs	ss - V _{MIN}			



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg[\operatorname{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_0}{2}\Big)$	$\left(\frac{n}{2}\right)$
---	----------------------------

Figure 15 Equation for Total_Area_Below_Vss

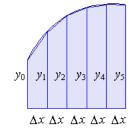
- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_DQ

Availability Condition:	Table 5	Set Up tab options for availability of tests	
-------------------------	---------	--	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	N/A	Yes	No	Yes	DQ			
Test ID & References:	Table 6 LPDDR	Table 6 LPDDR5 Test References from JESD209-5 specification						
	Symbol (in Specific	ation)	Test ID	Reference f	irom Specification			
	Maximum overshoot	area above V _{DD2H} /V _{DDQ}	152202	Table 311				
Overview:		The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.						
		When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.						
Procedure:		1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).						
	An "Oversho	 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing. 						
	3 Within Overs	3 Within OvershootRegion # 1:						
	<i>a</i> Evaluate (a Evaluate Overshoot Amplitude by:						
		g T _{MAX} , V _{MAX} to obta shootRegion.	ain the time-stamp of th	ie maximum	voltage on the			
	ii Calcu	ulate Overshoot Am	olitude using the equation	on:				
		Ove	rshoot Amplitude = V _{MA}	_X - V _{DDQ}				
	b Evaluate A	Area_below_V _{DDQ} us	sing the equation:					
	Area	_below_V _{DDQ} = (Ov	ershootRegion_End - Ov	vershootRegi	on_Start) x V _{DDQ}			
	c Evaluate	otal_Area_Above_0	V by using Trapezoidal N	/lethod Area	Calculation:			



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 16 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

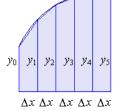
- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Area_DQ

Availability Condition:	Table 7	Set Up tab options for availability of tests
-------------------------	---------	--

N/A	N/A	Yes	No	Yes	DQ	
Test ID & References:	Table 8 LPDDR5	Test References from JES	SD209-5 specification			
	Symbol (in Specificat	ion)	Test ID	Reference f	rom Specification	
	Maximum undershoot	area above VSS	152203	Table 311		
Overview:	The purpose of this test is to verify the undershoot amplitude value of the test signal that is from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.					
Procedure:	1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).					
	 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing. 					
	3 Within UndershootRegion # 1:					
	a Evaluate Undershoot Amplitude by:					
	i Using T _{MIN} , V _{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.					
	ii Calculating Undershoot Amplitude using the equation:					
	Undershoot Amplitude = Vss - V _{MIN}					
	b Evaluate To	tal_Area_Below_Vs	ss by using Trapezoidal	Method Area	Calculation:	



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

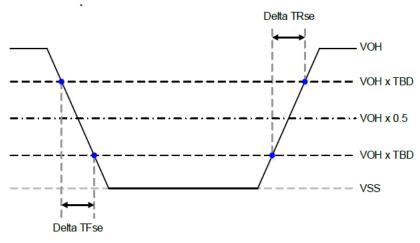
We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

$$ig| \operatorname{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 17 Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JEDEC specification.



Output slew rate for single-ended signals are measured as shown in Figure 18.

Figure 18 Single-ended output slew rate definition for DQ signal

SRQseR_DQ

Availability Condition:	Table 9	Set Up tab options for availability of tests
-------------------------	---------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)

Test ID & References: Table 10

LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
SRQse	150000	Table 325

Overview:

iew: The purpose of this test is to verify the rising slew rate value of the test signal within the read burst.

- **Procedure:** 1 Acquire and split the read and write burst of the acquired signal.
 - 2 Take the first valid READ burst found.
 - 3 Find all the valid rising edges in the specified burst. A valid rising edge starts at $V_{\rm OL}$ crossing and ends at the following $V_{\rm OH}$ crossing.
 - $\begin{array}{ll} 4 & \mbox{For all the valid rising edges, find the transition time, T_R.} \\ & \mbox{T_R}$ is the time starting at V_{OL} crossing and ending at the following V_{OH} crossing.} \end{array}$
 - 5 Calculate SRQseR_DQ using the equation:

 $SRQseR_DQ = [V_{OH} - V_{OL}] / T_R$

6 Determine the worst result from the set of SRQseR_DQ measured.

Expected/ The calculated Rising Slew (SRQseR_DQ) value for the test signal shall be within the conformance limits as per the JEDEC specification.

4 Electrical Tests

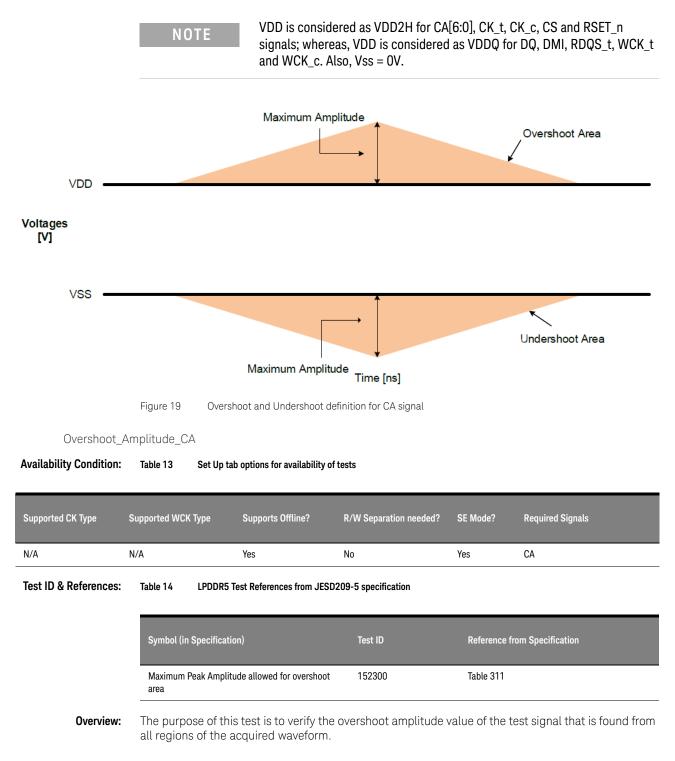
SRQseF_DQ

Availability Condition: Table 11 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)			
Test ID & References:	Table 12 LPDDR5	Test References from JE	SD209-5 specification					
	_							
	Symbol (in Specificat	ion)	Test ID	Reference f	from Specification			
	SRQse		150001 Table 325					
Overview:	The purpose of th	is test is to verify t	he falling slew rate valu	e of the test	signal within the read burst.			
Procedure:	1 Acquire and s	plit the read and w	rite burst of the acquire	d signal.				
	2 Take the first	valid READ burst f	ound.					
		3 Find all the valid falling edges in the specified burst. A valid falling edge starts at V_{OH} crossing and ends at the following V_{OI} crossing.						
	4 For all the val	4 For all the valid falling edges, find the transition time, T_F . T_R is the time starting at V _{OH} crossing and ending at the following V _{OL} crossing.						
	T _R is the time							
	5 Calculate SR	5 Calculate SRQseF_DQ using the equation:						
			SRQseF_DQ = [V _{OH} - V _O	_] / T _F				
	6 Determine the	e worst result from	the set of SRQseF_DQ r	neasured.				
/Expected Observable Results:		Illing Slew (SRQse IEDEC specificatio		signal shall	be within the conformance			

Command/Address tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 19.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

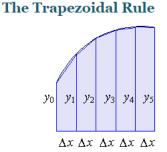
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 20 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

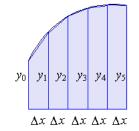
- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Amplitude_CA

Availability Condition: Table 15 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	? SE Mode?	Required Signals	
N/A	N/A	Yes	No	Yes	CA	
Test ID & References:	Table 16 LPDDR	5 Test References from J	IESD209-5 specification			
	Symbol (in Specific	ation)	Test ID	Reference	from Specification	
	Maximum Peak Amp area	litude allowed for unders	hoot 152301	Table 311		
Overview:	from all regions	of the acquired wa	the undershoot amplitu aveform. In case of an u al Method Area Calcula	ndershoot, the	ne test signal that is found e undershoot area is	
Procedure:		uire signal data an e adjustment).	d perform signal condit	ioning to max	imize screen resolution	
	2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the risir of Vss (0V) crossing.					
	3 Within Unde	rshootRegion # 1:				
	a Evaluate l	Jndershoot Amplit	ude by:			
		g T _{MIN} , V _{MIN} to obt ershootRegion.	ain the time-stamp of t	he minimum \	voltage on the	
	ii Calcu	ulating Undershoot	t Amplitude using the e	quation:		
		11				
		01	ndershoot Amplitude =	v 32 - v MIN		



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_0}{2} \Big)$	$\left(\frac{n}{2}\right)$	
--	----------------------------	--

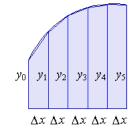
Figure 21 Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - · Overshoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_CA

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CA
Test ID & References:	Table 18 LPDDR	5 Test References from JE	SD209-5 specification		
	Symbol (in Specific	ation)	Test ID	Reference f	from Specification
	Maximum overshoot	area above V _{DD2H} /V _{DDQ}	152302	Table 311	
Overview:		his test is to verify t acquired waveforr		value of the t	test signal that is found from
	When there is o overshoot ampli		noot area is calculated b	ased on the	overshoot width and
Procedure:		uire signal data and e adjustment).	perform signal conditio	ning to maxi	mize screen resolution
	 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge V_{DD2H} crossing. 			d ends at the falling edge of	
	3 Within Overs	hootRegion # 1:			
	<i>a</i> Evaluate (Overshoot Amplitud	e by:		
	i Using T _{MAX} , V _{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.			voltage on the	
	ii Calcu	ılate Overshoot Am	plitude using the equation	on:	
	Overshoot Amplitude = $V_{MAX} - V_{DD2H}$				
	b Evaluate A	Area_below_V _{DD2H} (using the equation:		
	Area_	below_V _{DD2H} = (Ov	ershootRegion_End - O	vershootRegi	on_Start) x V _{DD2H}
	c Evaluate 1	otal_Area_Above_0	IV by using Trapezoidal N	Method Area	Calculation:



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg { m Area}pprox \Delta x \Big({y_0\over 2} + y_1 + y_2 + y_3 + \ldots +$	$\left(\frac{y_n}{2}\right)$
--	------------------------------

Figure 22 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_0V - Area_below_V_{DD2H}

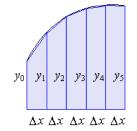
- e To find the worst case, save the following calculated results for later use:
 - · Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Area_CA

Availability Condition:	Table 19	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CA
Test ID & References:	Table 20 LPD	DR5 Test References from JE	SD209-5 specification		
	Symbol (in Speci	fication)	Test ID	Reference f	rom Specification
	Maximum unders	Maximum undershoot area above VSS		Table 311	
Overview:	w: The purpose of this test is to verify from all regions of the acquired way			e value of th	e test signal that is found
	In case of an u undershoot an		shoot area is calculated	based on th	e undershoot width and
Procedure:		quire signal data and	perform signal condition	ning to maxi	mize screen resolution
	(vertical so	ale adjustment).			
	2 Find the "l	JndershootRegion" ac shootRegion" starts a	cross the acquired wavef		and ends at the rising edg
	2 Find the "U An "Under of Vss (0V)	JndershootRegion" ac shootRegion" starts a	cross the acquired wavef		and ends at the rising edg
	2 Find the "l An "Under of Vss (0V)3 Within Under	IndershootRegion" ac shootRegion" starts a crossing.	cross the acquired wavef t the falling edge of Vss (and ends at the rising edg
	 2 Find the "l An "Under of Vss (0V) 3 Within Und a Evaluate i Usi 	IndershootRegion" ac shootRegion" starts a crossing. dershootRegion # 1: e Undershoot Amplitu	cross the acquired wavef t the falling edge of Vss ((OV) crossing	
	 Find the "l An "Under of Vss (0V) Within Und a Evaluate i Usi Un 	JndershootRegion" ac shootRegion" starts a crossing. dershootRegion # 1: e Undershoot Amplitu ng T _{MIN} , V _{MIN} to obta dershootRegion.	cross the acquired wavef t the falling edge of Vss (de by:	(OV) crossing e minimum v	and ends at the rising edg oltage on the
	 Find the "l An "Under of Vss (0V) Within Und a Evaluate i Usi Un 	UndershootRegion" ac shootRegion" starts a crossing. dershootRegion # 1: e Undershoot Amplitu ng T _{MIN} , V _{MIN} to obta dershootRegion. culating Undershoot	cross the acquired wavef t the falling edge of Vss (de by: in the time-stamp of the	(OV) crossing e minimum v lation:	



$$\mathrm{Area}pprox rac{1}{2}(y_0+y_1)\Delta x+rac{1}{2}(y_1+y_2)\Delta x+rac{1}{2}(y_2+y_3)\Delta x+\dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

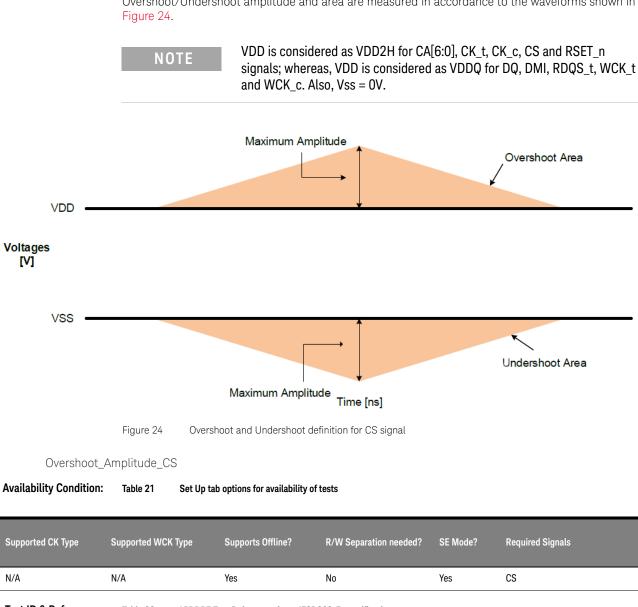
$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 23 Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - · Overshoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JEDEC specification.

Chip Select tests



Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in

Test ID & References: Table 22 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152400	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

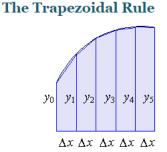
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 25 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

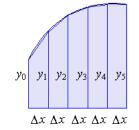
- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Amplitude_CS

Availability Condition: Table 23 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed	? SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CS
Test ID & References:	Table 24 LPDDF	R5 Test References from .	JESD209-5 specification		
	Symbol (in Specific	ation)	Test ID	Reference	from Specification
	Maximum Peak Am area	olitude allowed for unders	shoot 152401	Table 311	
Overview:	from all regions	of the acquired wa	r the undershoot amplit aveform. In case of an u Ial Method Area Calcula	Indershoot, th	he test signal that is found e undershoot area is
Procedure:		uire signal data an le adjustment).	d perform signal condit	tioning to max	imize screen resolution
	 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (OV) crossing and ends at the rising of Vss (OV) crossing. 			g and ends at the rising edge	
3 Within UndershootRegion # 1:					
	a Evaluate	Undershoot Amplit	tude by:		
		g T _{MIN} , V _{MIN} to obt ershootRegion.	tain the time-stamp of t	the minimum	voltage on the
	ii Calculating Undershoot Amplitude using the equation:				
	Undershoot Amplitude = Vss - V _{MIN}				
		U	ndershoot Amplitude =	Vss - V _{MIN}	



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_0}{2} \Big)$	$\left(\frac{n}{2}\right)$	
--	----------------------------	--

Figure 26 Equation for Total_Area_Below_Vss

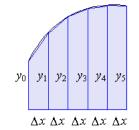
- *c* To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_CS

Availability Condition:	Table 25	Set Up tab options for availability of tests
		eet op ias optione tet aranasing et teete

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	N/A	Yes	No	Yes	CS	
Test ID & References:	Table 26 LPDDF	25 Test References from JE	SD209-5 specification			
	Symbol (in Specific	ation)	Test ID	Reference f	rom Specification	
	Maximum overshoo	t area above V _{DD2H} /V _{DDQ}	152402	Table 311		
Overview:		The purpose of this test is to verify the overshoot amplitude value of the test signal that is found fractional regions of the acquired waveform.			test signal that is found from	
	When there is o overshoot ampli		oot area is calculated b	ased on the	overshoot width and	
Procedure:	1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).					
	 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling V_{DD2H} crossing. 			d ends at the falling edge of		
	3 Within OvershootRegion # 1:					
	a Evaluate	a Evaluate Overshoot Amplitude by:				
	 Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on t OvershootRegion. 		voltage on the			
	ii Calc	ulate Overshoot Amp	olitude using the equation	on:		
	Overshoot Amplitude = V _{MAX} - V _{DD2H}					
	b Evaluate	Area_below_V _{DD2H} u	ising the equation:			
	Area_	_below_V _{DD2H} = (Ove	ershootRegion_End - O\	vershootRegi	on_Start) x V _{DD2H}	
	c Evaluate	otal_Area_Above_0 ^۱	V by using Trapezoidal N			



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg[\operatorname{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_0}{2}igg]$	$\left(\frac{n}{2}\right)$
--	----------------------------

Figure 27 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_0V - Area_below_V_{DD2H}

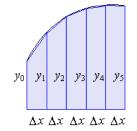
- e To find the worst case, save the following calculated results for later use:
 - · Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Area_CS

Availability Condition:	Table 27	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	N/A	Yes	No	Yes	CS	
Test ID & References:	Table 28 LPI	DDR5 Test References from JE	SD209-5 specification			
	Symbol (in Spec	ification)	Test ID	Reference f	from Specification	
	Maximum under	shoot area above VSS	152403	Table 311		
Overview:		The purpose of this test is to verify the undershoot amplitude value of the test signal that is foun from all regions of the acquired waveform.				
		In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.				
Procedure:		cquire signal data anc cale adjustment).	perform signal condition	ning to maxi	mize screen resolution	
	 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (OV) crossing and ends at the rising ed of Vss (OV) crossing. 					
				(OV) crossing	and ends at the rising edg	
	of Vss (OV			(OV) crossing	and ends at the rising edg	
	of Vss (OV 3 Within Ur) crossing.	t the falling edge of Vss ((OV) crossing	g and ends at the rising edg	
	of Vss (OV 3 Within Ur a Evaluat i Us) crossing. IdershootRegion # 1: Ie Undershoot Amplitu	t the falling edge of Vss (_		
	of Vss (OV 3 Within Ur a Evaluat i Us Ur) crossing. IdershootRegion # 1: In Undershoot Amplitu Ing T _{MIN} , V _{MIN} to obtain IndershootRegion.	t the falling edge of Vss (de by:	e minimum v		
	of Vss (OV 3 Within Ur a Evaluat i Us Ur) crossing. IdershootRegion # 1: Te Undershoot Amplitu Sing T _{MIN} , V _{MIN} to obtand IdershootRegion.	t the falling edge of Vss (de by: in the time-stamp of the	e minimum v ation:		



$$\mathrm{Area}pprox rac{1}{2}(y_0+y_1)\Delta x+rac{1}{2}(y_1+y_2)\Delta x+rac{1}{2}(y_2+y_3)\Delta x+\dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

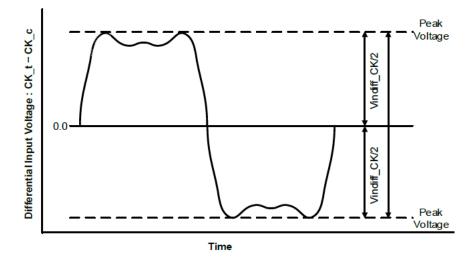
$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 28 Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - · Overshoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JEDEC specification.

Clock (Diff) Tests



Consider Figure 29 to understand how the minimum input differential voltage is measured at the input receiver.

Figure 29 CK Differential input voltage

Vindiff_CK

Availability Condition: Table 29 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	No	CK(Diff)	
Test ID & References:	Table 30 LPDDR	Test References from JE	SD209-5 specification			
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification	
	Vindiff_CK		151000		Table 313	
Overview:			that the peak-to-peak vo 0209-5 specification.	oltage on the	e test signal centered on OV	
Procedure:	1 Pre-conditior	the oscilloscope.				
	2 Trigger on the	e rising edge of the	e clock signal under test.			
	A valid positiv following vali	ve pulse on the Clo d falling edge of th		ng edge of t negative pu	he Clock and ends at the lse on the Clock starts at the	
	5 Calculate the	difference of the t	wo measurements and d	enote the re	sult as Vindiff_CK#1.	
			Vindiff_CK#1 = Vmax - '	Vmin		
	6 Then, measu	re Vmin of first neg	ative pulse and Vmax of	the second	positive pulse.	
	7 Calculate the	difference of the t	wo measurements and d	enote the re	sult as Vindiff_CK#2.	
	8 Continue ste	8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.				
	9 Determine th	e worst result from	the set of Vindiff_CK va	lues measur	ed.	
/Expected Observable Results:	The measured va JESD209-5 spec		or the test signal shall be	within the c	onformance limits as per the	

Vindiff_CK/2HighPulse

Availability Condition:	Table 31	Set Up tab options for availabil	ity of tests			
Supported CK Type	Supported WCI	(Type Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	No	CK(Diff)	
Test ID & References:	Table 32	LPDDR5 Test References from 、	JESD209-5 specification			
	Symbol (in	Specification)	Test ID	Reference f	rom Specification	
	Vindiff_CK		151001		Table 313	
Overview:		ose of this test is to verify t to the JESD209-5 speci	that the peak voltage of fication.	the high puls	e of the test signal is	
Procedure:	1 Pre-c	ondition the oscilloscope				
	2 Trigge	er on the rising edge of th	ne clock signal under test.			
	A vali					
		into the first pulse and m diff_CK/2.	neasure the max. Peak Vol	tage (Vmax).	Consider Vmax as the value	
	5 Conti	nue the previous step wit	h the rest of the positive p	oulses found	in the specified waveform.	
	6 Deter	mine the worst result fror	m the set of Vindiff_CK/2	alues that a	re measured.	
Expected/ Observable Results:		The measured value of Vindiff_CK/2 for the test signal shall be within the conformance limits as per the JESD209-5 specification.				

Vindiff_CK/2LowPulse

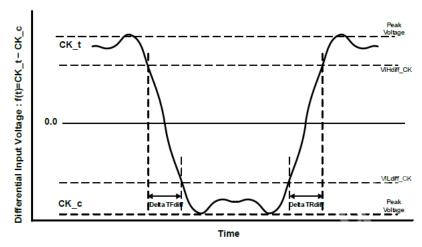
Availability Condition:	Table 33 Set Up	ab options for availability	v of tests			
	_	_				
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	No	CK(Diff)	
Test ID & References:	Table 34 LPDDR5	Test References from JE	SD209-5 specification			
	Symbol (in Specification) Test ID Reference from Specification			from Specification		
	Vindiff_CK		151002		Table 313	
Overview:		nis test is to verify t JESD209-5 specifi	hat the peak voltage of the cation.	the low pulse	e of the test signal is	
Procedure:	1 Pre-conditior	the oscilloscope.				
	2 Trigger on the	e falling edge of the	e clock signal under test			
	A valid negat					

5 Continue the previous step with the rest of the negative pulses found in the specified waveform.

6 Determine the worst result from the set of Vindiff_CK/2 values that are measured.

Expected/ Th Observable Results: th

The measured value of Vindiff_CK/2 for the test signal shall be within the conformance limits as per the JESD209-5 specification.



Input slew rate for differential signals are measured as shown in Figure 30.



VIHdiff_CK

Availability Condition: Table 35 Set Up tab options for availability of tests

Table 36

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References:

LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
VIHdiff_CK	151006	Table 316

Overview: The purpose of this test is to verify that the high level differential input voltage value of the test signal is compliant to the JESD209-5 specification.

Procedure:

- 1 Pre-condition the oscilloscope.
- 2 Trigger on the rising edge of the clock signal under test.
- 3 Find all valid Clock positive pulse in the triggered waveform. A valid Clock positive pulse starts at the OV crossing at valid Clock rising edge and ends at the OV crossing at the following valid Clock falling edge.
- 4 Zoom into the first pulse and measure the top voltage V_{TOP} . Here, V_{TOP} is the voltage value on the rising edge after which the signal loses the monotonicity of the slope. Consider the value of V_{TOP} as VIHdiff_CK.
- 5 Continue the previous step for all positive pulses found in the specified waveform.
- 6 Determine the worst result from the set of VIHdiff_CK values that are measured.

Expected/ The worst measured VIHdiff_CK for the test signal shall be within the conformance limits as per the JESD209-5 specification.

VILdiff_CK

Availability Condition: Table 37 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	No	CK(Diff)	
Test ID & References:	Table 38 LPDDR	5 Test References from JE	SD209-5 specification			
	Symbol (in Specifica	tion)	Test ID	Reference f	rom Specification	
	VILdiff_CK		151007		Table 316	
Overview:		The purpose of this test is to verify the low level differential input voltage value of the test signal is compliant to the JESD209-5 specification.				
Procedure:	1 Pre-conditior	the oscilloscope.				
	2 Trigger on th	e rising edge of the	e clock signal under test.			
	A valid Clock	3 Find all valid Clock negative pulse in the triggered waveform. A valid Clock negative pulse starts at the OV crossing at valid Clock falling edge and ends at the OV crossing at the following valid Clock rising edge.				
	on the falling					
	5 Continue the	previous step for a	ll negative pulses found	in the specif	ied waveform.	
	6 Determine th	e worst result from	the set of VILdiff_CK val	lues that are	measured.	
/Expected Observable Results:		The worst measured VILdiff_CK for the test signal shall be within the conformance limits as per the JESD209-5 specification.				

SRIdiffR_CK

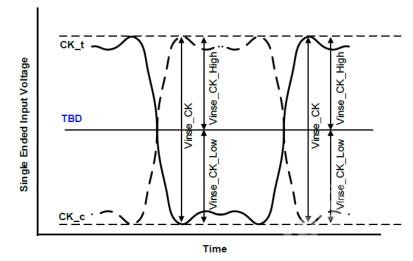
Availability Condition: Table 39 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	No	CK(Diff)	
Test ID & References:	Table 40 LPDDR5	Test References from JE	SD209-5 specification			
	Symbol (in Specificat	ion)	Test ID	Reference	from Specification	
	SRIdiffR_CK		151008		Table 317	
Overview:		The purpose of this test is to verify that the differential input slew rate for rising edge of the Clock signal is compliant to the JESD209-5 specification.				
Procedure:	1 Pre-condition	the oscilloscope.				
	2 Trigger on the	e rising edge of the	e clock signal under test.			
	3 Find all the va	alid Clock rising ed	ges in the entire wavefo	rm.		
	A valid clock crossing.	rising edge starts a	at VILdiff_CK crossing an	d ends at th	e following VIHdiff_CK	
		4 For all the valid Clock rising edges, measure the transition time, DeltaTRdiff. DeltaTRdiff is the time starting at VILdiff_CK crossing and ending at the following VIHdiff_CK				
	5 Calculate SRI	diffR_CK using the	equation:			
		SRIdiffR_Ck	K = [VIHdiff_CK - VILdiff_	CK] / Delta1	Rdiff	
	6 Determine the					
Expected/ Observable Results:		6 Determine the worst result from the set of SRIdiffR_CK measured. The measured value of SRIdiffR_CK for the Clock signal shall be within the conformance limits as per the JESD209-5 specification.				

SRIdiffF_CK

Availability Condition: Table 41 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	No	CK(Diff)	
Test ID & References:	Table 42 LPDDR5	Test References from JE	SD209-5 specification			
	Symbol (in Specificat	ion)	Test ID	Reference f	irom Specification	
	SRIdiffF_CK		151009		Table 317	
Overview:		The purpose of this test is to verify that the differential input slew rate for falling edge of the Clock signal is compliant to the JESD209-5 specification.				
Procedure:	 2 Trigger on the 3 Find all the valid clock is crossing. 4 For all the valid DeltaTFdiff is crossing. 5 Calculate SRI 	 signal is compliant to the JESD209-5 specification. Pre-condition the oscilloscope. Trigger on the falling edge of the clock signal under test. Find all the valid Clock falling edges in the entire waveform. A valid clock falling edge starts at VIHdiff_CK crossing and ends at the following VILdiff_CK crossing. For all the valid Clock falling edges, measure the transition time, DeltaTFdiff. DeltaTFdiff is the time starting at VIHdiff_CK crossing and ending at the following VILdiff_CK crossing. Calculate SRIdiffF_CK using the equation: SRIdiffF_CK = [VILdiff_CK - VIHdiff_CK] / DeltaTFdiff 				
Expected/ Observable Results:	6 Determine the worst result from the set of SRIdiffF_CK measured. The measured value of SRIdiffF_CK for the Clock signal shall be within the conformance limits as per the JESD209-5 specification.					



The minimum input single-ended voltage is measured as shown in Figure 31.

Figure 31 Clock Single-ended Input Voltage definition

Vinse_CK (Positive Pulse)

Availability Condition:	Table 43	Set Up tab options for availability of tests
-------------------------	----------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: Table 44 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK	151010	Table 314

Overview:

The purpose of this test is to verify the peak voltage of high pulse.

Procedure: 1 Pre-condition the oscilloscope.

- 2 Trigger on the rising edge of the clock signal under test.
- 3 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.
- 4 Zoom into the first pulse and measure V_{MAX} .
- 5 Calculate the value of Vinse_CK (Positive Pulse) using the equation:

Vinse_CK (Positive Pulse) = $V_{MAX} - V_{REF}$



For this test, the Test App considers Vref to be (V_{REFdiff CK}), which in turn, is typically set to OV.

- 6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
- 7 Determine the worst result from the set of Vinse_CK (Positive Pulse) measured.

Expected/The measured value of Vinse_CK (Positive Pulse) for the test signal shall be within the conformanceObservable Results:Limits as per the JEDEC specification.

Vinse_CK (Negative Pulse)

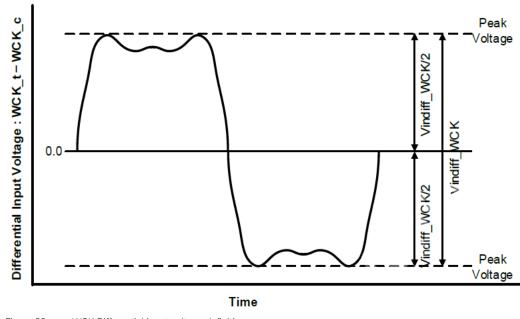
Availability Condition: Table 45 Set Up tab options for availability of tests

Burst & Continuous	N/A		Yes	No	No	CK(Diff)	
Test ID & References:	Table 4	6 LPDDR5	Test References from J	IESD209-5 specification			
	Symbol (in Specification) Vinse_CK			Test ID	Test IDReference from Specification151011Table 314		
				151011			
Overview:	The purpose of this test is to verify the peak voltage of low pulse.						
Procedure:	1 Pre-condition the oscilloscope.						
	2 Trigger on the falling edge of the clock signal under test.						
	A	3 Find all valid negative pulses of the Clock in the entire waveform. A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.					
	4 Z	4 Zoom into the first pulse and measure V _{MIN} .					
	5 C	5 Calculate the value of Vinse_CK (Negative Pulse) using the equation:					
	Vinse_CK (Negative Pulse) = $V_{REF} - V_{MIN}$						
		NOTE For this test, the Test App considers Vref to be (V _{REFdiff_CK}), which in turn, is typically set to OV.					

7 Determine the worst result from the set of Vinse_CK (Negative Pulse) measured.

Expected/ The measured value of Vinse_CK (Negative Pulse) for the test signal shall be within the conformance limits as per the JEDEC specification.

Write Clock (Diff) Tests



Consider Figure 32 to understand how the minimum input differential voltage is measured at the input receiver.

Figure 32 WCK Differential input voltage definition

Vindiff_WCK

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ		
Test ID & References:	Table 48 LPDDR	5 Test References from JE	SD209-5 specification				
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification		
	Vindiff_WCK		151100	Table 319			
Overview:			hat the peak-to-peak vo 209-5 specification.	oltage on the	e test signal centered on OV		
Procedure:	1 Pre-condition the oscilloscope.						
	2 Trigger on the rising edge of the Write Clock signal under test.						
	3 Find all valid positive and negative pulses of the Write Clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge of the Write Clock ends at the following valid falling edge of the Write Clock, whereas a valid negative pulse Write Clock starts at the valid falling edge of the Write Clock and ends at the following va rising edge of the Write Clock.						
		max. Peak Voltage first negative pulse	(Vmax) of the first positi e.	ve pulse and	d the Min. Peak Voltage		
	5 Calculate the	difference of the t	wo measurements and d	lenote the re	esult as Vindiff_WCK#1.		
		Ň	/indiff_WCK#1 = Vmax -	Vmin			
	6 Then, measu	re Vmin of first neg	ative pulse and Vmax of	the second	positive pulse.		
	7 Calculate the						
	8 Continue ste	os 4 to 7 for measu	rements on the remainir	ng pulse that	t was obtained.		
	9 Determine th	e worst result from	the set of Vindiff_WCK	values meas	ured.		
Expected/ Observable Results:	The measured va the JESD209-5 s		for the test signal shall	be within th	e conformance limits as pe		

Vindiff_WCK/2HighPulse

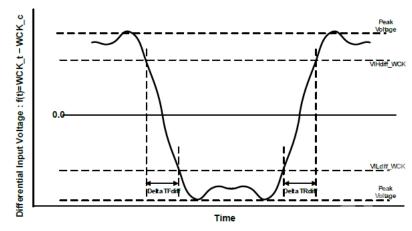
Availability Condition:	Table 49	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ			
Test ID & References:	Table 50 LPDDI	Table 50 LPDDR5 Test References from JESD209-5 specification						
	Symbol (in Specific	sation)	Test ID	Reference	from Specification			
	Vindiff_WCK		151101	Table 319				
Overview:		The purpose of this test is to verify that the peak voltage of the high pulse of the test signal is compliant to the JESD209-5 specification.						
Procedure:	1 Pre-conditio	on the oscilloscope.						
	2 Trigger on t	he rising edge of the	e Write Clock signal und	er test.				
	A valid posit	 Find all valid positive pulses of the Write Clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge of the Write Clock and ends at the following valid falling edge of the Write Clock. 						
		ne first pulse and me 'CK/2HighPulse.	easure the max. Peak Vol	tage (Vmax)	. Consider Vmax as the value			
	5 Continue th	e previous step with	the rest of the positive p	oulses found	in the specified waveform.			
	6 Determine t	he worst result from	the set of Vindiff_WCK/	2HighPulse	values that are measured.			
/Expected Observable Results:		alue of Vindiff_WCk JESD209-5 specifi		t signal shall	be within the conformance			

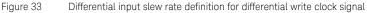
Vindiff_WCK/2LowPulse

Availability Condition:	Table 51	Set Up tab options for availability of tests	
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Supported CK Type	Supported	WCK Туре	Supports Offline?	R/W Separation	needed? SE Mode?	Required Signals		
Burst & Continuous	Burst		Yes	No	No	CK(Diff), WCK(Diff), DQ		
Test ID & References:	Table 5	Table 52 LPDDR5 Test References from JESD209-5 specification						
	Symb	ol (in Specific	ation)	Test ID	Referen	ice from Specification		
	Vindit	f_WCK		151102	Table 3	19		
Overview:		The purpose of this test is to verify that the peak voltage of the low pulse of the test signal is compliant to the JESD209-5 specification.						
Procedure:	1 Pr	1 Pre-condition the oscilloscope.						
	2 Tr	igger on th	ne falling edge of t	he Write Clock sig	signal under test.			
	 Find all valid negative pulses of the Write Clock in the entire waveform. A valid negative pulse on the Write Clock starts at the valid falling edge of the Write Clock ends at the following valid rising edge of the Write Clock. 							
			ne first pulse and m CK/2LowPulse.	neasure the min. F	Peak Voltage (Vm	in). Consider Vmin as the value		
	5 C	ontinue the	e previous step wit	h the rest of the n	egative pulses for	und in the specified waveform.		
	6 D	etermine th	ne worst result fror	n the set of Vindif	f_WCK/2LowPuls	e values that are measured.		
/Expected Observable Results:			alue of Vindiff_WC JESD209-5 specit		the test signal sha	all be within the conformance		



Input slew rate for differential WCK signals are measured as shown in Figure 33.



VIHdiff_WCK

Availability Condition:	Table 53	Set Up tab options for availability of tests
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Table 54

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References:

LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
VIHdiff_WCK	151106	Table 322

Overview: The purpose of this test is to verify that the high level differential input voltage value of the test signal is compliant to the JESD209-5 specification.

Procedure: 1 Pre-condition the oscilloscope.

- 2 Trigger on the rising edge of the Write Clock signal under test.
- 3 Find all valid Write Clock positive pulse in the triggered waveform. A valid Write Clock positive pulse starts at the 0V crossing at valid Write Clock rising edge and ends at the 0V crossing at the following valid Clock falling edge.
- 4 Zoom into the first pulse and measure the top voltage V_{TOP} . Here, V_{TOP} is the voltage value on the rising edge after which the signal loses the monotonicity of the slope. Consider the value of V_{TOP} as VIHdiff_WCK.
- 5 Continue the previous step for all positive pulses found in the specified waveform.
- 6 Determine the worst result from the set of VIHdiff_WCK values that are measured.

Expected/ The worst measured VIHdiff_WCK for the test signal shall be within the conformance limits as per the JESD209-5 specification.

VILdiff_WCK

Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ		
Test ID & References:	Table 56 L	PDDR5 Test References from	JESD209-5 specification				
	Symbol (in Spe	ecification)	Test ID	Referenc	e from Specification		
	VILdiff_WCK		151107	Table 322	2		
Overview:		e of this test is to verify the JESD209-5 spec		ial input volta	ge value of the test signal is		
Procedure:	1 Pre-condition the oscilloscope.						
	2 Trigger on the rising edge of the Write Clock signal under test.						
	3 Find all valid Write Clock negative pulse in the triggered waveform. A valid Write Clock negative pulse starts at the OV crossing at valid Write Clock falling edge and ends at the OV crossing at the following valid Write Clock rising edge.						
		0 1	following valid Write C	lock rising ed	ge.		
	ends at t 4 Zoom int on the fa	the OV crossing at the to the first pulse and r	measure the base volta In the signal loses the m	ge V _{BASE} . Her	e, V _{BASE} is the voltage value		
	ends at t 4 Zoom int on the fa Consider	the OV crossing at the to the first pulse and r alling edge after which r the value of V _{BASE} as	measure the base volta In the signal loses the m	ge V _{BASE} . Her nonotonicity of	e, V _{BASE} is the voltage value the slope.		

SRIdiffR_WCK

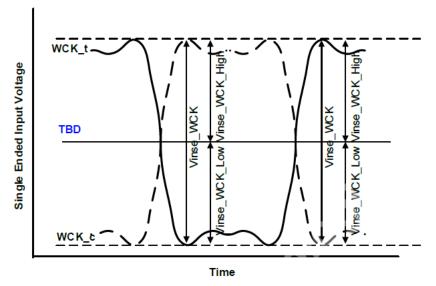
Availability Condition: Table 57 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ			
Test ID & References:	Table 58 LPDDR	5 Test References from JE	SD209-5 specification					
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification			
	SRIdiffR_WCK		151108	Table 323				
Overview:		The purpose of this test is to verify that the differential input slew rate for rising edge of the Write Clock signal is compliant to the JESD209-5 specification.						
Procedure:	1 Pre-conditior	the oscilloscope.						
	2 Trigger on th	e rising edge of the	Write Clock signal und	er test.				
	3 Find all the v	alid Write Clock ris	ing edges in the entire w	vaveform.				
		A valid Write Clock rising edge starts at VILdiff_WCK crossing and ends at the following VIHdiff_WCK crossing.						
		4 For all the valid Write Clock rising edges, measure the transition time, DeltaTRdiff. DeltaTRdiff is the time starting at VILdiff_WCK crossing and ending at the following VIHdiff_WCK						
	5 Calculate SR	ldiffR_WCK using t	he equation:					
		SRIdiffR WCK	= [VIHdiff_WCK - VILdiff	f WCK]/De	ltaTRdiff			
	6 Determine th	_	the set of SRIdiffR_WCI					
/Expected Observable Results:		lue of SRIdiffR_WC JESD209-5 specifie		gnal shall be	within the conformance			

SRIdiffF_WCK

Availability Condition:	Table 59	Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ		
Test ID & References:	Table 60 LPDDR5	Test References from JE	SD209-5 specification				
	Symbol (in Specificat	iion)	Test ID	Reference	from Specification		
	SRIdiffF_WCK		151109	Table 323			
Overview:				slew rate fo	or falling edge of the Write		
Procedure:	 2 Trigger on the 3 Find all the va A valid Write VILdiff_WCK of 4 For all the val DeltaTFdiff is crossing. 	 Clock signal is compliant to the JESD209-5 specification. Pre-condition the oscilloscope. Trigger on the falling edge of the Write Clock signal under test. Find all the valid Write Clock falling edges in the entire waveform. A valid Write Clock falling edge starts at VIHdiff_WCK crossing and ends at the following VILdiff_WCK crossing. For all the valid Write Clock falling edges, measure the transition time, DeltaTFdiff. DeltaTFdiff is the time starting at VIHdiff_WCK crossing and ending at the following VILdiff_WCK crossing. Calculate SRIdiffF_WCK using the equation: SRIdiffF_WCK = [VILdiff_WCK - VIHdiff_WCK] / DeltaTFdiff 					
Expected/ Observable Results:	The measured va		- K for the Write Clock sig		within the conformance		



Input slew rate for differential WCK signals are measured as shown in Figure 33.

Figure 34 Differential input slew rate definition for differential write clock signal

Vinse_WCK (Positive Pulse)

Availability Condition: Table 61 Set Up tab options for availability of tests

Supported CK Type	Supported V	/CK Type Supports Offline	? R/W Separation needed	1? SE Mode?	Required Signals	
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ	
Test ID & References:	Table 62	LPDDR5 Test References fro	m JESD209-5 specification			
	Symbol	Symbol (in Specification) Test ID Reference from Specification				
	Vinse_V	VCK	151110	Table 320		
Overview:	The pu	rpose of this test is to ver	ify the peak voltage of hi	gh pulse.		
Procedure:	1 Pre	-condition the oscillosco	pe.			
	2 Trig	ger on the rising edge of	the Write Clock signal u	nder test.		
	 Find all valid positive pulses of the Write Clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge of the Write Clock and ends at the following valid falling edge of the Write Clock. 					
				0	ige of the write Clock and	
	enc		alling edge of the Write C	0	ge of the write Clock and	

Vinse_WCK (Positive Pulse) = $V_{MAX} - V_{REF}$

NOTE

For this test, the Test App considers Vref to be (V_{REFdiff_WCK}), which in turn, is typically set to 0V.

- 6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
- 7 Determine the worst result from the set of Vinse_WCK (Positive Pulse) measured.

Expected/ Observable Results: The measured value of Vinse_WCK (Positive Pulse) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_WCK (Negative Pulse)

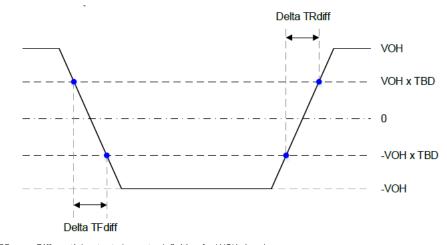
Availability Condition: Table 63 Set Up tab options for availability of tests

Burst & Continuous	Burst		Yes	No	No	CK(Diff), WCK(Diff), DQ
Test ID & References:	Ta	ble 64 LPDDR	Test References from	JESD209-5 specification		
		Symbol (in Specifica	tion)	Test ID	Reference	e from Specification
	,	Vinse_WCK		151111	Table 320)
Test Overview:	Tł	ne purpose of th	his test is to verify	/ the peak voltage of l	ow pulse.	
Test Overview: Test Procedure:	1 2 3 4 5	 2 Trigger on the falling edge of the Write Clock signal under test. 3 Find all valid negative pulses of the Write Clock in the entire waveform. A valid negative pulse on the Write Clock starts at the valid falling edge of the Write Clock and ends at the following valid rising edge of the Write Clock. 4 Zoom into the first pulse and measure V_{MIN}. 				

7 Determine the worst result from the set of Vinse_WCK (Negative Pulse) measured.

Expected/ The m Observable Results: confo

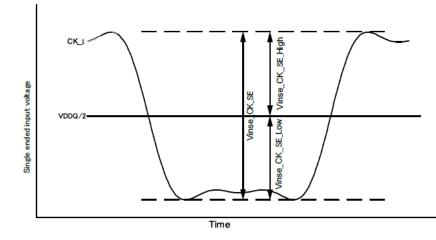
The measured value of Vinse_WCK (Negative Pulse) for the test signal shall be within the conformance limits as per the JEDEC specification.



Output slew rate for differential signals are measured as shown in Figure 35.

Figure 35 Differential output slew rate definition for WCK signal

Clock (SE Mode) Tests



The minimum single-ended CK input voltage is measured as shown in Figure 36.

Figure 36 Single-ended mode CK input Voltage definition

Vinse_CK_SE

Availability Condition:	Table 65	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	Yes	Yes	CK_t
Test ID & References:	Table 66 LPDDR5	Test References from JE	SD209-5 specification		
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	Vinse_CK_SE		251000		Table 328
Overview:		his test is to verify t liant to the JESD20		ltage on the	e test signal centered on
Procedure:		the oscilloscope.	clock signal under test		
	 2 Trigger on the rising edge of the clock signal under test. 3 Find all valid positive and negative pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge, whereas a valid negative pulse on the Clock starts at the valid falling edge and ends at the following valid rising edge. 				
		max. Peak Voltage first negative pulse	(Vmax) of the first positiv	ve pulse and	d the Min. Peak Voltage
	5 Calculate the	difference of the tw	vo measurements and d	enote the re	sult as Vinse CK_SE#1

Vinse_CK_SE#1 = Vmax - Vmin

- 6 Then, measure Vmin of first negative pulse and Vmax of the second positive pulse.
- 7 Calculate the difference of the two measurements and denote the result as Vinse_CK_SE#2.
- 8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.
- 9 Determine the worst result from the set of Vinse_CK_SE values measured.

Expected/ The measured value of Vinse_CK_SE for the test signal shall be within the conformance limits as per **Observable Results:** the JESD209-5 specification.

Vinse_CK_SE_High

Availability Condition:	Table 67	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	Yes	Yes	CK_t		
Test ID & References:	Table 68 LPDDR	5 Test References from JE	SD209-5 specification				
	Symbol (in Specifica	ation)	Test ID	Reference	from Specification		
	Vinse_CK_SE_High		251012	Table 328			
Test Overview:	The purpose of t	his test is to verify t	he peak voltage of high	pulse.			
Test Procedure:	1 Pre-conditio	n the oscilloscope.					
	2 Trigger on th	e rising edge of the	clock signal under test.				
			he Clock in the entire wa ck starts at the valid risi		l ends at the following valid		
	4 Zoom into th	e first pulse and me	easure V _{MAX} .				
	5 Calculate the	e value of Vinse_CK	_SE_High using the equ	ation:			
		Vi	nse_CK_SE_High = V _{MA}	_x - V _{REF}			
	NOTE	NOTE For this test, the Test App considers Vref to be $(V_{DDQ}/2)$.					
					in the specified waveform.		
	7 Determine th	ne worst result from	the set of Vinse_CK_SE	_High measi	ured.		

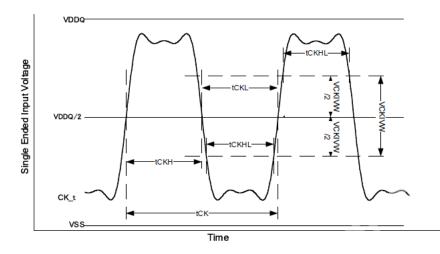
d/ The measured value of Vinse_CK_SE_High for the test signal shall be within the conformance limits as per the JEDEC specification.

Expected/ Observable Results: Vinse_CK_SE_Low

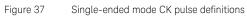
vailability Condition:	Table 69	Set Up	tab options for availability	of tests				
Supported CK Type	Supported	WCK Туре	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A		Yes	Yes	Yes	CK_t		
Test ID & References:	Table 70	LPDDR	5 Test References from JE	SD209-5 specification				
	Symbo	ol (in Specifica	tion)	Test ID	Reference	from Specification		
	Vinse_	CK_Low		251014	Table 328			
Overview:	The pu	irpose of t	his test is to verify t	he peak voltage of low p	oulse.			
Procedure:	1 Pre	1 Pre-condition the oscilloscope.						
	2 Tri	2 Trigger on the falling edge of the clock signal under test.						
	A١	valid negat				f the Clock and ends at the		
	4 Zo	om into th	e first pulse and me	easure V _{MIN} .				
	5 Ca	lculate the	e value of Vinse_CK	_SE_Low using the equa	tion:			
			Vi	nse_CK_SE_Low = V _{REF}	- V _{MIN}			
		NOTE For this test, the Test App considers Vref to be $(V_{DDQ}/2)$.						
	6 Cc	ntinue the	previous step with	the rest of the negative	pulses foun	d in the specified waveform		

7 Determine the worst result from the set of Vinse_CK_SE_Low measured.

Expected/ The measured value of Vinse_CK_SE_Low for the test signal shall be within the conformance limits as per the JEDEC specification.



The single-ended clock input slew rate can be measured as shown in Figure 37.



SRIseR_CKSE

Availability Condition:	Table 71	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	Yes	Yes	CK(Diff)		
Test ID & References:	Table 72 LPDDF	5 Test References from JE	SD209-5 specification				
	Symbol (in Specific	ation)	Test ID	Reference	from Specification		
	SRICKSE		251008		Table 328		
Overview:		The purpose of this test is to verify that the single-ended input slew rate for rising edge of the Clock signal is compliant to the JESD209-5 specification.					
Procedure:	 2 Trigger on th 3 Find all the v VIL_CK cross 4 For all the va DeltaTRdiff i 	 Pre-condition the oscilloscope. Trigger on the rising edge of the Clock (CK) signal under test. Find all the valid CK rising edges in the entire waveform. A valid Clock rising edge starts at VIL_CK crossing and ends at the following VIH_CK crossing. For all the valid CK rising edges, measure the transition time, DeltaTRdiff. DeltaTRdiff is the time starting at VIL_CK crossing and ending at the following VIH_CK crossing 					
	6 Determine tl		CK = ([VDDQ/2] - [VCk the set of SRIseR_CKSE	27			

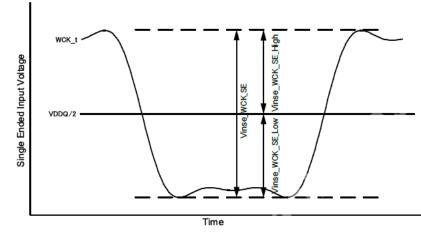
Expected/ The measured value of SRIseR_CKSE for the Clock signal shall be within the conformance limits as per the JESD209-5 specification.

SRIseF_CKSE

Availability Condition: Table 73 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	Yes	Yes	CK(Diff)		
Test ID & References:	Table 74 LPDDF	25 Test References from JE	SD209-5 specification				
	Symbol (in Specific	ation)	Test ID	Reference	from Specification		
	SRICKSE		251009		Table 328		
Overview:		The purpose of this test is to verify that the single-ended input slew rate for falling edge of the Clock signal is compliant to the JESD209-5 specification.					
Procedure:	1 Pre-conditio	n the oscilloscope.					
	2 Trigger on th	ne falling edge of th	e Clock (CK) signal unde	r test.			
			es in the entire waveform e following VIL_CK cross		ck falling edge starts at		
	4 For all the va	alid CK falling edges	s, measure the transition	time, Delta	TFdiff.		
	DeltaTFdiff i	s the time starting a	t VIH_CK crossing and e	ending at the	e following VIL_CK crossing.		
	5 Calculate SF	RIseF_CKSE using th	e equation:				
		SRIseF_C	KSE = [VIL_CK - VIH_CH	K] / DeltaTFc	liff		
		where,	VIH_CK = ([VDDQ/2] + [VCKIVW/2])			
		VIL	CK = ([VDDQ/2] - [VCk	(IVW/2])			
	6 Determine t		the set of SRIseF_CKSE				
/Expected Observable Results:		alue of SRIseF_CKS 9-5 specification.	E for the Clock signal sh	all be within	the conformance limits as		

Write Clock (SE Mode) Tests



The minimum single-ended WCK input voltage is measured as shown in Figure 36.

Figure 38 Single-ended mode WCK input Voltage definition

Vinse_WCK_SE

Availability Condition: Table 75 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 76 LPDDF	25 Test References from JE	SD209-5 specification		
	Symbol (in Specific	ation)	Test ID	Reference	from Specification
	Vinse_WCK_SE		251100	Table 327	
Overview:		this test is to verify t oliant to the JESD20		oltage on the	e test signal centered on
Procedure:		n the oscilloscope. ne rising edge of the	write clock signal unde	r test.	
	3 Find all valid positive and negative pulses of the Write Clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge and ends at the for valid falling edge, whereas a valid negative pulse on the Write Clock starts at the valid fall edge and ends at the following valid rising edge.				
		e max. Peak Voltage e first negative pulse		ve pulse and	d the Min. Peak Voltage
	5 Calculate th	e difference of the tw	wo measurements and c	lenote the re	esult as Vinse_WCK_SE#1.
		Vi	nse WCK SF#1 = Vmax	- Vmin	

Vinse_WCK_SE#1 = Vmax - Vmin

- 6 Then, measure Vmin of first negative pulse and Vmax of the second positive pulse.
- 7 Calculate the difference of the two measurements and denote the result as Vinse_WCK_SE#2.
- 8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.
- 9 Determine the worst result from the set of Vinse_WCK_SE values measured.

Expected/ The measured value of Vinse_WCK_SE for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Vinse_WCK_SE_High

Supported CK Type			·				
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ		
Test ID & References:	Table 78 LPDDR	5 Test References from JE	SD209-5 specification				
	Symbol (in Specification)		Test ID	Reference from Specification			
	Vinse_WCK_SE_Hig	1	251112	Table 327			
Overview:		his test is to verify t JESD209-5 specifi	hat the peak voltage of cation.	the high pul	se of the test signal is		
Procedure:	1 Pre-condition the oscilloscope.						
	2 Trigger on the rising edge of the write clock signal under test.						
		ve pulse on the Wri	he Write Clock in the en te Clock starts at the va		m. ge and ends at the following		
	4 Zoom into the first pulse and measure V _{MAX} .						
	5 Calculate the value of Vinse_WCK_SE_High using the equation:						
	Vinse_WCK_SE_High = V _{MAX} - V _{REF}						
	NOTE For this test, the Test App considers Vref to be (V _{refDQ} /2).						

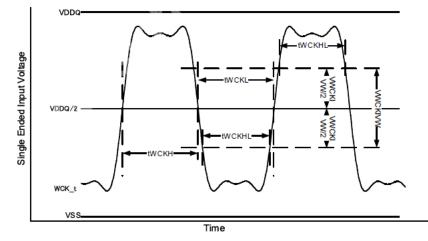
Expected/The measured value of Vinse_WCK_SE_High for the test signal shall be within the conformance limitsObservable Results:as per the JESD209-5 specification.

Vinse_WCK_SE_Low

Availability Condition:	Table 79	Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ	
Test ID & References:	Table 80 LPDDR5	Test References from JE	SD209-5 specification			
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification	
	Vinse_WCK_SE_Low		251114	Table 327		
Overview:		nis test is to verify t JESD209-5 specifi	hat the peak voltage of cation.	the low puls	e of the test signal is	
Procedure:	1 Pre-condition the oscilloscope.					
	2 Trigger on the	e falling edge of the	e write clock signal unde	er test.		
	A valid negat				rm. dge of the Clock and ends a	
	4 Zoom into the	e first pulse and me	easure V _{MIN} .			
	5 Calculate the	value of Vinse_WC	K_SE_Low using the eq	uation:		
		Vin	se_WCK_SE_Low = V _{RE}	_F - V _{MIN}		
	NOTE	For this test,	the Test App considers	Vref to be (V _{refDQ} /2).	
			the rest of the negative the set of Vinse_WCK_S	•	d in the specified waveform.	

Expected/The measured value of Vinse_WCK_SE_Low for the test signal shall be within the conformance limitsObservable Results:as per the JESD209-5 specification.



The single-ended write clock input slew rate can be measured as shown in Figure 39.

Figure 39 Single-ended mode WCK pulse definitions

SRIseR_WCKSE

Availability Condition:	Table 81	Set Up tab options for availability of tests
-------------------------	----------	--

Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ
Table 82 LPDDR5	Test References from JE	SD209-5 specification		
Symbol (in Specificati	on)	Test ID	Reference	from Specification
SRIWCKSE		251108	Table 327	
			out slew rate	e for rising edge of the Write
 2 Trigger on the 3 Find all the va at VIL_WCK c 4 For all the vali 	rising edge of the lid WCK rising edg rossing and ends a d WCK rising edge	ges in the entire wavefor It the following VIH_WC es, measure the transitio	m. A valid W K crossing. on time, Delt	/rite Clock rising edge starts aTRdiff.
	Burst Table 82 LPDDR5 Symbol (in Specificati SRIWCKSE The purpose of th Clock signal is cor Pre-condition Trigger on the Find all the val at VIL_WCK cr For all the vali	Burst Yes Table 82 LPDDR5 Test References from JE Symbol (in Specification) SRIWCKSE The purpose of this test is to verify the Clock signal is compliant to the JES 1 Pre-condition the oscilloscope. 2 Trigger on the rising edge of the 3 Find all the valid WCK rising edge at VIL_WCK crossing and ends at VIL_WCK rising edge 4 For all the valid WCK rising edge	Burst Yes Table 82 LPDDR5 Test References from JESD209-5 specification Symbol (in Specification) Test ID SRIWCKSE 251108 The purpose of this test is to verify that the single-ended in Clock signal is compliant to the JESD209-5 specification. 1 Pre-condition the oscilloscope. 2 Trigger on the rising edge of the Write Clock (WCK) sign 3 Find all the valid WCK rising edges in the entire wavefor at VIL_WCK crossing and ends at the following VIH_WC 4 For all the valid WCK rising edges, measure the transition	Burst Yes Yes Yes Table 82 LPDDR5 Test References from JESD209-5 specification Symbol (in Specification) Test ID Reference SRIWCKSE 251108 Table 327 The purpose of this test is to verify that the single-ended input slew rate Clock signal is compliant to the JESD209-5 specification. 1 Pre-condition the oscilloscope. 2 Trigger on the rising edge of the Write Clock (WCK) signal under test 3 Find all the valid WCK rising edges in the entire waveform. A valid W at VIL_WCK crossing and ends at the following VIH_WCK crossing.

6 Determine the worst result from the set of SRIseR_WCKSE measured.

Expected/ The measured value of SRIseR_WCKSE for the Write Clock signal shall be within the conformance limits as per the JESD209-5 specification.

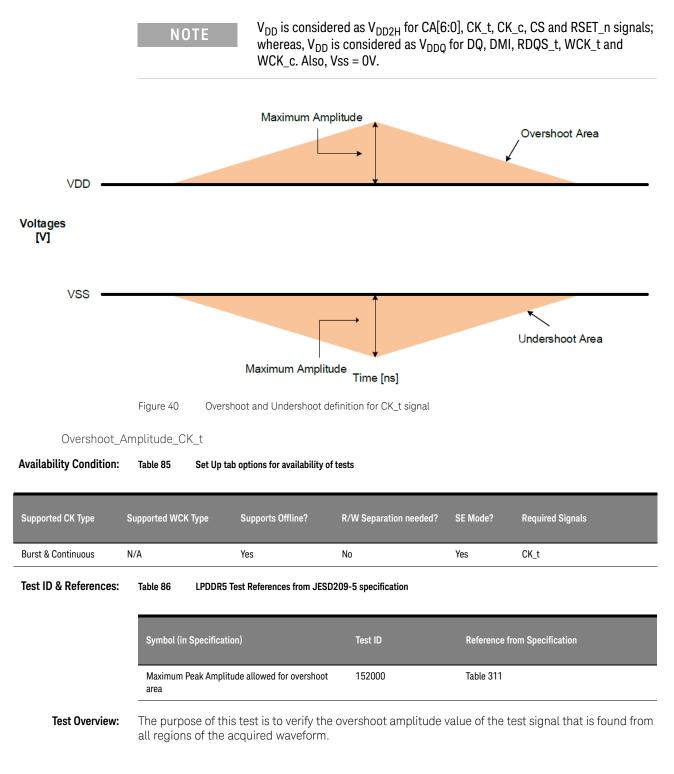
SRIseF_WCKSE

Availability Condition:	Table 83	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ
Test ID & References:	Table 84 LPDDR	5 Test References from JE	SD209-5 specification		
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	SRIWCKSE		251109	Table 327	
Overview:			hat the single-ended inp D209-5 specification.	out slew rate	e for falling edge of the Writ
Procedure:	1 Pre-conditior	the oscilloscope.			
	2 Trigger on th	e falling edge of the	e Write Clock (WCK) sig	nal under te	st.
			ges in the entire wavefor at the following VIL_WC		Vrite Clock falling edge start
	4 For all the va	lid WCK falling edg	es, measure the transiti	on time, Del	taTFdiff.
	DeltaTFdiff is crossing.	the time starting a	t VIH_WCK crossing and	d ending at t	the following VIL_WCK
	5 Calculate SR	lseF_WCKSE using	the equation:		
		SRIseF_WCk	SE = [VIL_WCK - VIH_V	VCK] / Delta	aTFdiff
		where, VI	H_WCK = ([VDDQ/2] +	WCKIVW/	2])
		VIL V	VCK = ([VDDQ/2] - [VW	CKIVW/2])	
	6 Determine th		the set of SRIseF_WCK		d.
Expected/ Observable Results:		lue of SRIseF_WCk JESD209-5 specific		signal shall	be within the conformance

Clock (SE) CK_t (Clock Plus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

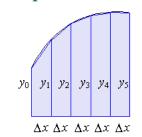
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 41 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

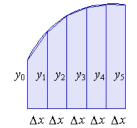
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Amplitude_CK_t

Availability Condition: Table 87 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK_t		
Test ID & References:	Table 88 LPDDR	5 Test References from JE	SD209-5 specification				
	Symbol (in Specifica	ition)	Test ID	Reference	from Specification		
	Maximum Peak Amp area	litude allowed for undersh	oot 152001	Table 311			
Test Overview:		his test is to verify t of the acquired way		de value of th	ne test signal that is found		
	In case of an unc Calculation.	dershoot, the under	shoot area is calculated	l based on th	ne Trapezoidal Method Area		
Test Procedure:		uire signal data and e adjustment).	perform signal conditic	ning to max	imize screen resolution		
	An "Undersh						
	3 Within Unde	rshootRegion # 1:					
	a Evaluate L	Indershoot Amplitu	de by:				
		g T _{MIN} , V _{MIN} to obta rshootRegion.	in the time-stamp of the	e minimum v	voltage on the		
	ii Calcu	llating Undershoot	Amplitude using the equ	uation:			
		Un	dershoot Amplitude = V	ss - V _{MIN}			
	b Evaluate T	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:		

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg[\operatorname{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_0}{2}\Big)$	$\left(\frac{n}{2}\right)$
---	----------------------------

Figure 42 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

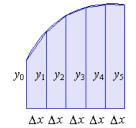
Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_CK_t

Availability Condition:	Table 89	Set Up tab options for availability of tests
-------------------------	----------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK_t		
Test ID & References:	Table 90 LPDDR5	Table 90 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Specificat	ion)	Test ID	Reference f	rom Specification		
	Maximum overshoot a	area above V _{DD2H} /V _{DDQ}	152002	Table 311			
Test Overview:		is test is to verify th acquired waveform		value of the t	est signal that is found from		
	When there is overshoot amplite		oot area is calculated b	ased on the	overshoot width and		
Test Procedure:	1 Sample/acqu (vertical scale		perform signal condition	ning to maxii	mize screen resolution		
		 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of 					
		nootRegion # 1:					
	a Evaluate O	vershoot Amplitude	e by:				
		T _{MAX} , V _{MAX} to obta nootRegion.	ain the time-stamp of th	e maximum	voltage on the		
	ii Calcul	ate Overshoot Amp	olitude using the equation	on:			
		Over	shoot Amplitude = V _{MAX}	_x - V _{DD2H}			
	b Evaluate A	rea_below_V _{DD2H} u	ising the equation:				
			ershootRegion_End - Ov V by using Trapezoidal N				

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 43 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_0V - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

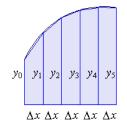
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Area_CK_t

Availability Condition: Table 91 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Typ	e Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK_t		
Test ID & References:	Table 92 LP	Table 92 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Spe	cification)	Test ID	Reference	from Specification		
	Maximum unde	ershoot area above VSS	152003	Table 311			
Test Overview:	from all region calculated ba	The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.					
Test Procedure:		1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).					
	 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing. 						
		√) crossing.			g and chas at the hoing eage		
	of Vss (0)	V) crossing.ndershootRegion # 1:			g and chas at the nsing cag		
	of Vss (0\ 3 Within Ui a Evalua	ndershootRegion # 1: ite Undershoot Ampliti	ude by:				
	of Vss (0\ 3 Within Ur a Evalua i U	ndershootRegion # 1: ite Undershoot Ampliti					
	of Vss (0\ 3 Within Ui a Evalua i U U	ndershootRegion # 1: te Undershoot Amplitu sing T _{MIN} , V _{MIN} to obta ndershootRegion.	ude by:	e minimum v			
	of Vss (0\ 3 Within Ui a Evalua i U U	ndershootRegion # 1: Ite Undershoot Amplitu sing T _{MIN} , V _{MIN} to obtandershootRegion. alculating Undershoot	ude by: ain the time-stamp of the	e minimum v Jation:			

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

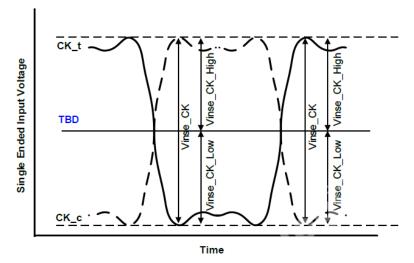
$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 44

re 44 Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JEDEC specification.



The minimum input single-ended voltage is measured as shown in Figure 45.

Figure 45 Clock Single-ended Input Voltage definition

Vinse_CK_High (CK_t)

Availability Condition	on: Table 93	Set Up tab options for availability of tests
------------------------	--------------	--

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_t

Test ID & References: Table 94 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_High	151012	Table 314

Test Overview: The purpose of this test is to verify the peak voltage of high pulse.

Test Procedure:

1 Pre-condition the oscilloscope.

- 2 Trigger on the rising edge of the clock signal under test.
- 3 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge.
- 4~ Zoom into the first pulse and measure $V_{\text{MAX}}.$
- 5 Calculate the value of Vinse_CK_High (CK_t) using the equation:

Vinse_CK_High (CK_t) = $V_{MAX} - V_{REF}$

NOTE

For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

- 6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
- 7 Determine the worst result from the set of Vinse_CK_High (CK_t) measured.

Expected/ The measured value of Vinse_CK_High (CK_t) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_CK_Low (CK_t)

Availability Condition: Table 95 Set Up	tab options for availability of tests
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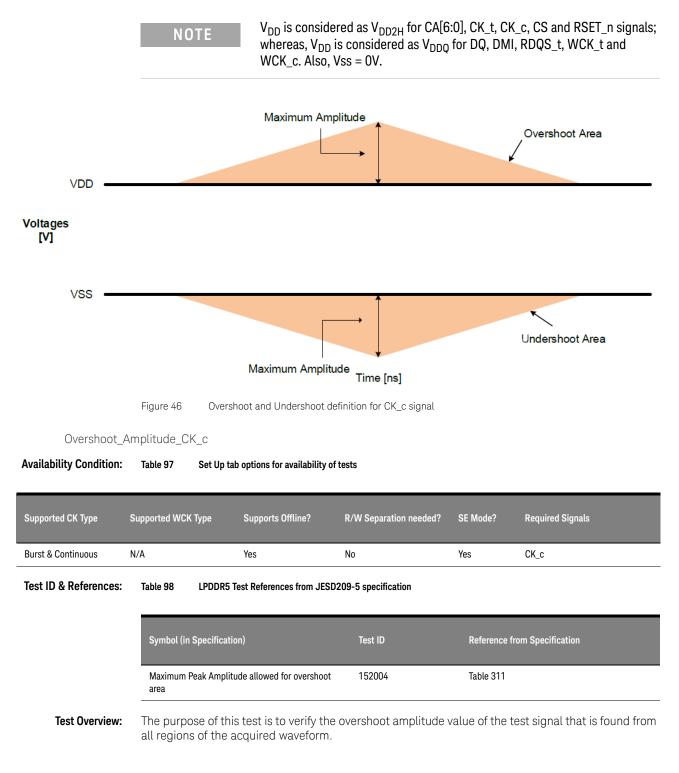
Supported CK Type	Suppo	orted WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A		Yes	No	No	CK_t	
Test ID & References:	Tat	Table 96 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Specification)		Test ID	Reference from Specification			
	١	Vinse_CK_Low		151014	Table 314		
Overview:	Th	ie purpose of t	his test is to verify t	he peak voltage of low p	oulse.		
Procedure:	1	1 Pre-condition the oscilloscope.					
	2	2 Trigger on the falling edge of the clock signal under test.					
	3	3 Find all valid negative pulses of the Clock in the entire waveform. A valid negative pulse on the Clock starts at the valid falling edge and ends at the following valid rising edge of the Clock.					
	4	4 Zoom into the first pulse and measure V _{MIN} .					
	5	5 Calculate the value of Vinse_CK_Low (CK_t) using the equation:					
		$Vinse_CK_Low (CK_t) = V_{REF} - V_{MIN}$					
	l	NOTE For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).					
	6	 6 Continue the previous step with the rest of the negative pulses found in the specified waveform. 7 Determine the worst result from the set of Vinse_CK_Low (CK_t) measured. 					

Expected/ The measuremeas

The measured value of Vinse_CK_Low (CK_t) for the test signal shall be within the conformance limits as per the JEDEC specification.

Clock (SE) CK_c (Clock Minus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 46.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

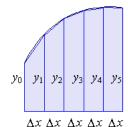
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DD2H}$

b Evaluate Area_below_V_{DD2H} using the equation:

Area_below_V_{DD2H} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD2H}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 47 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_OV - Area_below_V_{DD2H}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

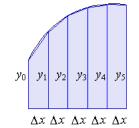
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Amplitude_CK_c

Availability Condition: Table 99 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Typ	e Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	Yes	CK_c	
Test ID & References:	Table 100 LP	DDR5 Test References from J	ESD209-5 specification			
	Symbol (in Spe	cification)	Test ID	Reference	from Specification	
	Maximum Peak area	Amplitude allowed for unders	hoot 152005	Table 311		
Test Overview:		of this test is to verify ons of the acquired wa		ide value of t	he test signal that is found	
	In case of an Calculation.	undershoot, the unde	rshoot area is calculate	d based on tl	he Trapezoidal Method Area	
Test Procedure:		acquire signal data an scale adjustment).	d perform signal condit	oning to max	imize screen resolution	
2 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) cross of Vss (0V) crossing.					g and ends at the rising edg	
	3 Within Ur	ndershootRegion # 1:				
	a Evalua	te Undershoot Amplit	ude by:			
		sing T _{MIN} , V _{MIN} to obt ndershootRegion.	ain the time-stamp of t	he minimum y	voltage on the	
	ii C	alculating Undershoot	Amplitude using the e	quation:		
	Undershoot Amplitude = Vss - V _{MIN}					
	b Evalua	te Total_Area_Below_\	√ss by using Trapezoida	l Method Are	a Calculation:	

The Trapezoidal Rule



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + 2 \Big)$	$\left(\frac{y_n}{2}\right)$
---	------------------------------

Figure 48 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

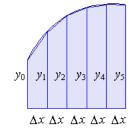
Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_CK_c

Availability Condition: Table 101 Set Up tab options for availability of	of tests
--	----------

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	Yes	CK_c	
Test ID & References:	Table 102 LPDD	R5 Test References from JE	SD209-5 specification			
	Symbol (in Specific	cation)	Test ID	Reference	from Specification	
	Maximum overshoo	t area above V _{DD2H} /V _{DDQ}	152006	Table 311		
Overview:		this test is to verify t e acquired waveforn		value of the	test signal that is found from	
	When there is c overshoot ampl		noot area is calculated b	ased on the	overshoot width and	
Procedure:		luire signal data and le adjustment).	perform signal conditio	ning to maxi	mize screen resolution	
	An "Oversho					
	3 Within Over	shootRegion # 1:				
	a Evaluate	Overshoot Amplitud	e by:			
		g T _{MAX} , V _{MAX} to obt shootRegion.	ain the time-stamp of th	ne maximum	voltage on the	
	ii Calc	ulate Overshoot Am	plitude using the equation	on:		
		Ove	rshoot Amplitude = V _{MA}	_X - V _{DD2H}		
	b Evaluate	Area_below_V _{DD2H} (using the equation:			
	Area	_below_V _{DD2H} = (Ov	ershootRegion_End - 0\	vershootReg	ion_Start) x V _{DD2H}	
	c Evaluate	Total_Area_Above_0	V by using Trapezoidal N	Method Area	Calculation:	

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 49 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_0V - Area_below_V_{DD2H}

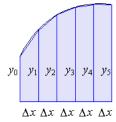
- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD2H}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Area_CK_c

Availability Condition: Table 103 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_c
Test ID & References: Table 104 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Speci	fication)	Test ID	Reference	from Specification
	Maximum unders	hoot area above VSS	152007	Table 311	
Overview:	from all region	s of the acquired way	the undershoot amplituc veform. In case of an und t width and undershoot	dershoot, the	ne test signal that is found e undershoot area is
Procedure:					
		dershootRegion # 1:			
	a Evaluate	e Undershoot Amplitu	de by:		
		ng T _{MIN} , V _{MIN} to obta dershootRegion.	in the time-stamp of the	e minimum \	oltage on the
	ii Cal	culating Undershoot	Amplitude using the equ	uation:	
		Un	dershoot Amplitude = V	ss - V _{MIN}	
	b Evaluate	e Total_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:
		The Trapezo	oidal Rule		



$$\mathrm{Area}pprox rac{1}{2}(y_0+y_1)\Delta x+rac{1}{2}(y_1+y_2)\Delta x+rac{1}{2}(y_2+y_3)\Delta x+\dots$$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal Rule}}$, for n trapezoids:

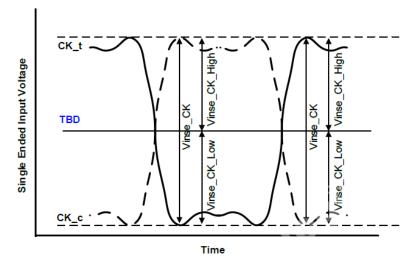
$$ig| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 50

Equation for Total_Area_Below_Vss

- *c* To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JEDEC specification.



The minimum input single-ended voltage is measured as shown in Figure 31.

Figure 51 Clock Single-ended Input Voltage definition

Vinse_CK_High (CK_c)

Availability Condition:	Table 105	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_c

Test ID & References: Table 106 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
 Vinse_CK_High	151013	Table 314

Overview: The purpose of this test is to verify the peak voltage of high pulse.

Procedure:

1 Pre-condition the oscilloscope.

- 2 Trigger on the rising edge of the clock signal under test.
- 3 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge.
- 4~ Zoom into the first pulse and measure $V_{\text{MAX}}.$
- 5 Calculate the value of Vinse_CK_High (CK_c) using the equation:

Vinse_CK_High (CK_c) = $V_{MAX} - V_{REF}$



For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

- 6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
- 7 Determine the worst result from the set of Vinse_CK_High (CK_c) measured.

Expected/The measured value of Vinse_CK_High (CK_c) for the test signal shall be within the conformanceObservable Results:limits as per the JEDEC specification.

Vinse_CK_Low (CK_c)

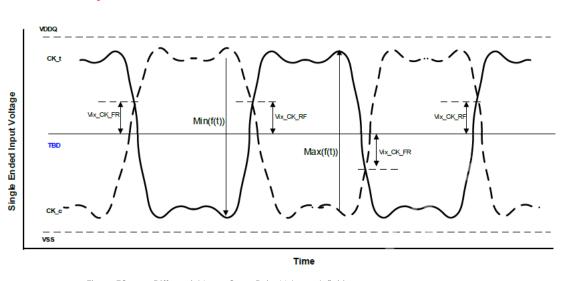
Availability Condition:	Table 107	Set Up tab options for availability of tests

Supported CK Type	Suppor	rted WCK Type	Supports Offline?	R/W Separation ne	eded? SE Mode?	Required Signals
Burst & Continuous	N/A		Yes	No	No	CK_c
Test ID & References:	Tabl	le 108 LPDDR	5 Test References from	n JESD209-5 specification		
	Sj	ymbol (in Specifica	ation)	Test ID	Referenc	e from Specification
	Vi	inse_CK_Low		151015	Table 314	4
Overview:	The	e purpose of t	his test is to veri	fy the peak voltage of	f low pulse.	
Procedure:	1	Pre-conditio	n the oscilloscop	e.		
	2	Trigger on th	e falling edge of	the clock signal unde	er test.	
	3			of the Clock in the er Clock starts at the va		and ends at the following vali
	4	Zoom into th	e first pulse and	measure V _{MIN} .		
	5	Calculate the	e value of Vinse_(CK_Low (CK_c) using	the equation:	
			١	/inse_CK_Low (CK_c)	$= V_{REF} - V_{MIN}$	
		NOTE		est, the Test App con r Measurement Three		VrefCA configuration value
	6 7			ith the rest of the neg om the set of Vinse_C		nd in the specified waveform

Expected/ Th Observable Results: lin

The measured value of Vinse_CK_Low (CK_c) for the test signal shall be within the conformance limits as per the JEDEC specification.

Clock (SE) CK_t & CK_c (Clock Plus & Minus) tests



The cross-point voltage of the differential input signals (CK_t, CK_c) is measured as shown in Figure 52.

Figure 52 Differential Input Cross Point Voltage definition

Vix_CK_ratio

Availability Condition: Table 109 Set Up table	options for availability of tests
--	-----------------------------------

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A	Yes	No	Yes	CK_t, CK_c	
Test ID & References:	Table 110 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Specification) Test ID Reference from Specification					
	Vix_CK_ratio		151016	Table 318		
Overview:		The purpose of this test is to verify the ratio of the calculated crossing point voltage from the value the measured crossing point voltage on the input differential pair test signals.				
	NOTE			p considers Vref to be the VrefCA asurement Thresholds).		

Procedure:

1

- Sample/Acquire data waveforms.
- 2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
- 3 Find the Vmax and Vmin of the differential signal denoted as Max(f(t)) and Min(f(t)) respectively.

- 4 Find the time-stamp of all differential CK crossing that crosses OV.
- 5 Use V_{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.
- 6 At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and V_{Ref}. The rising and falling crosspoint voltage differential is denoted as Vix_CK_RF and Vix_CK_FR respectively.
- 7 For each cross point voltage, calculate the final result using the equation (for Rising):

V_{IX}_CK_ratio = 100% x [Vix_CK_RF/Max(f(t))]

8 For each cross point voltage, calculate the final result using the equation (for Falling):

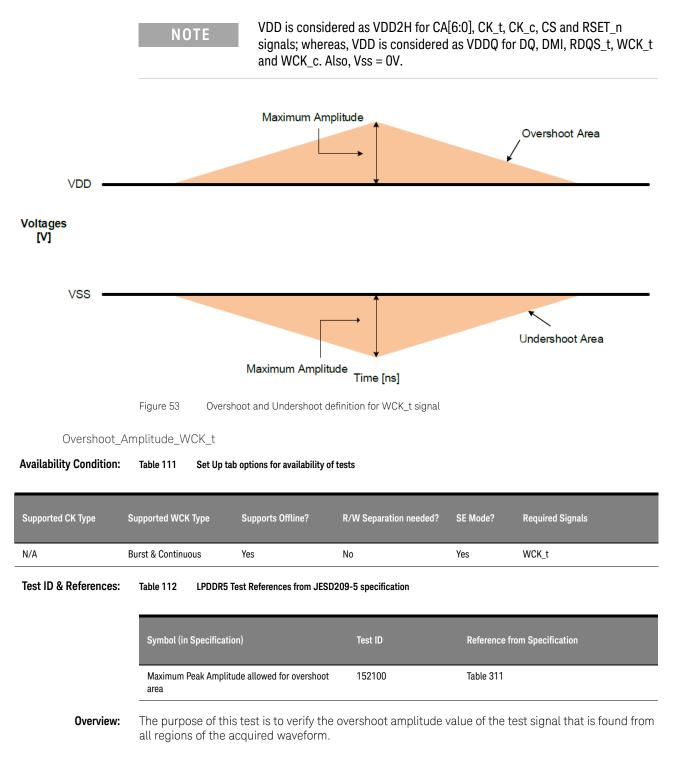
 V_{IX} CK_ratio = 100% x [Vix_CK_FR/Min(f(t))]

9 Determine the worst result from the set of V_{IX} -CK_ratio measured.

Expected/ The calculated value of the crossing point voltage ratio for the differential test signal pair shall be within the conformance limits as per the JEDEC specification in the References section.

Write Clock (SE) WCK_t (Write Clock Plus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 53.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

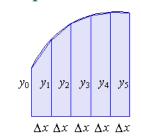
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 54 Equation for Total_Area_Above_OV

d Calculate Area_Above_ V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

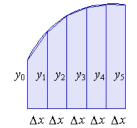
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Amplitude_WCK_t

Availability Condition: Table 113 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	Burst & Continuous	Yes	No	Yes	WCK_t		
Test ID & References	Table 114 LPDDR	Table 114 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Specifica	Symbol (in Specification) Test ID Reference from Specification					
	Maximum Peak Amplitude allowed for undershoot 152101 Table 311 area						
Test Overview:		nis test is to verify t of the acquired wav		le value of th	e test signal that is found		
	In case of an unc Calculation.	lershoot, the under	shoot area is calculated	based on th	e Trapezoidal Method Area		
Test Procedure:		iire signal data and e adjustment).	perform signal conditio	ning to maxi	mize screen resolution		
	An "Undersho						
	3 Within Under	shootRegion # 1:					
	a Evaluate U	ndershoot Amplitu	de by:				
		T _{MIN} , V _{MIN} to obta rshootRegion.	in the time-stamp of the	e minimum v	oltage on the		
	ii Calcu	lating Undershoot /	Amplitude using the equ	uation:			
		Und	dershoot Amplitude = V	ss - V _{MIN}			
	b Evaluate T	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:		

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg[\operatorname{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_0}{2}\Big)$	$\left(\frac{n}{2}\right)$
---	----------------------------

Figure 55 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

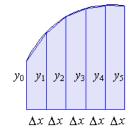
Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_WCK_t

Availability Condition: Table 115 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	Burst & Continuous	Yes	No	Yes	WCK_t			
Test ID & References:	es: Table 116 LPDDR5 Test References from JESD209-5 specification							
	Symbol (in Specifica	Symbol (in Specification) Test ID Reference from Specification						
	Maximum overshoot	area above V _{DD2H} /V _{DDQ}	152102	Table 311				
Overview:		nis test is to verify the acquired waveform		value of the t	test signal that is found from			
	When there is ov overshoot amplit		noot area is calculated b	ased on the	overshoot width and			
Procedure:		uire signal data and e adjustment).	perform signal conditio	ning to maxi	mize screen resolution			
		otRegion" starts at	oss the acquired wavefo the rising edge of V_{DDQ}		l ends at the falling edge of			
	3 Within Overs	hootRegion # 1:						
	<i>a</i> Evaluate C	vershoot Amplitud	e by:					
		J T _{MAX} , V _{MAX} to obt shootRegion.	ain the time-stamp of th	ie maximum	voltage on the			
	ii Calcu	late Overshoot Am	plitude using the equation	on:				
		Ove	ershoot Amplitude = V _{MA}	_X - V _{DDQ}				
	b Evaluate A	rea_below_V _{DDQ} u	sing the equation:					
	Area	_below_V _{DDQ} = (Ov	ershootRegion_End - Ov	vershootRegi	ion_Start) x V _{DDQ}			
	c Evaluate T	otal_Area_Above_0	V by using Trapezoidal N	/lethod Area	Calculation:			

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 56 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

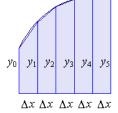
- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Area_WCK_t

Availability Condition: Table 117 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	Burst & Continuous	Yes	No	Yes	WCK_t	
Test ID & References:	Table 118 LPDDR5	Test References from JE	SD209-5 specification			
				_		
	Symbol (in Specificat	ion)	Test ID	Reference	from Specification	
	Maximum undershoot	area above VSS	152103	Table 311		
Overview:	from all regions o	f the acquired wav	he undershoot amplituc eform. In case of an unc width and undershoot	dershoot, the	e test signal that is found undershoot area is	
Procedure:	1 Sample/acqu (vertical scale		perform signal conditio	ning to maxi	mize screen resolution	
	2 Find the "Und	ershootRegion" ac otRegion" starts at	cross the acquired wavef t the falling edge of Vss		g and ends at the rising edge	
		ndershoot Amplitu	5			
		I _{MIN} , V _{MIN} to obta shootRegion.	in the time-stamp of the	e minimum v	oltage on the	
	ii Calcul	ating Undershoot /	Amplitude using the equ	uation:		
		Und	dershoot Amplitude = Vs	ss - V _{MIN}		
	b Evaluate To	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:	
		The Trapezo	idal Rule			



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal Rule}}$, for n trapezoids:

$$igg[\operatorname{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)\,igg]$$

Figure 57

Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JEDEC specification.

Vinse_WCK_High (WCK_t)

Availability Condition: Table 119 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Typ	e Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	Burst	Yes	No	No	WCK_t			
Test ID & References:	Table 120 LF	PDDR5 Test References from	JESD209-5 specification					
	Symbol (in Spe	cification)	Test ID	Reference	from Specification			
	Vinse_WCK_Hig	gh	151112	Table 320				
Overview:	The purpose	of this test is to verify	y the peak voltage of high	pulse.				
Procedure:	1 Pre-condition the oscilloscope.							
	2 Trigger on the rising edge of the write clock signal under test.							
		ositive pulse on the V	f the Write Clock in the er /rite Clock starts at the va		m. ge and ends at the followin			
	4 Zoom int	o the first pulse and r	measure V _{MAX} .					
	5 Calculate the value of Vinse_WCK_High (WCK_t) using the equation:							
	Vinse_WCK_High (WCK_t) = $V_{MAX} - V_{REF}$							
	NOTE For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).							
					in the specified waveform.			
	7 Determir	7 Determine the worst result from the set of Vinse_WCK_High (WCK_t) measured.						

Expected/ Observable Results: The measured value of Vinse_WCK_High (WCK_t) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_WCK_Low (WCK_t)

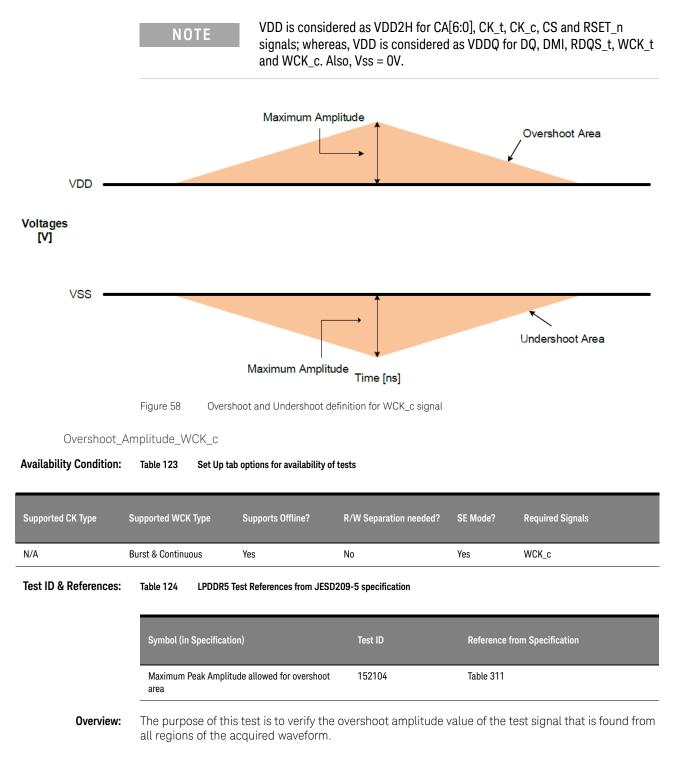
Availability Condition: Table 121 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	Burst	Yes	No	No	WCK_t			
Test ID & References:	Table 122 LPDDR	5 Test References from JE	SD209-5 specification					
	Symbol (in Specifica	ation)	Test ID	Reference	from Specification			
	Vinse_WCK_Low		151114	Table 320				
Overview:	The purpose of t	his test is to verify t	he peak voltage of low p	oulse.				
Procedure:	1 Pre-condition the oscilloscope.							
	2 Trigger on th	2 Trigger on the falling edge of the write clock signal under test.						
		tive pulse on the Wr	the Write Clock in the ei ite Clock starts at the va		rm. Ige and ends at the following			
	4 Zoom into th	ie first pulse and me	easure V _{MIN} .					
	5 Calculate the	e value of Vinse_W0	CK_Low (WCK_t) using t	he equation:	:			
		Vinse	$WCK_Low (WCK_t) = V$	/ _{REF} - V _{MIN}				
NOTE For Write Clock (WCK) signal, the Test App considered configuration value (set under Measurement Three)								
			the rest of the negative the set of Vinse_WCK_L	•	d in the specified waveform.			

Expected/ Observable Results: The measured value of Vinse_WCK_Low (WCK_t) for the test signal shall be within the conformance limits as per the JEDEC specification.

Write Clock (SE) WCK_c (Write Clock Minus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

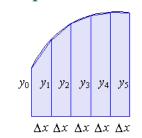
- **Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}}, V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$\mathrm{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_n}{2}\Big)$$

Figure 59 Equation for Total_Area_Above_OV

d Calculate Area_Above_ V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

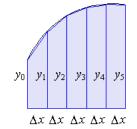
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Amplitude_WCK_c

Availability Condition: Table 125 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	Burst & Continuous	Yes	No	Yes	WCK_c		
Test ID & References:	Table 126 LPDDR	Table 126 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Specifica	from Specification					
	Maximum Peak Ampl area	itude allowed for undersho	oot 152105	Table 311			
Overview:		The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.					
	In case of an unc Calculation.	lershoot, the unders	shoot area is calculated	based on th	e Trapezoidal Method Area		
Procedure:		iire signal data and e adjustment).	perform signal conditic	ning to maxi	mize screen resolution		
	An "Undersho						
	3 Within Under	shootRegion # 1:					
	a Evaluate U	Indershoot Amplitue	de by:				
		T _{MIN} , V _{MIN} to obta rshootRegion.	in the time-stamp of the	e minimum v	oltage on the		
	ii Calcu	lating Undershoot /	Amplitude using the equ	uation:			
		Unc	dershoot Amplitude = V	ss - V _{MIN}			
	b Evaluate Te	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:		

The Trapezoidal Rule



$$\operatorname{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg { m Area}pprox \Delta x \Big({y_0\over 2} + y_1 + y_2 + y_3 + \ldots +$	$\left(\frac{y_n}{2}\right)$	
--	------------------------------	--

Figure 60 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

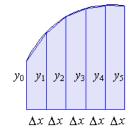
Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_WCK_c

Availability Condition: Table 127 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	Burst & Continuous	Yes	No	Yes	WCK_c			
Test ID & References:	Table 128 LPDDR	Table 128 LPDDR5 Test References from JESD209-5 specification						
	Symbol (in Specifica	Symbol (in Specification) Test ID Reference from Specification						
	Maximum overshoot	area above V _{DD2H} /V _{DDQ}	152106	Table 311				
Overview:		his test is to verify th acquired waveform		value of the t	test signal that is found from			
	When there is ov overshoot ampli		noot area is calculated b	ased on the	overshoot width and			
Procedure:		uire signal data and e adjustment).	perform signal conditio	ning to maxi	mize screen resolution			
		otRegion" starts at [.]	oss the acquired wavefo the rising edge of V_{DDQ}		ends at the falling edge of			
	3 Within Overs	hootRegion # 1:						
	a Evaluate (Overshoot Amplitude	e by:					
		g T _{MAX} , V _{MAX} to obta shootRegion.	ain the time-stamp of th	ie maximum	voltage on the			
	ii Calcu	Ilate Overshoot Am	plitude using the equation	on:				
		Ove	ershoot Amplitude = V _{MA}	_X - V _{DDQ}				
	b Evaluate A	Area_below_V _{DDQ} us	sing the equation:					
	Area	_below_V _{DDQ} = (Ov	ershootRegion_End - 0\	vershootRegi	on_Start) x V _{DDQ}			
	c Evaluate T	otal_Area_Above_0	V by using Trapezoidal N	/lethod Area	Calculation:			

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 61 Equation for Total_Area_Above_OV

d Calculate Area_Above_ V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

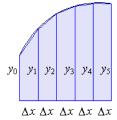
- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Area_WCK_c

Availability Condition: Table 129 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	Burst & Continuous	Yes	No	Yes	WCK_c		
Test ID & References:	ICES: Table 130 LPDDR5 Test References from JESD209-5 specification						
	Symbol (in Specifica	Symbol (in Specification) Test ID Reference from Specification					
	Maximum undershoo	ot area above VSS	152107	Table 311			
Overview:	from all regions	The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.					
Procedure:		uire signal data and e adjustment).	perform signal conditio	ning to maxi	mize screen resolution		
		ootRegion" starts a	cross the acquired wavef t the falling edge of Vss		g and ends at the rising edge		
		rshootRegion # 1:					
	a Evaluate l	Jndershoot Amplitu	de by:				
		g T _{MIN} , V _{MIN} to obta rshootRegion.	in the time-stamp of the	e minimum v	oltage on the		
	ii Calcu	lating Undershoot	Amplitude using the equ	lation:			
		Un	dershoot Amplitude = Vs	s - V _{MIN}			
	b Evaluate T	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:		
		The Trapezo	oidal Rule				



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

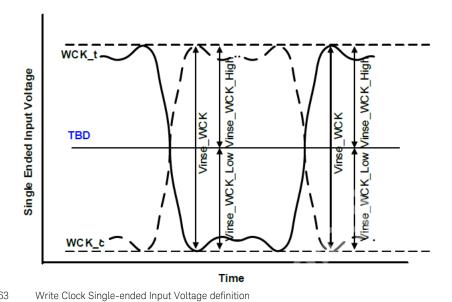
$$igg| \operatorname{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 62

Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JEDEC specification.



The minimum input single-ended voltage is measured as shown in Figure 63.

Figure 63

Vinse_WCK_High (WCK_c)

Availability Condition: Table 131 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	Burst	Yes	No	No	WCK_c		
Test ID & References:	Table 132 LPDDR	Table 132 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Specifica	Symbol (in Specification) Test ID Reference from Specification					
	Vinse_WCK_High		151113	Table 320			
Overview:	The purpose of t	his test is to verify t	he peak voltage of high	pulse.			
Procedure:	1 Pre-conditio	n the oscilloscope.					
	3 Find all valid A valid positi valid falling e	 2 Trigger on the rising edge of the write clock signal under test. 3 Find all valid positive pulses of the write clock in the entire waveform. A valid positive pulse on the Write Clock starts at the valid rising edge and ends at the followin valid falling edge. 					
	5 Calculate the	e value of Vinse_WC	K_High (WCK_c) using	the equation	1:		

Vinse_WCK_High (WCK_c) = $V_{MAX} - V_{REF}$

NOTE

For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).

- 6 Continue the previous step with the rest of the positive pulses found in the specified waveform.
- 7 Determine the worst result from the set of Vinse_WCK_High (WCK_c) measured.

Expected/ Observable Results: The measured value of Vinse_WCK_High (WCK_c) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_WCK_Low (WCK_c)

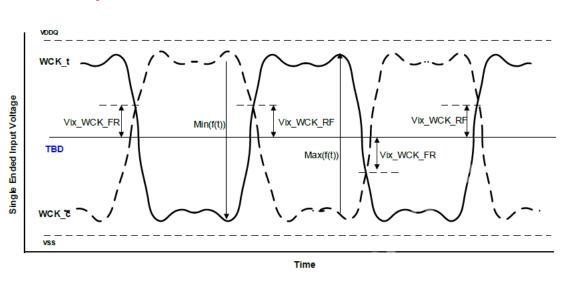
Availability Condition: Table 133 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	WCK_c
Test ID & References:	Table 134 LPDDR	25 Test References from JE	SD209-5 specification		
	Symbol (in Specific	ation)	Test ID	Reference	from Specification
	Vinse_WCK_Low		151115	Table 320	
Overview:	The purpose of t	this test is to verify t	he peak voltage of low p	oulse.	
Procedure:	1 Pre-conditio	n the oscilloscope.			
	2 Trigger on th	ne falling edge of th	e write clock signal unde	er test.	
		tive pulse on the Wr	the Write Clock in the ei ite Clock starts at the va		rm. Ige and ends at the followin
	-	ne first pulse and me	easure V _{MIN} .		
	5 Calculate th	e value of Vinse_W(CK_Low (WCK_c) using t	he equation	:
		Vinse	_WCK_Low (WCK_c) = \	/ _{REF} - V _{MIN}	
	NOTE For Write Clock (WCK) signal, the Test App considers Vref to be the V configuration value (set under Measurement Thresholds).				
			the rest of the negative the set of Vinse_WCK_L	•	d in the specified waveform

Expected/ The measured value **Observable Results:** limits as per the JEE

The measured value of Vinse_WCK_Low (WCK_c) for the test signal shall be within the conformance limits as per the JEDEC specification.

Write Clock (SE) WCK_t & WCK_c (Write Clock Plus & Minus) tests



The cross-point voltage of the differential input signals (WCK_t, WCK_c) is measured as shown in Figure 64.

Figure 64 Differential Input Cross Point Voltage definition for WCK signal

Vix_WCK_ratio

Availability Condition:	Table 135	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	No	WCK_t, WCK_c
Test ID & References: Table 136 LPDDR5 Test References from JESD209-5 specification					

Symbol (in Specification)	Test ID	Reference from Specification
Vix_WCK_ratio	151116	Table 324

Overview:

The purpose of this test is to verify the ratio of the calculated crossing point voltage from the value of the measured crossing point voltage on the input differential pair test signals.



For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).

Procedure:

- 1 Sample/Acquire data waveforms.
- 2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
- 3 Find the Vmax and VMin of the differential signal denoted as Max(f(t)) and Min(f(t)) respectively.

- 4 Find the time-stamp of all differential WCK crossing that crosses OV.
- 5 Use V_{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.
- 6 At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and V_{Ref}. The rising and falling crosspoint voltage differential is denoted as Vix_WCK_RF and Vix_WCK_FR respectively.
- 7 For each cross point voltage, calculate the final result using the equation (for Rising):

V_{IX}_WCK_ratio = 100% x [Vix_WCK_RF/Max(f(t))]

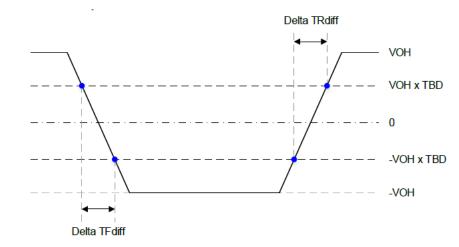
8 For each cross point voltage, calculate the final result using the equation (for Falling):

V_{IX}_WCK_ratio = 100% x [Vix_WCK_FR/Min(f(t))]

9 Determine the worst result from the set of V_{IX} -WCK_ratio measured.

Expected/ The calculated value of the crossing point voltage ratio for the differential test signal pair shall be within the conformance limits as per the JEDEC specification in the References section.

Read Data Strobe (Diff) tests



Output slew rate for differential signals are measured as shown in Figure 30.

Figure 65 Differential output slew rate definition for RDQS signal

SRQdiffR_RDQS

Availability Condition:	Table 137	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	No	DQ, RDQS(Diff)

Test ID & References: Table 138 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
SRQdiff	150002	Table 326

Overview: The purpose of this test is to verify the differential output slew rate for rising edge of the test signal within the read burst.

Procedure: 1 Acquire and split the read and write burst of the acquired signal.

- 2 Take the first valid READ burst found.
- 3 Find all the valid Strobe rising edges in the specified burst. A valid Strobe rising edge starts at V_{OL} crossing and ends at the following V_{OH} crossing.
- $\begin{array}{ll} \mbox{4} & \mbox{For all the valid Strobe rising edges, find the transition time, T_R.} \\ & \mbox{T_R}$ is the time starting at V_{OL} crossing and ending at the following V_{OH} crossing.} \end{array}$
- 5 Calculate SRQdiffR using the equation:

$$SRQdiffR = [V_{OH} - V_{OI}] / T_R$$

6 Determine the worst result from the set of SRQdiffR measured.

Expected/ The measured value of SRQdiffR for the test signal shall be within the conformance limits as per the JEDEC specification.

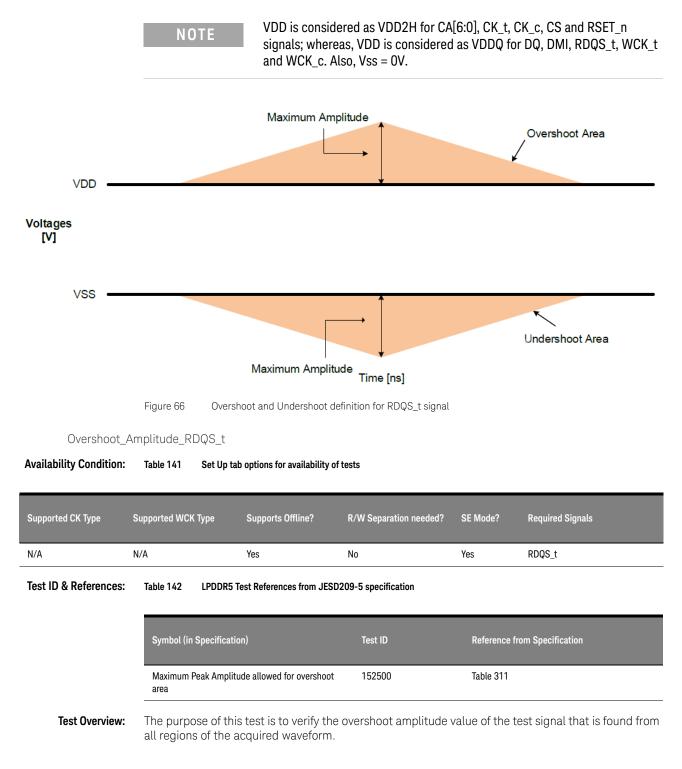
SRQdiffF_RDQS

Availability Condition: Table 139 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	No	DQ, RDQS(Diff)
Test ID & References:	Table 140 LPDDR5	Test References from JE	SD209-5 specification		
	Symbol (in Specificati	ion)	Test ID	Reference	from Specification
	SRQdiff		150003	Table 326	
Overview:	The purpose of th within the read bu		he differential output sl	ew rate for fa	alling edge of the test signal
Procedure:	 Acquire and split the read and write burst of the acquired signal. Take the first valid READ burst found. Find all the valid Strobe falling edges in the specified burst. A valid Strobe falling edge starts at V_{OH} crossing and ends at the following V_{OL} crossing. For all the valid Strobe falling edges, find the transition time, T_F. T_F is the time starting at V_{OH} crossing and ending at the following V_{OL} crossing. Calculate SRQdiffF using the equation: 				
Expected/ Observable Results:	SRQdiffF = [V _{OH} - V _{OL}] / T _F 6 Determine the worst result from the set of SRQdiffF measured. The measured value of SRQdiffF for the test signal shall be within the conformance limits as per the JEDEC specification.				

Read Data Strobe (SE) RDQS_t (Read Data Strobe Plus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

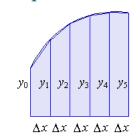
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}},\,V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude = $V_{MAX} - V_{DDQ}$

b Evaluate Area_below_V_{DDQ} using the equation:

Area_below_V_{DDQ} = (OvershootRegion_End - OvershootRegion_Start) x V_{DDQ}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 67 Equation for Total_Area_Above_OV

d Calculate Area_Above_ V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_OV - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

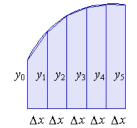
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Amplitude_RDQS_t

Availability Condition: Table 143 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A	Yes	No	Yes	RDQS_t		
Test ID & References:	Table 144 LPDDR	5 Test References from JE	SD209-5 specification				
	Symbol (in Specifica	tion)	Test ID	Reference f	from Specification		
	Maximum Peak Ampl area	itude allowed for undersho	oot 152501	Table 311			
Test Overview:		nis test is to verify t of the acquired wav		le value of th	e test signal that is found		
	In case of an unc Calculation.	lershoot, the under	shoot area is calculated	based on th	e Trapezoidal Method Area		
Test Procedure:		iire signal data and e adjustment).	perform signal conditio	ning to maxi	mize screen resolution		
	An "Undersho	-					
	3 Within Under	shootRegion # 1:					
	a Evaluate U	Indershoot Amplitu	de by:				
		i Using T _{MIN} , V _{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.					
	ii Calcu	lating Undershoot /	Amplitude using the equ	uation:			
		Und	dershoot Amplitude = V	ss - V _{MIN}			
	b Evaluate Te	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:		

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg[\operatorname{Area}pprox\Delta x \Big(rac{y_0}{2}+y_1+y_2+y_3+\ldots+rac{y_0}{2}\Big)$	$\left(\frac{n}{2}\right)$
---	----------------------------

Figure 68 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

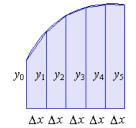
Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_RDQS_t

Availability Condition: Table 145 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_t
Test ID & References:	Table 146 LPDDR5	i Test References from JE	SD209-5 specification		
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	Maximum overshoot	area above V _{DD2H} /V _{DDQ}	152502	Table 311	
Test Overview:		nis test is to verify th acquired waveform		value of the ⁻	test signal that is found from
	When there is ov overshoot amplit		oot area is calculated b	ased on the	overshoot width and
Test Procedure:		ire signal data and adjustment).	perform signal conditio	ning to maxi	mize screen resolution
			bss the acquired wavefo the rising edge of V _{DDQ}		l ends at the falling edge of
	V _{DDQ} crossing			Ū	
		nootRegion # 1:			
		vershoot Amplitude	2		
	i Using Overs	T _{MAX} , V _{MAX} to obta hootRegion.	ain the time-stamp of th	ie maximum	voltage on the
	ii Calcu	late Overshoot Amp	olitude using the equation	on:	
		Ove	rshoot Amplitude = V _{MA}	_X - V _{DDQ}	
	b Evaluate A	rea_below_V _{DDQ} us	ing the equation:		
	Area_	_below_V _{DDQ} = (Ove	ershootRegion_End - 0\	vershootRegi	ion_Start) x V _{DDQ}
	c Evaluate To	otal_Area_Above_0	√ by using Trapezoidal N	Nethod Area	Calculation:

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 69 Equation for Total_Area_Above_OV

d Calculate Area_Above_ V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DDQ}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

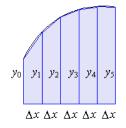
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Area_RDQS_t

Availability Condition: Table 147 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	N/A	Yes	No	Yes	RDQS_t			
Test ID & References:	Table 148 LPDDR	Table 148 LPDDR5 Test References from JESD209-5 specification						
	Symbol (in Specifica	ation)	Test ID	Reference	from Specification			
	Maximum undersho	ot area above VSS	152503	Table 311				
Test Overview:	from all regions	of the acquired wav	he undershoot amplitud eform. In case of an unc width and undershoot a	lershoot, the	ne test signal that is found e undershoot area is			
Test Procedure:		1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).						
	 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing. 							
		0	the falling edge of Vss ((UV) crossing	g and ends at the rising edgi			
	of Vss (0V) c	0	the falling edge of Vss ((UV) Crossing	g and ends at the rising edgi			
	of Vss (OV) c 3 Within Unde	rossing.		(UV) crossinę	g and ends at the rising edg			
	of Vss (OV) c 3 Within Unde a Evaluate U i Using	rossing. rshootRegion # 1: Jndershoot Amplitud						
	of Vss (0V) c 3 Within Unde a Evaluate L i Using Unde	rossing. rshootRegion # 1: Jndershoot Amplitud g T _{MIN} , V _{MIN} to obtai rshootRegion.	de by:	e minimum v				
	of Vss (0V) c 3 Within Unde a Evaluate L i Using Unde	rossing. rshootRegion # 1: Jndershoot Amplitud J T _{MIN} , V _{MIN} to obtai rshootRegion. Ilating Undershoot A	de by: in the time-stamp of the	e minimum v lation:				

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal\ Rule}}$, for n trapezoids:

$$igg| \operatorname{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 70

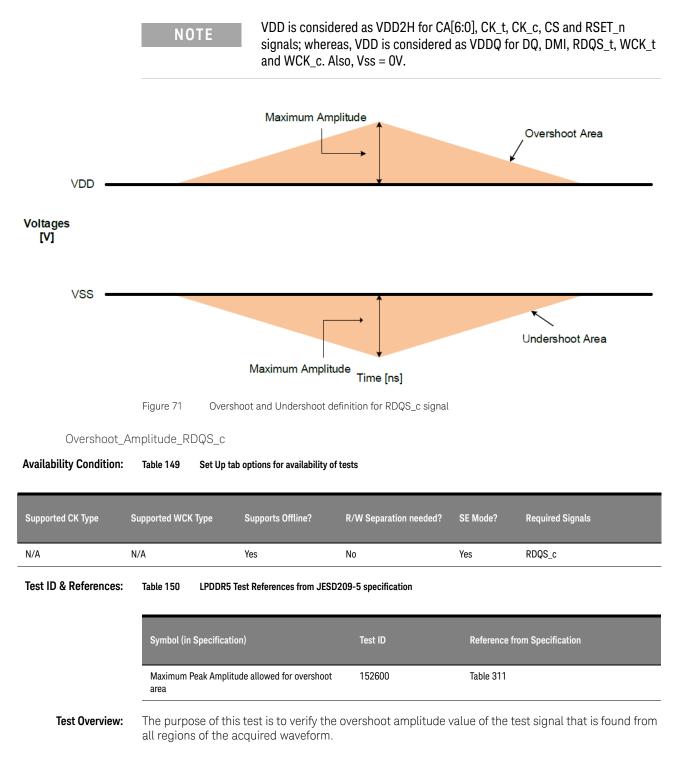
Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JEDEC specification.

Read Data Strobe (SE) RDQS_c (Read Data Strobe Minus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.



When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

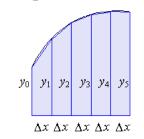
- **Test Procedure:** 1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).
 - 2 Find the "OvershootRegion" across the acquired waveform. An "OvershootRegion" starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DDQ} crossing.
 - 3 Within OvershootRegion # 1:
 - a Evaluate Overshoot Amplitude by:
 - i Using $T_{\text{MAX}}, V_{\text{MAX}}$ to obtain the time-stamp of the maximum voltage on the OvershootRegion.
 - ii Calculate Overshoot Amplitude using the equation:

Overshoot Amplitude =
$$V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

Area_below_V_{DD} = (OvershootRegion_End - OvershootRegion_Start) x V_{DD}

c Evaluate Total_Area_Above_OV by using Trapezoidal Method Area Calculation:



The Trapezoidal Rule

Area
$$\approx rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the **Trapezoidal Rule**, for n trapezoids:

$$ext{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 72 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD} using the equation:

Area_Above_V_{DD} = Total_Area_Above_OV - Area_below_V_{DD}

- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

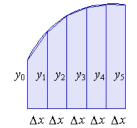
Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Amplitude_RDQS_c

Availability Condition: Table 151 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
N/A	N/A	Yes	No	Yes	RDQS_c	
Test ID & References	Table 152 LPDDR	5 Test References from JE	SD209-5 specification			
	Symbol (in Specifica	ation)	Test ID	Reference f	rom Specification	
	Maximum Peak Amp area	litude allowed for undersho	pot 152601	Table 311		
Test Overview		his test is to verify t of the acquired wav		le value of th	e test signal that is found	
	In case of an une Calculation.	dershoot, the under	shoot area is calculated	based on th	e Trapezoidal Method Area	
Test Procedure		uire signal data and e adjustment).	perform signal conditio	ning to maxi	mize screen resolution	
	An "Undersh	 Find the "UndershootRegion" across the acquired waveform. An "UndershootRegion" starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing. 				
	3 Within Unde	rshootRegion # 1:				
	a Evaluate l	Jndershoot Amplitu	de by:			
		i Using T _{MIN} , V _{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.				
	ii Calcu	ulating Undershoot /	Amplitude using the equ	uation:		
		Und	dershoot Amplitude = V	ss - V _{MIN}		
	b Evaluate 1	otal_Area_Below_V	ss by using Trapezoidal	Method Area	Calculation:	

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$igg \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + 2 \Big)$	$\left(\frac{y_n}{2}\right)$
---	------------------------------

Figure 73 Equation for Total_Area_Below_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limit.

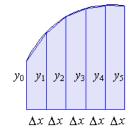
Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_RDQS_c

Availability Condition: Table 153 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_c
Test ID & References:	Table 154 LPDDR	5 Test References from JE	SD209-5 specification		
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	Maximum overshoot	area above V _{DD2H} /V _{DDQ}	152602	Table 311	
Overview:		nis test is to verify th acquired waveform		value of the [.]	test signal that is found from
	When there is ov overshoot amplit		oot area is calculated b	ased on the	overshoot width and
Procedure:		iire signal data and e adjustment).	perform signal conditio	ning to maxi	mize screen resolution
		otRegion" starts at t	oss the acquired wavefor the rising edge of V _{DD} cl		ends at the falling edge of
		hootRegion # 1:			
	a Evaluate C	vershoot Amplitude	e by:		
		T _{MAX} , V _{MAX} to obta hootRegion.	ain the time-stamp of th	e maximum	voltage on the
	ii Calcu	late Overshoot Am	olitude using the equation	on:	
		Ove	ershoot Amplitude = V _M	_{AX} - V _{DD}	
	b Evaluate A	rea_below_V _{DD} usi	ng the equation:		
		88	ershootRegion_End - Ov V by using Trapezoidal N	-	88

The Trapezoidal Rule



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the Trapezoidal Rule, for n trapezoids:

$$igg| \mathrm{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 74 Equation for Total_Area_Above_OV

d Calculate Area_Above_V_{DD} using the equation:

Area_Above_V_{DD} = Total_Area_Above_OV - Area_below_V_{DD}

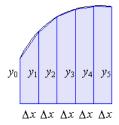
- e To find the worst case, save the following calculated results for later use:
 - Overshoot Amplitude
 - Area_Above_V_{DD}
- 4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/ The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per **Observable Results:** the JEDEC specification.

Undershoot_Area_RDQS_c

Availability Condition: Table 155 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A	Yes	No	Yes	RDQS_c		
Test ID & References:	Table 156 LPDDR	5 Test References from JE	SD209-5 specification				
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification		
	Maximum undershoo	ot area above VSS	152603	Table 311			
Overview:	from all regions	The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.					
Procedure:	(vertical scale 2 Find the "Un	e adjustment). dershootRegion" ac	perform signal conditio	orm.	mize screen resolution g and ends at the rising edge		
	of Vss (0V) ci	rossing.			g and ondo at the hoing odgo		
		rshootRegion # 1: Indershoot Amplitu	de hv:				
	i Using		in the time-stamp of the	e minimum v	roltage on the		
	ii Calcu	lating Undershoot	Amplitude using the equ	uation:			
		Un	dershoot Amplitude = Vs	ss - V _{MIN}			
	b Evaluate T	otal_Area_Below_V	ss by using Trapezoidal	Method Area	a Calculation:		
		The Trapezo	oidal Rule				



$$ext{Area} pprox rac{1}{2}(y_0+y_1)\Delta x + rac{1}{2}(y_1+y_2)\Delta x + rac{1}{2}(y_2+y_3)\Delta x + \dots$$

We can simplify this to give us the $\ensuremath{\mathbf{Trapezoidal Rule}}$, for n trapezoids:

$$igg| \operatorname{Area} pprox \Delta x \Big(rac{y_0}{2} + y_1 + y_2 + y_3 + \ldots + rac{y_n}{2} \Big)$$

Figure 75

5 Equation for Total_Area_Above_Vss

- c To find the worst case, save the following calculated results for later use:
 - Undershoot Amplitude
 - Total_Area_Below_Vss
- 4 Repeat step 3 for the rest of the "UndershootRegion" found in the acquired waveform.
- 5 Find the worst result from the stored results listed above.
- 6 Compare the test result with the compliance test limits.

Expected/The values for Undershoot Amplitude and Area measurement shall be within the conformance limitsObservable Results:as per the JEDEC specification.

4 Electrical Tests

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

5 Timing Tests

RDQS Detect Method for Read Write Separation 166 Clock (Diff) Tests 168 Clock (SE Mode) Tests 177 Write Clock (Diff) tests 180 Write Clock (SE Mode) Tests 192 Other timing tests 195



RDQS Detect Method for Read Write Separation

RDQS Detect is a read write separation method. This method works when the signal source contains at least an RDQS signal and a WCK signal. In this method, the Read/Write burst data is identified based on the presence of RDQS burst. If WCK burst contains an RDQS burst, then it is a Read burst. If the WCK burst does not contain an RDQS burst, then it is a Write burst.

If you select the RDQS Detect mode as the burst identification method, you must select the length of the WCK Postamble in the WCK Postamble Length section of the LPDDR5 General Setup dialog box.

LPDDR5 General Setup	?				
Set the data rate of the I	test signal by entering a custom value or select from the				
3200 MT					
WCK : CK Ratio 2:1	WCK Frequency : 1600 MHz Clock Frequency : 800 MHz				
Signal Source					
	nal source input for the current test trial. This option will test measurements. When the value for this option change, It will be reset.				
WCK_t (SE), WCK_c	(SE), RDQS_t (SE), RDQS_c (SE)				
Single-Ended M	ode				
Signal Operation Mod	e				
	ode of the signal source.				
CK (Diff) Continuou	is 🕑				
WCK (Diff) Burst	Burst WCK options				
RDQS Preamble/Posta	amble Length				
	QS Preamble and Postamble.				
RDQS Preamble	Static: 4 tWCK, Toggle: 0 tWCK				
RDQS Postamble	0.5 tWCK				
RDQS Postamble Mode Toggle					
WCK Postamble Length					
Identify the length of WCK Postamble.					
WCK Postamble	2.5 tWCK				
	2.5 tWCK				
🖌 Show Hints	4.5 tWCK OK Cancel				
	6.5 tWCK				

Figure 76 LPDDR5 General Setup Dialog



Figure 77 WCK Burst Options Setup Dialog

Tests that support the RDQS Detect Burst Identification Method

The following Timing tests support the RDQS Burst Identification method:

WRITE Tests

- tWCK2CK
- tWCKHL
- tWCKH
- tWCKL

READ Tests

- tRPRE
- tRPST
- tDQSQ
- tQSH
- tQSL

Method of Implementation for the RDQS Detect Burst Identification Method

The following are the steps for the method of implementation for the RDQS Detect burst identification method:

- 1 Populate the burst from WCK signal.
- 2 Locate FirstWCKRising for the burst.
- 3 Compute TimeA = FirstWCKRising + tWCKPRE_Toggle_RD * ClockCycleWidth.
- 4 Compute TimeB = Start of WCK postamble. For example, if tWCKPST=2.5nWCK then TimeB = time of second last rising edge of WCK burst. If tWCKPST=4.5nWCK then TimeB = time of fourth last rising edge of WCK burst.
- 5 Compute TimeC = 0.5*(TimeA+TimeB)
- 6 Compute VmaxTimeCWithinUI = Vmax range from (TimeC 1*UI) to (TimeC + 1*UI)
- 7 Compute VminTimeCWithinUI = Vmin range from (TimeC 1*UI) to (TimeC + 1*UI)
- 8 If [(VmaxTimeCWithinUI > VOHDiff_RDQS) AND (VminTimeCWithinUI < VOLDiff_RDQS)] then the burst will be recognized as a READ burst. Otherwise, the burst will be recognized as a WRITE burst.
- 9 Repeat steps 2 to 8 for the rest of burst.

Clock (Diff) Tests

The equations for the measurement of various parameters pertaining to Clock differential tests are given below:

$$tCK(avg) = \left(\sum_{j=1}^{N} tCKj\right)/N$$

where
$$N = 200$$

Figure 78 Calculation for tCK(avg)

$$tCH(avg) = \left(\sum_{j=1}^{N} tCHj\right) / (N \times tCK(avg))$$

where N = 200

Figure 79 Calculation for tCH(avg)

$$tCL(avg) = \left(\sum_{j=1}^{N} tCLj\right) / (N \times tCK(avg))$$

where N = 200

Figure 80 Calculation for tCL(avg)

tjit(per) = Min./Max. of {tCKi - tCK(avg), where i = 1 to 200}

Figure 81 Calculation for tjit(per)

Figure 82 Calculation for tjit(CC)



tCK(abs), tCH(abs) and tCL(abs) are measured directly on the Differential Clock signal and are considered as informative tests.

tCK(avg) Average Clock Period

Availability Condition: Table 157 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)		
Test ID & References:	Table 158 LPDDF	25 Test References from JI	SD209-5 specification				
	Symbol (in Specific	ation)	Test ID	Reference f	from Specification		
	tCK(avg)		102020		Tables 345 - 348		
Overview:					ndow. This test measures the waveform window.		
Procedure:	 period from the rising edge of a cycle to the next rising edge within the waveform window. Acquire 202 cycles from the test signal. Measure a sliding "window" of 200 cycles. Calculate the average period value for periods 1-200. Calculate the average period value for periods 2-201. Calculate the average period value for periods 3-202. Three measurement results are generated after step 4 is complete. Check the three measured results for the smallest and largest values, which are recorded as the worst case values. Campara the worst area values to the compliance test limits. 						
Expected/ Observable Results:		Compare the worst case values to the compliance test limits.The measured value of tCK(avg) shall be within the conformance limits as per the JESD209-5 specification.					

tCK(abs) Absolute Clock Period

Availability Condition: Table 159 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)		
Test ID & References:	Table 160 LPDDR5 Test References from JESD209-5 specification						
	Symbol (in Specificat	ion)	Test ID	Reference f	from Specification		
	tCK(abs)		102021		Tables 345 - 348		
Overview:			d within a waveform win t consecutive rising edge		st measures the period from waveform window.		
Procedure:	 Find the maxi Find the minir Check the two 	 Find the minimum period value for period 1-202. Check the two results for the worst case values. 					
Expected/ Observable Results:		5 Compare the worst case values to the compliance test limits. The measured value of tCK(abs) for the test signal is reported as "Information Only".					

tCH(avg) Average High pulse width

Availability Condition: Table 161 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)		
Test ID & References:	Table 162 LPDDF	R5 Test References from JI	SD209-5 specification				
	Symbol (in Specific	ation)	Test ID	Reference	from Specification		
	tCH(avg)		102022		Tables 345 - 348		
Overview:	tCH(avg) is the average pulse width across any consecutive 200 high pulses within a waveform window. This test measures the average duty cycle of all positive pulse widths within a window of 200 consecutive cycles.						
Procedure:	1 Acquire 202	cycles from the tes	signal.				
	2 Measure a s	liding "window" of 2	00 cycles.				
			ulses from cycle #1 to cy rates one measurement		nd determine the average		
		s window. This gene	ulses from cycle #2 to cy rates one more measure		d determine the average and two measurement		
	value for this						
	6 Check the three measured values for the smallest and largest values, which are recorded as worst case values.						
	7 Compare the	e worst case values	to the compliance test li	mits.			
/Expected Observable Results:	The measured v specification.	The measured value of tCH(avg) shall be within the conformance limits as per the JESD209-5					

tCL(avg) Average Low pulse width

Availability Condition: Table 163 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals					
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)					
Test ID & References:	Table 164 LPDDF	5 Test References from JE	SD209-5 specification							
	Symbol (in Specific	ation)	Test ID	Reference	from Specification					
	tCL(avg)		102023		Tables 345 - 348					
Overview:	window. This tes	tCL(avg) is the average pulse width across any consecutive 200 low pulses within a waveform window. This test measures the average duty cycle of all negative pulse widths within a window of 200 consecutive cycles.								
Procedure:		cycles from the test	0							
	3 Measure the		2		determine the average value					
					determine the average value wo measurement values					
		5 Measure the width of the low pulses from cycle#3 to cycle#202 and determines the average variable for this window. This generates one more measurement result and three measurement results.								
	7 Compare the	7 Compare the worst case values to the compliance test limits.								
/Expected Observable Results:	The measured v specification.	alue of tCL(avg) sha	ll be within the conform	ance limits a	The measured value of tCL(avg) shall be within the conformance limits as per the JESD209-5					

tCH(abs) Absolute HIGH Clock pulse width

Availability Condition: Table 165 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)
Test ID & References:	Table 166 LPDDR5	Test References from JE	SD209-5 specification		
	Symbol (in Specificat	ion)	Test ID	Reference	from Specification
	tCH(abs)		102024		Tables 345 - 348
Overview:	the following falli		measures the absolute c		ured from one rising edge t all positive pulse widths
Procedure:	 Acquire 202 cycles from the test signal. Find the maximum high pulses width value for positive pulses #1 to #202. Find the minimum high pulses width value for positive pulses #1 to #202. Check these two results for the worst case values. Compare the worst case values to the compliance test limits. 				
Expected/ Observable Results:			the test signal is reporte		nation Only".

tCL(abs) Absolute LOW Clock pulse width

Availability Condition: Table 167 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)		
Test ID & References:	Table 168 LPDDR5	Test References from JE	SD209-5 specification				
	Symbol (in Specifica	tion)	Test ID	Reference f	rom Specification		
	tCL(abs)		102025		Tables 345 - 348		
Overview:	the following risi		neasures the absolute d		ed from one falling edge to all negative pulse widths		
Procedure:	1 Acquire 202 d	cycles from the test	signal.				
	2 Find the max	mum low pulses w	idth value for negative p	ulses #1 to #	ŧ202.		
	3 Find the mini	mum low pulses wi	dth value for negative p	ulses #1 to #	202.		
	4 Check these two results for the worst case values.						
	5 Compare the	5 Compare the worst case values to the compliance test limits.					
Expected/ Observable Results:	The measured va	lue of tCL(abs) for	the test signal is reporte	d as "Inform	ation Only".		

tjit(CC) Maximum Clock Jitter between consecutive cycles

Availability Condition: Table 169 Set Up tab options for availability of tests

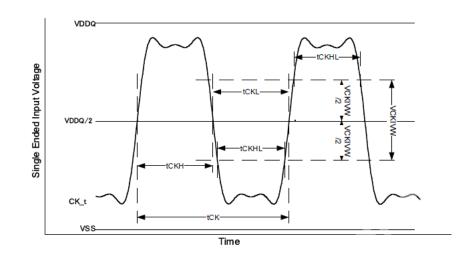
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)		
Test ID & References:	Table 170 LPDDR5	Table 170 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Specificat	ion)	Test ID	Reference	from Specification		
	tjit(CC)		102026		Tables 345 - 348		
Overview:					o consecutive clock cycles. to the next rising edge.		
Procedure:	 Acquire 202 cycles from the test signal. Measure the difference between every adjacent pair of periods. Generate a total of 201 measurement results. Check the results for the smallest and largest values, which are recorded as the worst case values. Compare the worst case values to the compliance test limits. 						
/Expected Observable Results:		The measured value of tJIT(cc) for the test signal is reported as "Information Only".					

tjit(per) Clock period jitter

Availability Condition: Table 171 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)		
Test ID & References:	Table 172 LPDD	R5 Test References from J	ESD209-5 specification				
	Symbol (in Specific	cation)	Test ID	Reference	from Specification		
	tjit(per)		102027		Tables 345 - 348		
Overview:	This test measu				y signal tCK from tCK(avg). d the average clock period		
Procedure:	2 Measure the whole winde	 Acquire 202 cycles from the test signal. Measure the difference between every period inside a 200 cycle window with the average of th whole window. Calculate the average for periods 1 to 200. Measure the difference between period #1, period #2 and so on up to period #200; with the average and save the resulting value as a measurement result. A total of 200 measurement results are generated. 					
	4 Measure the average and						
	5 For the next		-	w by one per	iod and measure the averag		
	Continue th	6 Compare period #2 with the new average. Continue the comparison for period #3, #4 and so on up to period #201. A total of 200 additional measurement results are generated such that there are 400 measure					
		set of measuremer period #3 up to perio		w by one m	ore period and measure the		
	 8 Compare period #3 with the new average. Continue the comparison for period #4, #5 and so on up to period #202. A total of 200 additional measurement results are generated such that there are 600 measurement values overall. 						
	9 Check the 6 values.	9 Check the 600 results for the smallest and largest values, which are recorded as the worst ca values.					
	10 Compare th	e worst case values	to the compliance test l	limits.			
Expected/ Observable Results:	The measured v	value of tJIT(per) for	the test signal is reported	ed as "Inforn	nation Only".		

Clock (SE Mode) Tests



The single-ended mode clock timing parameters can be measured as shown in Figure 83.

Figure 83 Single-ended mode CK pulse definitions

```
tCKHL
```

Availability Condition:	Table 173	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: Table 174 LPDDR5 Test References from JESD209-5 specification

	Symbol (in Specification)	Test ID	Reference from Specification				
	tCKHL	251007	Table 328				
Overview:	The purpose of this test is to verify the pulse width of all the high pulses and the low pulses in the te signal.						
Procedure:	 Perform steps for tCKH to measure the worst high pulse width in the test signal. Perform steps for tCKL to measure the worst low pulse width in the test signal. Determine the final worst result from the worst high pulse width and worst low pulse width measured. 						
Expected/ Observable Results:	The measured value of tCKHL shall be within the conformance limits as per the JESD209-5 specification.						

tCKH

Availability Condition: Table 175 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)			
Test ID & References:	Table 176 LPDDR5 Test References from JESD209-5 specification							
	Symbol (in Specifica	tion)	Test ID	Reference from Specification				
	tCKH		251010		Figure 210			
Overview:	The purpose of this test is to verify the pulse width of all the high pulse in the test signal.							
Procedure:	1 Pre-condition	1 Pre-condition the oscilloscope.						
	2 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.							

- 3 Find the maximum high pulse width value for all the positive pulses identified.
- 4 Find the minimum high pulse width value for all the positive pulses identified.
- 5 Determine the worst high pulse width (tCKH) in the test signal from the maximum and minimum pulse width measured.

The measured value of tCKH shall be considered for "Information Only" purposes.

Expected/ Observable Results:

tCKL

Availability Condition: Set Up tab options for availability of tests Table 177

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)		
est ID & References: Table 178 LPDDR5 Test References from JESD209-5 specification							
	Symbol (in Specification)		Test ID	Reference from Specification			
tCKL			251011		Figure 210		
Overview:	The purpose of this test is to verify the pulse width of all the low pulses in the test signal.						
Procedure:	1 Pre-condition the oscilloscope.						
	2 Find all valid negative pulses of the Clock in the entire waveform. A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.						
	3 Find the ma	3 Find the maximum low pulse width value for all the negative pulses identified.					
	4 Find the minimum low pulse width value for all the negative pulses identified.						
	5 Determine the worst low pulse width (tCKL) in the test signal from the maximum and minimum pulse width measured.						
Expected/	The measured value of tCKL shall be considered for "Information Only" purposes.						

Expected/ Observable Results:

Write Clock (Diff) tests

An LPDDR5 SDRAM utilizes two types of clock with different frequencies. The frequency of WCK is four times or twice higher than the command clock. LPDDR5 uses a DDR data interface. The data interface uses two differential forwarded clocks (WCK t/WCK c) that are source synchronous to the DQs. DDR means that the data is registered at every rising edge of WCK_t and rising edge of WCK_c. WCK_t and WCK_c operate at twice the frequency of the command/address clock (CK_t/CK_c). WCK t/WCK c is used to sample DQ data for write operation and toggle DQ data for read operation. WCK_t/WCK_c must start toggle before starting write or read DQ data burst. All data bits (DQ[7:0] for WCK t[0]/WCK c[0], and DQ[15:8] for WCK t[1]/WCK c[1]) carry the training feedback to the controller. WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition. The latency control unit inside the SDRAM performs clock domain change of WRITE or READ commands from CK domain to WCK domain. An LPDDR5 SDRAM supports WCK free running mode. The DRAM controller must keep WCK toggling at its full rate after WCK2CK synchronization regardless of DQ operation. An LPDDR5 SDRAM requires being in WCK2CK synchronization state before the internal write operation starts. For WRITE operations, WCK must be driven at least tWCKPRE_Static+tWCKPRE_Toggle_WR before the write DQ burst. LPDDR5 will have a WCK post-amble of 0.5*tCK or TBD*tCK, after completing all write DQ burst.

The equations for the measurement of various parameters pertaining to Write Clock differential tests are given below:

$$tWCK(avg) = \left(\sum_{j=1}^{N} tWCKj\right)/N$$

where N = 200

Figure 84 Calculation for tWCK(avg)

$$tWCH(avg) = \left(\sum_{j=1}^{N} tWCHj\right) / (N \times tWCK(avg))$$

Figure 85 Calculation for tWCH(avg)

$$tWCL(avg) = \left(\sum_{j=1}^{N} tWCLj\right) / (N \times tWCK(avg))$$

where N = 200

Figure 86 Calculation for tWCL(avg)

tjit(per) = Min./Max. of {tWCKi - tWCK(avg), where i = 1 to 200}

Figure 87 Calculation for tjit(per) for WCK (Diff)

tjit(CC) = Max. of |{tWCK(i + 1) - tWCK(i)}|

Figure 88

Calculation for tjit(CC) for WCK (Diff)



tWCK(abs), tWCH(abs) and tWCL(abs) are measured directly on the Differential Write Clock signal and are considered as informative tests.

tWCK(avg) Average Write Clock period

Availability Condition: Table 179 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: Table 180 LPDDR5 Test References from JESD209-5 specification

	S	Symbol (in Specification)	Test ID	Reference from Specification					
	ť	WCK(avg)	102000	Tables 349 - 351					
Overview:	m	tWCK(avg) is the average write clock period across a consecutive 200-cycle window. This test measures the period from the rising edge of a cycle to the next rising edge within the waveform window.							
Procedure:	1	Acquire 202 cycles from the	test signal.						
	2	Measure a sliding "window"	of 200 cycles.						
	3	Calculate the average period	d value for periods 1-200).					
	4	Calculate the average period	d value for periods 2-201						
	5	Calculate the average period Three measurement results a							

- 6 Check the three measured results for the smallest and largest values, which are recorded as the worst case values.
- 7 Compare the worst case values to the compliance test limits.

Expected/ The measured value of tWCK(avg) shall be within the conformance limits as per the JESD209-5 specification.

tWCK(abs) Absolute Write Clock period

Availability Condition: Table 181 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)			
Test ID & References: Table 182 LPDDR5 Test References from JESD209-5 specification								
	Symbol (in Specifica	tion)	Test ID	Reference f	rom Specification			
	tWCK(abs)		102001		Tables 349 - 351			
Overview:			k period within a wavefu e to the next consecutiv		. This test measures the e within the waveform			
Procedure:	 Find the maxil Find the mini Check the tw 	cycles from the test imum period value f mum period value f o results for the wo worst case values t	for period 1-202. for period 1-202.	mits.				
/Expected Observable Results:	The measured va	lue of tWCK(abs) fo	or the test signal is repo	rted as "Infoi	rmation Only".			

tWCKH(avg) Average High pulse width

Availability Condition: Table 183 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)			
Test ID & References:	Table 184 LPDDR	Table 184 LPDDR5 Test References from JESD209-5 specification						
	Symbol (in Specifica	ation)	Test ID	Reference	from Specification			
	tWCKH(avg)		102002		Tables 349 - 351			
Overview:	window. This tes	tWCKH(avg) is the average pulse width across any consecutive 200 high pulses within a waveform window. This test measures the average duty cycle of all positive pulse widths within a window of 200 consecutive cycles.						
Procedure:	1 Acquire 202	cycles from the tes	st signal.					
		iding "window" of 2	5					
			oulses from cycle #1 to cy erates one measurement		d determine the average			
		window. This gene	oulses from cycle #2 to cy erates one more measure		d determine the average and two measurement			
		window.This gene	pulses from cycle #3 to cy rates one more measure		d determines the average and three measurement			
	6 Check the th worst case v		es for the smallest and la	argest values	s, which are recorded as the			
	7 Compare the	worst case values	to the compliance test li	imits.				
/Expected Observable Results:	The measured va specification.	alue of tWCKH(avg) shall be within the conf	ormance lim	its as per the JESD209-5			

tWCKL(avg) Average Low pulse width

Availability Condition: Table 185 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)			
Test ID & References:	Table 186 LPDDR5	Test References from JE	SD209-5 specification					
	Symbol (in Specifica	tion)	Test ID	Reference 1	from Specification			
	tWCKL(avg)		102003		Tables 349 - 351			
Overview:	window. This test	tWCKL(avg) is the average pulse width across any consecutive 200 low pulses within a waveform window. This test measures the average duty cycle of all negative pulse widths within a window of 200 consecutive cycles.						
Procedure:		cycles from the test	0					
	3 Measure the		5		determine the average value			
			Ilses from cycle#2 to cyc one more measurement		determine the average value vo measurement values			
					determine the average value nree measurement results			
	6 Check the the worst case va		es for the smallest and la	irgest values	, which are recorded as the			
	7 Compare the	worst case values	to the compliance test li	mits.				
/Expected Observable Results:	The measured va specification.	lue of tWCKL(avg)	shall be within the confe	ormance limi	its as per the JESD209-5			

tWCKH(abs) Absolute HIGH Write Clock pulse width

Availability Condition: Table 187 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)			
Test ID & References: Table 188 LPDDR5 Test References from JESD209-5 specification								
	Symbol (in Specificat	ion)	Test ID	Reference	from Specification			
	tWCKH(abs)		102004		Tables 349 - 351			
Overview:	edge to the follow		his test measures the ab		as measured from one rising cycle of all positive pulse			
Procedure:	1 Acquire 202 c	cycles from the test	signal.					
	2 Find the maxi	mum high pulses v	vidth value for positive p	ulses #1 to	#202.			
	3 Find the mini	mum high pulses w	idth value for positive p	ulses #1 to #	‡202.			
	4 Check these t	wo results for the v	worst case values.					
	5 Compare the	worst case values t	to the compliance test li	mits.				
/Expected Observable Results:	The measured va	lue of tWCKH(abs)	for the test signal is rep	orted as "In	formation Only".			

tWCKL(abs) Absolute LOW Write Clock pulse width

Availability Condition:	Table 189 Set Up	ab options for availability o	of tests		
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)
Test ID & References:	Table 190 LPDDRS	Test References from JES	D209-5 specification		
	Symbol (in Specifica	tion)	Test ID	Reference fr	rom Specification
	tWCKL(abs)		102005		Tables 349 - 351
Overview:	edge to the follow		is test measures the ab		s measured from one falling cycle of all negative pulse
Procedure:	1 Acquire 202 d	cycles from the test	signal.		
	2 Find the max	mum low pulses wi	dth value for negative p	ulses #1 to #	202.
		I I	Ith value for negative p	ulses #1 to #2	202.
	4 Check these	two results for the w	vorst case values.		
	5 Compare the	worst case values to	o the compliance test li	mits.	
Expected/ Observable Results:	The measured va	lue of tWCKL(abs) f	or the test signal is repo	orted as "Info	ormation Only".

tjit(CC) Maximum Write Clock Jitter between consecutive cycles

Availability Condition: Table 191 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)			
Test ID & References:	Table 192 LPDDR5	Table 192 LPDDR5 Test References from JESD209-5 specification						
	Symbol (in Specificat	ion)	Test ID	Reference f	rom Specification			
	tjit(CC)		102006		Tables 349 - 351			
Overview:		test measures the			en two consecutive write dge of a write clock cycle to			
Procedure:	2 Measure the d	ycles from the test difference between tal of 201 measure	every adjacent pair of p	eriods.				
	4 Check the res values.	ults for the smalles	st and largest values, wh	nich are recor	rded as the worst case			
	5 Compare the	worst case values ⁻	to the compliance test li	mits.				
/Expected Observable Results:	The measured va	lue of tJIT(cc) for tl	ne test signal is reported	d as "Informa	tion Only".			

tjit(per) Write Clock period jitter

Availability Condition: Table 193 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)
Test ID & References:	Table 194 LPDDR	5 Test References from JE	SD209-5 specification		
	Symbol (in Specifica	ation)	Test ID	Reference	from Specification
	tjit(per)		102007		Tables 349 - 351
Overview:	tWCK(avg). This	test measures the	efined as the largest dev difference between a me nultiple cycles of the writ	easured write	e clock period and the
Procedure:	1 Acquire 202	cycles from the test	signal.		
	2 Measure the whole windo		every period inside a 20	00 cycle wind	dow with the average of the
	3 Calculate the	e average for period	s 1 to 200.		
	average and		period #1, period #2 an alue as a measurement ults are generated.		o period #200; with the
		set of measurement up to period #201.	values, slide the windov	v by one peri	iod and measure the average
	Continue the) additional measur	riod #3, #4 and so on up		201. at there are 400 measured
		set of measurement eriod #3 up to peric		w by one mo	pre period and measure the
	Continue the) additional measur	riod #4, #5 and so on up		202. lat there are 600 measured
	9 Check the 60 values.	00 results for the sm	nallest and largest value	s, which are	recorded as the worst case
	10 Compare the	worst case values	to the compliance test li	imits.	
Expected/ Observable Results:	The measured va	alue of tJIT(per) for	the test signal is reporte	ed as "Inform	nation Only".

tERR(2per) Write Clock Cumulative error across 2 cycles

Availability Condition: Table 195 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)
Test ID & References:	Table 196 LPDDR5	i Test References from JE	SD209-5 specification		
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification
	tERR(2per)		102008	Table 349	- 351
Overview:	average clock pe		e cycles of the clock. S		red clock period and the easurements include multiple
Procedure:	Example input te	st signal:			
	Frequency: 1 kHz	z, Number of cycles	acquired: 202		
	compared agains the large 200-cyo n is the number of procedure cover 1 Calculate the 2 Calculate the would cover p	st equivalent numb cle window (n x C), of cycles. In the cas for all cycles, wher average period ins small window widt period #1 and perio cumulative error v	er of consecutive average where C is the average se of tERR(2per), $n = 2$. In n is replaced by the me side the first large 200- ch, W (total width of 2 co od #2.	age cycles (de e value of the The steps de espective nur cycle window consecutive c	-
		·	n is the number of cons	-	
	(the next sma		over period #2 and per		the next 2 consecutive cycles
	6 Repeat the p		steps 1 to 5 until the I	ast small wir	ndow within C ₁ (from
	7 Find the wors	st error from step 4	and denote it as Cum	Err1.	
			mErr2 (for the second hird large 200-cycle wi		cle window of period cycle #2 od cycle #3 to #202).
	9 Determine th for tERR(2per		Err1, CumErr2 and Cun	nErr3. Report	the worst value as the result
		same as tERR(2pe ndow size of 4-cyc		ll window siz	e is 3-cycle wide. tERR(4per)
Expected/ Observable Results:	All measured valu		or the test signal shall b	be within the	conformance limits as per the

tERR(3per) Write Clock Cumulative error across 3 cycles

Availability Condition: Table 197 Set Up tab options for availability of tests

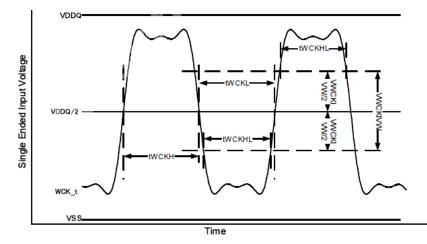
Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)
Test ID & References:	Table 198 LPDDR5	Test References from JE	SD209-5 specification		
	Symbol (in Specificat	tion)	Test ID	Reference	from Specification
	tERR(3per)		102009	Table 349 -	- 351
Overview:	average clock pe				ed clock period and the asurements include multiple
Procedure:	Example input te	st signal:			
	Frequency: 1 kHz	, Number of cycles	s acquired: 202		
	compared agains the large 200-cyc n is the number of procedure cover 1 Calculate the 2 Calculate the would cover p	t equivalent numb cle window (n x C), of cycles. In the cas for all cycles, wher average period ins small window widt period #1 and perio	er of consecutive average where C is the average se of tERR(3per), $n = 3$. In n is replaced by the reside the first large 200-c th, W (total width of 2 co od #2.	e cycles (de value of the Fhe steps de spective num ycle window onsecutive cy	nber of cycles.
	n=3 for tERR(
	tERR(nper) = \	W - n x C_1 , where r	n is the number of conse	ecutive cycles	S
			by one period and find t over period #2 and perio		he next 2 consecutive cycles
		3 with the new valu			
		ocess described in period#200) is co	i steps 1 to 5 until the la vered.	st small wind	dow within C_1 (from
			and denote it as CumEr		
			mErr2 (for the second la hird large 200-cycle win		le window of period cycle #2 d cycle #3 to #202).
		e worst error Cum			the worst value as the result
		same as tERR(2pe ndow size of 4-cyc		window size	is 3-cycle wide. tERR(4per)
/Expected Observable Results:	All measured valu JEDEC specificat		or the test signal shall be	e within the c	conformance limits as per the

tERR(4per) Write Clock Cumulative error across 4 cycles

Availability Condition: Table 199 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)
Test ID & References:	Table 200 LPDDR5	Test References from JE	SD209-5 specification		
	Symbol (in Specificat	tion)	Test ID	Reference	from Specification
	tERR(4per)		102010	Table 349	- 351
Overview:	average clock pe		e cycles of the clock. Su		ed clock period and the asurements include multiple
Procedure:	Example input te	st signal:			
	Frequency: 1 kHz	z, Number of cycles	s acquired: 202		
	compared agains the large 200-cyc n is the number of procedure cover 1 Calculate the 2 Calculate the would cover p	st equivalent numb cle window (n x C), of cycles. In the cas for all cycles, wher average period ins small window widt period #1 and perio cumulative error v	er of consecutive average where C is the average se of tERR(4per), $n = 4$. in n is replaced by the reside the first large 200-c th, W (total width of 2 co od #2.	ge cycles (de value of the Fhe steps de spective nur cycle windov onsecutive c	-
	tERR(nper) = \	W - n x C ₁ , where r	n is the number of conse	ecutive cycle	2S
	(the next sma	all window would c	over period #2 and perio		the next 2 consecutive cycles
	6 Repeat the pr	3 with the new valu rocess described in o period#200) is co	steps 1 to 5 until the la	st small win	dow within C ₁ (from
	7 Find the wors	st error from step 4	and denote it as CumEr	r1.	
			mErr2 (for the second la nird large 200-cycle win		cle window of period cycle #2 od cycle #3 to #202).
	9 Determine the for tERR(2per		Err1, CumErr2 and Cuml	Err3. Report	the worst value as the result
		same as tERR(2pe ndow size of 4-cyc		window size	e is 3-cycle wide. tERR(4per)
Expected/ Observable Results:	All measured valu JEDEC specificat		or the test signal shall be	e within the o	conformance limits as per the

Write Clock (SE Mode) Tests



The single-ended mode write clock timing parameters can be measured as shown in Figure 83.

Figure 89 Single-ended mode WCK pulse definitions

tWCKHL

Availability Condition:	Table 201	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	N/A	Yes	No	Yes	WCK(Diff)			
Test ID & References: Table 202 LPDDR5 Test References from JESD209-5 specification								
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification			
	tWCKHL		251107		Table 327			
Overviev	• The nurnose of th	nie taet ie to varify th	na nulse width of all the	niah nulses :	and the low pulses in the t			

Overview: The purpose of this test is to verify the pulse width of all the high pulses and the low pulses in the test signal.

Procedure: 1 Perform steps for tWCKH to measure the worst high pulse width in the test signal.

- 2 Perform steps for tWCKL to measure the worst low pulse width in the test signal.
- 3 Determine the final worst result from the worst high pulse width and worst low pulse width measured.

Expected/ The measured value of tWCKHL shall be within the conformance limits as per the JESD209-5 **Observable Results:** specification.

tWCKH

Availability Condition: Table 203 Set Up tab options for availability of tests

Supported CK Type	Suppo	orted WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A		Yes	Yes	Yes	WCK(Diff)	
Test ID & References:	Tat	ble 204 LPDDR	5 Test References from JE	SD209-5 specification			
	Symbol (in Specification) Test ID Reference from Specification						
	t	WCKH		251110		Figure 208	
Overview:	Th	ne purpose of t	his test is to verify t	he pulse width of all the	e high pulses	in the test signal.	
Procedure:	1 2 3 4 5 6	 Consider the first valid WRITE burst found. Find all valid positive pulses of the Write Clock in the specified burst. A valid positive pulse on t Write Clock starts at the valid rising edge of the Write Clock and ends at the following valid falling edge of the Write Clock. Find the maximum high pulse width value for all the positive pulses identified. Find the minimum high pulse width value for all the positive pulses identified. 					
Expected/ Observable Results:	Th	minimum pulse width measured. The measured value of tWCKH shall be considered for "Information Only" purposes.					

tWCKL

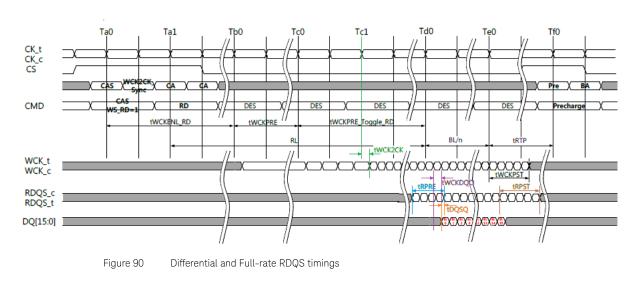
Availability Condition: Table 205 Set Up tab options for availability of tests

Supported CK Type	Suppo	rted WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A		Yes	Yes	Yes	WCK(Diff)	
Test ID & References:	References: Table 206 LPDDR5 Test References from JESD209-5 specification						
	s	ymbol (in Specifica	tion)	Test ID	Reference	from Specification	
	t۱	WCKL		251111		Figure 208	
Overview:	Th	e purpose of th	nis test is to verify t	he pulse width of all the	low pulses	in the test signal.	
Procedure:	1		2	burst data of the test sig	jnal.		
	2	Consider the	first valid WRITE b	urst found.			
	3	3 Find all valid negative pulses of the Write Clock in the specified burst. A valid negative pulse on the Write Clock starts at the valid falling edge of the Write Clock and ends at the following valid rising edge of the Write Clock.					
	4	4 Find the maximum low pulse width value for all the negative pulses identified.					
	5 Find the minimum low pulse width value for all the negative pulses identified.						
	6		e worst low pulse v			the maximum and minimun	
Exposted/	ть	a maggurad va	luc of tMCKL oball	be considered for "Infor	mation Only	["]	

Expected/ The measured value of tWCKL shall be considered for "Information Only" purposes.

Observable Results:

Other timing tests



To check for various timing parameters, consider the timing diagram shown in Figure 90.



Availability Condition: Table 207 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
Burst & Continuous	Burst only	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ			
Test ID & References:	Table 208 LPDDR	Test References from JE	SD209-5 specification					
	Symbol (in Specification) Test ID Reference from Specification							
	tWCK2CK		131000	Table 242				
Overview:	The purpose of th (WCK) signal.	nis test is to verify t	he phase offset betweer	n the Clock (CK) signal and Write Clock			
Procedure:	 Validate the I Take the first Find the first Find the near 	 Acquire and split read and write burst of the acquired signal. Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded. Take the first valid WRITE burst found. Find the first valid rising WCK edge (excluding the preamble pattern) of the specified burst. Find the nearest CK edge. 						
/Expected Observable Results:		The measured value of tWCK2CK shall be within the conformance limits as per the JESD209-5						

tRPRE

Availability Condition: Table 209 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals				
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)				
Test ID & References:	Test ID & References: Table 210 LPDDR5 Test References from JESD209-5 specification								
	Symbol (in Specificat	ion)	Test ID	Reference f	rom Specification				
	tRPRE		130000		Table 173				
Overview:		The purpose of this test is to verify the time when RDQS starts driving high (*preamble behavior) to the first DQ signal crossing for the Read Cycle.							
Procedure:		valid RDQS burst f old (0V) of the spec	ound, find the first rising	g edge (befo	re the preamble) at the				
		2 Find the next edge after the defined RDQS preamble length, which is configured in the General Setup window of the Set Up tab.							
	4 Report the me	easurement as tRPI	RE.						
Expected/ Observable Results:	The measured va specification.	lue of tRPRE shall b	be within the conforman	ice limits as j	per the JESD209-5				

tRPST

Availability Condition: Table 211 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)			
Test ID & References:	Table 212 LPDDR5	Test References from JE	SD209-5 specification					
	Symbol (in Specification) Test ID Reference from Specification							
	tRPST		130001		Table 173			
Overview:			the time when RDQS is n nal crossing (last bit of th		ving from high/low state to a burst).			
Procedure:	2 Find the edge3 Measure the til	3 Measure the time difference between these two edges.						
Expected/ Observable Results:	The measured val specification.	The measured value of tRPST shall be within the conformance limits as per the JESD209-5						

tDQSQ

Availability Condition: Table 213 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals			
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)			
Test ID & References: Table 214 LPDDR5 Test References from JESD209-5 specification								
	Symbol (in Specification) Test ID Reference from Specification							
	tDQSQ		130002		Table 173			
Overview:			he time interval from the DQ rising and falling) sig		QS rising and falling edges)			
Procedure:	 For all DQ cro Measure the t 	 2 For all DQ crossings found, locate the nearest RDQS edges. 3 Measure the time difference between these two edges. 						
Expected/ Observable Results:	The measured val specification.	The measured value of tDQSQ shall be within the conformance limits as per the JESD209-5						

tQSH

Availability Condition: Table 215 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A	Yes	Yes	Yes	WCK(Diff), DQ, RDQS(Diff)		
Test ID & References:	Table 216 LPDDR	5 Test References from JE	SD209-5 specification				
	Symbol (in Specifica	tion)	Test ID	Reference	from Specification		
	tQSH		130003		Table 242		
Overview:	The purpose of t	nis test is to verify t	he width of the positive	pulse of the	RDQS signal.		
Procedure:	the following 2 Capture all vi						
Expected/ Observable Results:	3 Determine the worst result from the set of tQSH measured. The measured value of tQSH shall be within the conformance limits as per the JESD209-5 specification.						

tQSL

Availability Condition: Table 217 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals		
N/A	N/A	Yes	Yes	Yes	WCK(Diff), DQ, RDQS(Diff)		
Test ID & References:	Table 218 LPDDR	5 Test References from JE	SD209-5 specification				
	Symbol (in Specifica	Symbol (in Specification) Test ID Reference from Specification					
	tQSL		130004		Table 242		
Overview:	The purpose of t	his test is to verify t	he width of the negative	pulse of the	e RDQS signal.		
Procedure:	the following 2 Capture all v						
/Expected Observable Results:		The measured value of tQSL shall be within the conformance limits as per the JESD209-5					

Keysight D9050LDDC LPDDR5 Test Application Methods of Implementation

6 Eye Diagram Tests

RDQS Detect Method for Read Write Separation202DQ Rx Voltage and Timing (WRITE) tests206DQ Rx Voltage and Timing (WRITE) tests206DQ Rx Voltage and Timing (READ) tests216CA Rx Voltage and Timing tests221CS Rx Voltage and Timing tests231



RDQS Detect Method for Read Write Separation

RDQS Detect is a read write separation method. This method works when the signal source contains at least an RDQS signal and a WCK signal. In this method, the Read/Write burst data is identified based on the presence of RDQS burst. If WCK burst contains an RDQS burst, then it is a Read burst. If the WCK burst does not contain an RDQS burst, then it is a Write burst.

If you select the RDQS Detect mode as the burst identification method, you must select the length of the WCK Postamble in the WCK Postamble Length section of the LPDDR5 General Setup dialog box.

LPDDR5 General Setup	? —	X					
Set the data rate of the test signal by entering a custom value or select from the JEDEC standard data rate values. 3200 MT/s JEDEC standard values WCK Frequency : 1600 MHz							
WCK : CK Ratio 2:1	Clock Frequency : 800 MHz	Π					
Signal Source							
WCK_t (SE), WCK_c	(SE), RDQS_t (SE), RDQS_c (SE)						
Single-Ended M	ode						
Signal Operation Mod	e						
CK (Diff) Continuou	is 💙						
WCK (Diff) Burst	Burst WCK options						
RDQS Preamble/Posta	amble Length						
RDQS Preamble	Static: 4 tWCK, Toggle: 0 tWCK						
RDQS Postamble	0.5 tWCК						
RDQS Postamble Mode							
WCK Postamble Length							
	CK Postamble.						
WCK Postamble	2.5 tWCK						
	2.5 tWCK						
🖌 Show Hints	4.5 tWCK OK Cancel						
	6.5 tWCK	۷					

Figure 91 LPDDR5 General Setup Dialog



Figure 92 WCK Burst Options Setup Dialog

Tests that support the RDQS Detect Burst Identification Method

The following Eye Diagram tests support the RDQS Burst Identification method:

WRITE Tests

- tDIVW1 Margin
- tDIVW2 Margin
- vDIVW Margin
- tDIPW
- tDIHL
- · VDIHL_AC
- tWCK2DQI_HF

READ Tests

- tQW
- tWCK2DQO_HF

Method of Implementation for the RDQS Detect Burst Identification Method

The following are the steps for the method of implementation for the RDQS Detect burst identification method:

- 1 Populate the burst from WCK signal.
- 2 Locate FirstWCKRising for the burst.
- 3 Compute TimeA = FirstWCKRising + tWCKPRE_Toggle_RD * ClockCycleWidth.
- 4 Compute TimeB = Start of WCK postamble. For example, if tWCKPST=2.5nWCK then TimeB = time of second last rising edge of WCK burst. If tWCKPST=4.5nWCK then TimeB = time of fourth last rising edge of WCK burst.
- 5 Compute TimeC = 0.5*(TimeA+TimeB)
- 6 Compute VmaxTimeCWithinUI = Vmax range from (TimeC 1*UI) to (TimeC + 1*UI)
- 7 Compute VminTimeCWithinUI = Vmin range from (TimeC 1*UI) to (TimeC + 1*UI)
- 8 If [(VmaxTimeCWithinUI > VOHDiff_RDQS) AND (VminTimeCWithinUI < VOLDiff_RDQS)] then the burst will be recognized as a READ burst. Otherwise, the burst will be recognized as a WRITE burst.
- 9 Repeat steps 2 to 8 for the rest of burst.

References for DQ Rx Voltage and Timing tests

LPDDR5 DQ, DMI, Parity and DBI Rx mask is defined as hexagonal mask as shown in Figure 93. The mask (vDIVW, tDIVW1, tDIVW2) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal.

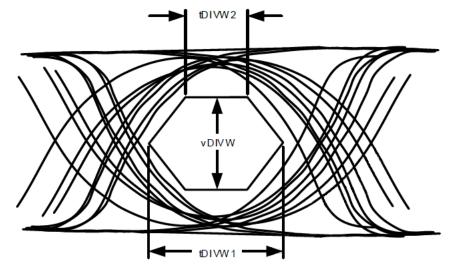


Figure 93 DQ Rx Mask definition

Rx mask voltage vDIVW has to be centered around VrefDQ as shown in Figure 94. DQ single input pulse amplitude into the receiver has to meet or exceed vDIHL_AC at any point over the total UI. vDIHL_AC is the peak to peak voltage centered around VrefDQ such that vDIHL_AC/2 min has to be met both above and below VrefDQ.

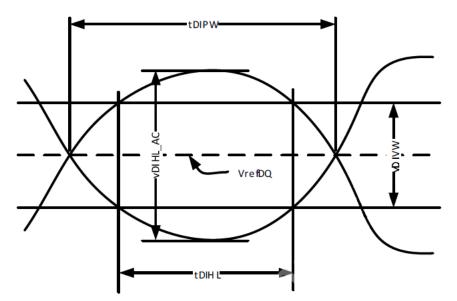


Figure 94 Identifying DQ Rx Mask parameters with respect to VrefDQ

tWCK2DQI is measured at the center (midpoint) of the tDIVW window, as shown in Figure 95. The LPDDR5-SDRAM uses an un-matched WCK-DQ path for lower power, so the WCK must arrive at the SDRAM ball prior to the DQ signal by the amount of tWCKDQI. The WCK must be trained to arrive at the DQ pad center-aligned with the DQ-data.

DQ, WCK data-in at DRAM Pin

Non Minimum Data Eye / Maximum Rx Mask

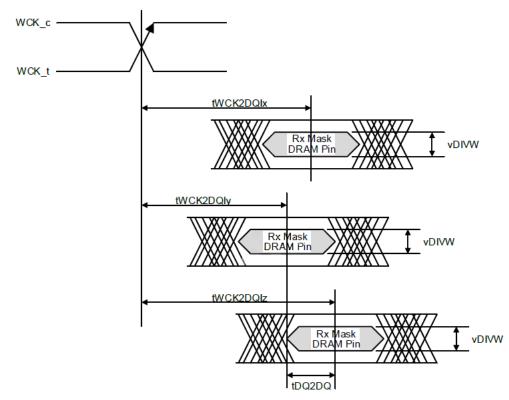


Figure 95 Identifying DQ Rx Mask parameters with respect to WCK

DQ Rx Voltage and Timing (WRITE) tests

tDIVW1 Margin

Availability Condition: Table 219 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: Table 220 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tDIVW1	141000	Table 355

Overview: The purpose of this test is to measure the minimum tDIVW1 Margin of the WRITE eye diagram generated.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid WCK input test signals by verifying its frequency and amplitude values.

- 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
 - b Set up measurement threshold values for the DQx channel and the WCKx channel input.
 - c Set up fixed vertical scale values for DQx channel and WCKx channel input.
 - d Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered WCK, Rise/Fall Edge

- g Set the Real Time Eye on SDA to ON.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - *c* Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - · Select a positive value greater than 0 to specify vCENT.

Availability Condition:	Table 221 Set Up tab options for availability of tests
tDIVW2 Marg	in
Expected/ Observable Results:	The measured tDIVW1 Margin value for the test signal indicates if there is a violation in the mask region.
	where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2. 10 Report the worst time gap and margin percentage as test results.
	Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%
	9 Calculate the margin (in percentage) using the equation:
	8 Find the minimum value between tDIVW1_m1 and tDIVW1_m2. Use the minimum value as the worst time gap.
	 Use the Histogram feature in the Infiniium Application to measure the tDIVW1 Margin value for both corners of the Test Mask. The tDIVW1 Margin for each Test Mask corner is denoted by tDIVW1_m1 and tDIVW1_m2.
	6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
	iii Use the voltage level at the widest eye opening as the value for Vcent.
	ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
	i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
	To obtain the vCENT value with 'WidestOpening' selected:

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: Table 222 LPDDR5 Test References from JESD209-5 specification

	Symbol (in Specification)	Test ID	Reference from Specification		
	tDIVW2	141001	Table 355		
Overview:	The purpose of this test is to measure the minimum tDIVW2 Margin of the WRITE eye diagram generated.				
Procedure:	1 Calculate the initial time s Application.	scale value based on selected s	speed grade options in the Test		

2 Check for valid WCK input test signals by verifying its frequency and amplitude values.

- 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
 - b Set up measurement threshold values for the DQx channel and the WCKx channel input.
 - c Set up fixed vertical scale values for DQx channel and WCKx channel input.
 - d Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.
 - : Explicit clock, Source = filtered WCK, Rise/Fall Edge
 - g Set the Real Time Eye on SDA to ON.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - *c* Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.

· Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 7 Use the Histogram feature in the Infinitum Application to measure the tDIVW2 Margin value for all the four corners of the Test Mask. The tDIVW2 Margin for each Test Mask corner is denoted by tDIVW2_m1, tDIVW2_m2, tDIVW2_m3 and tDIVW2_m4.
- 8 Find the minimum value between tDIVW2_m1, tDIVW2_m2, tDIVW2_m3 and tDIVW2_m4. Use the minimum value as the worst time gap.
- 9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.

10 Report the worst time gap and margin percentage as test results.

Expected/ The measured tDIVW2 Margin value for the test signal indicates if there is a violation in the mask region.

vDIVW Margin

Availability Condition: Table 223 Set Up tab options for availability of tests

upported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
urst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ
est ID & References:	Table 224 LPDDR5 Te	est References from JE	SD209-5 specification		
	Symbol (in Specificatio	n)	Test ID	Reference	from Specification
	vDIVW		141002		Table 355
Overview:	The purpose of this generated.	s test is to measu	re the minimum vDIVW	Margin of th	e WRITE eye diagram
Procedure:	1 Calculate the ir Application.	nitial time scale v	alue based on selected s	speed grade	options in the Test
		WCK input test s	signals by verifying its fre	equency and	amplitude values.
	3 Set up the osci	lloscope:			
			arate Write burst and re ed for eye folding later.	turn the filte	red WCK signals as
			ld values for the DQx cha	annel and th	e WCKx channel input.
	c Set up fixed	vertical scale val	ues for DQx channel and	I WCKx char	nnel input.
	d Set the Colo	r Grade Display o	option to ON.		
	e Set up Mask	Test.			
	f Set up Clock	Recovery on SD	Α.		
	: Explicit clo	ck, Source = filter	ed WCK, Rise/Fall Edge		
		Time Eye on SDA	-		
	4 Perform Mask 7	Testing:			
	a Set the Masl	< Test Run Until s	etting to 'Forever'.		
	b Load the ma	sk file and start t	he Mask Test.		
			counter for 'Total Wavef onfiguration option 'Total		ds the number of required
	5 Determine and	store the Vcent v	value. To determine the v	alue of Vcer	nt:
	a In the Config	jure tab of the Te	st Application, choose N	lode as Deb	ug.
			vigate to DQ Rx Voltage nere the vertical center c		tests > WRITE > vCENT D ask is placed.
	 Select 'Wide 	stOpening' to us	e the widest eye opening	g as vCENT.	
	 Select a posi- 	itive value greate	r than 0 to specify vCEN	т	

	÷		9A/2 - La - + O 2 2 1	a al c	
			'WidestOpening' select		amplitudo (that is the
	heig	ht measured at the o	center of the eye diagra	am).	amplitude (that is, the eye
	ii Sca 5m\	-	opening at the mention	ed search ra	nge with a scan resolution
	iii Use	the voltage level at	the widest eye opening	as the value	for Vcent.
		the Test Mask so tha n the Configure tab.	t it is centered on the V	/cent value w	ith the Test Mask width and
	top and the	bottom area of the	Test Mask.		e vDIVW Margin value for t nd vDIVW Margin lower.
		nimum value betwee t voltage gap.	en vDIVW Margin Uppe	r and vDIVW	Margin lower. Use this valu
			ercentage) using the e	quation:	
		Margin (%) = [(Woi	rst_voltage_gap) / (Hal	f of mask hei	ght)] x 100%
	where, Wors bottom.	st_voltage_gap is the	e voltage gap between t	the mask and	d the eye at the top and
	10 Report the	worst voltage gap ar	nd the margin percenta	ge as test res	sults.
Expected/ Observable Results:	The measured region.	value of vDIVW Marg	in for the test signal in	dicates if the	re is a violation in the mask
tDIPW					
Availability Conditions	T-1-1-005 0-1-1	a tab anti-na fan an Uabilit			
Availability Condition:	Table 225 Set U	p tab options for availability	/ of tests	_	
Availability Condition: Supported CK Type	Table 225 Set U Supported WCK Type	p tab options for availability Supports Offline?	y of tests R/W Separation needed?	SE Mode?	Required Signals
-				SE Mode? Yes	Required Signals CK(Diff), WCK(Diff), DQ
Supported CK Type	Supported WCK Type Burst only	Supports Offline? No R5 Test References from JE	R/W Separation needed? Yes	Yes	
Supported CK Type Burst & Continuous	Supported WCK Type Burst only Table 226 LPDD Symbol (in Specifi	Supports Offline? No R5 Test References from JE	R/W Separation needed? Yes SD209-5 specification Test ID	Yes	CK(Diff), WCK(Diff), DQ
Supported CK Type Burst & Continuous	Supported WCK Type Burst only Table 226 LPDD	Supports Offline? No R5 Test References from JE	R/W Separation needed? Yes SD209-5 specification	Yes	CK(Diff), WCK(Diff), DQ
Supported CK Type Burst & Continuous	Supported WCK Type Burst only Table 226 LPDD Symbol (in Specifi tDIPW	Supports Offline? No R5 Test References from JE cation)	R/W Separation needed? Yes SD209-5 specification Test ID 141003	Yes Reference	CK(Diff), WCK(Diff), DQ

Expected/ Observable Results: tDIHL	 Process all valid edges in the WRITE data burst. Collect all tDIPW. Determine the worst result from the set of tDIPW values measured and report it as the final test result. The measured value of tDIPW for the test signal shall be within the conformance limit as per the JESD209-5 specification. 				
Availability Condition:	Table 227 Set Up tab options for availabil	ity of tests			
Supported CK Type	Supported WCK Type Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	Burst only No	Yes	Yes	CK(Diff), WCK(Diff), DQ	
Test ID & References:	Table 228 LPDDR5 Test References from s Symbol (in Specification)	JESD209-5 specification Test ID	Reference	from Specification	
	tDIHL	141004		Table 355	
Overview:	The purpose of this test is to verify defined at the Vcent_DQ.	the minimum input DQ R	x pulse widt	th above and below vDIVW	
Procedure:	 Calculate the initial time scale Application. Check for valid WCK input test Set up the oscilloscope: a Using UDF methodology, se Recovered Clock, which is u b Set up measurement thresh c Set up fixed vertical scale va d Set the Color Grade Display e Set up Mask Test. f Set up Clock Recovery on S : Explicit clock, Source = filt g Set the Real Time Eye on SE Perform Mask Test Run Until b Load the mask file and start c Stop the Mask Test when th waveforms specified in the original 	t signals by verifying its free eparate Write burst and re- ised for eye folding later. old values for the DQx cha- alues for DQx channel and option to ON. DA. ered WCK, Rise/Fall Edge DA to ON. setting to 'Forever'. the Mask Test. e counter for 'Total Wavef	equency and turn the filte annel and th I WCKx char	amplitude values. ered WCK signals as ne WCKx channel input. nnel input.	
	5 Determine and store the Vcent a In the Configure tab of the T	value. To determine the v Test Application, choose N	value of Vcer Iode as Deb	nt: ug.	

b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.

	Select 'WidestOpening' to use the widest eye opening as vCENT.					
	Select a positive value greater than 0 to specify vCENT.					
	To obtain the vCENT value with 'WidestOpening' selected:					
	i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).					
	ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.					
	iii Use the voltage level at the widest eye opening as the value for Vcent.					
	6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.					
	7 Use the Histogram feature to measure the width of the eye opening at the top and bottom of the mask.					
	8 The worst value of the width obtained between the top and bottom is reported as tDIHL.					
Expected/ Observable Results:	The measured value of tDIHL for the test signal shall be within the conformance limit as per the JESD209-5 specification.					

```
vDIHL_AC
```

Availability Condition: Table 229 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: Table 230 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
VDIHL_AC	141005	Table 355

Overview: The purpose of this test is to measure the DQ single input pulse amplitude vDIHL_AC that the pulse must meet or exceed at any point over the total UI.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

- 2 Check for valid WCK input test signals by verifying its frequency and amplitude values.
- 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
 - *b* Set up measurement threshold values for the DQx channel and the WCKx channel input.
 - c Set up fixed vertical scale values for DQx channel and WCKx channel input.
 - *d* Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered WCK, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - Select 'WidestOpening' to use the widest eye opening as vCENT.
 - · Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 7 Use the Histogram feature in the Infiniium Application to measure the vDIHL_AC/2 values for the top and the bottom area of the Test Mask.
- The measured vDIHL_AC/2 values is denoted as vDIHL_AC/2_top and vDIHL_AC/2_bottom.
- 8 Calculate vDIHL_AC using the equation:
 - vDIHL_AC = [vDIHL_AC/2_top] [vDIHL_AC/2_bottom]
- 9 Report the measured vDIHL_AC as test result.

Expected/ The measured value of vDIHL_AC for the test signal shall be within the conformance limit as per the JESD209-5 specification.

tWCK2DQI_HF

Availability Condition: Table 231 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: Table 232 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tWCK2DQI_HF	141007	Table 301

Overview: The purpose of this test is to verify the offset between the WCK signal and the start of DQ input pulse / DQ input Rx mask.

- **Procedure:** 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
 - 2 Check for valid WCK input test signals by verifying its frequency and amplitude values.
 - 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
 - *b* Set up measurement threshold values for the DQx channel and the WCKx channel input.
 - c Set up fixed vertical scale values for DQx channel and WCKx channel input.
 - *d* Set the Color Grade Display option to ON.
 - e Set up Mask Test.
 - f Set up Clock Recovery on SDA.
 - : Explicit clock, Source = filtered WCK, Rise/Fall Edge
 - g Set the Real Time Eye on SDA to ON.
 - 4 Realign the eye opening of the first transition DQ bit to the center of the screen:
 - *a* Increase the search range on the screen to the range specified in the 'First DQ Transition Search Range (ps)' configuration option in the Configure tab, so that the crossing point of the eye is visible on the screen.
 - *b* Use the Histogram feature to find the first crossing point at 'VRefDQ' level horizontally across the screen.
 - *c* Realign the center of the eye to the middle time position.

NOTE

If the Test Application is unable to find any cross point within the search range, it prompts an error and this test run is aborted.

5 Perform Mask Testing:

- a Set the Mask Test Run Until setting to 'Forever'.
- *b* Load the mask file and start the Mask Test.
- c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 6 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - Select 'WidestOpening' to use the widest eye opening as vCENT.
 - · Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 7 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 8 Find the mid-point in time at the Vcent level of the eye diagram and denote it as EyeCenterLoc.
- 9 Determine the location of the filtered WCK rising edges used in the recovered clock and denote it as FilteredWCKLoc.

10 Compute the final test result using the equation:

tWCK2DQI_HF = EyeCenterLoc - FilteredWCKLoc

11 Determine the worst result from the set of tWCK2DQI_HF values measured and report it as the final test result.

Expected/ The measured value of tWCK2DQI_HF for the test signal is considered for 'Information-Only' **Observable Results:** purpose.

DQ Rx Voltage and Timing (READ) tests

tQW

Availability Condition: Table 233 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	Yes	Yes	CK(Diff), DQ, RDQS(Diff)
Test ID & References: Table 234 LPDDR5 Test References from JESD209-5 specification					
	Symbol (in Specification)		Test ID	Reference from Specification	
	tQW		140000	Note: No pass limits defined. However, a Read eye diagram formation indicates that the test has passed.	
Overview:	The purpose of t	his test is to verify th	he tQW parameter by m	easuring the	DQ Read Eye.

Procedure:

Calculate initial time scale value based on selected LPDDR5 speed grade options. 1

- 2 Check for valid RDQS input test signals by verifying its frequency and amplitude values.
- 3 Set up the oscilloscope:
 - a Using UDF methodology, separate Write burst and return the filtered RDQS signals as recovered clock for eye folding later.
 - b Set up measurement threshold values for the DQ channel and the RDQS channel input.
 - c Set up vertical scale values for DQ channel and RDQS channel input.
 - d Set Color Grade Display option to ON.
 - e Set up Mask Test settings.
 - f Set up Clock Recovery settings on SDA.
 - : Explicit clock, Source = filtered RDQS, Rise/Fall Edge
 - g Set Real Time Eye on SDA to ON.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Measure the Eye Height and Eye Width.
- 6 Report the measured Eye Height and Eye Width.

The measured tQW value for the test signal is considered for 'Information-Only' purpose.

Expected/ **Observable Results:**

tWCK2DQO_HF

Availability Condition:	Table 235	Set Up tab options for availability of tests
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Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ		
Test ID & References:	Table 236 LPDD	R5 Test References from JE	SD209-5 specification				
	Symbol (in Specifie	cation)	Test ID	Reference	from Specification		
	tWCK2DQ0_HF		140007		Table 301		
Overview:	The purpose of pulse / DQ outp		the offset between the W	/CK signal a	nd the start of DQ output		
Procedure:	1 Calculate th Application		alue based on selected s	speed grade	e options in the Test		
	2 Check for valid WCK input test signals by verifying its frequency and amplitude values.						
	3 Set up the oscilloscope:						
	 Using UDF methodology, separate Read burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later. 						
	<i>b</i> Set up measurement threshold values for the DQx channel and the WCKx channel input.						
	c Set up fixed vertical scale values for DQx channel and WCKx channel input.						
		color Grade Display o	option to ON.				
	e Set up M	ask Test.					
	f Set up Cl	lock Recovery on SD	Α.				
	: Explicit	clock, Source = filter	red WCK, Rise/Fall Edge				
	g Set the Real Time Eye on SDA to ON.						
	4 Realign the eye opening of the first transition DQ bit to the center of the screen:						
	a Increase the search range on the screen to the range specified in the 'First DQ Transition Search Range (ps)' configuration option in the Configure tab, so that the crossing point of the eye is visible on the screen.						
	<i>b</i> Use the Histogram feature to find the first crossing point at 'VRefDQ' level horizontally across the screen.						
	c Realign the center of the eye to the middle time position.						
	NOTE If the Test Application is unable to find any cross point within the search range, it prompts an error and this test run is aborted.						

- a Set the Mask Test Run Until setting to 'Forever'.
- *b* Load the mask file and start the Mask Test.
- c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

- 6 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - · Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 7 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 8 Find the mid-point in time at the Vcent level of the eye diagram and denote it as EyeCenterLoc.
- 9 Determine the location of the filtered WCK rising edges used in the recovered clock and denote it as FilteredWCKLoc.
- 10 Compute the final test result using the equation:

tWCK2DQO_HF = EyeCenterLoc - FilteredWCKLoc

11 Determine the worst result from the set of tWCK2DQO_HF values measured and report it as the final test result.

Expected/ The measured value of tWCK2DQO_HF for the test signal is considered for 'Information-Only' **Observable Results:** purpose.

References for CA Rx Voltage and Timing tests

LPDDR5 command and address interface operates from a differential clock (CK_t and CK_c). Commands and addresses are registered single data rate (SDR) at every rising edge of CK. Chip Select (CS) is part of the command code, and is sampled on the rising(falling) edge of CK_t (CK_c). The Read/Write command behavior depends on the bank architecture. The READ and WRITE commands are each initiated with CS, and CA[6:0] asserted to the proper state at the rising and falling edges of CK, as defined by the Command Truth Table (refer to *Table 154* of the *JESD209-5* specification). Command/Address ODT (On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the SDRAM to turn on/off termination resistance for CK_t, CK_c, and CA[6:0] signals.

LPDDR5 CA Rx mask is defined as hexagonal mask shape as shown in Figure 96. All CA signals apply the same compliance mask and operate in double data rate mode. The receiver mask (Rx Mask vCIVW, tCIVW1, tCIVW2) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal. CA Rx mask window center is around CK_t/CK_c cross point (differential mode). Rx mask voltage vCIVWI(max) has to be centered around VrefCA. CA single input pulse signal amplitude into the receiver has to meet or exceed vCIHL_AC at any point over the total UI. vCIHL_AC is the peak to peak voltage centered around VrefCA such that vCIHL_AC/2 min has to be met both above and below VrefCA. vCIHL_AC does not have to be met when no transitions are occurring. tCA2CA is defined fastest CA[x] mask center to slowest CA[y] mask center.

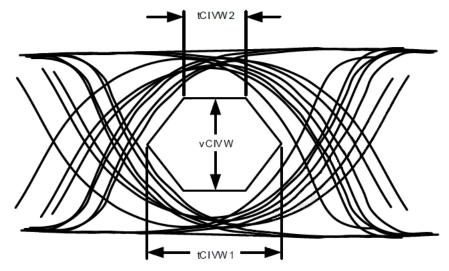
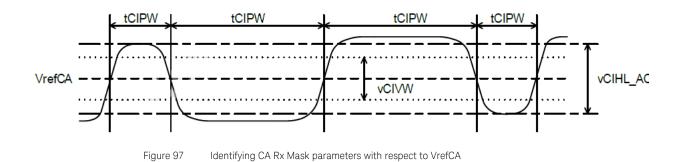
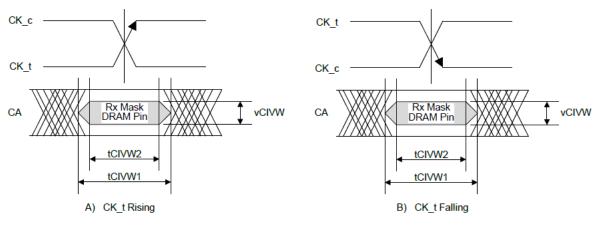


Figure 96 CA Rx Mask Defintion







CA Rx Voltage and Timing tests

tCIVW1 Margin

Availability Condition: Table 237 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA
Test ID & References:	Table 238 LPDD	R5 Test References from J	ESD209-5 specification		
	Symbol (in Specifi	cation)	Test ID	Reference	from Specification
	tCIVW1		142001		Table 354
Overview:	The purpose of generated.	this test is to measu	ire the minimum tCIVW1	Margin of t	he CA eye diagram
Procedure:	1 Calculate th Application		value based on selected s	speed grade	options in the Test
	2 Check for v values.	alid Clock (CK) and	CA input test signals by \	verifying its f	requency and amplitude
	3 On the Osc	illoscope:			
	a Set the T	rigger to 'Auto-Swe	ep'.		
	b Set the S	Sampling Rate of the	Oscilloscope to the max	imum value.	
	Eye Diag	ram Tests Only' cont	iguration option in the C		he 'Sampling Points (Pts) fo of the Test Application.
		tion 1 to duplicate t	-		
		Color Grade Display	option to ON.		
		lask Test settings.	A		
		lock Recovery on SE			
		clock, Source = Fun			
		Real Time Eye on SD.	ld values for Function 1 :	and CA inpu	t signals
					Edges to prevent timeout fo
			s activity on CA bus.	sing/ ratting	
	4 Perform Ma	ask Testing:			
	a Set the M	Aask Test Run Until	setting to 'Forever'.		
	b Load the	mask file and start	the Mask Test.		
			counter for 'Total Wavef onfiguration option 'Total		ds the number of required
	5 Determine	and store the Vcent	value. To determine the v	value of Vcer	ht.

- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- · Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 7 Use the Histogram feature in the Infiniium Application to measure the tCIVW1 Margin value for both corners of the Test Mask.

The tCIVW1 Margin for each Test Mask corner is denoted by tCIVW1_m1 and tCIVW1_m2.

- 8 Find the minimum value between tCIVW1_m1 and tCIVW1_m2. Use the minimum value as the worst time gap.
- 9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2. 10 Report the worst time gap and margin percentage as test results.

Expected/ The measured tCIVW1 Margin value for the test signal indicates if there is a violation in the mask region.

tCIVW2 Margin

Availability Condition:	Table 239	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References: Table 240 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tCIVW2	142002	Table 354

Overview: The purpose of this test is to measure the minimum tCIVW2 Margin of the CA eye diagram generated.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CA input test signals by verifying its frequency and amplitude values.

- 3 On the Oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - *b* Set the Sampling Rate of the Oscilloscope to the maximum value.
 - c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
 - *d* Set Function 1 to duplicate the CK signal.
 - e Set the Color Grade Display option to ON.
 - f Set up Mask Test settings.
 - g Set up Clock Recovery on SDA.
 - : Explicit clock, Source = Function 1, Rising Edge
 - h Set the Real Time Eye on SDA to ON.
 - *i* Set up measurement threshold values for Function 1 and CA input signals.
 - *j* Change Trigger Source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the tCIVW2 Margin value for all the four corners of the Test Mask. The tCIVW2 Margin for each Test Mask corner is denoted by tCIVW2_m1, tCIVW2_m2, tCIVW2_m3 and tCIVW2_m4.

- 8 Find the minimum value between tCIVW2_m1, tCIVW2_m2, tCIVW2_m3 and tCIVW2_m4. Use the minimum value as the worst time gap.
- 9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.

10 Report the worst time gap and margin percentage as test results.

Expected/ The measured tCIVW2 Margin value for the test signal indicates if there is a violation in the mask region.

vCIVW Margin

Availability Condition: Table 241 Set Up tab options for availability of tests

	N1/A				0//(D://) 04	
urst & Continuous	N/A	No	No	Yes	CK(Diff), CA	
est ID & References:	Table 242 LPDDF	25 Test References from J	ESD209-5 specification			
	Symbol (in Specific	ation)	Test ID	Reference	from Specification	
	vCIVW		142003		Table 354	
Overview:	The purpose of	this test is to measu	ure the minimum vCIVW	Margin of th	ne CA eye diagram generate	
Procedure:		e initial time scale v	value based on selected	speed grade	e options in the Test	
	Application.				£	
	2 Check for va values.	IIId Clock (CK) and I	CA input test signals by v	veritying its	frequency and amplitude	
	3 On the Oscil	loscope:				
	a Set the Tr	igger to 'Auto-Swe	ep'.			
	 b Set the Sampling Rate of the Oscilloscope to the maximum value. c Set the Sampling Points to the user defined value configured for the 'Sampling Points Eye Diagram Tests Only' configuration option in the Configure tab of the Test Applicat 					
		ion 1 to duplicate t	-			
		olor Grade Display	option to UN.			
		ask Test settings.				
	0	ock Recovery on SE				
			ction 1, Rising Edge			
		eal Time Eye on SD.				
			old values for Function 1		0	
			a input signal' on both Ri is activity on CA bus.	sing/Falling	Edges to prevent timeout	
	4 Perform Mas	sk Testing:				
	a Set the M	ask Test Run Until	setting to 'Forever'.			
		mask file and start				
			e counter for 'Total Wave onfiguration option 'Tota		eds the number of required	
	5 Determine and store the Vcent value. To determine the value of Vcent:					
	a In the Co	nfigure tab of the Te	est Application, choose N	lode as Deb	oug.	
			vigate to CA Rx Voltage ertical center of the Eye N		tests > vCENT CA mode (V ed.	
	 Select 'W 	idestOpening' to us	e the widest eye opening	a as vCENT.		

	То с	btain the	vCENT value with	'WidestOpening' selecte	ed:		
				unge is from 40% to 60% center of the eye diagrar		amplitude (that is, the eye	
		ii Scant 5mV.	for the widest eye o	opening at the mentione	ed search rar	ge with a scan resolution of	
		iii Use th	ne voltage level at t	he widest eye opening a	as the value	for Vcent.	
			e Test Mask so tha [.] the Configure tab.	t it is centered on the Vo	ent value wi	th the Test Mask width and	
	top	and the b	ottom area of the T			e vCIVW Margin value for the	
	8 Find	the mini	0	0		Margin lower. Use this value	
			ulate the worst margin (in percentage) using the equation:				
			Margin (%) = [(Wor	st_voltage_gap) / (Half	of mask heig	ht)] x 100%	
	whe		_voltage_gap is the	voltage gap between th	ne mask and	the eye at the top and	
	10 Rep	ort the w	orst voltage gap ar	d the margin percentag	e as test res	ults.	
Expected/ Observable Results:	The me region.	asured va	lue of vCIVW Marg	in for the test signal ind	icates if ther	e is a violation in the mask	
tCIPW							
Availability Condition:	Table 243	Set Up t	ab options for availability	of tests			
Supported CK Type	Supported W	СК Туре	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals	
Burst & Continuous	N/A		No	No	Yes	CK(Diff), CA	
Test ID & References:	Table 244	LPDDR5	i Test References from JE	SD209-5 specification			
	Symbol	(in Specificat	tion)	Test ID	Reference	from Specification	
	tCIPW			142004		Table 354	
Overview:	The pur	pose of tł	nis test is to verify t	he minimum input CA R	x pulse widt	h defined at the Vcent_CA.	
Procedure:	1 This	test requ	ires the following p	pre-requisite test:			
		-	in (Test ID: 142001) /cent is determined) I and its value is stored.			

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	2 Perform the pulse width on the CA signal:
	a Set to ON the positive pulse width measurement and jitter statistics to measure all the edges.
	b Set the measurement threshold to a hysteresis of ± CA mask height at the threshold level of Vcent_CA.
	c Obtain the minimum result from the measurements as the worst positive pulse width.
	d Repeat steps a to c for negative pulse width and store the minimum result from the measurement as the worst negative pulse width.
	3 Compare the minimum values from the positive and negative pulse width results.
	4 Measure tDIPW as the time starting from a rising/falling edge of the CA signal to the time ending at the following falling/rising edge.
	5 Capture all values of tCIPW.
	6 Convert the unit for the values from seconds to UI.
	7 Determine the worst result from the set of tCIPW values measured and report it as the final test result.
Expected/ Observable Results:	The measured value of tCIPW for the test signal shall be within the conformance limit as per the JESD209-5 specification.
VCIHL_AC	

Availability Condition: Table 245 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References: Table 246 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
vCIHL_AC	142005	Table 354

Overview: The purpose of this test is to measure the CA single input pulse amplitude vCIHL_AC that the pulse must meet or exceed at any point over the total UI.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CA input test signals by verifying its frequency and amplitude values.

3 Set up the oscilloscope:

a Set the Trigger to 'Auto-Sweep'.

b Set up measurement threshold values for the CAx channel and the CKx channel input.

c Set up fixed vertical scale values for CAx channel and CKx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered CK, Rise/Fall Edge g Set the Real Time Eye on SDA to ON. 4 Perform Mask Testing: a Set the Mask Test Run Until setting to 'Forever'. b Load the mask file and start the Mask Test. c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'. 5 Determine and store the Vcent value. To determine the value of Vcent: a In the Configure tab of the Test Application, choose Mode as Debug. b Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed. · Select 'WidestOpening' to use the widest eye opening as vCENT. Select a positive value greater than 0 to specify vCENT. To obtain the vCENT value with 'WidestOpening' selected: The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye i height measured at the center of the eye diagram). Scan for the widest eye opening at the mentioned search range with a scan resolution of ii 5mV. iii Use the voltage level at the widest eye opening as the value for Vcent. 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab. 7 Use the Histogram feature in the Infiniium Application to measure the vCIHL_AC/2 values for the top and the bottom area of the Test Mask. The measured vCIHL_AC/2 values is denoted as vCIHL_AC/2_top and vCIHL_AC/2_bottom. 8 Calculate vCIHL_AC using the equation: vCIHL_AC = [vCIHL_AC/2_top] - [vCIHL_AC/2_bottom] 9 Report the measured vCIHL_AC as test result. Expected/ The measured value of vCIHL AC for the test signal shall be within the conformance limit as per the **Observable Results:** JESD209-5 specification. tCA2CA Availability Condition: Table 247 Set Up tab options for availability of tests Supported CK Type SE Mode? Supported WCK Type Supports Offline? **R/W Separation needed? Required Signals** CK(Diff), CA[x], CA[y] **Burst & Continuous** N/A No No Yes **Test ID & References:** Table 248 LPDDR5 Test References from JESD209-5 specification Symbol (in Specification) Test ID **Reference from Specification**

Overview: The purpose of this test is to verify the mask offset between the fastest CA[x] mask center to the slowest CA[y] mask center.

142000

tCA2CA

Table 354

- **Procedure:** 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
 - 2 Check for valid Clock (CK), CA[x] and CA[y] input test signals by verifying its frequency and amplitude values.
 - 3 On the Oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - b Set the Sampling Rate of the Oscilloscope to the maximum value.
 - *c* Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
 - d Enable CK, CA[x] and CA[y] source channels.
 - e Set the Color Grade Display option to ON.
 - f Set up Mask Test settings.
 - g Set up Clock Recovery on SDA.
 - : Explicit clock, Source = CK source channel, Rising Edge
 - h Set the Real Time Eye on SDA to ON.
 - *i* Set up measurement threshold values for CK, CA[x] & CA[y] input signals.
 - *j* Change Trigger Source to 'CA[x] input signal' and 'CA[y] input signal', respectively on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.
 - 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
 - 5 Determine and store the Vcent values for CA[x] and CA[y]. To determine the value of Vcent, perform the following steps for each CA[x] and CA[y] input signals:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - Select 'WidestOpening' to use the widest eye opening as vCENT.
 - · Select a positive value greater than 0 to specify vCENT.

- The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[x] eye, find its midpoint. Denote this value as CA[x]_mid.
- 7 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[y] eye, find its midpoint. Denote this value as CA[y]_mid.
- 8 Calculate tCA2CA using the equation:

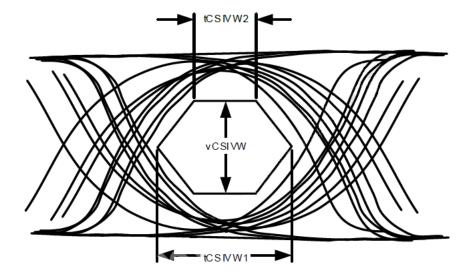
 $tCA2CA = CA[x]_mid - CA[y]_mid$

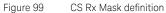
9 Report this difference as tCA2CA.

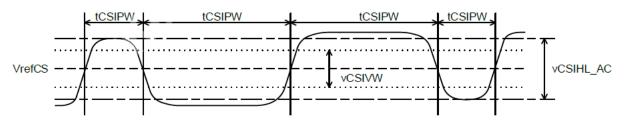
Expected/The measured value of tCA2CA shall be within the conformance limits as per the JESD209-5Observable Results:specification.

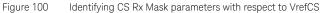
References for CS Rx Voltage and Timing tests

LPDDR5 CS Rx mask for Synchronous mode is defined as hexagonal mask shape as shown in Figure 219. CS signals apply the same compliance mask and operate in single data rate mode. The receiver mask (Rx Mask vCSIVW, tCSIVW1, tCSIVW2) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal.









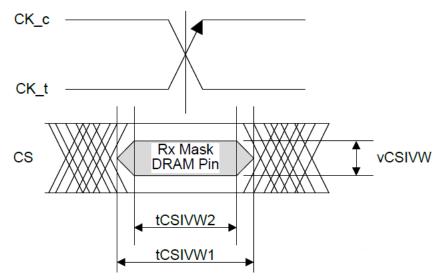


Figure 101 Identifying CS Rx Mask parameters with respect to CK

CS Rx Voltage and Timing tests

tCSIVW1 Margin

Availability Condition: Table 249 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS
Test ID & Peferences		Tast Bafaranaas from JEG	CD200 E constituention		

Test ID & References: Table 250 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tCSIVW1	142020	Table 353

Overview: The purpose of this test is to measure the minimum tCSIVW1 Margin of the CS eye diagram generated.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

- 2 Check for valid Clock (CK) and CS input test signals by verifying its frequency and amplitude values.
- 3 On the Oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - *b* Set the Sampling Rate of the Oscilloscope to the maximum value.
 - *c* Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
 - d Set Function 1 to duplicate the CK signal.
 - e Set the Color Grade Display option to ON.
 - f Set up Mask Test settings.
 - g Set up Clock Recovery on SDA.
 - : Explicit clock, Source = Function 1, Rising Edge
 - h Set the Real Time Eye on SDA to ON.
 - *i* Set up measurement threshold values for Function 1 and CS input signals.
 - *j* Change Trigger Source to 'CS input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CS bus.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - *c* Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
- a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CS Rx Voltage and Timing tests > vCENT CS mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- · Select 'WidestOpening' to use the widest eye opening as vCENT.
- · Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 7 Use the Histogram feature in the Infiniium Application to measure the tCSIVW1 Margin value for both corners of the Test Mask.

The tCSIVW1 Margin for each Test Mask corner is denoted by tCSIVW1_m1 and tCSIVW1_m2.

- 8 Find the minimum value between tCSIVW1_m1 and tCSIVW1_m2. Use the minimum value as the worst time gap.
- 9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2.

10 Report the worst time gap and margin percentage as test results.

Expected/ The measured tCSIVW1 Margin value for the test signal indicates if there is a violation in the mask region.

tCSIVW2 Margin

Availability Condition:	Table 251	Set Up tab options for availability of tests
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Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References: Table 252 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tCSIVW2	142021	Table 353

Overview: The purpose of this test is to measure the minimum tCSIVW2 Margin of the CS eye diagram generated.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CS input test signals by verifying its frequency and amplitude values.

- 3 On the Oscilloscope:
 - a Set the Trigger to 'Auto-Sweep'.
 - *b* Set the Sampling Rate of the Oscilloscope to the maximum value.
 - c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
 - *d* Set Function 1 to duplicate the CK signal.
 - e Set the Color Grade Display option to ON.
 - f Set up Mask Test settings.
 - g Set up Clock Recovery on SDA.
 - : Explicit clock, Source = Function 1, Rising Edge
 - h Set the Real Time Eye on SDA to ON.
 - i Set up measurement threshold values for Function 1 and CS input signals.
 - *j* Change Trigger Source to 'CS input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CS bus.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - *b* Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - *b* Under Eye Diagram Tests, navigate to CS Rx Voltage and Timing tests > vCENT CS mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.

- i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
- ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the tCSIVW2 Margin value for all the four corners of the Test Mask. The tCSIVW2 Margin for each Test Mask corner is denoted by tCSIVW2_m1, tCSIVW2_m2, tCSIVW2_m3 and tCSIVW2_m4.

- 8 Find the minimum value between tCSIVW2_m1, tCSIVW2_m2, tCSIVW2_m3 and tCSIVW2_m4. Use the minimum value as the worst time gap.
- 9 Calculate the margin (in percentage) using the equation:

Margin (%) = [(Worst_time_gap) / (Half of mask width)] x 100%

where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.

10 Report the worst time gap and margin percentage as test results.

Expected/ The measured tCSIVW2 Margin value for the test signal indicates if there is a violation in the mask region.

vCSIVW Margin

Availability Condition: Table 253 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS
Test ID & References:	Table 254 LPDDR5 To	est References from JES	SD209-5 specification		
	Symbol (in Specificatio	n)	Test ID	Reference	from Specification
	vCSIVW		142022		Table 353
Overview:	The purpose of this generated.	test is to measu	re the minimum vCSIVV	V Margin of t	he CS eye diagram
Procedure:	 Application. Check for valid values. On the Oscillos a Set the Trigg b Set the Sam c Set the Sam c Set the Sam g Set Function e Set the Colo f Set up Mask g Set up Clock : Explicit clock : Explicit clock : Explicit clock : Set up meas j Change Trigg such cases, 4 Perform Mask T a Set the Mask b Load the ma c Stop the Max waveforms s 5 Determine and a In the Config b Under Eye D 	Clock (CK) and C cope: Jer to 'Auto-Swee pling Rate of the pling Points to the Tests Only' confi- 1 to duplicate th r Grade Display o Test settings. Recovery on SDA ck, Source = Func Time Eye on SDA urement threshol- ger Source to 'CS when there is less Testing: Test Run Until se sk file and start the pecified in the co store the Vcent v jure tab of the Tes iagram Tests, nav	p'. Oscilloscope to the maxe user defined value con guration option in the C e CK signal. ption to ON. A. tion 1, Rising Edge to ON. d values for Function 1 input signal' on both Rise activity on CS bus. etting to 'Forever'. ne Mask Test. counter for 'Total Wave nfiguration option 'Tota alue. To determine the st Application, choose N	verifying its f ximum value. nfigured for t Configure tab and CS inpu ising/Falling forms' excee I Waveform'. value of Vcer Mode as Deb and Timing t	requency and amplitude he 'Sampling Points (Pts) for of the Test Application. t signals. Edges to prevent timeout for ds the number of required ht: ug. rests > vCENT CS mode (V).

		To obta	ain the vCEI	NT value with	'WidestOpening' s	selectec	ł:	
		i			ange is from 40% t center of the eye c			nplitude (that is, the eye
		ii	Scan for th 5mV.	ne widest eye	opening at the me	entionec	l search rang	e with a scan resolution of
		iii	Use the vo	ltage level at	the widest eye ope	ening as	s the value fo	r Vcent.
	6			st Mask so tha Configure tab.		the Vce	ent value with	the Test Mask width and
	7	the top	and the bo	ottom area of	the Test Mask.			vCSIVW Margin value for I vCSIVW Margin lower.
	8			n value betwe t voltage gap.		n Upper	and vCSIVW	Margin lower. Use this
	9	Calcula	ate the wors	st margin (in _l	percentage) using [.]	the equ	ation:	
			Març	gin (%) = [(Wc	orst_voltage_gap) /	′ (Half o	f mask heigh	t)] x 100%
		where, v bottom.		age_gap is th	e voltage gap betw	veen the	e mask and th	ne eye at the top and
	10	Report	the worst v	voltage gap a	nd the margin perc	centage	as test resul	ts.
/Expected Observable Results:		e measu gion.	ired value c	of vCSIVW Ma	argin for the test sig	gnal ind	licates if there	e is a violation in the mask
tCSIPW								
Availability Condition:	Tab	le 255	Set Up tab opt	tions for availabilit	ty of tests			
Supported CK Type	Suppo	orted WCK 1	lype Su	pports Offline?	R/W Separation ne	eeded?	SE Mode?	Required Signals
Burst & Continuous	N/A		No)	No		Yes	CK(Diff), CS
Test ID & References:	Tab	ole 256	LPDDR5 Test F	References from J	ESD209-5 specification			
	s	ymbol (in S	pecification)		Test ID		Reference fro	m Specification
	t	CSIPW			142023			Table 353
Overview:	Th	e purpos	se of this te	est is to verify	the minimum inpu	it CS Rx	pulse width	defined at the Vcent_CS.
Procedure:	1	This te:	st requires †	the following	pre-requisite test:			
	•		-	est ID: 142020				
		Locatic	on for Vcent	t is determine	d and its value is s	stored.		

	2 Perform the pulse width on the CS signal:
	a Set to ON the positive pulse width measurement and jitter statistics to measure all the edges.
	b Set the measurement threshold to a hysteresis of ±CS mask height at the threshold level of Vcent_CS.
	c Obtain the minimum result from the measurements as the worst positive pulse width.
	d Repeat steps a to c for negative pulse width and store the minimum result from the measurement as the worst negative pulse width.
	3 Compare the minimum values from the positive and negative pulse width results.
	4 Measure tDIPW as the time starting from a rising/falling edge of the CS signal to the time ending at the following falling/rising edge.
	5 Capture all values of tCSIPW.
	6 Convert the unit for the values from seconds to UI.
	7 Determine the worst result from the set of tCSIPW values measured and report it as the final test result.
Expected/ Observable Results:	The measured value of tCSIPW for the test signal shall be within the conformance limit as per the JESD209-5 specification.
vCSIHL_AC	
Availability Condition:	Table 257 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References: Table 258 LPDDR5 Test References from JESD209-5 specification

	Symbol (in Specification)	Test ID	Reference from Specification
-	vCSIHL_AC	142024	Table 353

Overview: The purpose of this test is to measure the CS single input pulse amplitude vCSIHL_AC that the pulse must meet or exceed at any point over the total UI.

Procedure: 1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CS input test signals by verifying its frequency and amplitude values.

3 Set up the oscilloscope:

a Set the Trigger to 'Auto-Sweep'.

b Set up measurement threshold values for the CSx channel and the CKx channel input.

c Set up fixed vertical scale values for CSx channel and CKx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered CK, Rise/Fall Edge

- g Set the Real Time Eye on SDA to ON.
- 4 Perform Mask Testing:
 - a Set the Mask Test Run Until setting to 'Forever'.
 - b Load the mask file and start the Mask Test.
 - c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
- 5 Determine and store the Vcent value. To determine the value of Vcent:
 - a In the Configure tab of the Test Application, choose Mode as Debug.
 - b Under Eve Diagram Tests, navigate to CS Rx Voltage and Timing tests > vCENT CS mode (V). This is the level, where the vertical center of the Eye Mask is placed.
 - · Select 'WidestOpening' to use the widest eye opening as vCENT.
 - Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

- The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye i height measured at the center of the eye diagram).
- Scan for the widest eye opening at the mentioned search range with a scan resolution of ii 5mV.
- iii Use the voltage level at the widest eye opening as the value for Vcent.
- 6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
- 7 Use the Histogram feature in the Infiniium Application to measure the vCSIHL_AC/2 values for the top and the bottom area of the Test Mask. The measured vCSIHL_AC/2 values is denoted as vCSIHL_AC/2_top and vCSIHL_AC/2_bottom.
- 8 Calculate vCSIHL_AC using the equation:

vCSIHL_AC = [vCSIHL_AC/2_top] - [vCSIHL_AC/2_bottom]

9 Report the measured vCSIHL_AC as test result.

Expected/ The measured value of vCSIHL AC for the test signal shall be within the conformance limit as per the JESD209-5 specification.

Observable Results:

6 Eye Diagram Tests



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