Keysight D9050LDDC LPDDR5 Test Application

KEYSIGHT TECHNOLOGIES

Methods of Implementation

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1 Overview

LPDDR5 Automated Testing—At a Glance

The Keysight D9050LDDC LPDDR5 Test Application helps you verify compliance of the SDRAM type (LPDDR5) to the respective JEDEC specifications using a supported Keysight Infiniium Oscilloscope. The Keysight D9050LDDC LPDDR5 Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE **The tests performed by the Keysight D9050LDDC LPDDR5 Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.**

For each SDRAM type being tested, you may refer to the following specification documents for compliance testing measurements. For more information, see the JEDEC website: https://www.jedec.org/.

SDRAM Type	Reference Documents
LPDDR5	JEDEC Standard, LPDDR5, JESD209-5, February 2019

Required Equipment and Software

In order to run the LPDDR5 automated tests, you need the following equipment and software:

Hardware

- Use one of the following Oscilloscope models. Refer to www.keysight.com for the respective bandwidth ranges.
  - Keysight DSO9000A-Series, DSO90000A-Series and DSOX90000A/Q/Z/V-Series Oscilloscopes with a minimum bandwidth of 8GHz (recommended) for accurate measurements. For faster speed grade devices, a minimum bandwidth of 13GHz bandwidth is recommended.
  - Keysight UXR Oscilloscopes
- Target Device Under Test (DUT)
- InfiniiMax probe amplifiers:
  - N1169A – 12GHz InfiniiMax II probe amplifier
  - N2803A – 30GHz InfiniiMax III probe amplifier
  - N2802A – 25GHz InfiniiMax III probe amplifier
  - N2801A – 20GHz InfiniiMax III probe amplifier
  - N2800A – 16GHz InfiniiMax III probe amplifier
  - N2831A – 8GHz InfiniiMax III probe amplifier
  - N2832A – 12GHz InfiniiMax III probe amplifier
- InfiniiMax probe heads – InfiniiMax I/II probe heads and accessories (compatible with 9000 Series and 90000 Series, use N5442A precision BNC adapter with 90000X/Q Series):
  - N5381A – InfiniiMax II 12GHz differential solder-in probe head and accessories
  - N5382A – InfiniiMax II 12GHz differential browser
  - E2677A – InfiniiMax II 12GHz differential solder-in probe head and accessories
  - N5425A – InfiniiMax II 12GHz ZIF probe head
  - N5426A – InfiniiMax II ZIF tips (×10)
- InfiniiMax III probe heads and accessories:
  - N5451A – Long Wire tips (×10)
  - N5439A – ZIF probe head
  - N5445A – Browser (hand held) probe head
  - N5441A – Solder-in probe head
  - N2838A - 450 **Ω** PCB ZIF tips (set of 5)
  - N2848A – InfiniiMax III QuickTip head
  - N2849A – InfiniiMax III Quick tips (4 per kit)
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Precision 3.5 mm BNC to SMA male adapter, Keysight p/n 54855-67604, qty = 2 (provided with the Keysight 54855A and 80000B series oscilloscopes)
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length
- Keysight also recommends using a second monitor to view the test application.

Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight D9050LDDC LPDDR5 Test Application Release Notes)
- Keysight D9050LDDC LPDDR5 Test Application software
- Keysight E2688A Serial Data Analysis and Clock Recovery software (for clock recovery)

Licensing information

Refer to the *Data Sheet* pertaining to LPDDR5 Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9050LDDC" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 17 to see the difference in installing a license key using either of the applications on your machine.

In This Book

This manual describes the tests that are performed by the Keysight D9050LDDC LPDDR5 Test Application in more detail; it contains information from (and refers to) the LPDDR5 specification and it describes how the tests are performed.

- Chapter 1, “Overview” gives an overview of the automated test application and the required equipment and software.
- Chapter 2, “Installing the Test Application and Licenses” explains how to obtain the installer for the automated test application and install the associated licenses (if it was purchased separately).
- Chapter 3, “Preparing to Take Measurements” describes how to launch the Keysight D9050LDDC LPDDR5 Test Application and gives a brief overview of how it is used.
- Chapter 4, “Electrical Tests” describes the methods of implementation for WRITE and READ cycle electrical tests performed on LPDDR5 devices.
- Chapter 5, “Timing Tests” describes the methods of implementation for timing tests performed on LPDDR5 devices.
- Chapter 6, “Eye Diagram Tests” describes the methods of implementation for eye diagram tests performed on LPDDR5 devices.

See Also

The Keysight D9050LDDC LPDDR5 Test Application’s Online Help, which describes:

- Starting the LPDDR5 Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

2 Installing the Test Application and Licenses

If you purchased the D9050LDDC LPDDR5 Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

Installing the Test Application

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9050LDDC release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.
2. To obtain the LPDDR5 Test Application, go to Keysight website: "http://www.keysight.com/find/D9050LDDC".
3. In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

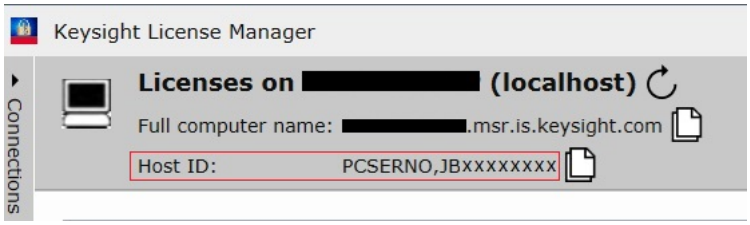

Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

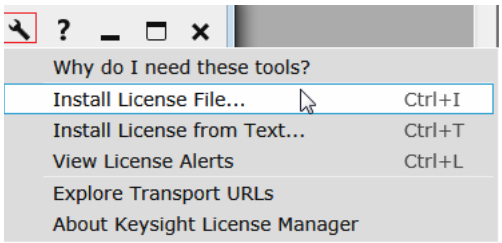

Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1. Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

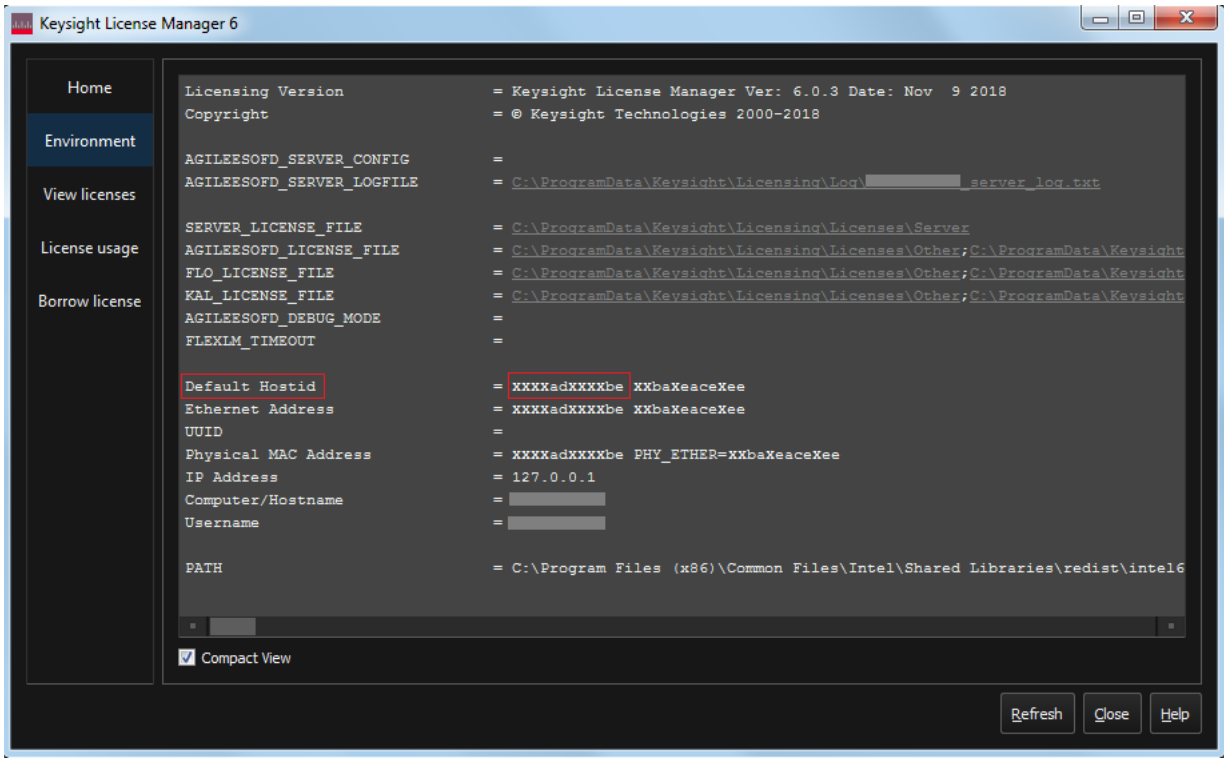

Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager 6.

3 From the Home tab, use one of the options to install each license file.

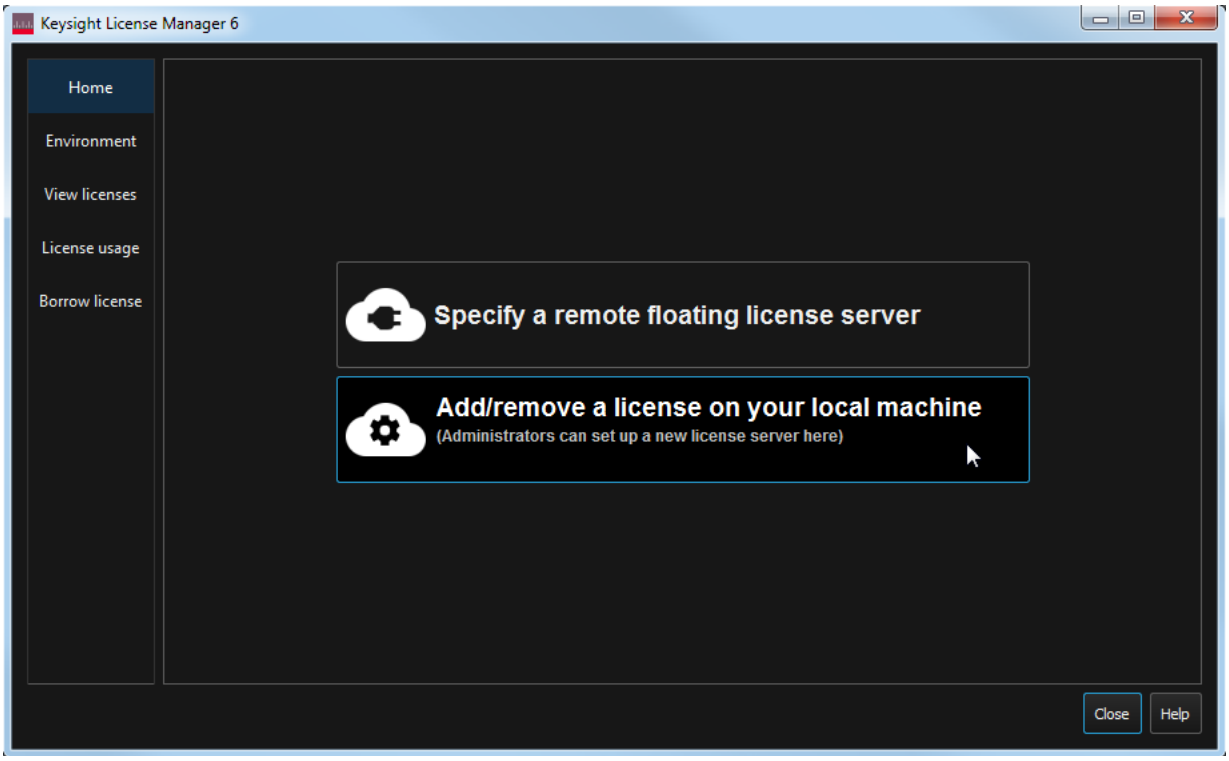

Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

3 Preparing to Take Measurements

Before running the automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the LPDDR5 Test Application and perform the measurements.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the LPDDR5 Test Application

1 Ensure that the LPDDR5 Device Under Test (DUT) is operating and set to desired test modes. To start the LPDDR5 Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9050LDDC LPDDR5 Test App**.

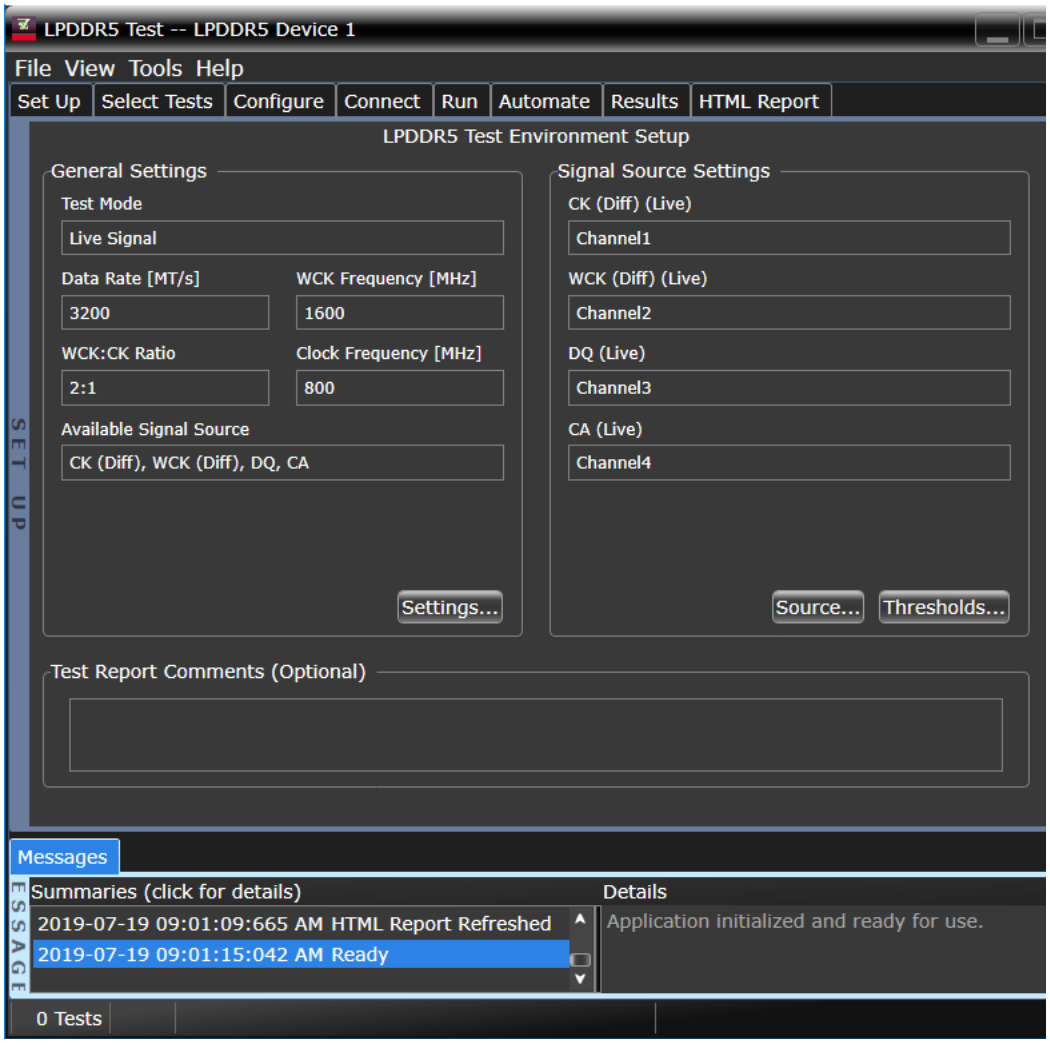

Figure 5 LPDDR5 Test Application Main Window

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9050LDDC LPDDR5 Test Application Online Help* available in the Help menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

Configuring Set Up tab for availability of specific tests

The **Set Up** tab consists of configuration options that correspond to the LPDDR5 device under test (DUT). Select the appropriate options for the relevant tests to appear.

The configuration options specified in the previous table can be set in specific areas of the LPDDR5 Test Application:

- **LPDDR5 General Setup**—Configure parameters specific to the DUT. To access this window, click **Settings...** under the **Set Up** tab.

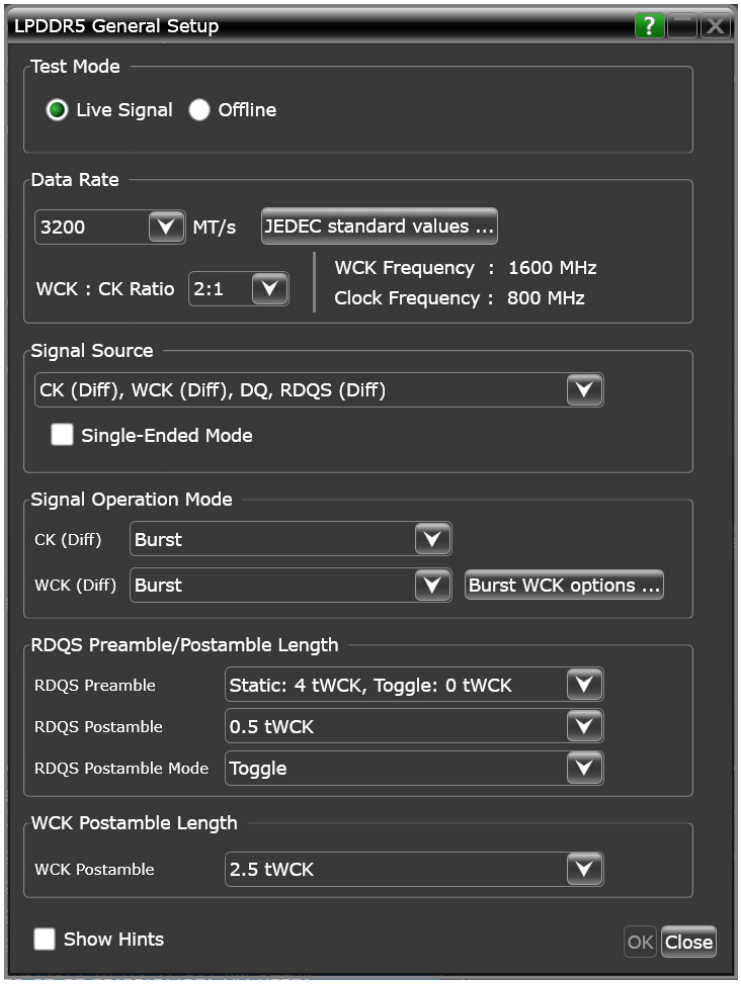

Figure 6 General Settings under Set Up tab

- **Test Mode**—select whether to run tests on a live signal (with DUT connected) or on offline signal (saved waveforms).
- **Data Rate**—select the speed grade for test signal transmission and the frequency ratio for Write Clock (WCK) and Clock (CK) signal.
- **Signal Source**—Select the combination of signals for the corresponding LPDDR5 tests to appear in the Select Tests tab.
- **Signal Operation Mode**—select whether the differential clock and differential write clock signals will be transmitted in either continuous or burst modes. For WCK bursts, you may select the read/write separation technique.

- **RDQS Preamble/Postamble Length**—Select the length of RDQS preamble and postamble when RDQS (Diff) is selected as one of the test signals.
- **WCK Postamble Length**—Select the length of WCK postamble when WCK (Diff) is selected as one of the test signals.

- **Signal Source Setup**—To access this window, click **Source...** under the **Set Up** tab.
  - For **Live** Signal Test Mode, assign Oscilloscope Channels to each signal selected under **Signal Source**.

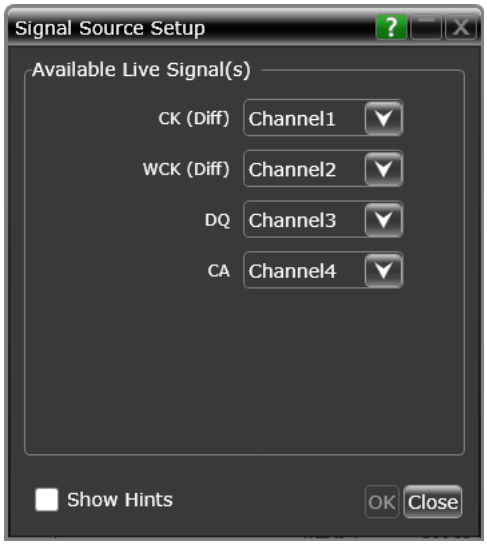

Figure 7 Signal Source Settings under Set Up tab

  - For **Offline** Test Mode, click **Browse...** against each signal type and select the offline waveform file in *wfm* format.

Figure 8 Signal Source Settings under Set Up tab

- Threshold Setup—To access this window, click **Thresholds...** under the **Set Up** tab.
  - Under **Signal Thresholds** tab, verify or modify the upper, middle and lower threshold values for each selected **Signal Source** type.

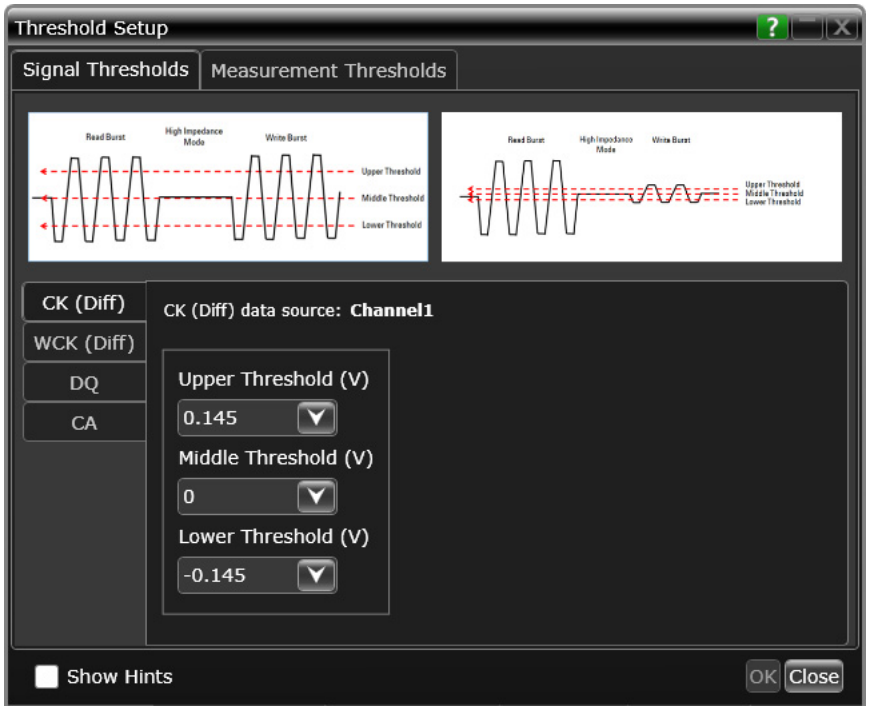

Figure 9 Signal threshold settings

- Under **Measurement Thresholds** tab, verify or modify the corresponding threshold values required for measurements to be performed on each selected **Signal Source** type.

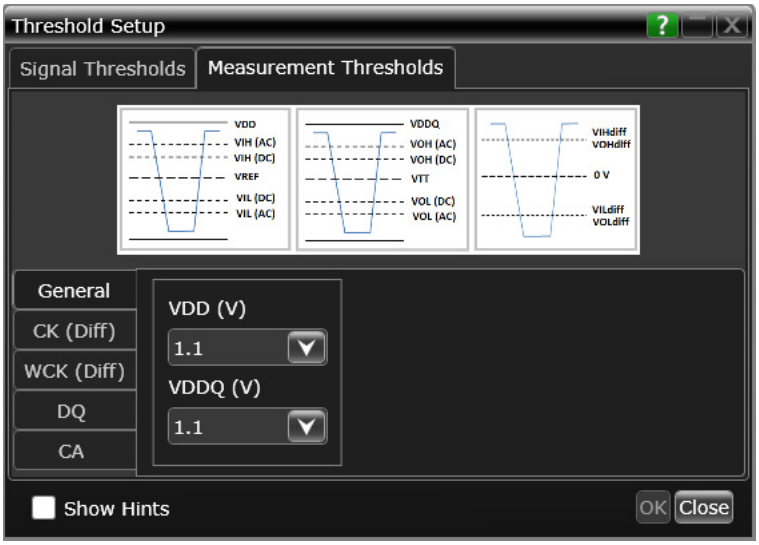

Figure 10 Measurement threshold settings

Click **OK** to apply and save any changes made to each window for the settings to take effect.

NOTE

The prerequisite Test IDs indicate all such tests that must be run prior to the corresponding tests. It is possible that one or more of the prerequisite tests may not have been selected prior to running the related test. However, the LPDDR5 Test Application automatically runs such tests and displays the resulting values.

4 Electrical Tests

RDQS Detect Method for Read Write Separation

RDQS Detect is a read write separation method. This method works when the signal source contains at least an RDQS signal and a WCK signal. In this method, the Read/Write burst data is identified based on the presence of RDQS burst. If WCK burst contains an RDQS burst, then it is a Read burst. If the WCK burst does not contain an RDQS burst, then it is a Write burst.

If you select the RDQS Detect mode as the burst identification method, you must select the length of the WCK Postamble in the WCK Postamble Length section of the LPDDR5 General Setup dialog box.

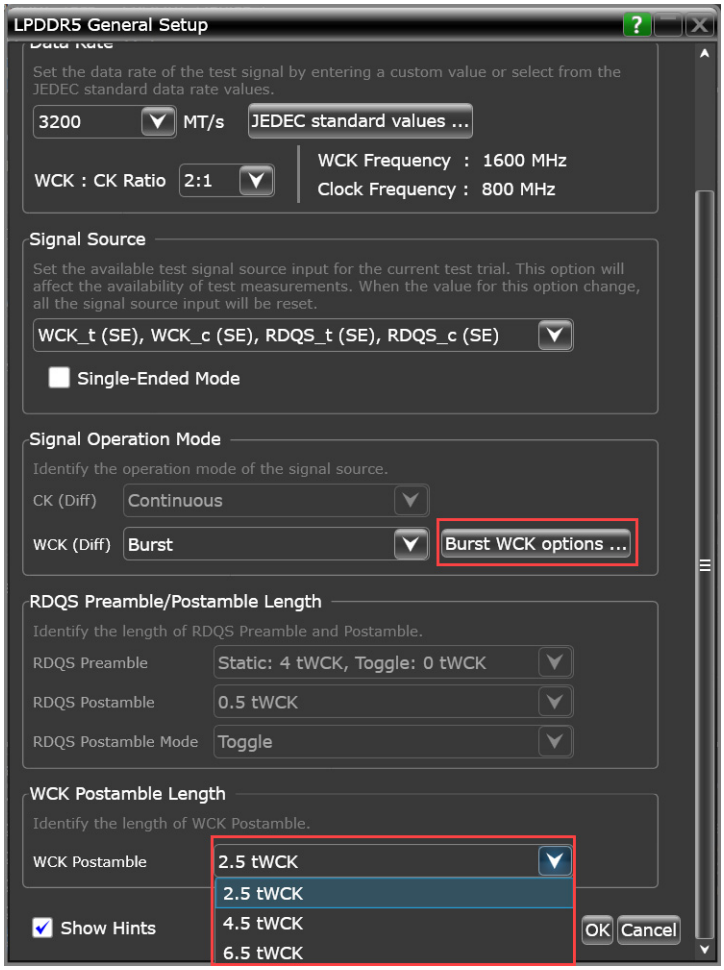

Figure 11 LPDDR5 General Setup Dialog

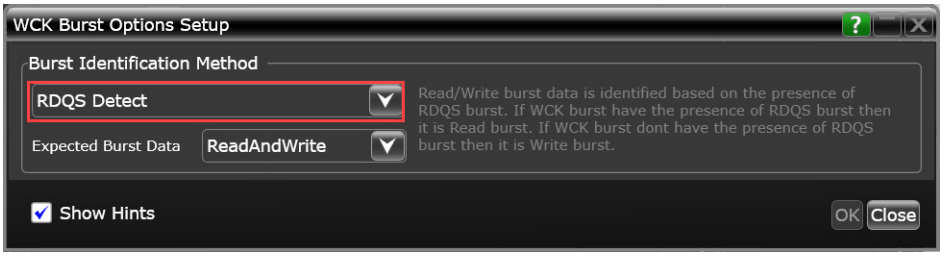

Figure 12 WCK Burst Options Setup Dialog

Tests that support the RDQS Detect Burst Identification Method

The following Electrical tests support the RDQS Burst Identification method:

WRITE Tests

- Vindiff_WCK
- Vindiff_WCK/2HighPulse
- Vindiff_WCK/2LowPulse
- Vinse_WCK (Positive Pulse)
- Vinse_WCK (Negative Pulse)
- Vinse_WCK_High (WCK_t)
- Vinse_WCK_High (WCK_c)
- Vinse_WCK_Low (WCK_t)
- Vinse_WCK_Low (WCK_c)
- VIHdiff_WCK
- VILdiff_WCK
- SRIdiffR_WCK
- SRIdiffF_WCK
- Vix_WCK_Ratio
- Vinse_WCK_SE
- Vinse_WCK_SE_High
- Vinse_WCK_SE_Low
- SRIseR_WCKSE
- SRIseF_WCKSE

READ Tests

- SRQseR_DQ
- SRQseF_DQ
- SRQdiffR_RDQS
- SRQdiffF_RDQS

Method of Implementation for the RDQS Detect Burst Identification Method

The following are the steps for the method of implementation for the RDQS Detect burst identification method:

1 Populate the burst from WCK signal.

2 Locate FirstWCKRising for the burst.

3 Compute TimeA = FirstWCKRising + tWCKPRE_Toggle_RD * ClockCycleWidth.

4 Compute TimeB = Start of WCK postamble. For example, if tWCKPST=2.5nWCK then TimeB = time of second last rising edge of WCK burst. If tWCKPST=4.5nWCK then TimeB = time of fourth last rising edge of WCK burst.

5 Compute TimeC = 0.5*(TimeA+TimeB)

6 Compute VmaxTimeCWithinUI = Vmax range from (TimeC - 1*UI) to (TimeC + 1*UI)

7 Compute VminTimeCWithinUI = Vmin range from (TimeC - 1*UI) to (TimeC + 1*UI)

8 If [(VmaxTimeCWithinUI > VOHDiff_RDQS) AND (VminTimeCWithinUI < VOLDiff_RDQS)] then the burst will be recognized as a READ burst. Otherwise, the burst will be recognized as a WRITE burst.

9 Repeat steps 2 to 8 for the rest of burst.

Data tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 13.

NOTE VDD is considered as VDD2H for CA[6:0], CK_t, CK_c, CS and RSET_n signals; whereas, VDD is considered as VDDQ for DQ, DMI, RDQS_t, WCK_t and WCK_c. Also, Vss = 0V.

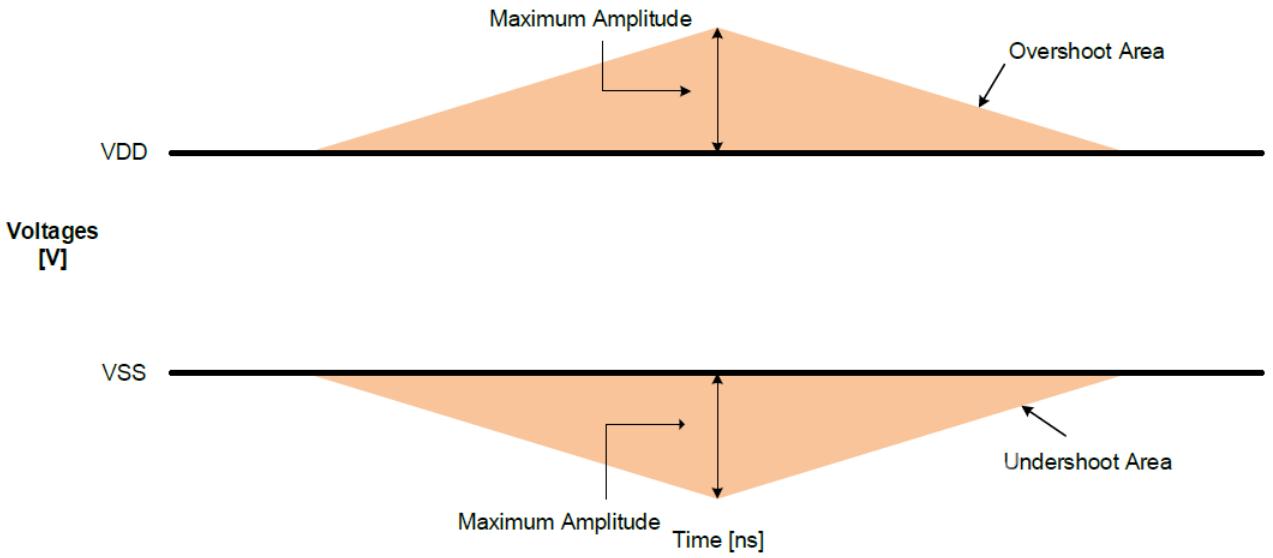

Figure 13 Overshoot and Undershoot definition for DQ signal

Overshoot_Amplitude_DQ

Availability Condition: **Table 1 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	DQ

Test ID & References: **Table 2 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152200	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the "OvershootRegion" across the acquired waveform.
An "OvershootRegion" starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

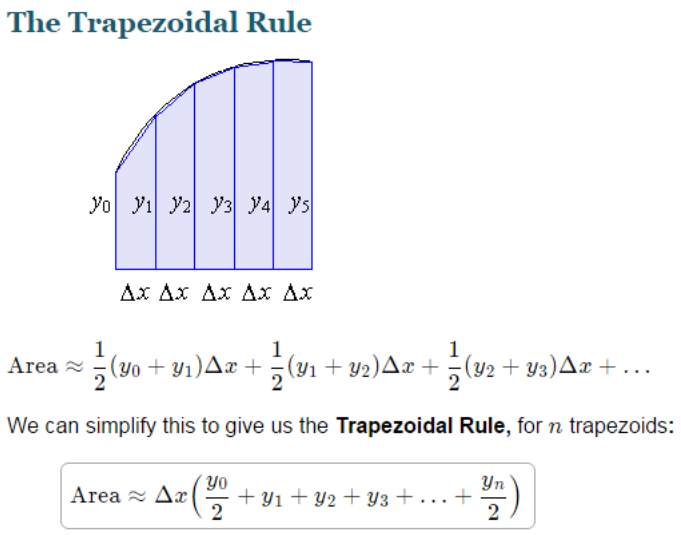

Figure 14 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

4 Repeat step 3 for the rest of the "OvershootRegion" found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Amplitude_DQ

Availability Condition: **Table 3 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	DQ

Test ID & References: **Table 4 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152201	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

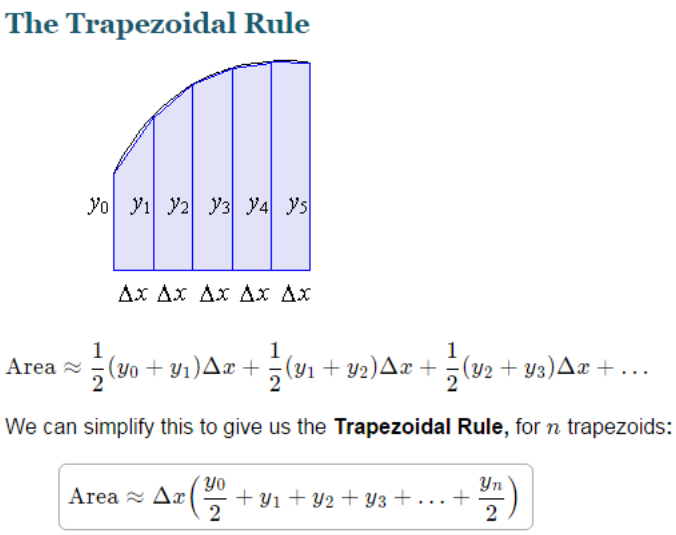

Figure 15 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Undershoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_DQ

Availability Condition: **Table 5 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	DQ

Test ID & References: **Table 6 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152202	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

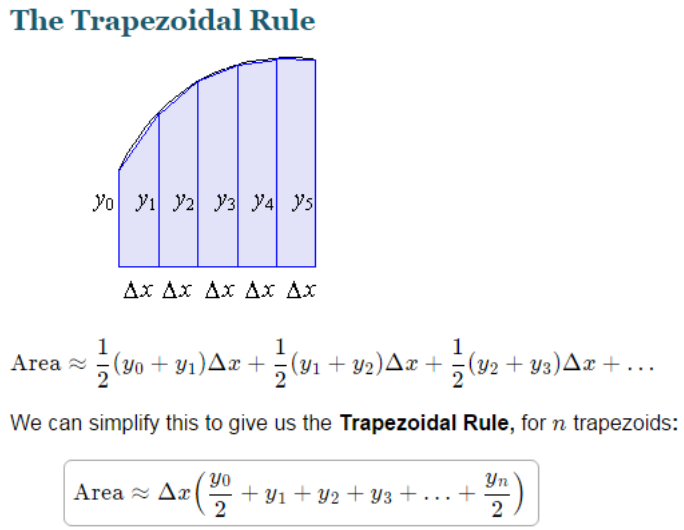

Figure 16 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Area_DQ

Availability Condition: **Table 7 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	DQ

Test ID & References: **Table 8 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum undershoot area above VSS	152203	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

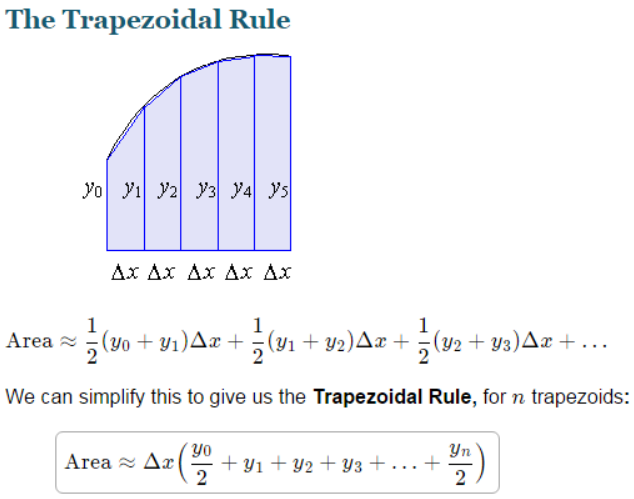

Figure 17 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
   - Undershoot Amplitude
   - Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Output slew rate for single-ended signals are measured as shown in Figure 18.

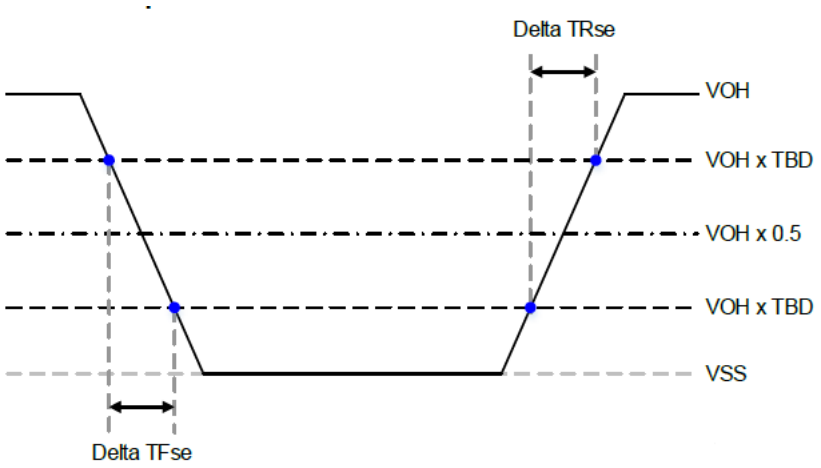

Figure 18 Single-ended output slew rate definition for DQ signal

SRQseR_DQ

Availability Condition: **Table 9 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)

Test ID & References: **Table 10 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRQse	150000	Table 325

Overview: The purpose of this test is to verify the rising slew rate value of the test signal within the read burst.

Procedure:

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all the valid rising edges in the specified burst.
A valid rising edge starts at V_{OL} crossing and ends at the following V_{OH} crossing.

4 For all the valid rising edges, find the transition time, T_R.
T_R is the time starting at V_{OL} crossing and ending at the following V_{OH} crossing.

5 Calculate SRQseR_DQ using the equation:

$$SRQseR\_DQ = [V_{OH} - V_{OL}] / T_R$$

6 Determine the worst result from the set of SRQseR_DQ measured.

Expected/ Observable Results: The calculated Rising Slew (SRQseR_DQ) value for the test signal shall be within the conformance limits as per the JEDEC specification.

SRQseF_DQ

Availability Condition: **Table 11 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)

Test ID & References: **Table 12 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRQse	150001	Table 325

Overview: The purpose of this test is to verify the falling slew rate value of the test signal within the read burst.

Procedure:

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all the valid falling edges in the specified burst.
A valid falling edge starts at V_{OH} crossing and ends at the following V_{OL} crossing.

4 For all the valid falling edges, find the transition time, T_F.
T_R is the time starting at V_{OH} crossing and ending at the following V_{OL} crossing.

5 Calculate SRQseF_DQ using the equation:

$$SRQseF\_DQ = [V_{OH} - V_{OL}] / T_F$$

6 Determine the worst result from the set of SRQseF_DQ measured.

Expected/ Observable Results: The calculated Falling Slew (SRQseF_DQ) value for the test signal shall be within the conformance limits as per the JEDEC specification.

Command/Address tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 19.

NOTE VDD is considered as VDD2H for CA[6:0], CK_t, CK_c, CS and RSET_n signals; whereas, VDD is considered as VDDQ for DQ, DMI, RDQS_t, WCK_t and WCK_c. Also, Vss = 0V.

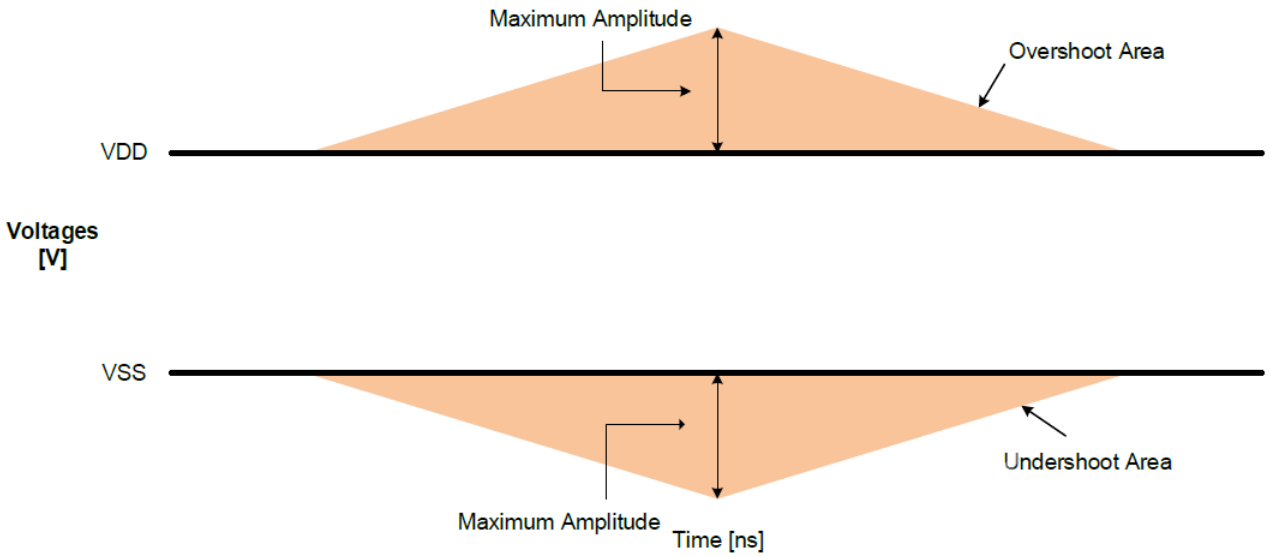

Figure 19 Overshoot and Undershoot definition for CA signal

Overshoot_Amplitude_CA

Availability Condition: **Table 13 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CA

Test ID & References: **Table 14 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152300	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD2H}$$

b Evaluate Area_below_V_{DD2H} using the equation:

$$\text{Area\_below\_}V_{DD2H} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD2H}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

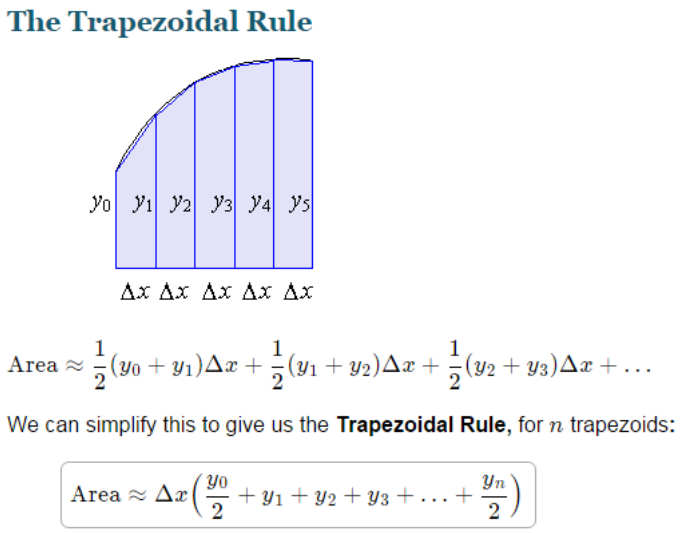

Figure 20 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD2H} using the equation:

$$\text{Area\_Above\_}V_{DD2H} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD2H}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD2H}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Amplitude_CA

Availability Condition: **Table 15 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CA

Test ID & References: **Table 16 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152301	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

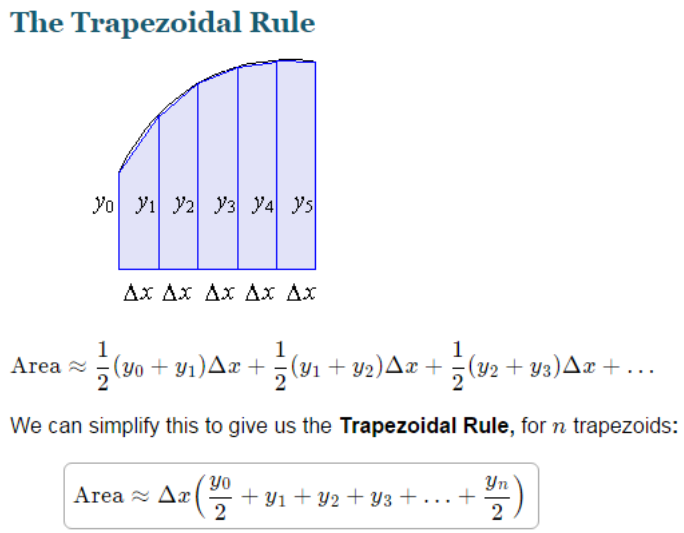

Figure 21 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Overshoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_CA

Availability Condition: **Table 17 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CA

Test ID & References: **Table 18 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152302	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD2H}$$

b Evaluate Area_below_V_{DD2H} using the equation:

$$\text{Area\_below\_}V_{DD2H} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD2H}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

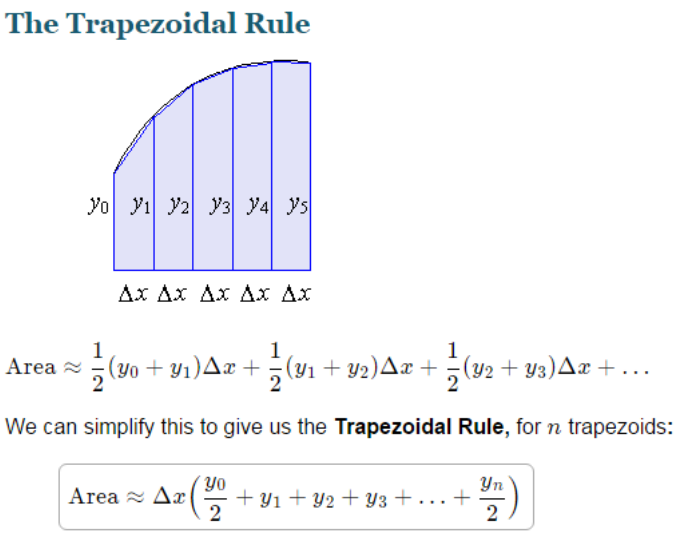

Figure 22 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_0V - Area_below_V_{DD2H}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD2H}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Area_CA

Availability Condition: **Table 19 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CA

Test ID & References: **Table 20 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum undershoot area above VSS	152303	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

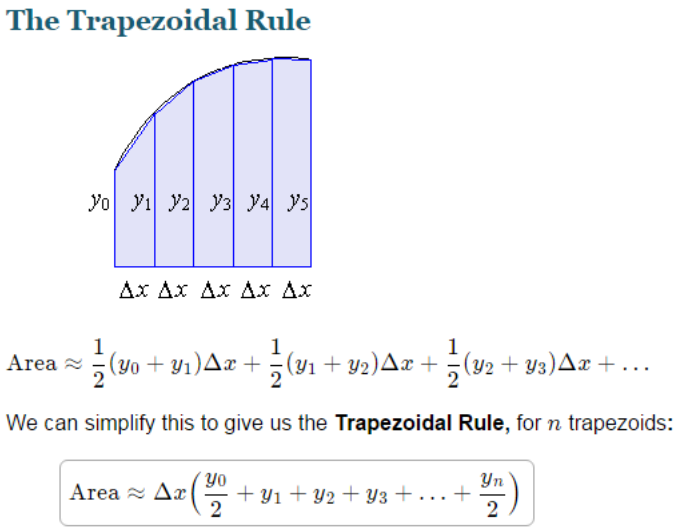

Figure 23 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Overshoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Chip Select tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.

NOTE VDD is considered as VDD2H for CA[6:0], CK_t, CK_c, CS and RSET_n signals; whereas, VDD is considered as VDDQ for DQ, DMI, RDQS_t, WCK_t and WCK_c. Also, Vss = 0V.

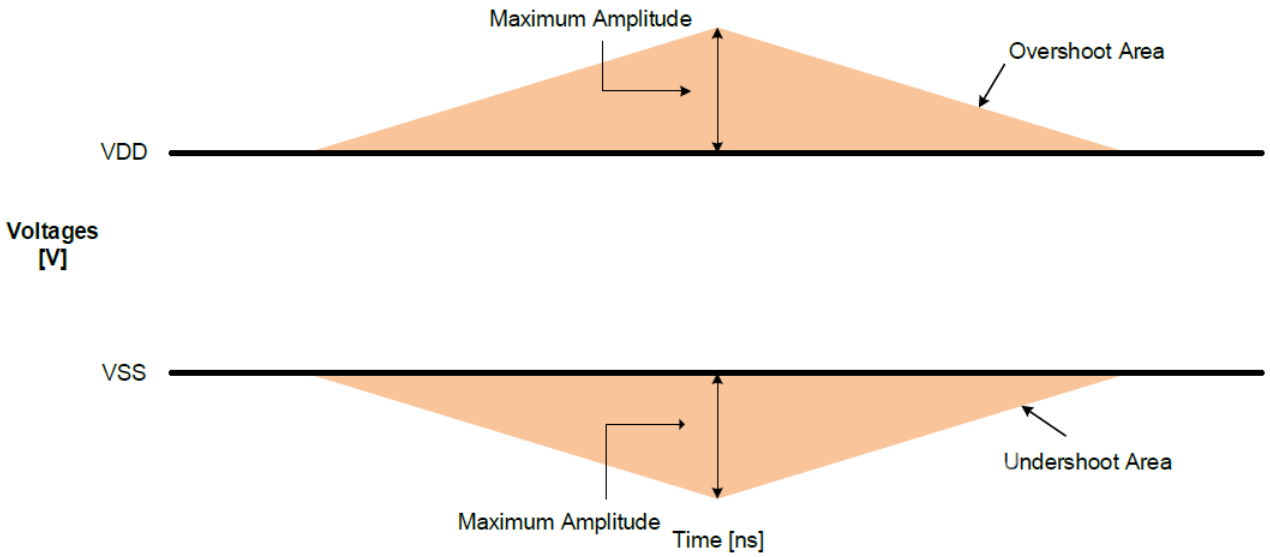

Figure 24 Overshoot and Undershoot definition for CS signal

Overshoot_Amplitude_CS

Availability Condition: **Table 21 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CS

Test ID & References: **Table 22 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152400	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD2H}$$

b Evaluate Area_below_V_{DD2H} using the equation:

$$\text{Area\_below\_}V_{DD2H} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD2H}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

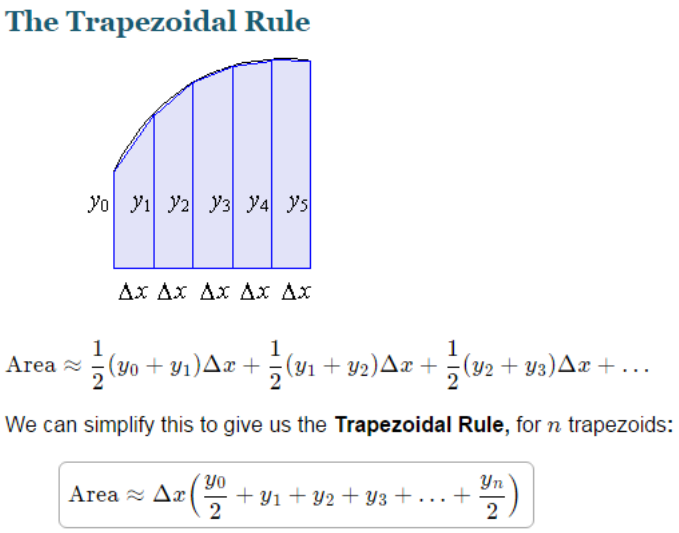

Figure 25 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD2H} using the equation:

$$\text{Area\_Above\_}V_{DD2H} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD2H}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD2H}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Amplitude_CS

Availability Condition: **Table 23 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CS

Test ID & References: **Table 24 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152401	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

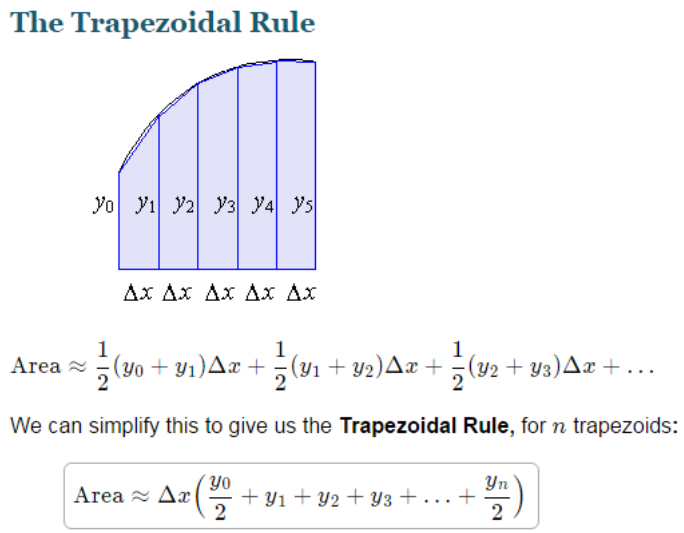

Figure 26 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Overshoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_CS

Availability Condition: **Table 25 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CS

Test ID & References: **Table 26 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152402	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD2H}$$

b Evaluate Area_below_V_{DD2H} using the equation:

$$\text{Area\_below\_}V_{DD2H} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD2H}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

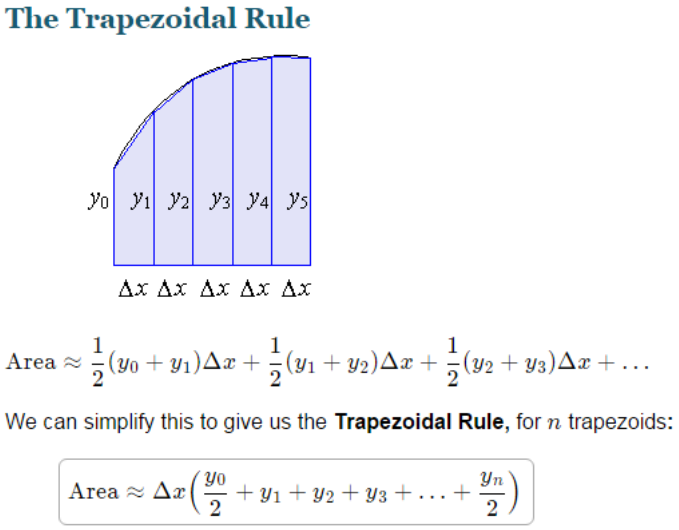

Figure 27 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_0V - Area_below_V_{DD2H}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD2H}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Area_CS

Availability Condition: **Table 27 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	CS

Test ID & References: **Table 28 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum undershoot area above VSS	152403	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

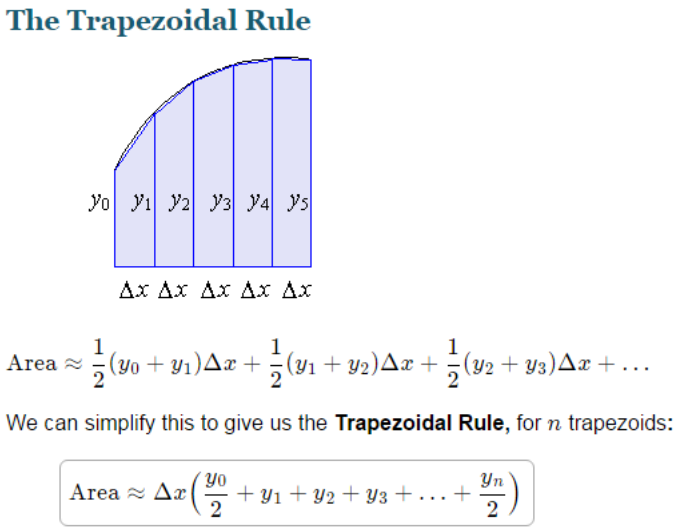

Figure 28 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Overshoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Clock (Diff) Tests

Consider Figure 29 to understand how the minimum input differential voltage is measured at the input receiver.

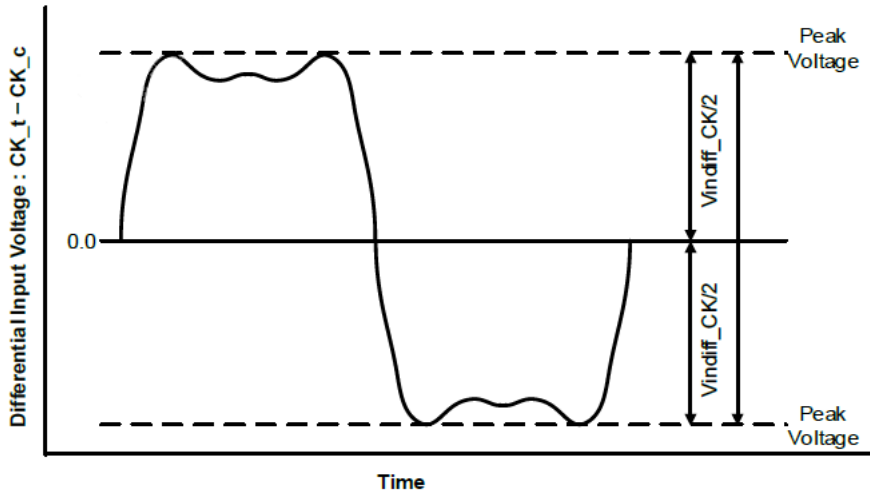

Figure 29 CK Differential input voltage

Vindiff_CK

Availability Condition: **Table 29 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: **Table 30 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vindiff_CK	151000	Table 313

Overview: The purpose of this test is to verify that the peak-to-peak voltage on the test signal centered on 0V differential is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid positive and negative pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock, whereas a valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.

4 Measure the max. Peak Voltage (Vmax) of the first positive pulse and the Min. Peak Voltage (Vmin) of the first negative pulse.

5 Calculate the difference of the two measurements and denote the result as Vindiff_CK#1.

$$Vindiff\_CK\#1 = Vmax - Vmin$$

6 Then, measure Vmin of first negative pulse and Vmax of the second positive pulse.

7 Calculate the difference of the two measurements and denote the result as Vindiff_CK#2.

8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.

9 Determine the worst result from the set of Vindiff_CK values measured.

Expected/ Observable Results: The measured value of Vindiff_CK for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Vindiff_CK/2HighPulse

Availability Condition: **Table 31 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: **Table 32 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vindiff_CK	151001	Table 313

Overview: The purpose of this test is to verify that the peak voltage of the high pulse of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid positive pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.

4 Zoom into the first pulse and measure the max. Peak Voltage (Vmax). Consider Vmax as the value of Vindiff_CK/2.

5 Continue the previous step with the rest of the positive pulses found in the specified waveform.

6 Determine the worst result from the set of Vindiff_CK/2 values that are measured.

Expected/ Observable Results: The measured value of Vindiff_CK/2 for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Vindiff_CK/2LowPulse

Availability Condition: **Table 33 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: **Table 34 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vindiff_CK	151002	Table 313

Overview: The purpose of this test is to verify that the peak voltage of the low pulse of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the clock signal under test.

3 Find all valid negative pulses of the Clock in the entire waveform.
A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.

4 Zoom into the first pulse and measure the min. Peak Voltage (Vmin). Consider Vmin as the value of Vindiff_CK/2.

5 Continue the previous step with the rest of the negative pulses found in the specified waveform.

6 Determine the worst result from the set of Vindiff_CK/2 values that are measured.

Expected/ Observable Results: The measured value of Vindiff_CK/2 for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Input slew rate for differential signals are measured as shown in Figure 30.

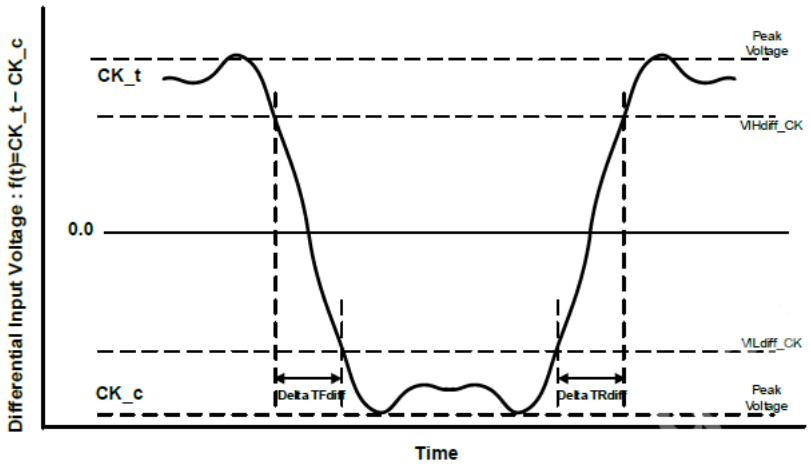

Figure 30 Differential input slew rate definition for differential clock signal

VIHdiff_CK

Availability Condition: **Table 35 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: **Table 36 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
VIHdiff_CK	151006	Table 316

Overview: The purpose of this test is to verify that the high level differential input voltage value of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock positive pulse in the triggered waveform.
A valid Clock positive pulse starts at the 0V crossing at valid Clock rising edge and ends at the 0V crossing at the following valid Clock falling edge.

4 Zoom into the first pulse and measure the top voltage V_{TOP}. Here, V_{TOP} is the voltage value on the rising edge after which the signal loses the monotonicity of the slope.
Consider the value of V_{TOP} as VIHdiff_CK.

5 Continue the previous step for all positive pulses found in the specified waveform.

6 Determine the worst result from the set of VIHdiff_CK values that are measured.

Expected/ Observable Results: The worst measured VIHdiff_CK for the test signal shall be within the conformance limits as per the JESD209-5 specification.

VILdiff_CK

Availability Condition: **Table 37 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: **Table 38 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
VILdiff_CK	151007	Table 316

Overview: The purpose of this test is to verify the low level differential input voltage value of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid Clock negative pulse in the triggered waveform.
A valid Clock negative pulse starts at the 0V crossing at valid Clock falling edge and ends at the 0V crossing at the following valid Clock rising edge.

4 Zoom into the first pulse and measure the base voltage V_{BASE}. Here, V_{BASE} is the voltage value on the falling edge after which the signal loses the monotonicity of the slope.
Consider the value of V_{BASE} as VILdiff_CK.

5 Continue the previous step for all negative pulses found in the specified waveform.

6 Determine the worst result from the set of VILdiff_CK values that are measured.

Expected/ Observable Results: The worst measured VILdiff_CK for the test signal shall be within the conformance limits as per the JESD209-5 specification.

SRIdiffR_CK

Availability Condition: **Table 39 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: **Table 40 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRIdiffR_CK	151008	Table 317

Overview: The purpose of this test is to verify that the differential input slew rate for rising edge of the Clock signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all the valid Clock rising edges in the entire waveform.

A valid clock rising edge starts at VILdiff_CK crossing and ends at the following VIHdiff_CK crossing.

4 For all the valid Clock rising edges, measure the transition time, DeltaTRdiff.
DeltaTRdiff is the time starting at VILdiff_CK crossing and ending at the following VIHdiff_CK crossing.

5 Calculate SRIdiffR_CK using the equation:

$$SRIdiffR\_CK = [VIHdiff\_CK - VILdiff\_CK] / DeltaTRdiff$$

6 Determine the worst result from the set of SRIdiffR_CK measured.

Expected/ Observable Results: The measured value of SRIdiffR_CK for the Clock signal shall be within the conformance limits as per the JESD209-5 specification.

SRIdiffF_CK

Availability Condition: **Table 41 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: **Table 42 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRIdiffF_CK	151009	Table 317

Overview: The purpose of this test is to verify that the differential input slew rate for falling edge of the Clock signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the clock signal under test.

3 Find all the valid Clock falling edges in the entire waveform.

A valid clock falling edge starts at VIHdiff_CK crossing and ends at the following VILdiff_CK crossing.

4 For all the valid Clock falling edges, measure the transition time, DeltaTFdiff.
DeltaTFdiff is the time starting at VIHdiff_CK crossing and ending at the following VILdiff_CK crossing.

5 Calculate SRIdiffF_CK using the equation:

$$SRIdiffF\_CK = [VILdiff\_CK - VIHdiff\_CK] / DeltaTFdiff$$

6 Determine the worst result from the set of SRIdiffF_CK measured.

Expected/ Observable Results: The measured value of SRIdiffF_CK for the Clock signal shall be within the conformance limits as per the JESD209-5 specification.

The minimum input single-ended voltage is measured as shown in Figure 31.

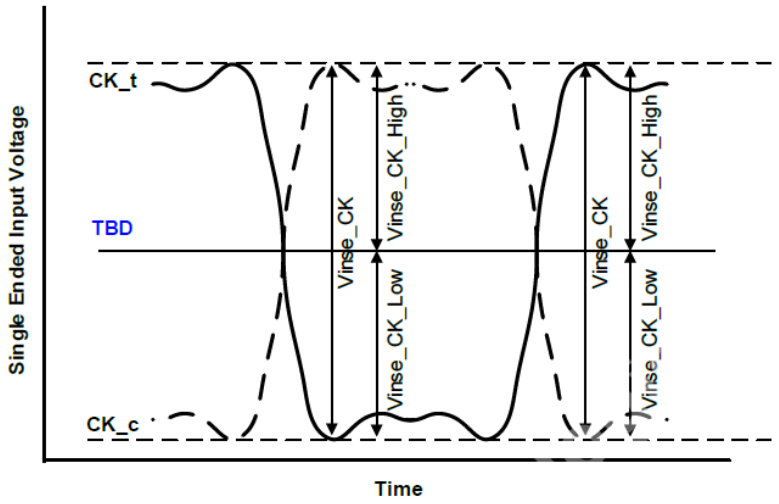

Figure 31 Clock Single-ended Input Voltage definition

Vinse_CK (Positive Pulse)

Availability Condition: **Table 43 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: **Table 44 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK	151010	Table 314

Overview: The purpose of this test is to verify the peak voltage of high pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid positive pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.

4 Zoom into the first pulse and measure V_{MAX}.

5 Calculate the value of Vinse_CK (Positive Pulse) using the equation:

$$\text{Vinse\_CK (Positive Pulse)} = V_{MAX} - V_{REF}$$

NOTE For this test, the Test App considers Vref to be ($V_{REFdiff\_CK}$), which in turn, is typically set to 0V.

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK (Positive Pulse) measured.

Expected/ Observable Results: The measured value of Vinse_CK (Positive Pulse) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_CK (Negative Pulse)

Availability Condition: **Table 45 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK(Diff)

Test ID & References: **Table 46 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK	151011	Table 314

Overview: The purpose of this test is to verify the peak voltage of low pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the clock signal under test.

3 Find all valid negative pulses of the Clock in the entire waveform.
A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.

4 Zoom into the first pulse and measure V_{MIN}.

5 Calculate the value of Vinse_CK (Negative Pulse) using the equation:

$$\text{Vinse\_CK (Negative Pulse)} = V_{REF} - V_{MIN}$$

NOTE For this test, the Test App considers Vref to be ($V_{REFdiff\_CK}$), which in turn, is typically set to 0V.

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK (Negative Pulse) measured.

Expected/ Observable Results: The measured value of Vinse_CK (Negative Pulse) for the test signal shall be within the conformance limits as per the JEDEC specification.

Write Clock (Diff) Tests

Consider Figure 32 to understand how the minimum input differential voltage is measured at the input receiver.

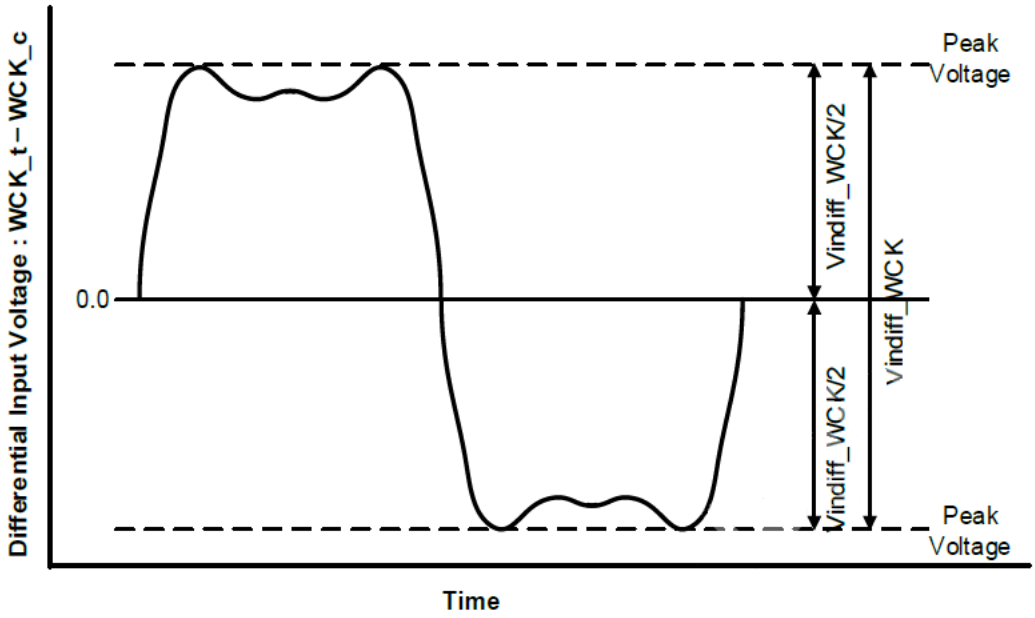

Figure 32 WCK Differential input voltage definition

Vindiff_WCK

Availability Condition: **Table 47 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 48 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vindiff_WCK	151100	Table 319

Overview: The purpose of this test is to verify that the peak-to-peak voltage on the test signal centered on 0V differential is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the Write Clock signal under test.

3 Find all valid positive and negative pulses of the Write Clock in the entire waveform.
A valid positive pulse on the Write Clock starts at the valid rising edge of the Write Clock and ends at the following valid falling edge of the Write Clock, whereas a valid negative pulse on the Write Clock starts at the valid falling edge of the Write Clock and ends at the following valid rising edge of the Write Clock.

4 Measure the max. Peak Voltage (Vmax) of the first positive pulse and the Min. Peak Voltage (Vmin) of the first negative pulse.

5 Calculate the difference of the two measurements and denote the result as Vindiff_WCK#1.

$$Vindiff\_WCK\#1 = Vmax - Vmin$$

6 Then, measure Vmin of first negative pulse and Vmax of the second positive pulse.

7 Calculate the difference of the two measurements and denote the result as Vindiff_WCK#2.

8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.

9 Determine the worst result from the set of Vindiff_WCK values measured.

Expected/ Observable Results: The measured value of Vindiff_WCK for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Vindiff_WCK/2HighPulse

Availability Condition: **Table 49 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 50 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vindiff_WCK	151101	Table 319

Overview: The purpose of this test is to verify that the peak voltage of the high pulse of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the Write Clock signal under test.

3 Find all valid positive pulses of the Write Clock in the entire waveform.
A valid positive pulse on the Write Clock starts at the valid rising edge of the Write Clock and ends at the following valid falling edge of the Write Clock.

4 Zoom into the first pulse and measure the max. Peak Voltage (Vmax). Consider Vmax as the value of Vindiff_WCK/2HighPulse.

5 Continue the previous step with the rest of the positive pulses found in the specified waveform.

6 Determine the worst result from the set of Vindiff_WCK/2HighPulse values that are measured.

Expected/ Observable Results: The measured value of Vindiff_WCK/2HighPulse for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Vindiff_WCK/2LowPulse

Availability Condition: **Table 51 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 52 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vindiff_WCK	151102	Table 319

Overview: The purpose of this test is to verify that the peak voltage of the low pulse of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the Write Clock signal under test.

3 Find all valid negative pulses of the Write Clock in the entire waveform.
A valid negative pulse on the Write Clock starts at the valid falling edge of the Write Clock and ends at the following valid rising edge of the Write Clock.

4 Zoom into the first pulse and measure the min. Peak Voltage (Vmin). Consider Vmin as the value of Vindiff_WCK/2LowPulse.

5 Continue the previous step with the rest of the negative pulses found in the specified waveform.

6 Determine the worst result from the set of Vindiff_WCK/2LowPulse values that are measured.

Expected/ Observable Results: The measured value of Vindiff_WCK/2LowPulse for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Input slew rate for differential WCK signals are measured as shown in Figure 33.

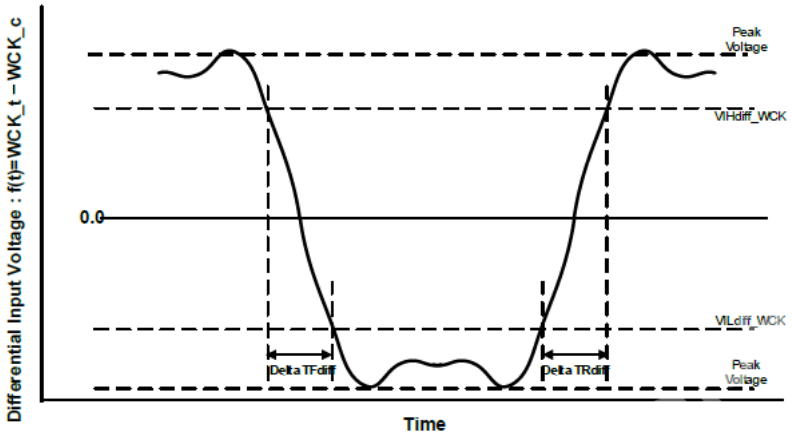

Figure 33 Differential input slew rate definition for differential write clock signal

VIHdiff_WCK

Availability Condition: **Table 53 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 54 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
VIHdiff_WCK	151106	Table 322

Overview: The purpose of this test is to verify that the high level differential input voltage value of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the Write Clock signal under test.

3 Find all valid Write Clock positive pulse in the triggered waveform.
A valid Write Clock positive pulse starts at the 0V crossing at valid Write Clock rising edge and ends at the 0V crossing at the following valid Clock falling edge.

4 Zoom into the first pulse and measure the top voltage V_{TOP}. Here, V_{TOP} is the voltage value on the rising edge after which the signal loses the monotonicity of the slope.
Consider the value of V_{TOP} as VIHdiff_WCK.

5 Continue the previous step for all positive pulses found in the specified waveform.

6 Determine the worst result from the set of VIHdiff_WCK values that are measured.

Expected/ Observable Results: The worst measured VIHdiff_WCK for the test signal shall be within the conformance limits as per the JESD209-5 specification.

VILdiff_WCK

Availability Condition: **Table 55 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 56 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
VILdiff_WCK	151107	Table 322

Overview: The purpose of this test is to verify the low level differential input voltage value of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the Write Clock signal under test.

3 Find all valid Write Clock negative pulse in the triggered waveform.
A valid Write Clock negative pulse starts at the 0V crossing at valid Write Clock falling edge and ends at the 0V crossing at the following valid Write Clock rising edge.

4 Zoom into the first pulse and measure the base voltage V_{BASE}. Here, V_{BASE} is the voltage value on the falling edge after which the signal loses the monotonicity of the slope.
Consider the value of V_{BASE} as VILdiff_WCK.

5 Continue the previous step for all negative pulses found in the specified waveform.

6 Determine the worst result from the set of VILdiff_WCK values that are measured.

Expected/ Observable Results: The worst measured VILdiff_WCK for the test signal shall be within the conformance limits as per the JESD209-5 specification.

SRIdiffR_WCK

Availability Condition: **Table 57 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 58 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRIdiffR_WCK	151108	Table 323

Overview: The purpose of this test is to verify that the differential input slew rate for rising edge of the Write Clock signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the Write Clock signal under test.

3 Find all the valid Write Clock rising edges in the entire waveform.

A valid Write Clock rising edge starts at VILdiff_WCK crossing and ends at the following VIHdiff_WCK crossing.

4 For all the valid Write Clock rising edges, measure the transition time, DeltaTRdiff. DeltaTRdiff is the time starting at VILdiff_WCK crossing and ending at the following VIHdiff_WCK crossing.

5 Calculate SRIdiffR_WCK using the equation:

$$SRIdiffR\_WCK = [VIHdiff\_WCK - VILdiff\_WCK] / DeltaTRdiff$$

6 Determine the worst result from the set of SRIdiffR_WCK measured.

Expected/ Observable Results: The measured value of SRIdiffR_WCK for the Write Clock signal shall be within the conformance limits as per the JESD209-5 specification.

SRIdiffF_WCK

Availability Condition: **Table 59 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 60 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRIdiffF_WCK	151109	Table 323

Overview: The purpose of this test is to verify that the differential input slew rate for falling edge of the Write Clock signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the Write Clock signal under test.

3 Find all the valid Write Clock falling edges in the entire waveform.

A valid Write Clock falling edge starts at VIHdiff_WCK crossing and ends at the following VILdiff_WCK crossing.

4 For all the valid Write Clock falling edges, measure the transition time, DeltaTFdiff. DeltaTFdiff is the time starting at VIHdiff_WCK crossing and ending at the following VILdiff_WCK crossing.

5 Calculate SRIdiffF_WCK using the equation:

$$SRIdiffF\_WCK = [VILdiff\_WCK - VIHdiff\_WCK] / DeltaTFdiff$$

6 Determine the worst result from the set of SRIdiffF_WCK measured.

Expected/ Observable Results: The measured value of SRIdiffF_WCK for the Write Clock signal shall be within the conformance limits as per the JESD209-5 specification.

Input slew rate for differential WCK signals are measured as shown in Figure 33.

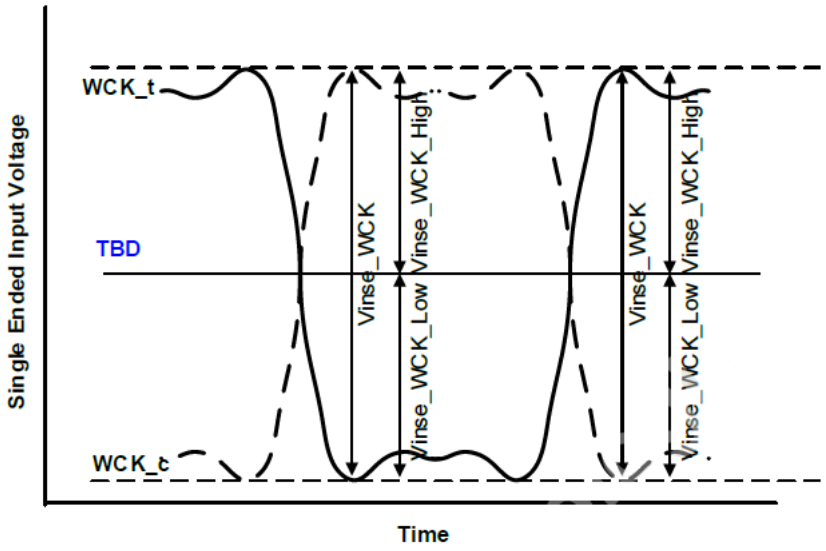

Figure 34 Differential input slew rate definition for differential write clock signal

Vinse_WCK (Positive Pulse)

Availability Condition: **Table 61 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 62 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK	151110	Table 320

Overview: The purpose of this test is to verify the peak voltage of high pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the Write Clock signal under test.

3 Find all valid positive pulses of the Write Clock in the entire waveform.
A valid positive pulse on the Write Clock starts at the valid rising edge of the Write Clock and ends at the following valid falling edge of the Write Clock.

4 Zoom into the first pulse and measure V_{MAX}.

5 Calculate the value of Vinse_WCK (Positive Pulse) using the equation:

$$\text{Vinse\_WCK (Positive Pulse)} = V_{MAX} - V_{REF}$$

NOTE For this test, the Test App considers Vref to be ($V_{REFdiff\_WCK}$), which in turn, is typically set to 0V.

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_WCK (Positive Pulse) measured.

Expected/ Observable Results: The measured value of Vinse_WCK (Positive Pulse) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_WCK (Negative Pulse)

Availability Condition: **Table 63 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 64 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK	151111	Table 320

Test Overview: The purpose of this test is to verify the peak voltage of low pulse.

Test Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the Write Clock signal under test.

3 Find all valid negative pulses of the Write Clock in the entire waveform.
A valid negative pulse on the Write Clock starts at the valid falling edge of the Write Clock and ends at the following valid rising edge of the Write Clock.

4 Zoom into the first pulse and measure V_{MIN}.

5 Calculate the value of Vinse_WCK (Negative Pulse) using the equation:

$$\text{Vinse\_WCK (Negative Pulse)} = V_{REF} - V_{MIN}$$

NOTE For this test, the Test App considers Vref to be ($V_{REFdiff\_CK}$), which in turn, is typically set to 0V.

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_WCK (Negative Pulse) measured.

Expected/ Observable Results: The measured value of Vinse_WCK (Negative Pulse) for the test signal shall be within the conformance limits as per the JEDEC specification.

Output slew rate for differential signals are measured as shown in Figure 35.

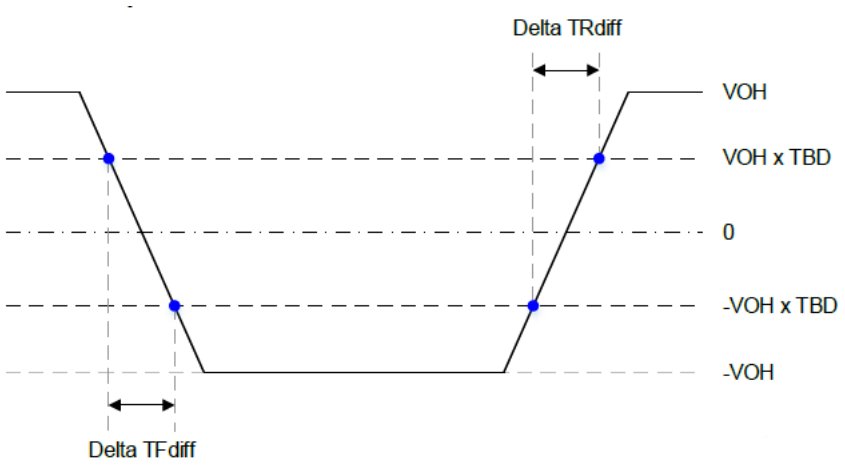

Figure 35 Differential output slew rate definition for WCK signal

Clock (SE Mode) Tests

The minimum single-ended CK input voltage is measured as shown in Figure 36.

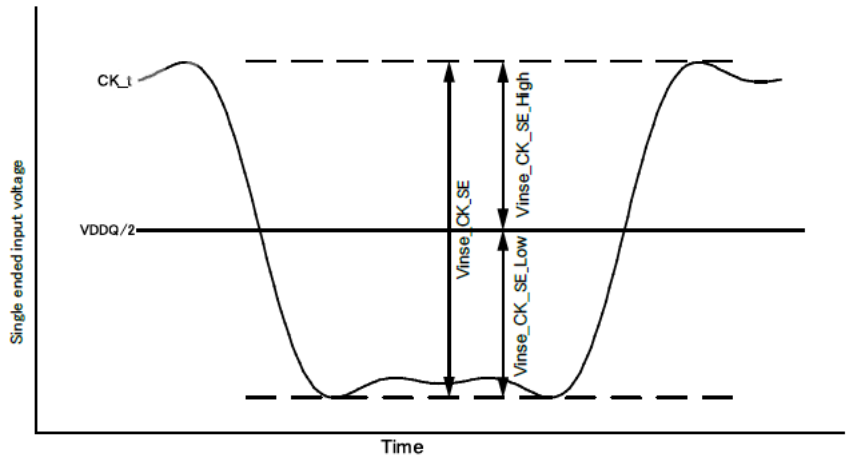

Figure 36 Single-ended mode CK input Voltage definition

Vinse_CK_SE

Availability Condition: **Table 65 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	Yes	Yes	CK_t

Test ID & References: **Table 66 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_SE	251000	Table 328

Overview: The purpose of this test is to verify that the peak-to-peak voltage on the test signal centered on VDDQ/2 is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid positive and negative pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge, whereas a valid negative pulse on the Clock starts at the valid falling edge and ends at the following valid rising edge.

4 Measure the max. Peak Voltage (Vmax) of the first positive pulse and the Min. Peak Voltage (Vmin) of the first negative pulse.

5 Calculate the difference of the two measurements and denote the result as Vinse_CK_SE#1.

$$Vinse\_CK\_SE\#1 = Vmax - Vmin$$

6 Then, measure Vmin of first negative pulse and Vmax of the second positive pulse.

7 Calculate the difference of the two measurements and denote the result as Vinse_CK_SE#2.

8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.

9 Determine the worst result from the set of Vinse_CK_SE values measured.

Expected/ Observable Results: The measured value of Vinse_CK_SE for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Vinse_CK_SE_High

Availability Condition: **Table 67 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	Yes	Yes	CK_t

Test ID & References: **Table 68 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_SE_High	251012	Table 328

Test Overview: The purpose of this test is to verify the peak voltage of high pulse.

Test Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid positive pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge.

4 Zoom into the first pulse and measure V_{MAX}.

5 Calculate the value of Vinse_CK_SE_High using the equation:

$$Vinse\_CK\_SE\_High = V_{MAX} - V_{REF}$$

NOTE For this test, the Test App considers Vref to be (V_{DDQ}/2).

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK_SE_High measured.

Expected/ Observable Results: The measured value of Vinse_CK_SE_High for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_CK_SE_Low

Availability Condition: **Table 69 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	Yes	Yes	CK_t

Test ID & References: **Table 70 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_Low	251014	Table 328

Overview: The purpose of this test is to verify the peak voltage of low pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the clock signal under test.

3 Find all valid negative pulses of the Clock in the entire waveform.
A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.

4 Zoom into the first pulse and measure V_{MIN}.

5 Calculate the value of Vinse_CK_SE_Low using the equation:

$$Vinse\_CK\_SE\_Low = V_{REF} - V_{MIN}$$

NOTE For this test, the Test App considers Vref to be (V_{DDQ}/2).

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK_SE_Low measured.

Expected/ Observable Results: The measured value of Vinse_CK_SE_Low for the test signal shall be within the conformance limits as per the JEDEC specification.

The single-ended clock input slew rate can be measured as shown in Figure 37.

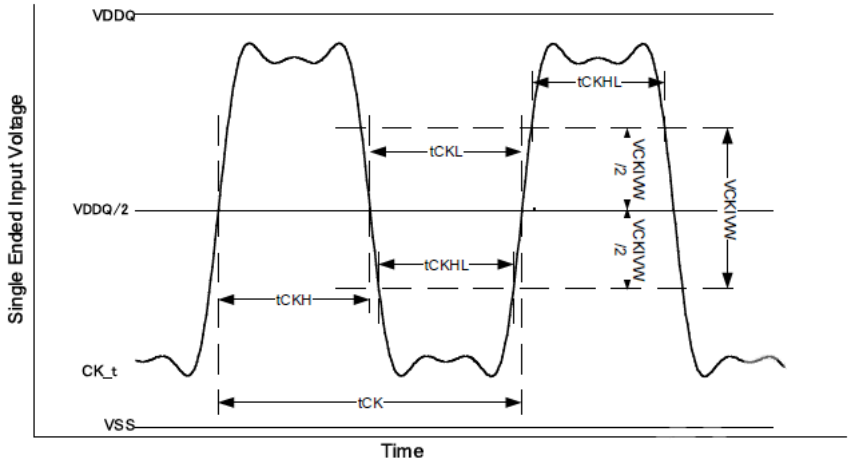

Figure 37 Single-ended mode CK pulse definitions

SRIseR_CKSE

Availability Condition: **Table 71 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	Yes	Yes	CK(Diff)

Test ID & References: **Table 72 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRICKSE	251008	Table 328

Overview: The purpose of this test is to verify that the single-ended input slew rate for rising edge of the Clock signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the Clock (CK) signal under test.

3 Find all the valid CK rising edges in the entire waveform. A valid Clock rising edge starts at VIL_CK crossing and ends at the following VIH_CK crossing.

4 For all the valid CK rising edges, measure the transition time, DeltaTRdiff.

DeltaTRdiff is the time starting at VIL_CK crossing and ending at the following VIH_CK crossing.

5 Calculate SRIseR_CKSE using the equation:

$$SRIseR\_CKSE = [VIH\_CK - VIL\_CK] / DeltaTRdiff$$

where, $VIH\_CK = ([VDDQ/2] + [VCKIVW/2])$

$$VIL\_CK = ([VDDQ/2] - [VCKIVW/2])$$

6 Determine the worst result from the set of SRIseR_CKSE measured.

Expected/ Observable Results: The measured value of SRIseR_CKSE for the Clock signal shall be within the conformance limits as per the JESD209-5 specification.

SRIseF_CKSE

Availability Condition: **Table 73 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	Yes	Yes	CK(Diff)

Test ID & References: **Table 74 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRICKSE	251009	Table 328

Overview: The purpose of this test is to verify that the single-ended input slew rate for falling edge of the Clock signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the Clock (CK) signal under test.

3 Find all the valid CK falling edges in the entire waveform. A valid Clock falling edge starts at VIH_CK crossing and ends at the following VIL_CK crossing.

4 For all the valid CK falling edges, measure the transition time, DeltaTFdiff.

DeltaTFdiff is the time starting at VIH_CK crossing and ending at the following VIL_CK crossing.

5 Calculate SRIseF_CKSE using the equation:

$$SRIseF\_CKSE = [VIL\_CK - VIH\_CK] / DeltaTFdiff$$

where, $VIH\_CK = ([VDDQ/2] + [VCKIVW/2])$

$$VIL\_CK = ([VDDQ/2] - [VCKIVW/2])$$

6 Determine the worst result from the set of SRIseF_CKSE measured.

Expected/ Observable Results: The measured value of SRIseF_CKSE for the Clock signal shall be within the conformance limits as per the JESD209-5 specification.

Write Clock (SE Mode) Tests

The minimum single-ended WCK input voltage is measured as shown in Figure 36.

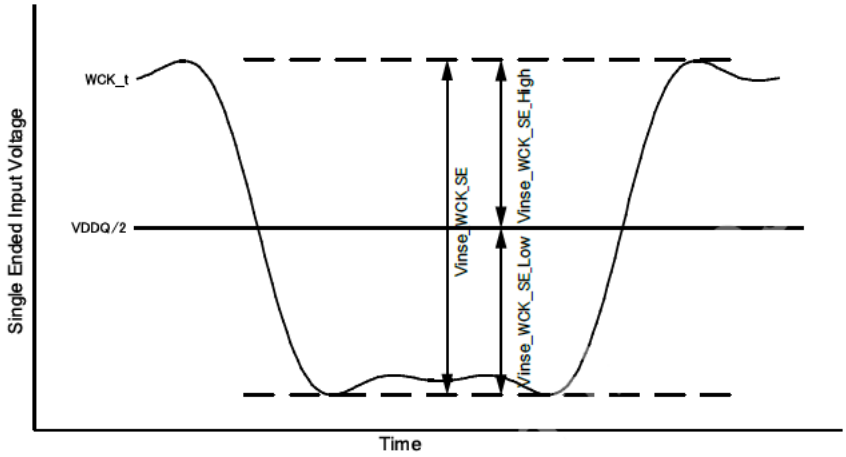

Figure 38 Single-ended mode WCK input Voltage definition

Vinse_WCK_SE

Availability Condition: **Table 75 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 76 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK_SE	251100	Table 327

Overview: The purpose of this test is to verify that the peak-to-peak voltage on the test signal centered on VDDQ/2 is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the write clock signal under test.

3 Find all valid positive and negative pulses of the Write Clock in the entire waveform.
A valid positive pulse on the Write Clock starts at the valid rising edge and ends at the following valid falling edge, whereas a valid negative pulse on the Write Clock starts at the valid falling edge and ends at the following valid rising edge.

4 Measure the max. Peak Voltage (Vmax) of the first positive pulse and the Min. Peak Voltage (Vmin) of the first negative pulse.

5 Calculate the difference of the two measurements and denote the result as Vinse_WCK_SE#1.

$$Vinse\_WCK\_SE\#1 = Vmax - Vmin$$

6 Then, measure Vmin of first negative pulse and Vmax of the second positive pulse.
7 Calculate the difference of the two measurements and denote the result as Vinse_WCK_SE#2.
8 Continue steps 4 to 7 for measurements on the remaining pulse that was obtained.
9 Determine the worst result from the set of Vinse_WCK_SE values measured.

Expected/ Observable Results: The measured value of Vinse_WCK_SE for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Vinse_WCK_SE_High

Availability Condition: **Table 77 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 78 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK_SE_High	251112	Table 327

Overview: The purpose of this test is to verify that the peak voltage of the high pulse of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the write clock signal under test.

3 Find all valid positive pulses of the Write Clock in the entire waveform.
A valid positive pulse on the Write Clock starts at the valid rising edge and ends at the following valid falling edge.

4 Zoom into the first pulse and measure V_{MAX}.

5 Calculate the value of Vinse_WCK_SE_High using the equation:

$$Vinse\_WCK\_SE\_High = V_{MAX} - V_{REF}$$

NOTE For this test, the Test App considers Vref to be ($V_{refDQ}/2$).

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_WCK_SE_High measured.

Expected/ Observable Results: The measured value of Vinse_WCK_SE_High for the test signal shall be within the conformance limits as per the JESD209-5 specification.

Vinse_WCK_SE_Low

Availability Condition: **Table 79 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 80 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK_SE_Low	251114	Table 327

Overview: The purpose of this test is to verify that the peak voltage of the low pulse of the test signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the write clock signal under test.

3 Find all valid negative pulses of the Write Clock in the entire waveform.
A valid negative pulse on the Write Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Write Clock.

4 Zoom into the first pulse and measure V_{MIN}.

5 Calculate the value of Vinse_WCK_SE_Low using the equation:

$$Vinse\_WCK\_SE\_Low = V_{REF} - V_{MIN}$$

NOTE For this test, the Test App considers Vref to be (V_{refDQ}/2).

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_WCK_SE_Low measured.

Expected/ Observable Results: The measured value of Vinse_WCK_SE_Low for the test signal shall be within the conformance limits as per the JESD209-5 specification.

The single-ended write clock input slew rate can be measured as shown in Figure 39.

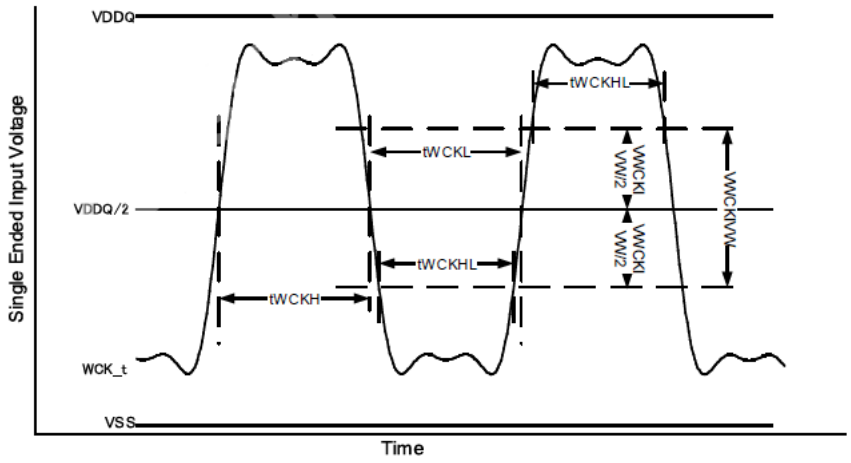

Figure 39 Single-ended mode WCK pulse definitions

SRIseR_WCKSE

Availability Condition: **Table 81 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 82 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRIWCKSE	251108	Table 327

Overview: The purpose of this test is to verify that the single-ended input slew rate for rising edge of the Write Clock signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the Write Clock (WCK) signal under test.

3 Find all the valid WCK rising edges in the entire waveform. A valid Write Clock rising edge starts at VIL_WCK crossing and ends at the following VIH_WCK crossing.

4 For all the valid WCK rising edges, measure the transition time, DeltaTRdiff.

DeltaTRdiff is the time starting at VIL_WCK crossing and ending at the following VIH_WCK crossing.

5 Calculate SRIseR_WCKSE using the equation:

$$SRIseR\_WCKSE = [VIH\_WCK - VIL\_WCK] / DeltaTRdiff$$

where, $VIH\_WCK = ([VDDQ/2] + [VWCKIVW/2])$

$$VIL\_WCK = ([VDDQ/2] - [VWCKIVW/2])$$

6 Determine the worst result from the set of SRIseR_WCKSE measured.

Expected/ Observable Results: The measured value of SRIseR_WCKSE for the Write Clock signal shall be within the conformance limits as per the JESD209-5 specification.

SRIseF_WCKSE

Availability Condition: **Table 83 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 84 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRIWCKSE	251109	Table 327

Overview: The purpose of this test is to verify that the single-ended input slew rate for falling edge of the Write Clock signal is compliant to the JESD209-5 specification.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the Write Clock (WCK) signal under test.

3 Find all the valid WCK falling edges in the entire waveform. A valid Write Clock falling edge starts at VIH_WCK crossing and ends at the following VIL_WCK crossing.

4 For all the valid WCK falling edges, measure the transition time, DeltaTFdiff.

DeltaTFdiff is the time starting at VIH_WCK crossing and ending at the following VIL_WCK crossing.

5 Calculate SRIseF_WCKSE using the equation:

$$SRIseF\_WCKSE = [VIL\_WCK - VIH\_WCK] / DeltaTFdiff$$

where, $VIH\_WCK = ([VDDQ/2] + [VWCKIVW/2])$

$$VIL\_WCK = ([VDDQ/2] - [VWCKIVW/2])$$

6 Determine the worst result from the set of SRIseF_WCKSE measured.

Expected/ Observable Results: The measured value of SRIseF_WCKSE for the Write Clock signal shall be within the conformance limits as per the JESD209-5 specification.

Clock (SE) CK_t (Clock Plus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.

NOTE V_{DD} is considered as V_{DD2H} for CA[6:0], CK_t, CK_c, CS and RSET_n signals; whereas, V_{DD} is considered as V_{DDQ} for DQ, DMI, RDQS_t, WCK_t and WCK_c. Also, Vss = 0V.

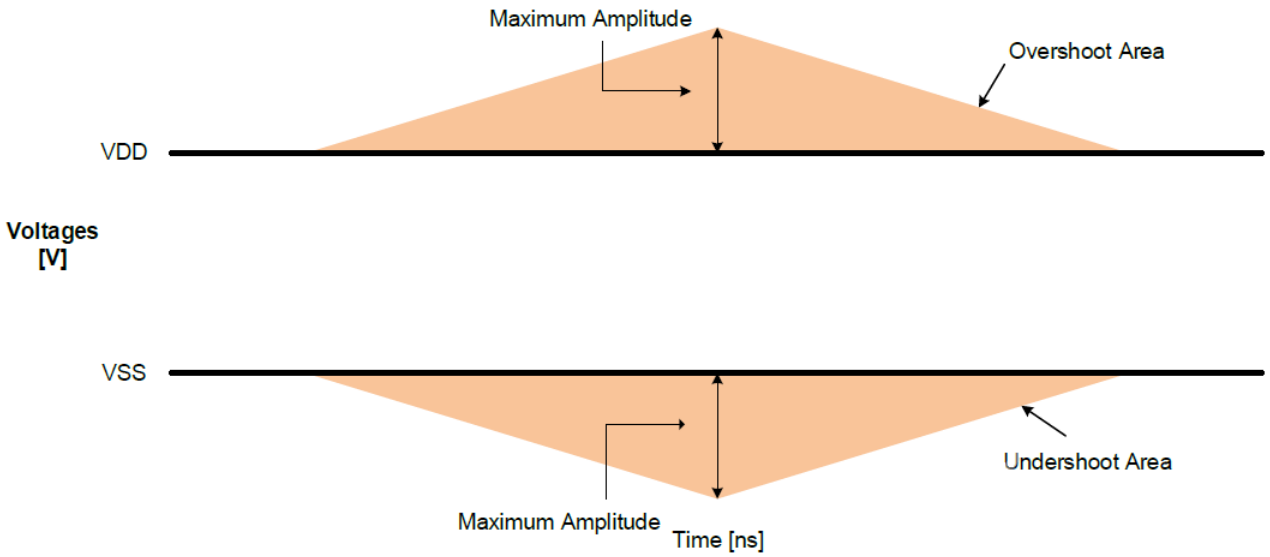

Figure 40 Overshoot and Undershoot definition for CK_t signal

Overshoot_Amplitude_CK_t

Availability Condition: **Table 85 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_t

Test ID & References: **Table 86 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152000	Table 311

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD2H}$$

b Evaluate Area_below_V_{DD2H} using the equation:

$$\text{Area\_below\_}V_{DD2H} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD2H}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

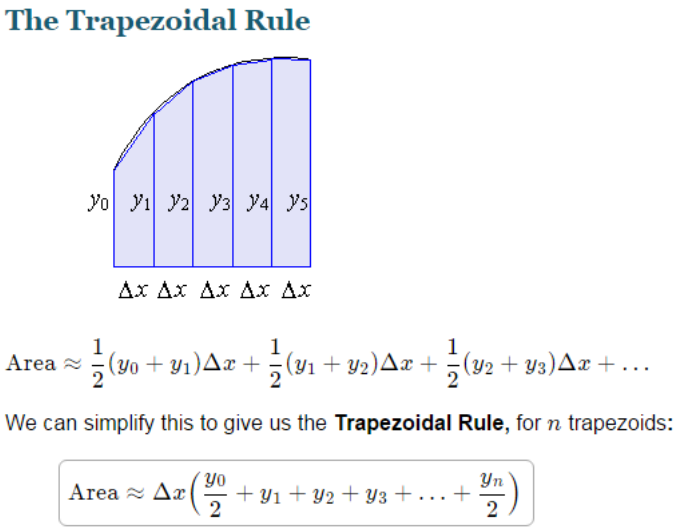

Figure 41 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD2H} using the equation:

$$\text{Area\_Above\_}V_{DD2H} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD2H}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD2H}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Amplitude_CK_t

Availability Condition: **Table 87 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_t

Test ID & References: **Table 88 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152001	Table 311

Test Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

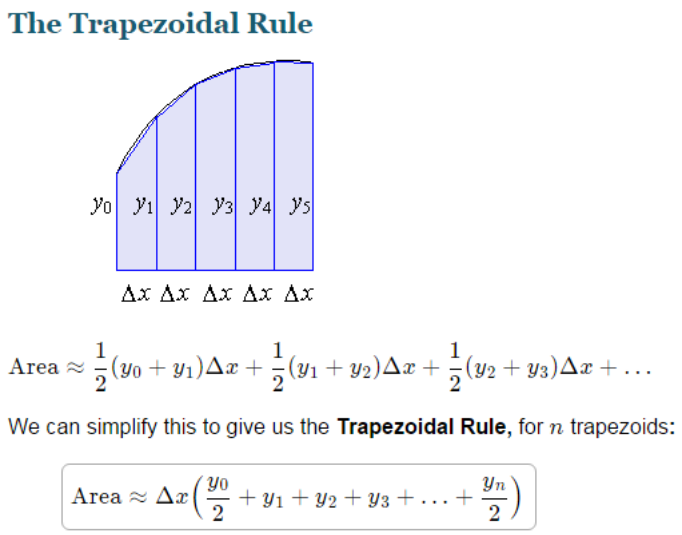

Figure 42 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Undershoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_CK_t

Availability Condition: **Table 89 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_t

Test ID & References: **Table 90 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152002	Table 311

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD2H}$$

b Evaluate Area_below_V_{DD2H} using the equation:

$$\text{Area\_below\_}V_{DD2H} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD2H}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

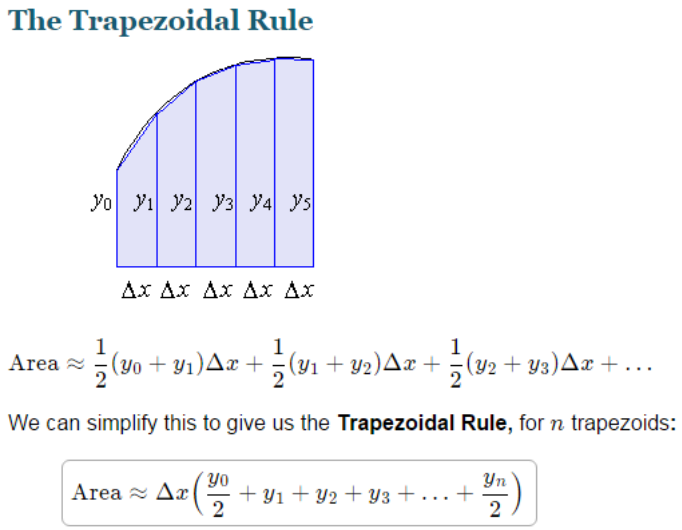

Figure 43 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_0V - Area_below_V_{DD2H}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD2H}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Area_CK_t

Availability Condition: **Table 91 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_t

Test ID & References: **Table 92 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum undershoot area above VSS	152003	Table 311

Test Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

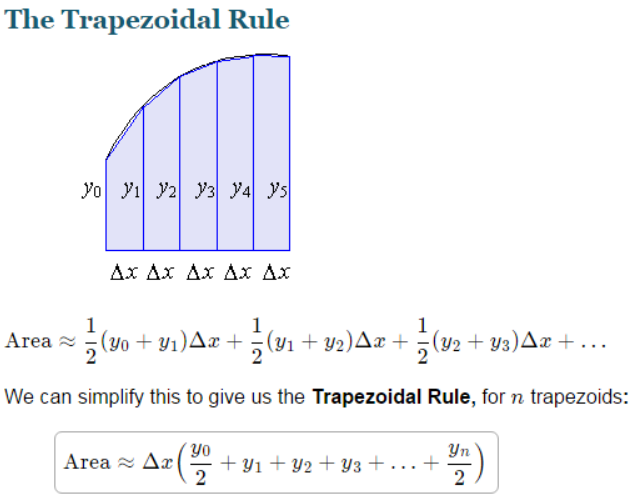

Figure 44 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
   - Undershoot Amplitude
   - Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

The minimum input single-ended voltage is measured as shown in Figure 45.

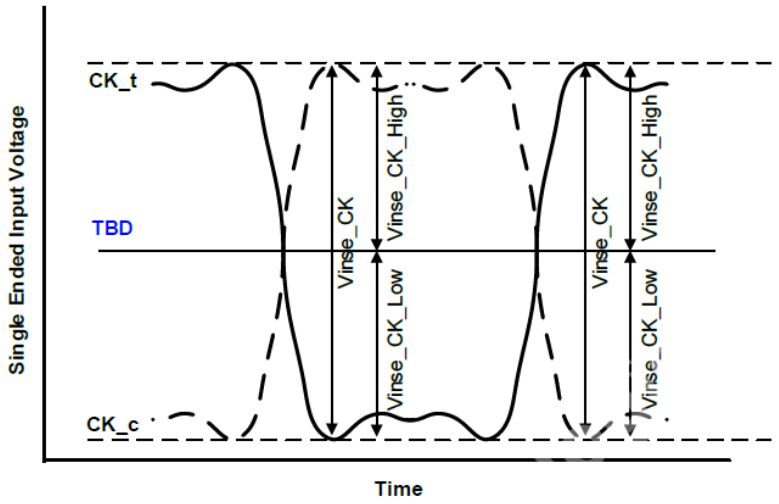

Figure 45 Clock Single-ended Input Voltage definition

Vinse_CK_High (CK_t)

Availability Condition: **Table 93 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_t

Test ID & References: **Table 94 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_High	151012	Table 314

Test Overview: The purpose of this test is to verify the peak voltage of high pulse.

Test Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid positive pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge.

4 Zoom into the first pulse and measure V_{MAX}.

5 Calculate the value of Vinse_CK_High (CK_t) using the equation:

$$Vinse\_CK\_High\ (CK\_t) = V_{MAX} - V_{REF}$$

NOTE For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK_High (CK_t) measured.

Expected/ Observable Results: The measured value of Vinse_CK_High (CK_t) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_CK_Low (CK_t)

Availability Condition: **Table 95 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_t

Test ID & References: **Table 96 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_Low	151014	Table 314

Overview: The purpose of this test is to verify the peak voltage of low pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the clock signal under test.

3 Find all valid negative pulses of the Clock in the entire waveform.
A valid negative pulse on the Clock starts at the valid falling edge and ends at the following valid rising edge of the Clock.

4 Zoom into the first pulse and measure V_{MIN}.

5 Calculate the value of Vinse_CK_Low (CK_t) using the equation:

$$\text{Vinse\_CK\_Low (CK\_t)} = V_{REF} - V_{MIN}$$

NOTE For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK_Low (CK_t) measured.

Expected/ Observable Results: The measured value of Vinse_CK_Low (CK_t) for the test signal shall be within the conformance limits as per the JEDEC specification.

Clock (SE) CK_c (Clock Minus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 46.

NOTE V_{DD} is considered as V_{DD2H} for CA[6:0], CK_t, CK_c, CS and RSET_n signals; whereas, V_{DD} is considered as V_{DDQ} for DQ, DMI, RDQS_t, WCK_t and WCK_c. Also, Vss = 0V.

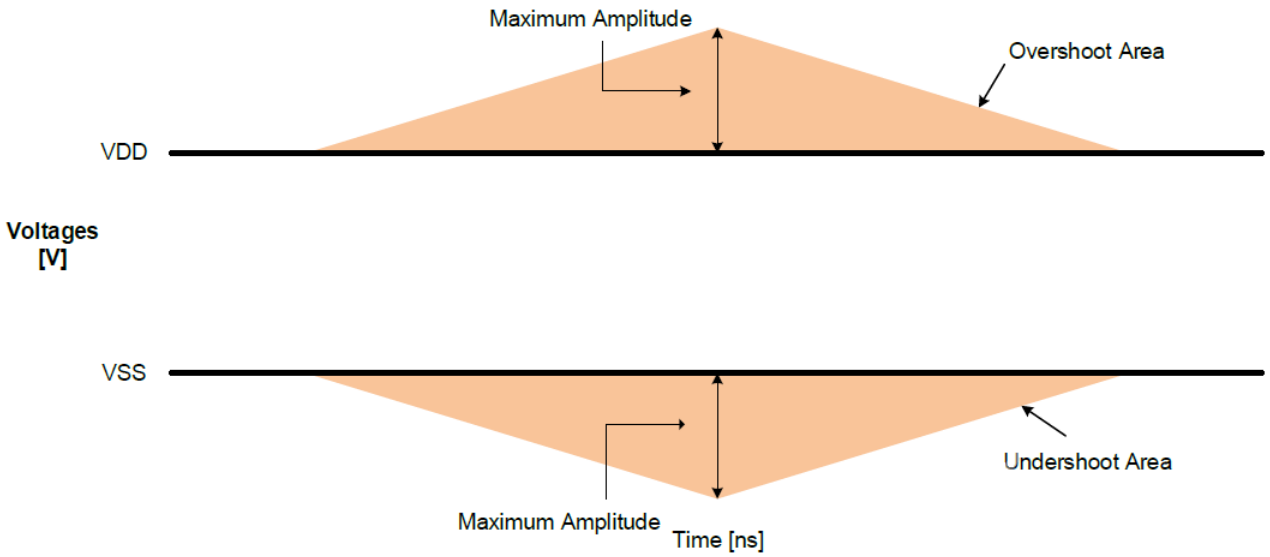

Figure 46 Overshoot and Undershoot definition for CK_c signal

Overshoot_Amplitude_CK_c

Availability Condition: **Table 97 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_c

Test ID & References: **Table 98 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152004	Table 311

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD2H}$$

b Evaluate Area_below_V_{DD2H} using the equation:

$$\text{Area\_below\_}V_{DD2H} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD2H}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

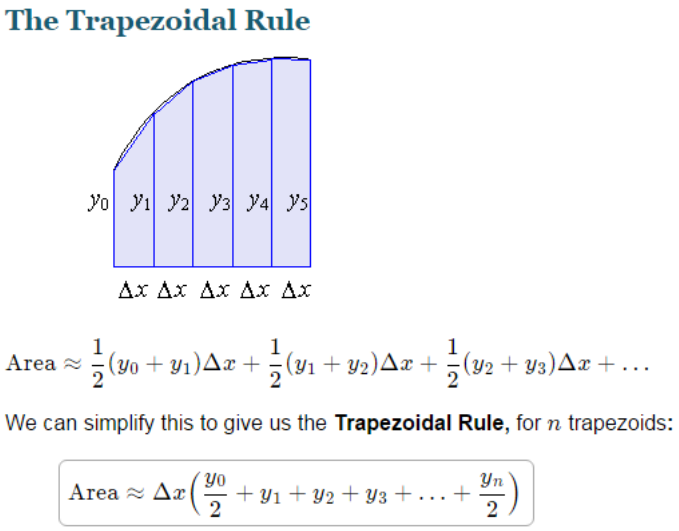

Figure 47 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD2H} using the equation:

$$\text{Area\_Above\_}V_{DD2H} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD2H}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD2H}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Amplitude_CK_c

Availability Condition: **Table 99 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_c

Test ID & References: **Table 100 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152005	Table 311

Test Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

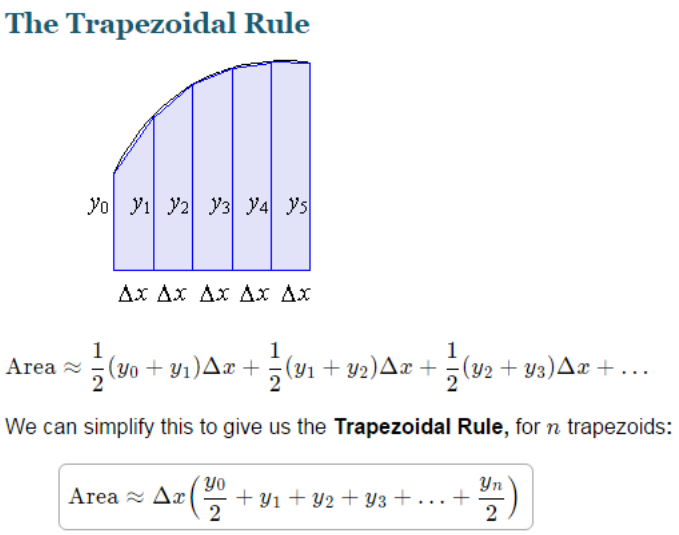

Figure 48 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Undershoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_CK_c

Availability Condition: **Table 101 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_c

Test ID & References: **Table 102 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152006	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD2H} crossing and ends at the falling edge of V_{DD2H} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD2H}$$

b Evaluate Area_below_V_{DD2H} using the equation:

$$\text{Area\_below\_}V_{DD2H} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD2H}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

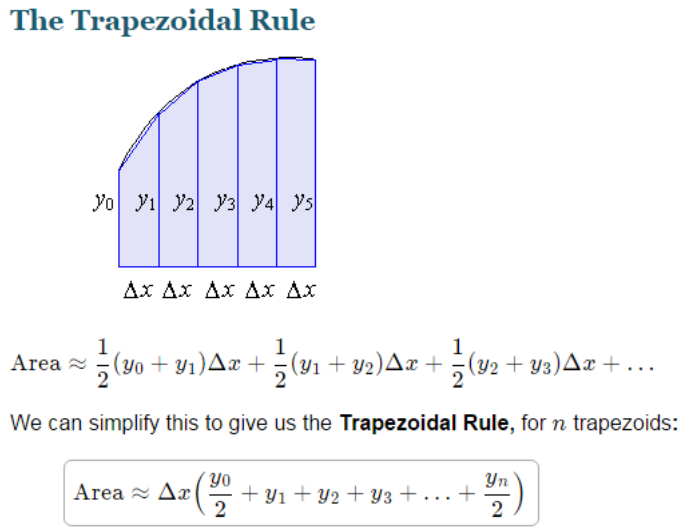

Figure 49 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD2H} using the equation:

Area_Above_V_{DD2H} = Total_Area_Above_0V - Area_below_V_{DD2H}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD2H}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Area_CK_c

Availability Condition: **Table 103 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_c

Test ID & References: **Table 104 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum undershoot area above VSS	152007	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

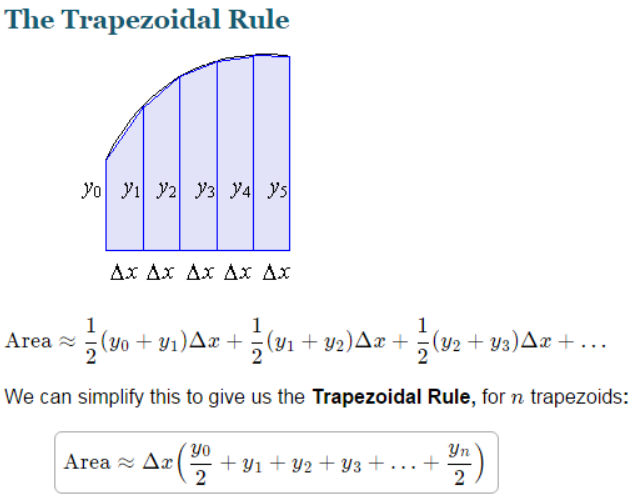

Figure 50 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
   - Undershoot Amplitude
   - Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

The minimum input single-ended voltage is measured as shown in Figure 31.

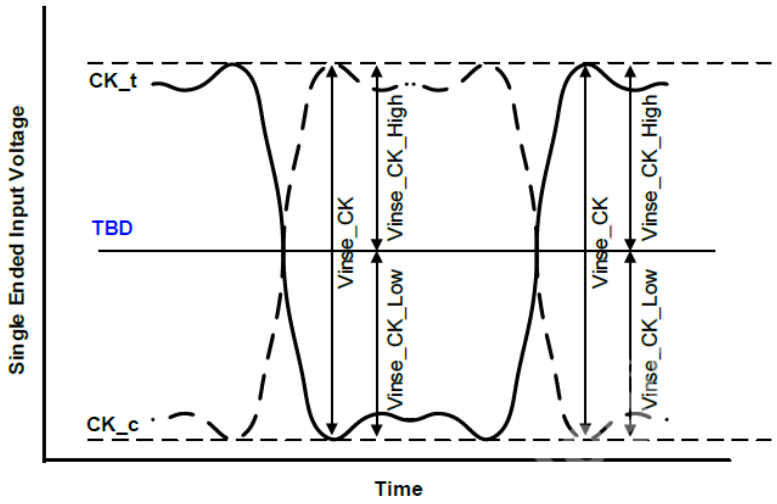

Figure 51 Clock Single-ended Input Voltage definition

Vinse_CK_High (CK_c)

Availability Condition: **Table 105 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_c

Test ID & References: **Table 106 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_High	151013	Table 314

Overview: The purpose of this test is to verify the peak voltage of high pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the clock signal under test.

3 Find all valid positive pulses of the Clock in the entire waveform.
A valid positive pulse on the Clock starts at the valid rising edge and ends at the following valid falling edge.

4 Zoom into the first pulse and measure V_{MAX}.

5 Calculate the value of Vinse_CK_High (CK_c) using the equation:

$$\text{Vinse\_CK\_High (CK\_c)} = V_{MAX} - V_{REF}$$

NOTE For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK_High (CK_c) measured.

Expected/ Observable Results: The measured value of Vinse_CK_High (CK_c) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_CK_Low (CK_c)

Availability Condition: **Table 107 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	No	CK_c

Test ID & References: **Table 108 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_CK_Low	151015	Table 314

Overview: The purpose of this test is to verify the peak voltage of low pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the clock signal under test.

3 Find all valid negative pulses of the Clock in the entire waveform.
A valid negative pulse on the Clock starts at the valid falling edge and ends at the following valid rising edge.

4 Zoom into the first pulse and measure V_{MIN}.

5 Calculate the value of Vinse_CK_Low (CK_c) using the equation:

$$\text{Vinse\_CK\_Low (CK\_c)} = V_{REF} - V_{MIN}$$

NOTE For this test, the Test App considers Vref to be VrefCA configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_CK_Low (CK_c) measured.

Expected/ Observable Results: The measured value of Vinse_CK_Low (CK_c) for the test signal shall be within the conformance limits as per the JEDEC specification.

Clock (SE) CK_t & CK_c (Clock Plus & Minus) tests

The cross-point voltage of the differential input signals (CK_t, CK_c) is measured as shown in Figure 52.

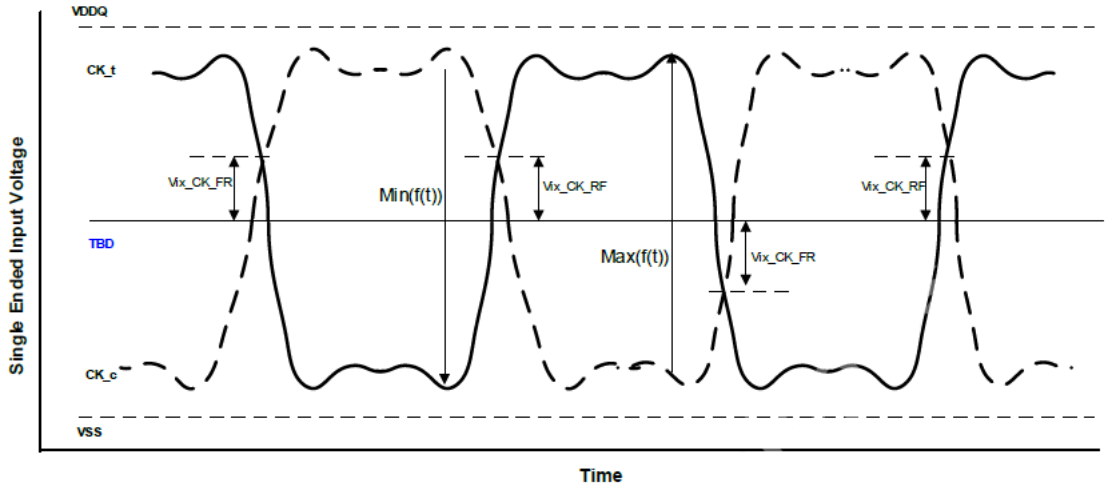

Figure 52 Differential Input Cross Point Voltage definition

Vix_CK_ratio

Availability Condition: **Table 109 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK_t, CK_c

Test ID & References: **Table 110 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vix_CK_ratio	151016	Table 318

Overview: The purpose of this test is to verify the ratio of the calculated crossing point voltage from the value of the measured crossing point voltage on the input differential pair test signals.

NOTE For Clock (CK) signal, the Test App considers Vref to be the VrefCA configuration value (set under Measurement Thresholds).

Procedure:

1 Sample/Acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
3 Find the Vmax and Vmin of the differential signal denoted as Max(f(t)) and Min(f(t)) respectively.

4 Find the time-stamp of all differential CK crossing that crosses 0V.

5 Use V_{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.

6 At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and V_{Ref}. The rising and falling crosspoint voltage differential is denoted as Vix_CK_RF and Vix_CK_FR respectively.

7 For each cross point voltage, calculate the final result using the equation (for Rising):

$$V_{IX}\_CK\_ratio = 100\% \times [Vix\_CK\_RF/Max(f(t))]$$

8 For each cross point voltage, calculate the final result using the equation (for Falling):

$$V_{IX}\_CK\_ratio = 100\% \times [Vix\_CK\_FR/Min(f(t))]$$

9 Determine the worst result from the set of V_{IX}_CK_ratio measured.

Expected/ Observable Results: The calculated value of the crossing point voltage ratio for the differential test signal pair shall be within the conformance limits as per the JEDEC specification in the References section.

Write Clock (SE) WCK_t (Write Clock Plus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 53.

NOTE VDD is considered as VDD2H for CA[6:0], CK_t, CK_c, CS and RSET_n signals; whereas, VDD is considered as VDDQ for DQ, DMI, RDQS_t, WCK_t and WCK_c. Also, Vss = 0V.

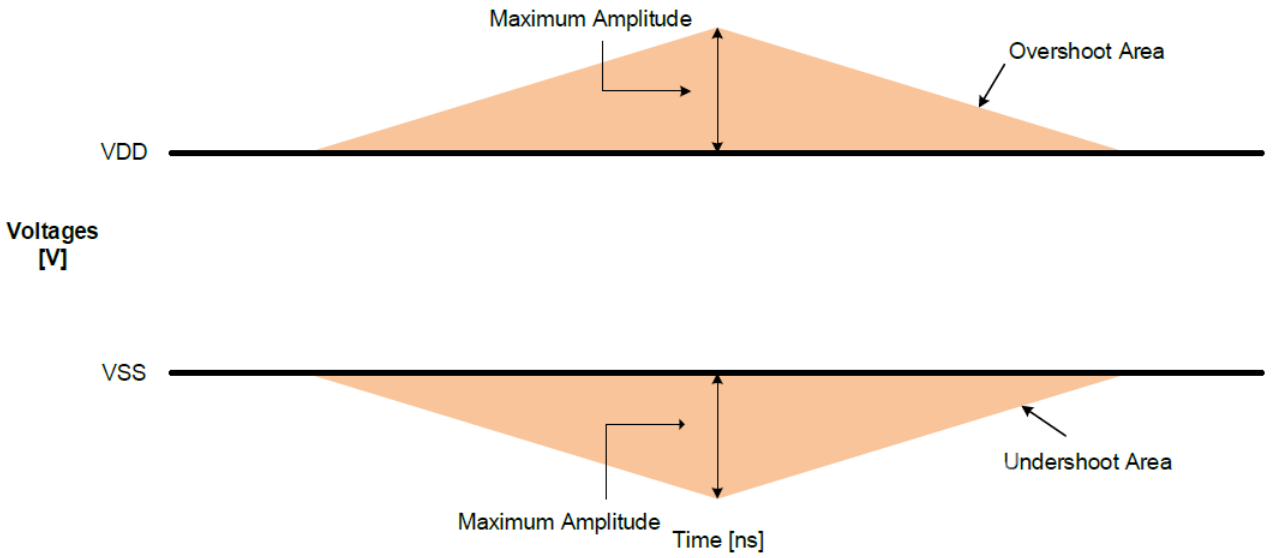

Figure 53 Overshoot and Undershoot definition for WCK_t signal

Overshoot_Amplitude_WCK_t

Availability Condition: **Table 111 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK_t

Test ID & References: **Table 112 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152100	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

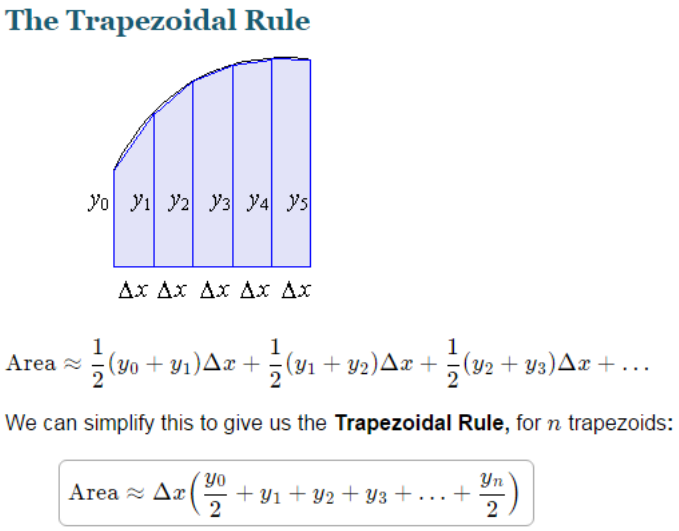

Figure 54 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Amplitude_WCK_t

Availability Condition: **Table 113 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK_t

Test ID & References: **Table 114 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152101	Table 311

Test Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

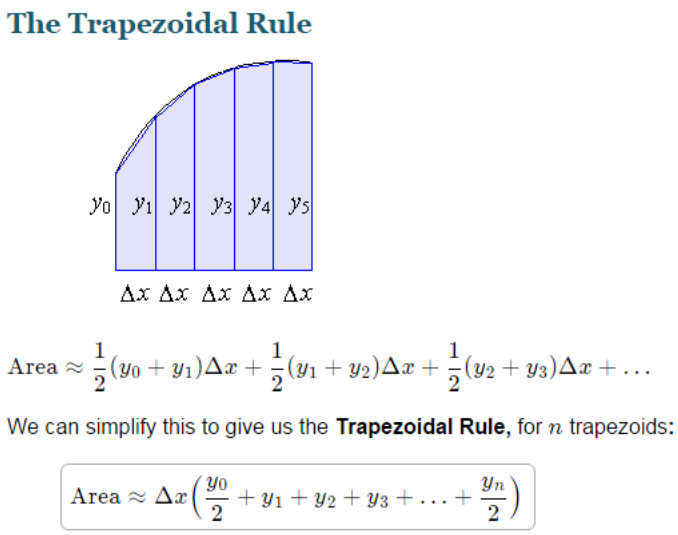

Figure 55 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Undershoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_WCK_t

Availability Condition: **Table 115 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK_t

Test ID & References: **Table 116 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152102	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

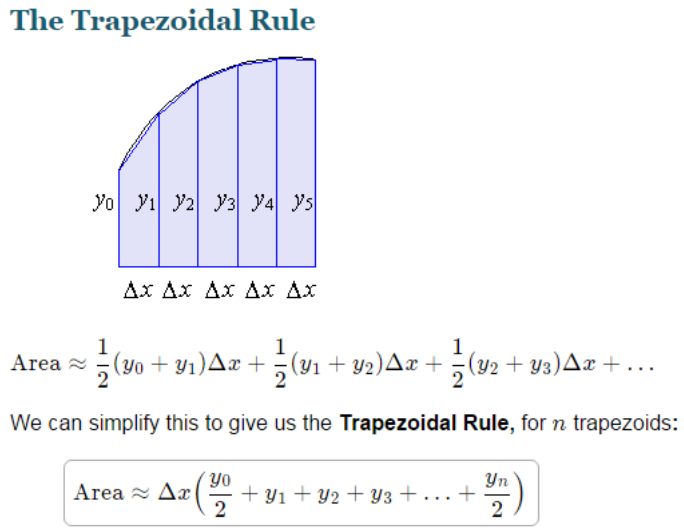

Figure 56 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

Area_Above_V_{DDQ} = Total_Area_Above_0V - Area_below_V_{DDQ}

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Area_WCK_t

Availability Condition: **Table 117 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK_t

Test ID & References: **Table 118 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum undershoot area above VSS	152103	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

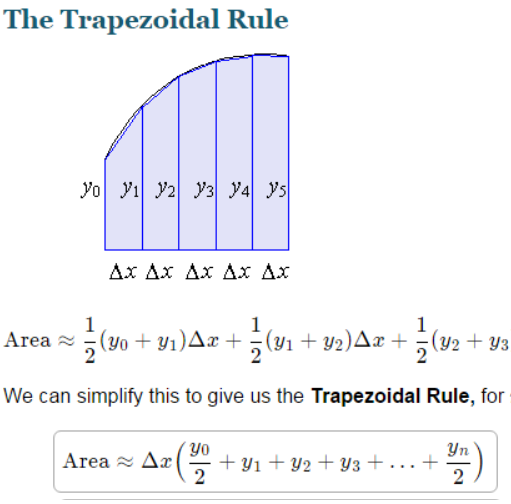

Figure 57 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
   - Undershoot Amplitude
   - Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Vinse_WCK_High (WCK_t)

Availability Condition: **Table 119 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	WCK_t

Test ID & References: **Table 120 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK_High	151112	Table 320

Overview: The purpose of this test is to verify the peak voltage of high pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the write clock signal under test.

3 Find all valid positive pulses of the Write Clock in the entire waveform.
A valid positive pulse on the Write Clock starts at the valid rising edge and ends at the following valid falling edge.

4 Zoom into the first pulse and measure V_{MAX}.

5 Calculate the value of Vinse_WCK_High (WCK_t) using the equation:

$$\text{Vinse\_WCK\_High (WCK\_t)} = V_{MAX} - V_{REF}$$

NOTE For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_WCK_High (WCK_t) measured.

Expected/ Observable Results: The measured value of Vinse_WCK_High (WCK_t) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_WCK_Low (WCK_t)

Availability Condition: **Table 121 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	WCK_t

Test ID & References: **Table 122 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK_Low	151114	Table 320

Overview: The purpose of this test is to verify the peak voltage of low pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the write clock signal under test.

3 Find all valid negative pulses of the Write Clock in the entire waveform.
A valid negative pulse on the Write Clock starts at the valid falling edge and ends at the following valid rising edge.

4 Zoom into the first pulse and measure V_{MIN}.

5 Calculate the value of Vinse_WCK_Low (WCK_t) using the equation:

$$Vinse\_WCK\_Low\ (WCK\_t) = V_{REF} - V_{MIN}$$

NOTE For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_WCK_Low (WCK_t) measured.

Expected/ Observable Results: The measured value of Vinse_WCK_Low (WCK_t) for the test signal shall be within the conformance limits as per the JEDEC specification.

Write Clock (SE) WCK_c (Write Clock Minus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.

NOTE VDD is considered as VDD2H for CA[6:0], CK_t, CK_c, CS and RSET_n signals; whereas, VDD is considered as VDDQ for DQ, DMI, RDQS_t, WCK_t and WCK_c. Also, Vss = 0V.

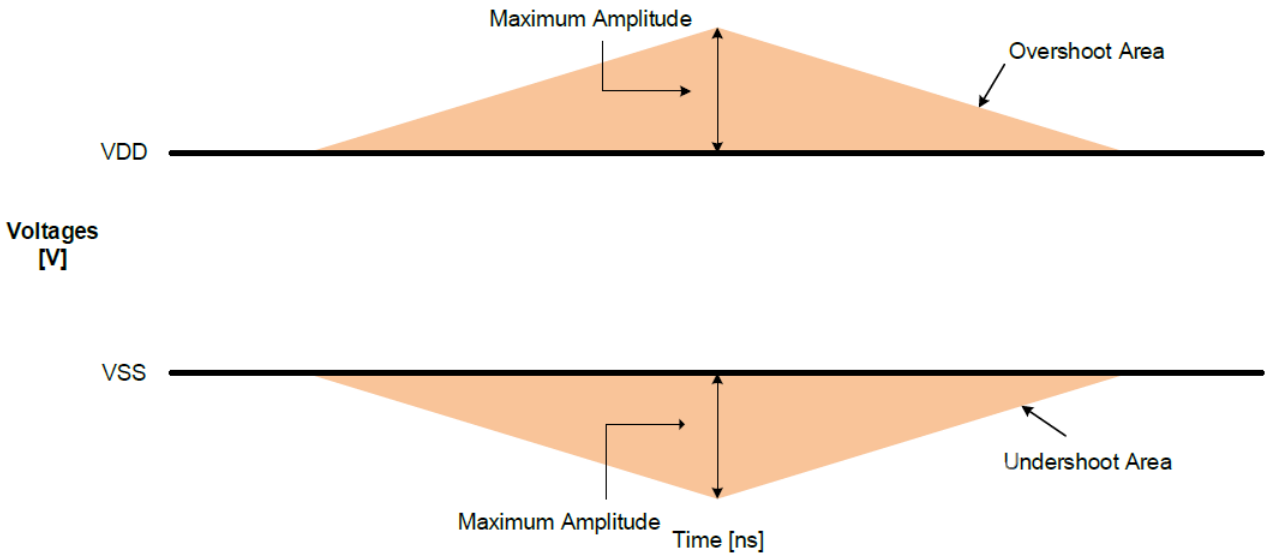

Figure 58 Overshoot and Undershoot definition for WCK_c signal

Overshoot_Amplitude_WCK_c

Availability Condition: **Table 123 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK_c

Test ID & References: **Table 124 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152104	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

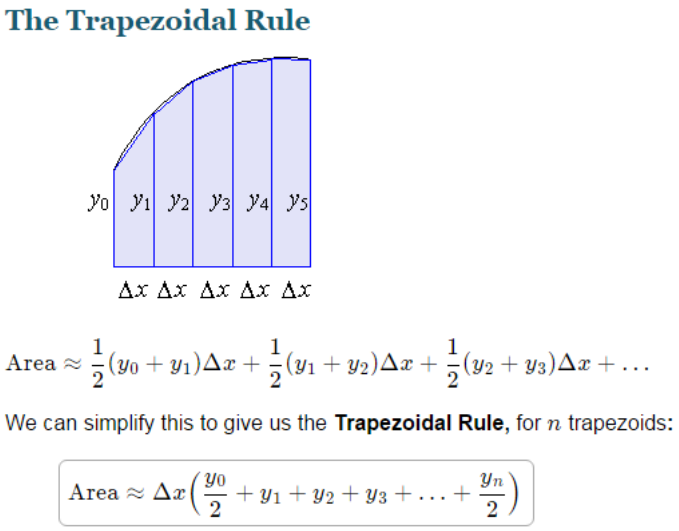

Figure 59 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Amplitude_WCK_c

Availability Condition: **Table 125 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK_c

Test ID & References: **Table 126 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152105	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

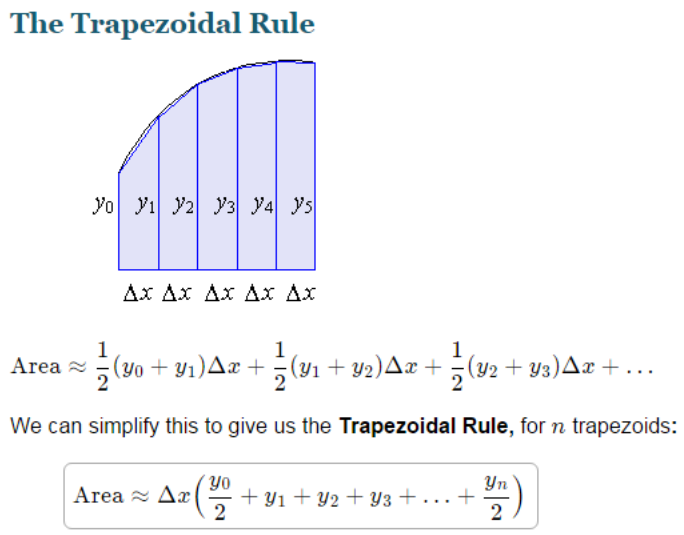

Figure 60 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Undershoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_WCK_c

Availability Condition: **Table 127 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK_c

Test ID & References: **Table 128 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152106	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

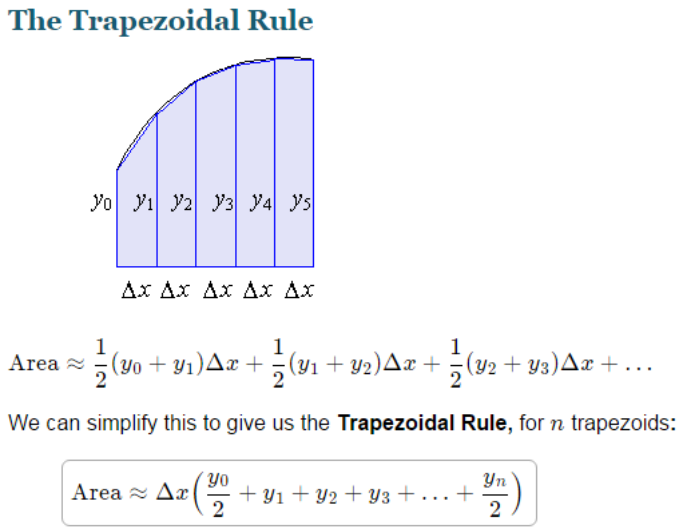

Figure 61 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Area_WCK_c

Availability Condition: **Table 129 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK_c

Test ID & References: **Table 130 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum undershoot area above VSS	152107	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

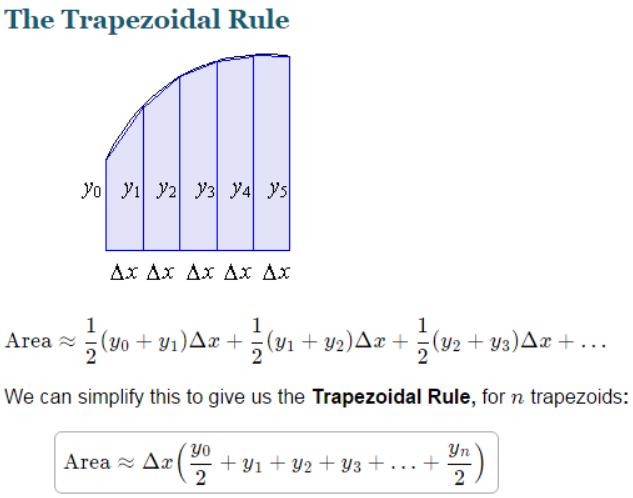

Figure 62 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
   - Undershoot Amplitude
   - Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

The minimum input single-ended voltage is measured as shown in Figure 63.

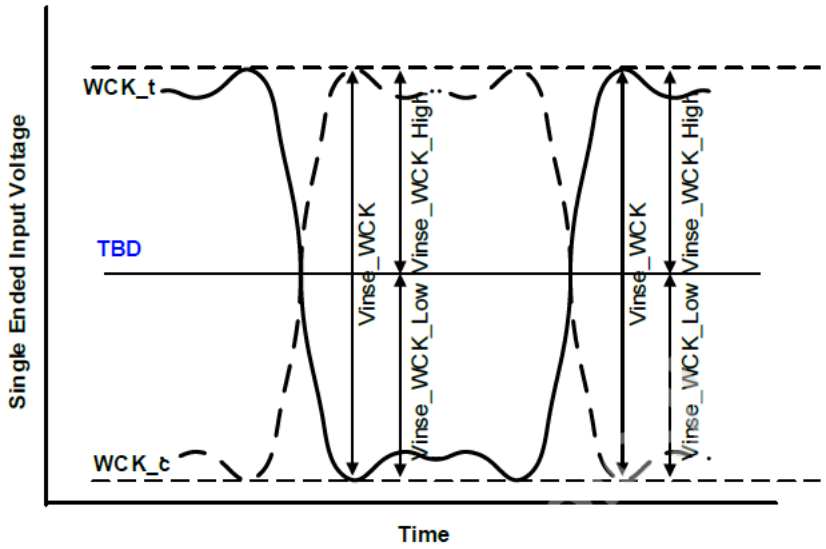

Figure 63 Write Clock Single-ended Input Voltage definition

Vinse_WCK_High (WCK_c)

Availability Condition: **Table 131 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	WCK_c

Test ID & References: **Table 132 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK_High	151113	Table 320

Overview: The purpose of this test is to verify the peak voltage of high pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the rising edge of the write clock signal under test.

3 Find all valid positive pulses of the write clock in the entire waveform.
A valid positive pulse on the Write Clock starts at the valid rising edge and ends at the following valid falling edge.

4 Zoom into the first pulse and measure V_{MAX}.

5 Calculate the value of Vinse_WCK_High (WCK_c) using the equation:

$$\text{Vinse\_WCK\_High (WCK\_c)} = V_{MAX} - V_{REF}$$

NOTE For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the positive pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_WCK_High (WCK_c) measured.

Expected/ Observable Results: The measured value of Vinse_WCK_High (WCK_c) for the test signal shall be within the conformance limits as per the JEDEC specification.

Vinse_WCK_Low (WCK_c)

Availability Condition: **Table 133 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	No	No	WCK_c

Test ID & References: **Table 134 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vinse_WCK_Low	151115	Table 320

Overview: The purpose of this test is to verify the peak voltage of low pulse.

Procedure:

1 Pre-condition the oscilloscope.

2 Trigger on the falling edge of the write clock signal under test.

3 Find all valid negative pulses of the Write Clock in the entire waveform.
A valid negative pulse on the Write Clock starts at the valid falling edge and ends at the following valid rising edge.

4 Zoom into the first pulse and measure V_{MIN}.

5 Calculate the value of Vinse_WCK_Low (WCK_c) using the equation:

$$Vinse\_WCK\_Low\ (WCK\_c) = V_{REF} - V_{MIN}$$

NOTE For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).

6 Continue the previous step with the rest of the negative pulses found in the specified waveform.

7 Determine the worst result from the set of Vinse_WCK_Low (WCK_c) measured.

Expected/ Observable Results: The measured value of Vinse_WCK_Low (WCK_c) for the test signal shall be within the conformance limits as per the JEDEC specification.

Write Clock (SE) WCK_t & WCK_c (Write Clock Plus & Minus) tests

The cross-point voltage of the differential input signals (WCK_t, WCK_c) is measured as shown in Figure 64.

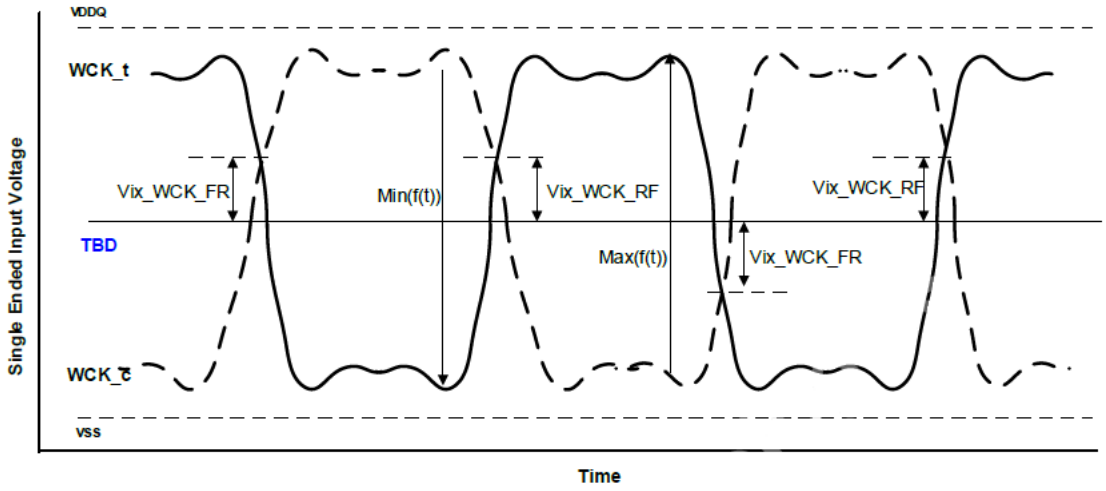

Figure 64 Differential Input Cross Point Voltage definition for WCK signal

Vix_WCK_ratio

Availability Condition: **Table 135 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst	Yes	Yes	No	WCK_t, WCK_c

Test ID & References: **Table 136 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Vix_WCK_ratio	151116	Table 324

Overview: The purpose of this test is to verify the ratio of the calculated crossing point voltage from the value of the measured crossing point voltage on the input differential pair test signals.

NOTE For Write Clock (WCK) signal, the Test App considers Vref to be the VrefDQ configuration value (set under Measurement Thresholds).

Procedure:

1 Sample/Acquire data waveforms.
2 Use Subtract FUNC to generate the differential waveform from the 2-source input.
3 Find the Vmax and VMin of the differential signal denoted as Max(f(t)) and Min(f(t)) respectively.

4 Find the time-stamp of all differential WCK crossing that crosses 0V.

5 Use V_{Time} to get the actual crossing point voltage value using the time-stamp obtained in the previous step.

6 At each crosspoint (rising and falling) found, find the voltage differential between the crosspoint and V_{Ref}. The rising and falling crosspoint voltage differential is denoted as Vix_WCK_RF and Vix_WCK_FR respectively.

7 For each cross point voltage, calculate the final result using the equation (for Rising):

$$V_{IX}\_WCK\_ratio = 100\% \times [Vix\_WCK\_RF/Max(f(t))]$$

8 For each cross point voltage, calculate the final result using the equation (for Falling):

$$V_{IX}\_WCK\_ratio = 100\% \times [Vix\_WCK\_FR/Min(f(t))]$$

9 Determine the worst result from the set of V_{IX}_WCK_ratio measured.

Expected/ Observable Results: The calculated value of the crossing point voltage ratio for the differential test signal pair shall be within the conformance limits as per the JEDEC specification in the References section.

Read Data Strobe (Diff) tests

Output slew rate for differential signals are measured as shown in Figure 30.

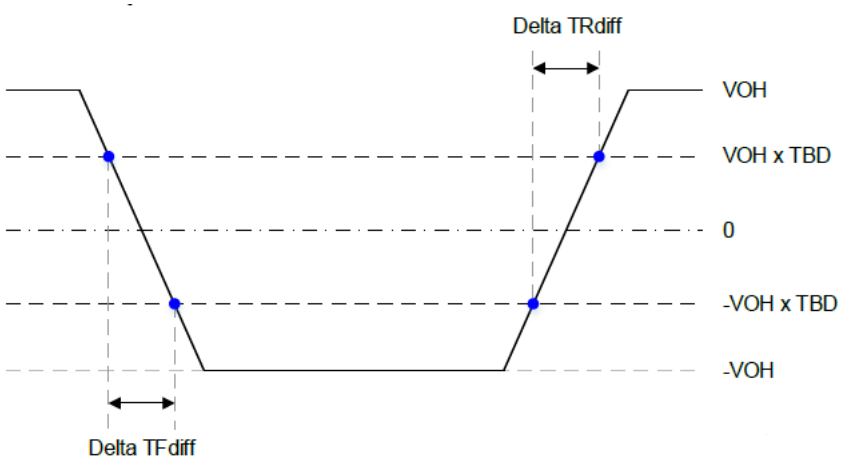

Figure 65 Differential output slew rate definition for RDQS signal

SRQdiffR_RDQS

Availability Condition: **Table 137 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	No	DQ, RDQS(Diff)

Test ID & References: **Table 138 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRQdiff	150002	Table 326

Overview: The purpose of this test is to verify the differential output slew rate for rising edge of the test signal within the read burst.

Procedure:

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all the valid Strobe rising edges in the specified burst.
A valid Strobe rising edge starts at V_{OL} crossing and ends at the following V_{OH} crossing.

4 For all the valid Strobe rising edges, find the transition time, T_R.
T_R is the time starting at V_{OL} crossing and ending at the following V_{OH} crossing.

5 Calculate SRQdiffR using the equation:

$$SRQdiffR = [V_{OH} - V_{OL}] / T_R$$

6 Determine the worst result from the set of SRQdiffR measured.

Expected/ Observable Results: The measured value of SRQdiffR for the test signal shall be within the conformance limits as per the JEDEC specification.

SRQdiffF_RDQS

Availability Condition: **Table 139 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	No	DQ, RDQS(Diff)

Test ID & References: **Table 140 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
SRQdiff	150003	Table 326

Overview: The purpose of this test is to verify the differential output slew rate for falling edge of the test signal within the read burst.

Procedure:

1 Acquire and split the read and write burst of the acquired signal.

2 Take the first valid READ burst found.

3 Find all the valid Strobe falling edges in the specified burst.
A valid Strobe falling edge starts at V_{OH} crossing and ends at the following V_{OL} crossing.

4 For all the valid Strobe falling edges, find the transition time, T_F.
T_F is the time starting at V_{OH} crossing and ending at the following V_{OL} crossing.

5 Calculate SRQdiffF using the equation:

$$SRQdiffF = [V_{OH} - V_{OL}] / T_F$$

6 Determine the worst result from the set of SRQdiffF measured.

Expected/ Observable Results: The measured value of SRQdiffF for the test signal shall be within the conformance limits as per the JEDEC specification.

Read Data Strobe (SE) RDQS_t (Read Data Strobe Plus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.

NOTE VDD is considered as VDD2H for CA[6:0], CK_t, CK_c, CS and RSET_n signals; whereas, VDD is considered as VDDQ for DQ, DMI, RDQS_t, WCK_t and WCK_c. Also, Vss = 0V.

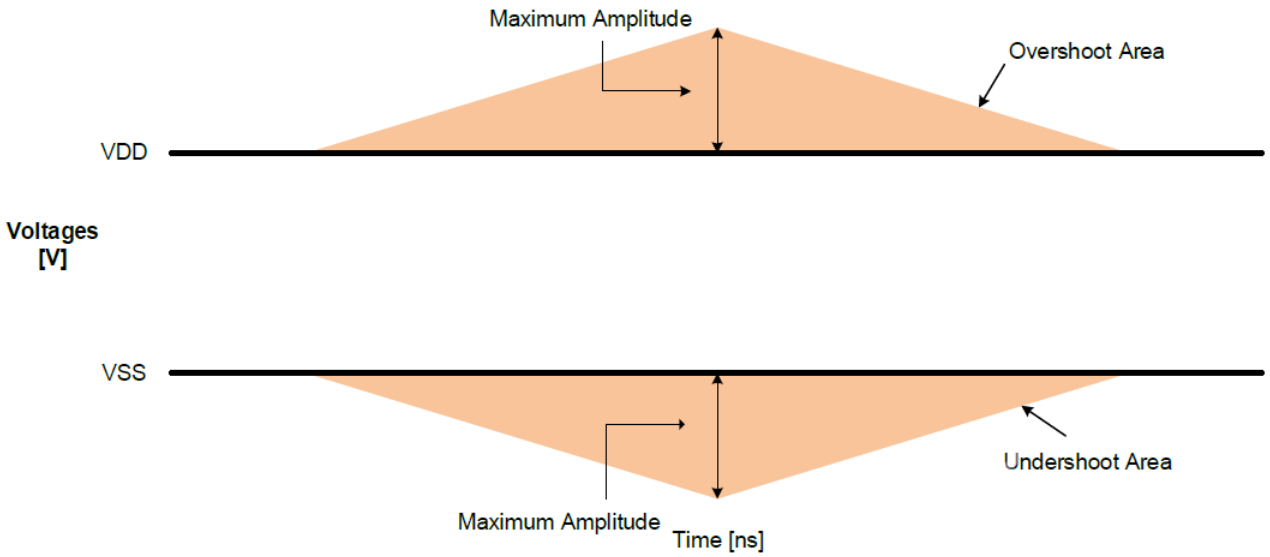

Figure 66 Overshoot and Undershoot definition for RDQS_t signal

Overshoot_Amplitude_RDQS_t

Availability Condition: **Table 141 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_t

Test ID & References: **Table 142 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152500	Table 311

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

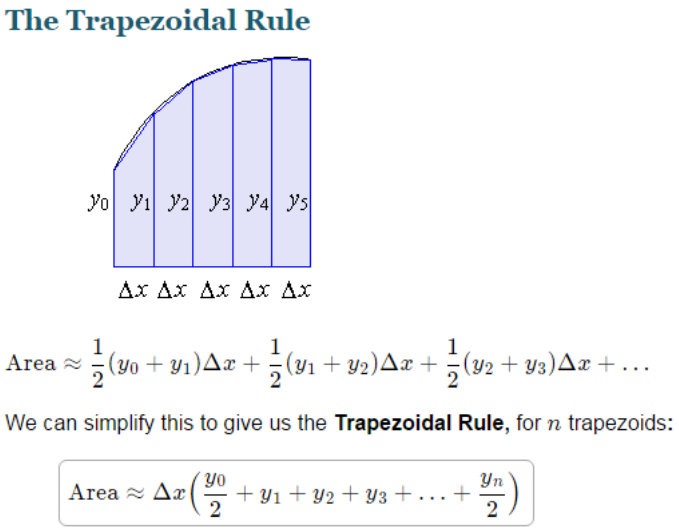

Figure 67 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Amplitude_RDQS_t

Availability Condition: **Table 143 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_t

Test ID & References: **Table 144 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152501	Table 311

Test Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

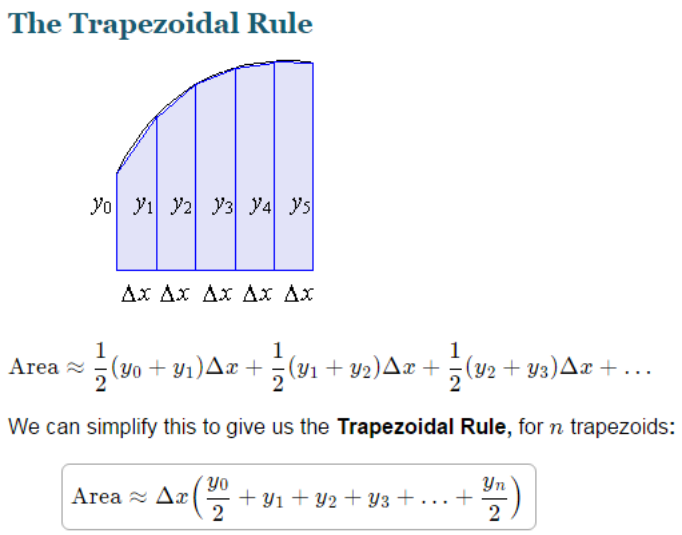

Figure 68 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Undershoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_RDQS_t

Availability Condition: **Table 145 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_t

Test ID & References: **Table 146 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152502	Table 311

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DDQ} crossing and ends at the falling edge of V_{DDQ} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DDQ}$$

b Evaluate Area_below_V_{DDQ} using the equation:

$$\text{Area\_below\_}V_{DDQ} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DDQ}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

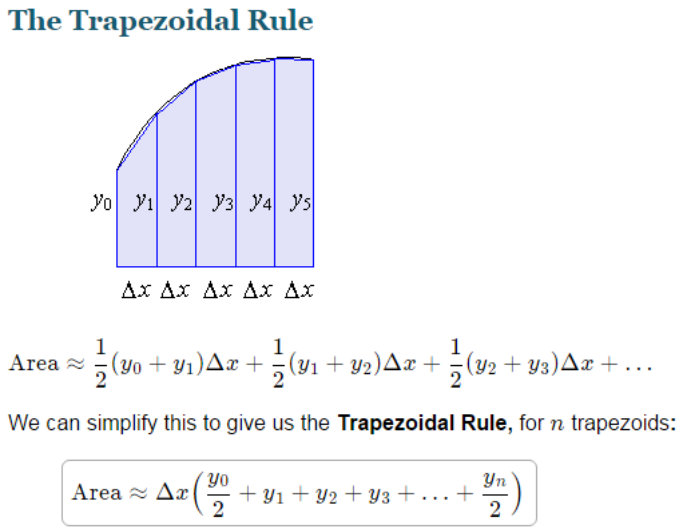

Figure 69 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DDQ} using the equation:

$$\text{Area\_Above\_}V_{DDQ} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DDQ}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DDQ}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Area_RDQS_t

Availability Condition: **Table 147 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_t

Test ID & References: **Table 148 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum undershoot area above VSS	152503	Table 311

Test Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

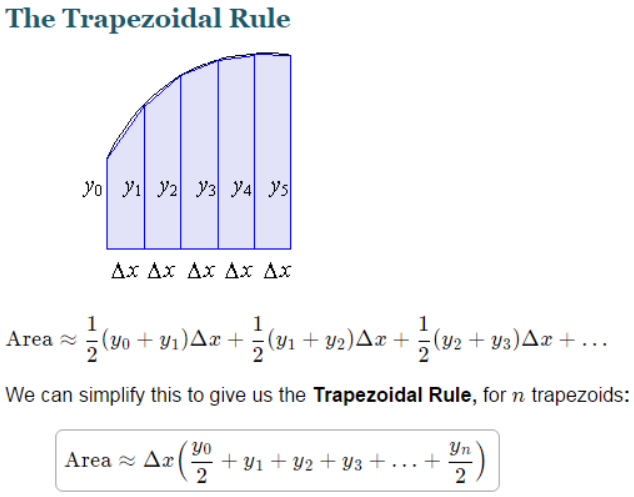

Figure 70 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
   - Undershoot Amplitude
   - Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Read Data Strobe (SE) RDQS_c (Read Data Strobe Minus) tests

Overshoot/Undershoot amplitude and area are measured in accordance to the waveforms shown in Figure 24.

NOTE VDD is considered as VDD2H for CA[6:0], CK_t, CK_c, CS and RSET_n signals; whereas, VDD is considered as VDDQ for DQ, DMI, RDQS_t, WCK_t and WCK_c. Also, Vss = 0V.

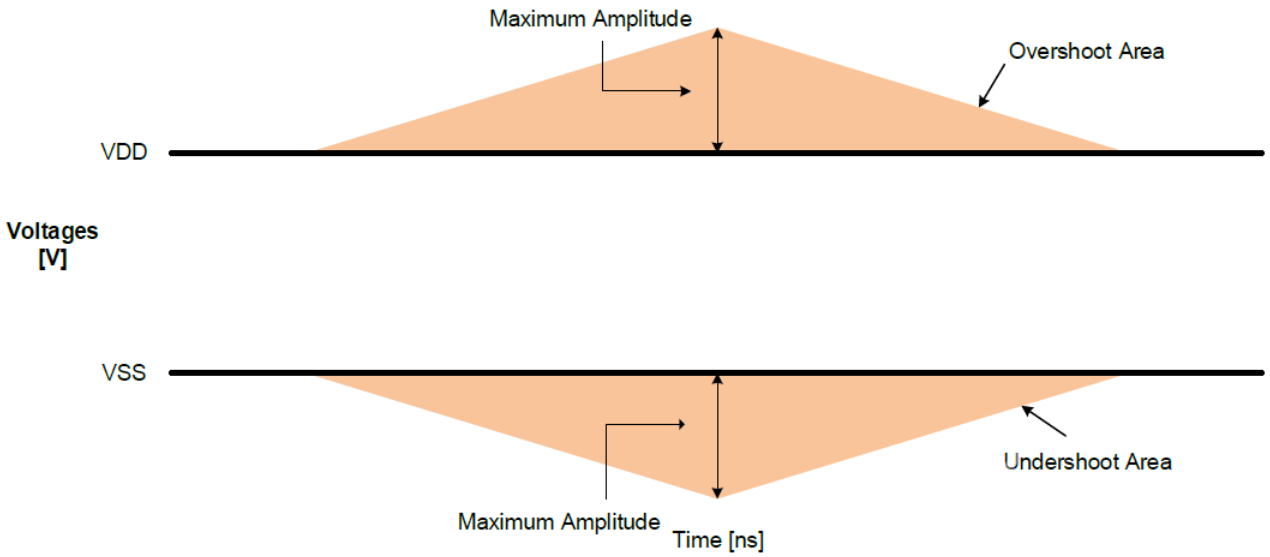

Figure 71 Overshoot and Undershoot definition for RDQS_c signal

Overshoot_Amplitude_RDQS_c

Availability Condition: **Table 149 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_c

Test ID & References: **Table 150 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for overshoot area	152600	Table 311

Test Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DDQ} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

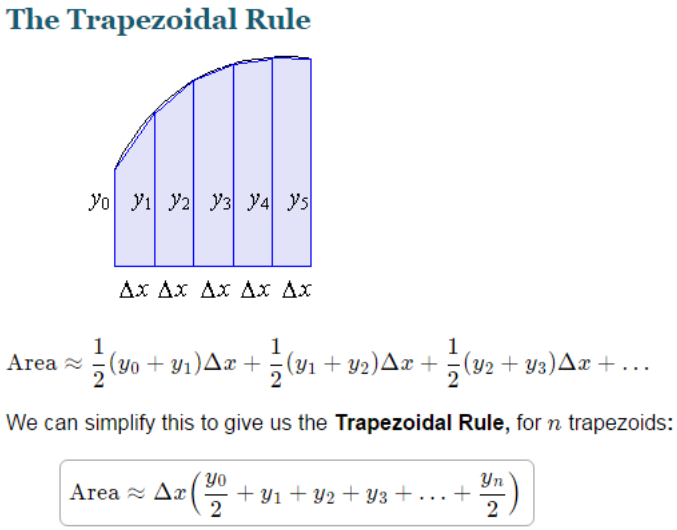

Figure 72 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Amplitude_RDQS_c

Availability Condition: **Table 151 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_c

Test ID & References: **Table 152 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum Peak Amplitude allowed for undershoot area	152601	Table 311

Test Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform.

In case of an undershoot, the undershoot area is calculated based on the Trapezoidal Method Area Calculation.

Test Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

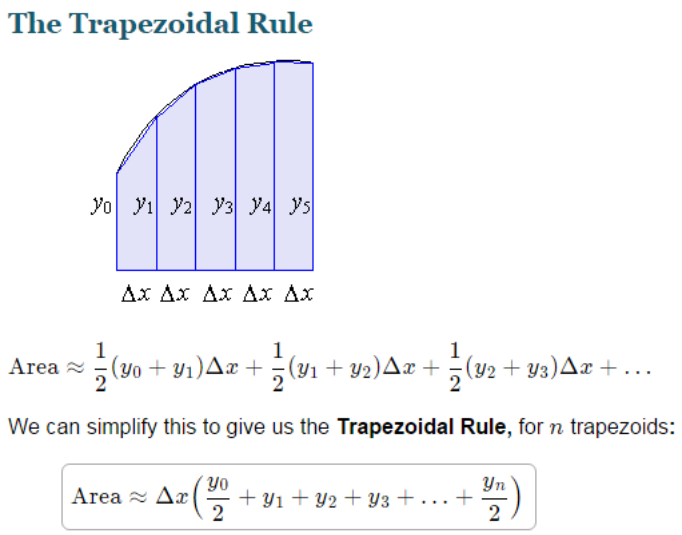

Figure 73 Equation for Total_Area_Below_Vss

c To find the worst case, save the following calculated results for later use:
- Undershoot Amplitude
- Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limit.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

Overshoot_Area_RDQS_c

Availability Condition: **Table 153 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_c

Test ID & References: **Table 154 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum overshoot area above V_{DD2H}/V_{DDQ}	152602	Table 311

Overview: The purpose of this test is to verify the overshoot amplitude value of the test signal that is found from all regions of the acquired waveform.

When there is overshoot, the overshoot area is calculated based on the overshoot width and overshoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “OvershootRegion” across the acquired waveform.
An “OvershootRegion” starts at the rising edge of V_{DD} crossing and ends at the falling edge of V_{DD} crossing.

3 Within OvershootRegion # 1:

a Evaluate Overshoot Amplitude by:

i Using T_{MAX}, V_{MAX} to obtain the time-stamp of the maximum voltage on the OvershootRegion.

ii Calculate Overshoot Amplitude using the equation:

$$\text{Overshoot Amplitude} = V_{MAX} - V_{DD}$$

b Evaluate Area_below_V_{DD} using the equation:

$$\text{Area\_below\_}V_{DD} = (\text{OvershootRegion\_End} - \text{OvershootRegion\_Start}) \times V_{DD}$$

c Evaluate Total_Area_Above_0V by using Trapezoidal Method Area Calculation:

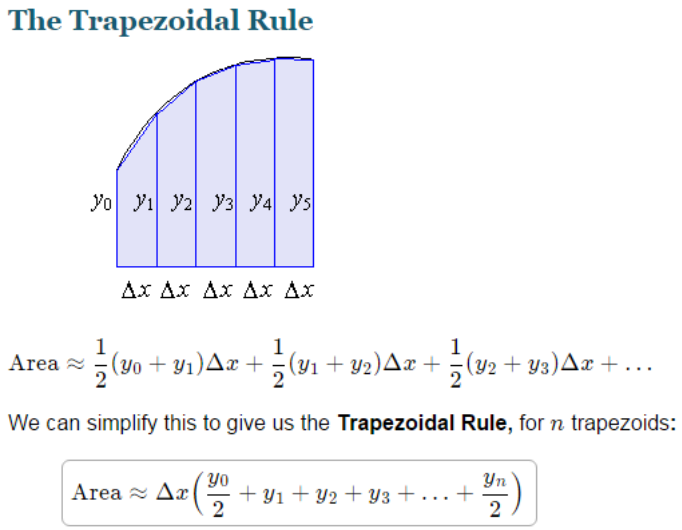

Figure 74 Equation for Total_Area_Above_0V

d Calculate Area_Above_V_{DD} using the equation:

$$\text{Area\_Above\_}V_{DD} = \text{Total\_Area\_Above\_0V} - \text{Area\_below\_}V_{DD}$$

e To find the worst case, save the following calculated results for later use:

- Overshoot Amplitude
- Area_Above_V_{DD}

4 Repeat step 3 for the rest of the “OvershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The Overshoot Amplitude and Area measurement value shall be within the conformance limits as per the JEDEC specification.

Undershoot_Area_RDQS_c

Availability Condition: **Table 155 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	No	Yes	RDQS_c

Test ID & References: **Table 156 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
Maximum undershoot area above VSS	152603	Table 311

Overview: The purpose of this test is to verify the undershoot amplitude value of the test signal that is found from all regions of the acquired waveform. In case of an undershoot, the undershoot area is calculated based on the undershoot width and undershoot amplitude.

Procedure:

1 Sample/acquire signal data and perform signal conditioning to maximize screen resolution (vertical scale adjustment).

2 Find the “UndershootRegion” across the acquired waveform.
An “UndershootRegion” starts at the falling edge of Vss (0V) crossing and ends at the rising edge of Vss (0V) crossing.

3 Within UndershootRegion # 1:

a Evaluate Undershoot Amplitude by:

i Using T_{MIN}, V_{MIN} to obtain the time-stamp of the minimum voltage on the UndershootRegion.

ii Calculating Undershoot Amplitude using the equation:

$$\text{Undershoot Amplitude} = Vss - V_{MIN}$$

b Evaluate Total_Area_Below_Vss by using Trapezoidal Method Area Calculation:

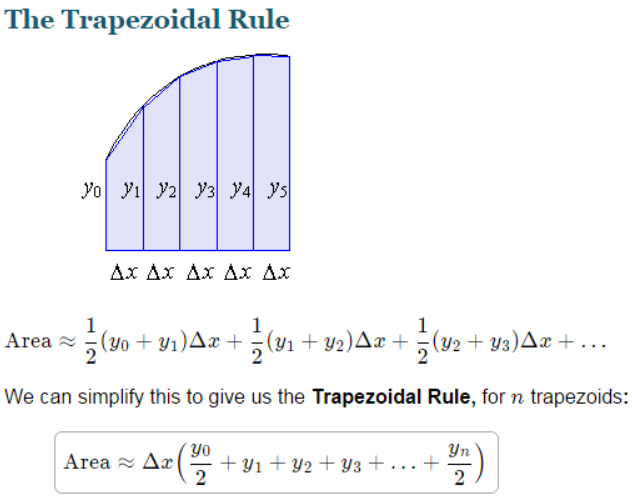

Figure 75 Equation for Total_Area_Above_Vss

c To find the worst case, save the following calculated results for later use:
   - Undershoot Amplitude
   - Total_Area_Below_Vss

4 Repeat step 3 for the rest of the “UndershootRegion” found in the acquired waveform.

5 Find the worst result from the stored results listed above.

6 Compare the test result with the compliance test limits.

Expected/ Observable Results: The values for Undershoot Amplitude and Area measurement shall be within the conformance limits as per the JEDEC specification.

5 Timing Tests

RDQS Detect Method for Read Write Separation

RDQS Detect is a read write separation method. This method works when the signal source contains at least an RDQS signal and a WCK signal. In this method, the Read/Write burst data is identified based on the presence of RDQS burst. If WCK burst contains an RDQS burst, then it is a Read burst. If the WCK burst does not contain an RDQS burst, then it is a Write burst.

If you select the RDQS Detect mode as the burst identification method, you must select the length of the WCK Postamble in the WCK Postamble Length section of the LPDDR5 General Setup dialog box.

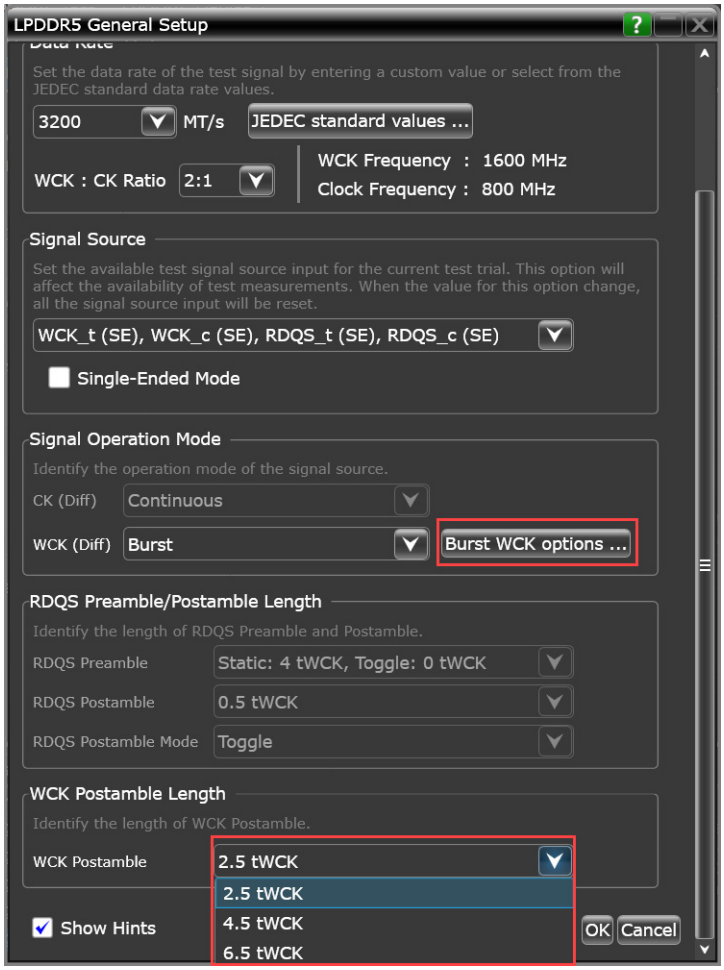

Figure 76 LPDDR5 General Setup Dialog

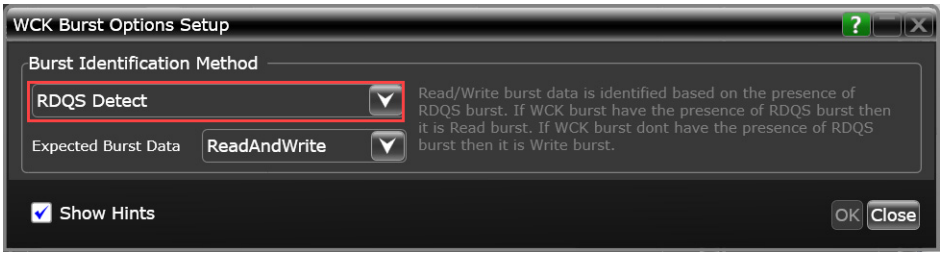

Figure 77 WCK Burst Options Setup Dialog

Tests that support the RDQS Detect Burst Identification Method

The following Timing tests support the RDQS Burst Identification method:

WRITE Tests

- tWCK2CK
- tWCKHL
- tWCKH
- tWCKL

READ Tests

- tRPRE
- tRPST
- tDQSQ
- tQSH
- tQSL

Method of Implementation for the RDQS Detect Burst Identification Method

The following are the steps for the method of implementation for the RDQS Detect burst identification method:

1 Populate the burst from WCK signal.

2 Locate FirstWCKRising for the burst.

3 Compute TimeA = FirstWCKRising + tWCKPRE_Toggle_RD * ClockCycleWidth.

4 Compute TimeB = Start of WCK postamble. For example, if tWCKPST=2.5nWCK then TimeB = time of second last rising edge of WCK burst. If tWCKPST=4.5nWCK then TimeB = time of fourth last rising edge of WCK burst.

5 Compute TimeC = 0.5*(TimeA+TimeB)

6 Compute VmaxTimeCWithinUI = Vmax range from (TimeC - 1*UI) to (TimeC + 1*UI)

7 Compute VminTimeCWithinUI = Vmin range from (TimeC - 1*UI) to (TimeC + 1*UI)

8 If [(VmaxTimeCWithinUI > VOHDiff_RDQS) AND (VminTimeCWithinUI < VOLDiff_RDQS)] then the burst will be recognized as a READ burst. Otherwise, the burst will be recognized as a WRITE burst.

9 Repeat steps 2 to 8 for the rest of burst.

Clock (Diff) Tests

The equations for the measurement of various parameters pertaining to Clock differential tests are given below:

$$tCK(avg) = \left(\sum_{j=1}^{N} tCKj\right)/N$$

$$where\ N = 200$$

Figure 78 Calculation for tCK(avg)

$$tCH(avg) = \left(\sum_{j=1}^{N} tCHj\right)/(N \times tCK(avg))$$

$$where\ N = 200$$

Figure 79 Calculation for tCH(avg)

$$tCL(avg) = \left(\sum_{j=1}^{N} tCLj\right)/(N \times tCK(avg))$$

$$where\ N = 200$$

Figure 80 Calculation for tCL(avg)

$$tjit(per) = Min./Max.\ of\ \{tCKi - tCK(avg),\ where\ i = 1\ to\ 200\}$$

Figure 81 Calculation for tjit(per)

$$tjit(cc) = Max.\ of\ |\{tCK(i+1) - tCK(i)\}|$$

Figure 82 Calculation for tjit(CC)

NOTE tCK(abs), tCH(abs) and tCL(abs) are measured directly on the Differential Clock signal and are considered as informative tests.

tCK(avg) Average Clock Period

Availability Condition: **Table 157 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 158 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCK(avg)	102020	Tables 345 - 348

Overview: tCK(avg) is the average clock period across a consecutive 200-cycle window. This test measures the period from the rising edge of a cycle to the next rising edge within the waveform window.

Procedure:

1 Acquire 202 cycles from the test signal.

2 Measure a sliding “window” of 200 cycles.

3 Calculate the average period value for periods 1-200.

4 Calculate the average period value for periods 2-201.

5 Calculate the average period value for periods 3-202.
Three measurement results are generated after step 4 is complete.

6 Check the three measured results for the smallest and largest values, which are recorded as the worst case values.

7 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tCK(avg) shall be within the conformance limits as per the JESD209-5 specification.

tCK(abs) Absolute Clock Period

Availability Condition: **Table 159 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 160 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCK(abs)	102021	Tables 345 - 348

Overview: tCK(abs) is the absolute clock period within a waveform window. This test measures the period from the rising edge of a cycle to the next consecutive rising edge within the waveform window.

Procedure:

1 Acquire 202 cycles from the test signal.
2 Find the maximum period value for period 1-202.
3 Find the minimum period value for period 1-202.
4 Check the two results for the worst case values.
5 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tCK(abs) for the test signal is reported as “Information Only”.

tCH(avg) Average High pulse width

Availability Condition: **Table 161 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 162 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCH(avg)	102022	Tables 345 - 348

Overview: tCH(avg) is the average pulse width across any consecutive 200 high pulses within a waveform window. This test measures the average duty cycle of all positive pulse widths within a window of 200 consecutive cycles.

Procedure:

1 Acquire 202 cycles from the test signal.

2 Measure a sliding “window” of 200 cycles.

3 Measure the width of the high pulses from cycle #1 to cycle #200 and determine the average value for this window. This generates one measurement result.

4 Measure the width of the high pulses from cycle #2 to cycle #201 and determine the average value for this window. This generates one more measurement result and two measurement values, overall.

5 Measure the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window.This generates one more measurement result and three measurement results, overall.

6 Check the three measured values for the smallest and largest values, which are recorded as the worst case values.

7 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tCH(avg) shall be within the conformance limits as per the JESD209-5 specification.

tCL(avg) Average Low pulse width

Availability Condition: **Table 163 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 164 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCL(avg)	102023	Tables 345 - 348

Overview: tCL(avg) is the average pulse width across any consecutive 200 low pulses within a waveform window. This test measures the average duty cycle of all negative pulse widths within a window of 200 consecutive cycles.

Procedure:

1 Acquire 202 cycles from the test signal.

2 Measure a sliding “window” of 200 cycles.

3 Measure the width of the low pulses from cycle#1 to cycle#200 and determine the average value for this window. This generates one measurement result.

4 Measure the width of the low pulses from cycle#2 to cycle#201 and determine the average value for this window. This generates one more measurement result and two measurement values overall.

5 Measure the width of the low pulses from cycle#3 to cycle#202 and determines the average value for this window. This generates one more measurement result and three measurement results overall.

6 Check the three measured values for the smallest and largest values, which are recorded as the worst case values.

7 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tCL(avg) shall be within the conformance limits as per the JESD209-5 specification.

tCH(abs) Absolute HIGH Clock pulse width

Availability Condition: **Table 165 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 166 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCH(abs)	102024	Tables 345 - 348

Overview: tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge. This test measures the absolute duty cycle of all positive pulse widths within a window of consecutive 200 cycles.

Procedure:

1 Acquire 202 cycles from the test signal.
2 Find the maximum high pulses width value for positive pulses #1 to #202.
3 Find the minimum high pulses width value for positive pulses #1 to #202.
4 Check these two results for the worst case values.
5 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tCH(abs) for the test signal is reported as “Information Only”.

tCL(abs) Absolute LOW Clock pulse width

Availability Condition: **Table 167 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 168 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCL(abs)	102025	Tables 345 - 348

Overview: tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge. This test measures the absolute duty cycle of all negative pulse widths within a window of 200 consecutive cycles.

Procedure:

1 Acquire 202 cycles from the test signal.
2 Find the maximum low pulses width value for negative pulses #1 to #202.
3 Find the minimum low pulses width value for negative pulses #1 to #202.
4 Check these two results for the worst case values.
5 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tCL(abs) for the test signal is reported as “Information Only”.

tjit(CC) Maximum Clock Jitter between consecutive cycles

Availability Condition: **Table 169 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 170 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tjit(CC)	102026	Tables 345 - 348

Overview: tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles. This test measures the clock period from the rising edge of a clock cycle to the next rising edge.

Procedure:

1 Acquire 202 cycles from the test signal.

2 Measure the difference between every adjacent pair of periods.

3 Generate a total of 201 measurement results.

4 Check the results for the smallest and largest values, which are recorded as the worst case values.

5 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tJIT(cc) for the test signal is reported as “Information Only”.

tjit(per) Clock period jitter

Availability Condition: **Table 171 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 172 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tjit(per)	102027	Tables 345 - 348

Overview: tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg). This test measures the difference between a measured clock period and the average clock period across multiple cycles of the clock.

Procedure:

1 Acquire 202 cycles from the test signal.

2 Measure the difference between every period inside a 200 cycle window with the average of the whole window.

3 Calculate the average for periods 1 to 200.

4 Measure the difference between period #1, period #2 and so on up to period #200; with the average and save the resulting value as a measurement result.
A total of 200 measurement results are generated.

5 For the next set of measurement values, slide the window by one period and measure the average of period #2 up to period #201.

6 Compare period #2 with the new average.
Continue the comparison for period #3, #4 and so on up to period #201.
A total of 200 additional measurement results are generated such that there are 400 measured values overall.

7 For the next set of measurement values, slide the window by one more period and measure the average of period #3 up to period #202.

8 Compare period #3 with the new average.
Continue the comparison for period #4, #5 and so on up to period #202.
A total of 200 additional measurement results are generated such that there are 600 measured values overall.

9 Check the 600 results for the smallest and largest values, which are recorded as the worst case values.

10 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tJIT(per) for the test signal is reported as “Information Only”.

Clock (SE Mode) Tests

The single-ended mode clock timing parameters can be measured as shown in Figure 83.

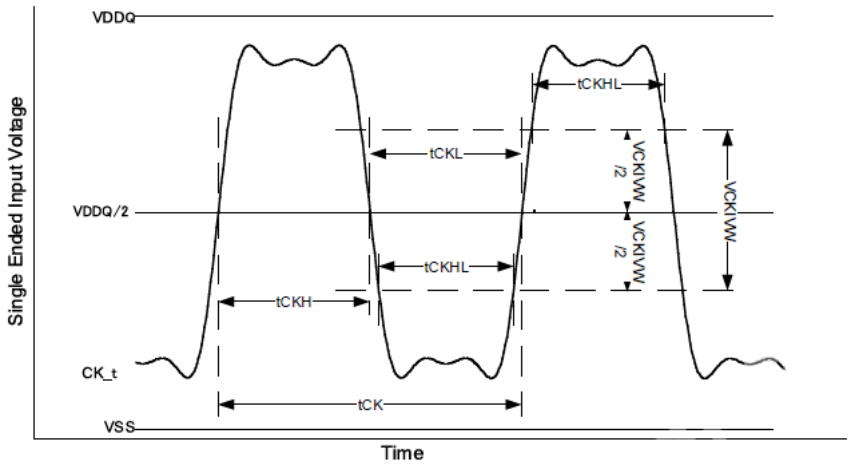

Figure 83 Single-ended mode CK pulse definitions

tCKHL

Availability Condition:

Table 173 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References:

Table 174 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tCKHL	251007	Table 328

Overview: The purpose of this test is to verify the pulse width of all the high pulses and the low pulses in the test signal.

Procedure:

1 Perform steps for tCKH to measure the worst high pulse width in the test signal.

2 Perform steps for tCKL to measure the worst low pulse width in the test signal.

3 Determine the final worst result from the worst high pulse width and worst low pulse width measured.

Expected/ Observable Results: The measured value of tCKHL shall be within the conformance limits as per the JESD209-5 specification.

tCKH

Availability Condition: **Table 175 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 176 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCKH	251010	Figure 210

Overview: The purpose of this test is to verify the pulse width of all the high pulse in the test signal.

Procedure:

1 Pre-condition the oscilloscope.

2 Find all valid positive pulses of the Clock in the entire waveform. A valid positive pulse on the Clock starts at the valid rising edge of the Clock and ends at the following valid falling edge of the Clock.

3 Find the maximum high pulse width value for all the positive pulses identified.

4 Find the minimum high pulse width value for all the positive pulses identified.

5 Determine the worst high pulse width (tCKH) in the test signal from the maximum and minimum pulse width measured.

Expected/ Observable Results: The measured value of tCKH shall be considered for “Information Only” purposes.

tCKL

Availability Condition: **Table 177 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	CK(Diff)

Test ID & References: **Table 178 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCKL	251011	Figure 210

Overview: The purpose of this test is to verify the pulse width of all the low pulses in the test signal.

Procedure:

1 Pre-condition the oscilloscope.

2 Find all valid negative pulses of the Clock in the entire waveform. A valid negative pulse on the Clock starts at the valid falling edge of the Clock and ends at the following valid rising edge of the Clock.

3 Find the maximum low pulse width value for all the negative pulses identified.

4 Find the minimum low pulse width value for all the negative pulses identified.

5 Determine the worst low pulse width (tCKL) in the test signal from the maximum and minimum pulse width measured.

Expected/ Observable Results: The measured value of tCKL shall be considered for “Information Only” purposes.

Write Clock (Diff) tests

An LPDDR5 SDRAM utilizes two types of clock with different frequencies. The frequency of WCK is four times or twice higher than the command clock. LPDDR5 uses a DDR data interface. The data interface uses two differential forwarded clocks (WCK_t/WCK_c) that are source synchronous to the DQs. DDR means that the data is registered at every rising edge of WCK_t and rising edge of WCK_c. WCK_t and WCK_c operate at twice the frequency of the command/address clock (CK_t/CK_c). WCK_t/WCK_c is used to sample DQ data for write operation and toggle DQ data for read operation. WCK_t/WCK_c must start toggle before starting write or read DQ data burst. All data bits (DQ[7:0] for WCK_t[0]/WCK_c[0], and DQ[15:8] for WCK_t[1]/WCK_c[1]) carry the training feedback to the controller. WCK is required to be trained to arrive at the DQ latch center-aligned with the Data eye training is accomplished by delaying the DQ signals relative to WCK such that the Data eye arrives at the receiver latch centered on the WCK transition. The latency control unit inside the SDRAM performs clock domain change of WRITE or READ commands from CK domain to WCK domain. An LPDDR5 SDRAM supports WCK free running mode. The DRAM controller must keep WCK toggling at its full rate after WCK2CK synchronization regardless of DQ operation. An LPDDR5 SDRAM requires being in WCK2CK synchronization state before the internal write operation starts. For WRITE operations, WCK must be driven at least tWCKPRE_Static+tWCKPRE_Toggle_WR before the write DQ burst. LPDDR5 will have a WCK post-amble of 0.5*tCK or TBD*tCK, after completing all write DQ burst.

The equations for the measurement of various parameters pertaining to Write Clock differential tests are given below:

$$tWCK(avg) = \left(\sum_{j=1}^{N} tWCKj\right)/N$$

$$where\ N = 200$$

Figure 84 Calculation for tWCK(avg)

$$tWCH(avg) = \left(\sum_{j=1}^{N} tWCHj\right)/(N \times tWCK(avg))$$

Figure 85 Calculation for tWCH(avg)

$$tWCL(avg) = \left(\sum_{j=1}^{N} tWCLj\right)/(N \times tWCK(avg))$$

$$where\ N = 200$$

Figure 86 Calculation for tWCL(avg)

$$tjit(per) = Min./Max.\ of\ \{tWCKi - tWCK(avg),\ where\ i = 1\ to\ 200\}$$

Figure 87 Calculation for tjit(per) for WCK (Diff)

$$tjit(CC) = Max.\ of\ |\{tWCK(i + 1) - tWCK(i)\}|$$

Figure 88 Calculation for tjit(CC) for WCK (Diff)

NOTE tWCK(abs), tWCH(abs) and tWCL(abs) are measured directly on the Differential Write Clock signal and are considered as informative tests.

tWCK(avg) Average Write Clock period

Availability Condition: **Table 179 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 180 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCK(avg)	102000	Tables 349 - 351

Overview: tWCK(avg) is the average write clock period across a consecutive 200-cycle window. This test measures the period from the rising edge of a cycle to the next rising edge within the waveform window.

Procedure:

1 Acquire 202 cycles from the test signal.
2 Measure a sliding “window” of 200 cycles.
3 Calculate the average period value for periods 1-200.
4 Calculate the average period value for periods 2-201.
5 Calculate the average period value for periods 3-202.
Three measurement results are generated after step 4 is complete.
6 Check the three measured results for the smallest and largest values, which are recorded as the worst case values.
7 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tWCK(avg) shall be within the conformance limits as per the JESD209-5 specification.

tWCK(abs) Absolute Write Clock period

Availability Condition: **Table 181 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 182 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCK(abs)	102001	Tables 349 - 351

Overview: tWCK(abs) is the absolute write clock period within a waveform window. This test measures the period from the rising edge of a cycle to the next consecutive rising edge within the waveform window.

Procedure:

1 Acquire 202 cycles from the test signal.
2 Find the maximum period value for period 1-202.
3 Find the minimum period value for period 1-202.
4 Check the two results for the worst case values.
5 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tWCK(abs) for the test signal is reported as “Information Only”.

tWCKH(avg) Average High pulse width

Availability Condition: **Table 183 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 184 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCKH(avg)	102002	Tables 349 - 351

Overview: tWCKH(avg) is the average pulse width across any consecutive 200 high pulses within a waveform window. This test measures the average duty cycle of all positive pulse widths within a window of 200 consecutive cycles.

Procedure:

1 Acquire 202 cycles from the test signal.

2 Measure a sliding “window” of 200 cycles.

3 Measure the width of the high pulses from cycle #1 to cycle #200 and determine the average value for this window. This generates one measurement result.

4 Measure the width of the high pulses from cycle #2 to cycle #201 and determine the average value for this window. This generates one more measurement result and two measurement values, overall.

5 Measure the width of the high pulses from cycle #3 to cycle #202 and determines the average value for this window.This generates one more measurement result and three measurement results, overall.

6 Check the three measured values for the smallest and largest values, which are recorded as the worst case values.

7 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tWCKH(avg) shall be within the conformance limits as per the JESD209-5 specification.

tWCKL(avg) Average Low pulse width

Availability Condition: **Table 185 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 186 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCKL(avg)	102003	Tables 349 - 351

Overview: tWCKL(avg) is the average pulse width across any consecutive 200 low pulses within a waveform window. This test measures the average duty cycle of all negative pulse widths within a window of 200 consecutive cycles.

Procedure:

1 Acquire 202 cycles from the test signal.

2 Measure a sliding “window” of 200 cycles.

3 Measure the width of the low pulses from cycle#1 to cycle#200 and determine the average value for this window. This generates one measurement result.

4 Measure the width of the low pulses from cycle#2 to cycle#201 and determine the average value for this window. This generates one more measurement result and two measurement values overall.

5 Measure the width of the low pulses from cycle#3 to cycle#202 and determine the average value for this window. This generates one more measurement result and three measurement results overall.

6 Check the three measured values for the smallest and largest values, which are recorded as the worst case values.

7 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tWCKL(avg) shall be within the conformance limits as per the JESD209-5 specification.

tWCKH(abs) Absolute HIGH Write Clock pulse width

Availability Condition: **Table 187 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 188 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCKH(abs)	102004	Tables 349 - 351

Overview: tWCKH(abs) is the absolute instantaneous write clock high pulse width, as measured from one rising edge to the following falling edge. This test measures the absolute duty cycle of all positive pulse widths within a window of consecutive 200 cycles.

Procedure:

1 Acquire 202 cycles from the test signal.
2 Find the maximum high pulses width value for positive pulses #1 to #202.
3 Find the minimum high pulses width value for positive pulses #1 to #202.
4 Check these two results for the worst case values.
5 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tWCKH(abs) for the test signal is reported as “Information Only”.

tWCKL(abs) Absolute LOW Write Clock pulse width

Availability Condition: **Table 189 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 190 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCKL(abs)	102005	Tables 349 - 351

Overview: tWCKL(abs) is the absolute instantaneous write clock low pulse width, as measured from one falling edge to the following rising edge. This test measures the absolute duty cycle of all negative pulse widths within a window of 200 consecutive cycles.

Procedure:

1 Acquire 202 cycles from the test signal.
2 Find the maximum low pulses width value for negative pulses #1 to #202.
3 Find the minimum low pulses width value for negative pulses #1 to #202.
4 Check these two results for the worst case values.
5 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tWCKL(abs) for the test signal is reported as “Information Only”.

tjit(CC) Maximum Write Clock Jitter between consecutive cycles

Availability Condition: **Table 191 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 192 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tjit(CC)	102006	Tables 349 - 351

Overview: tJIT(cc) is defined as the absolute difference in write clock period between two consecutive write clock cycles. This test measures the write clock period from the rising edge of a write clock cycle to the next rising edge.

Procedure:

1 Acquire 202 cycles from the test signal.

2 Measure the difference between every adjacent pair of periods.

3 Generate a total of 201 measurement results.

4 Check the results for the smallest and largest values, which are recorded as the worst case values.

5 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tJIT(cc) for the test signal is reported as “Information Only”.

tjit(per) Write Clock period jitter

Availability Condition: **Table 193 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 194 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tjit(per)	102007	Tables 349 - 351

Overview: tJIT(per) is the single period jitter defined as the largest deviation of any signal tWCK from tWCK(avg). This test measures the difference between a measured write clock period and the average write clock period across multiple cycles of the write clock signal.

Procedure:

1 Acquire 202 cycles from the test signal.

2 Measure the difference between every period inside a 200 cycle window with the average of the whole window.

3 Calculate the average for periods 1 to 200.

4 Measure the difference between period #1, period #2 and so on up to period #200; with the average and save the resulting value as a measurement result.
A total of 200 measurement results are generated.

5 For the next set of measurement values, slide the window by one period and measure the average of period #2 up to period #201.

6 Compare period #2 with the new average.
Continue the comparison for period #3, #4 and so on up to period #201.
A total of 200 additional measurement results are generated such that there are 400 measured values overall.

7 For the next set of measurement values, slide the window by one more period and measure the average of period #3 up to period #202.

8 Compare period #3 with the new average.
Continue the comparison for period #4, #5 and so on up to period #202.
A total of 200 additional measurement results are generated such that there are 600 measured values overall.

9 Check the 600 results for the smallest and largest values, which are recorded as the worst case values.

10 Compare the worst case values to the compliance test limits.

Expected/ Observable Results: The measured value of tJIT(per) for the test signal is reported as “Information Only”.

tERR(2per) Write Clock Cumulative error across 2 cycles

Availability Condition: **Table 195 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 196 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tERR(2per)	102008	Table 349 - 351

Overview: The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of “n” (for “n” cycles).

Procedure: Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

tERR(2per) is very similar to tJIT(per), except that a small 2-cycle window is formed inside a large 200-cycle window. The width of the total consecutive cycles for the small window (denoted as W) is compared against equivalent number of consecutive average cycles (denoted as C) obtained from the large 200-cycle window (n x C), where C is the average value of the 200 cycle large window and n is the number of cycles. In the case of tERR(2per), n = 2. The steps described in the following procedure cover for all cycles, when n is replaced by the respective number of cycles.

1 Calculate the average period inside the first large 200-cycle window, denote as C_1.

2 Calculate the small window width, W (total width of 2 consecutive cycles). The first small window would cover period #1 and period #2.

3 Calculate the cumulative error value from C_1 and W found above using the equation below, where n=2 for tERR(2 per).

$tERR(nper) = W - n \times C_1$, where n is the number of consecutive cycles

4 Sweep the small window across by one period and find the width of the next 2 consecutive cycles (the next small window would cover period #2 and period #3).

5 Repeat step 3 with the new value of W.

6 Repeat the process described in steps 1 to 5 until the last small window within C_1 (from period#199 to period#200) is covered.

7 Find the worst error from step 4 and denote it as CumErr1.

8 Repeat steps 1 to 7 to derive CumErr2 (for the second large 200-cycle window of period cycle #2 to #201) and CumErr3 (for the third large 200-cycle window of period cycle #3 to #202).

9 Determine the worst error CumErr1, CumErr2 and CumErr3. Report the worst value as the result for tERR(2per).

tERR(3per) is the same as tERR(2per) except that the small window size is 3-cycle wide. tERR(4per) uses a smaller window size of 4-cycle period.

Expected/ Observable Results: All measured values of tERR(2per) for the test signal shall be within the conformance limits as per the JEDEC specification.

tERR(3per) Write Clock Cumulative error across 3 cycles

Availability Condition: **Table 197 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 198 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tERR(3per)	102009	Table 349 - 351

Overview: The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of “n” (for “n” cycles).

Procedure: Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

tERR(3per) is very similar to tJIT(per), except that a small 3-cycle window is formed inside a large 200-cycle window. The width of the total consecutive cycles for the small window (denoted as W) is compared against equivalent number of consecutive average cycles (denoted as C) obtained from the large 200-cycle window (n x C), where C is the average value of the 200 cycle large window and n is the number of cycles. In the case of tERR(3per), n = 3. The steps described in the following procedure cover for all cycles, when n is replaced by the respective number of cycles.

1 Calculate the average period inside the first large 200-cycle window, denote as C_1.
2 Calculate the small window width, W (total width of 2 consecutive cycles). The first small window would cover period #1 and period #2.
3 Calculate the cumulative error value from C_1 and W found above using the equation below, where n=3 for tERR(3per).

   tERR(nper) = W - n x C_1, where n is the number of consecutive cycles
4 Sweep the small window across by one period and find the width of the next 2 consecutive cycles (the next small window would cover period #2 and period #3).
5 Repeat step 3 with the new value of W.
6 Repeat the process described in steps 1 to 5 until the last small window within C_1 (from period#199 to period#200) is covered.
7 Find the worst error from step 4 and denote it as CumErr1.
8 Repeat steps 1 to 7 to derive CumErr2 (for the second large 200-cycle window of period cycle #2 to #201) and CumErr3 (for the third large 200-cycle window of period cycle #3 to #202).
9 Determine the worst error CumErr1, CumErr2 and CumErr3. Report the worst value as the result for tERR(3per).

tERR(3per) is the same as tERR(2per) except that the small window size is 3-cycle wide. tERR(4per) uses a smaller window size of 4-cycle period.

Expected/ Observable Results: All measured values of tERR(3per) for the test signal shall be within the conformance limits as per the JEDEC specification.

tERR(4per) Write Clock Cumulative error across 4 cycles

Availability Condition: **Table 199 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	Burst & Continuous	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 200 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tERR(4per)	102010	Table 349 - 351

Overview: The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. Supported measurements include multiple cycle windows with values of “n” (for “n” cycles).

Procedure: Example input test signal:

Frequency: 1 kHz, Number of cycles acquired: 202

tERR(4per) is very similar to tJIT(per), except that a small 4-cycle window is formed inside a large 200-cycle window. The width of the total consecutive cycles for the small window (denoted as W) is compared against equivalent number of consecutive average cycles (denoted as C) obtained from the large 200-cycle window (n x C), where C is the average value of the 200 cycle large window and n is the number of cycles. In the case of tERR(4per), n = 4. The steps described in the following procedure cover for all cycles, when n is replaced by the respective number of cycles.

1 Calculate the average period inside the first large 200-cycle window, denote as C_1.

2 Calculate the small window width, W (total width of 2 consecutive cycles). The first small window would cover period #1 and period #2.

3 Calculate the cumulative error value from C_1 and W found above using the equation below, where n=4 for tERR(4per).

$tERR(nper) = W - n \times C_1$, where n is the number of consecutive cycles

4 Sweep the small window across by one period and find the width of the next 2 consecutive cycles (the next small window would cover period #2 and period #3).

5 Repeat step 3 with the new value of W.

6 Repeat the process described in steps 1 to 5 until the last small window within C_1 (from period#199 to period#200) is covered.

7 Find the worst error from step 4 and denote it as CumErr1.

8 Repeat steps 1 to 7 to derive CumErr2 (for the second large 200-cycle window of period cycle #2 to #201) and CumErr3 (for the third large 200-cycle window of period cycle #3 to #202).

9 Determine the worst error CumErr1, CumErr2 and CumErr3. Report the worst value as the result for tERR(2per).

tERR(3per) is the same as tERR(2per) except that the small window size is 3-cycle wide. tERR(4per) uses a smaller window size of 4-cycle period.

Expected/ Observable Results: All measured values of tERR(4per) for the test signal shall be within the conformance limits as per the JEDEC specification.

Write Clock (SE Mode) Tests

The single-ended mode write clock timing parameters can be measured as shown in Figure 83.

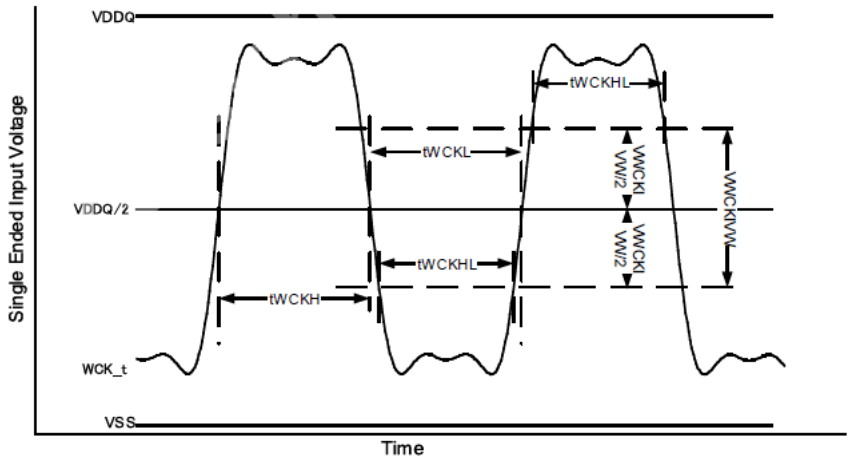

Figure 89 Single-ended mode WCK pulse definitions

tWCKHL

Availability Condition: **Table 201 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	No	Yes	WCK(Diff)

Test ID & References: **Table 202 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCKHL	251107	Table 327

Overview: The purpose of this test is to verify the pulse width of all the high pulses and the low pulses in the test signal.

Procedure:
1. Perform steps for tWCKH to measure the worst high pulse width in the test signal.
2. Perform steps for tWCKL to measure the worst low pulse width in the test signal.
3. Determine the final worst result from the worst high pulse width and worst low pulse width measured.

Expected/ Observable Results: The measured value of tWCKHL shall be within the conformance limits as per the JESD209-5 specification.

tWCKH

Availability Condition: **Table 203 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	Yes	Yes	WCK(Diff)

Test ID & References: **Table 204 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCKH	251110	Figure 208

Overview: The purpose of this test is to verify the pulse width of all the high pulses in the test signal.

Procedure:

1 Acquire and identify the WRITE burst data of the test signal.

2 Consider the first valid WRITE burst found.

3 Find all valid positive pulses of the Write Clock in the specified burst. A valid positive pulse on the Write Clock starts at the valid rising edge of the Write Clock and ends at the following valid falling edge of the Write Clock.

4 Find the maximum high pulse width value for all the positive pulses identified.

5 Find the minimum high pulse width value for all the positive pulses identified.

6 Determine the worst high pulse width (tWCKH) in the test signal from the maximum and minimum pulse width measured.

Expected/ Observable Results: The measured value of tWCKH shall be considered for “Information Only” purposes.

tWCKL

Availability Condition: **Table 205 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	Yes	Yes	Yes	WCK(Diff)

Test ID & References: **Table 206 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCKL	251111	Figure 208

Overview: The purpose of this test is to verify the pulse width of all the low pulses in the test signal.

Procedure:

1 Acquire and identify the WRITE burst data of the test signal.

2 Consider the first valid WRITE burst found.

3 Find all valid negative pulses of the Write Clock in the specified burst. A valid negative pulse on the Write Clock starts at the valid falling edge of the Write Clock and ends at the following valid rising edge of the Write Clock.

4 Find the maximum low pulse width value for all the negative pulses identified.

5 Find the minimum low pulse width value for all the negative pulses identified.

6 Determine the worst low pulse width (tWCKL) in the test signal from the maximum and minimum pulse width measured.

Expected/ Observable Results: The measured value of tWCKL shall be considered for “Information Only” purposes.

Other timing tests

To check for various timing parameters, consider the timing diagram shown in Figure 90.

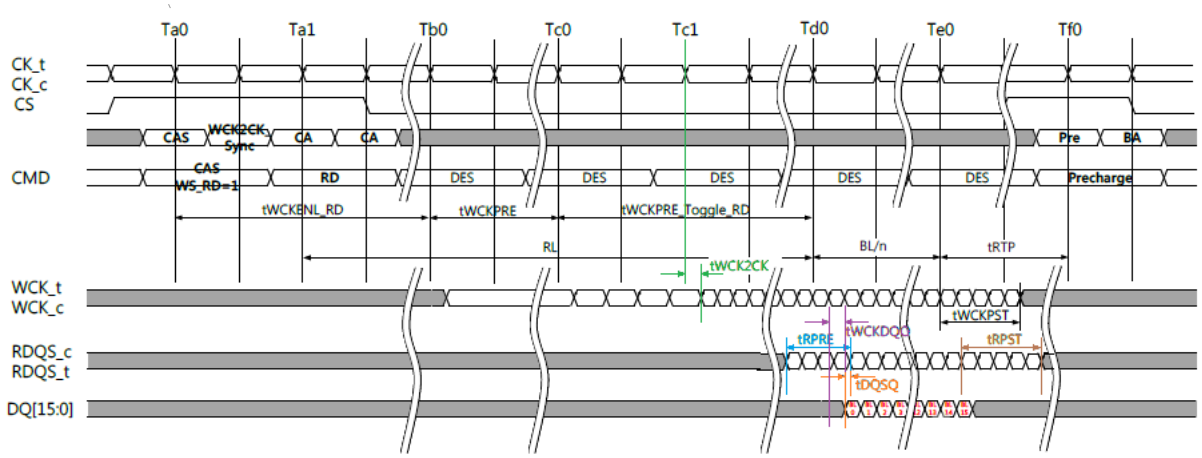

Figure 90 Differential and Full-rate RDQS timings

tWCK2CK

Availability Condition: **Table 207 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	Yes	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 208 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCK2CK	131000	Table 242

Overview: The purpose of this test is to verify the phase offset between the Clock (CK) signal and Write Clock (WCK) signal.

Procedure:

1 Acquire and split read and write burst of the acquired signal.
2 Validate the Read and Write bursts obtained in the previous step. Invalid bursts are disregarded.
3 Take the first valid WRITE burst found.
4 Find the first valid rising WCK edge (excluding the preamble pattern) of the specified burst.
5 Find the nearest CK edge.
6 Measure tWCK2CK as the time difference between these two edges of WCK and CK.

Expected/ Observable Results: The measured value of tWCK2CK shall be within the conformance limits as per the JESD209-5 specification.

tRPRE

Availability Condition: **Table 209 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)

Test ID & References: **Table 210 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tRPRE	130000	Table 173

Overview: The purpose of this test is to verify the time when RDQS starts driving high (*preamble behavior) to the first DQ signal crossing for the Read Cycle.

Procedure:

1 From the first valid RDQS burst found, find the first rising edge (before the preamble) at the middle threshold (0V) of the specified burst.

2 Find the next edge after the defined RDQS preamble length, which is configured in the **General Setup** window of the **Set Up** tab.

3 Measure the time difference between these two edges.

4 Report the measurement as tRPRE.

Expected/ Observable Results: The measured value of tRPRE shall be within the conformance limits as per the JESD209-5 specification.

tRPST

Availability Condition: **Table 211 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)

Test ID & References: **Table 212 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tRPST	130001	Table 173

Overview: The purpose of this test is to verify the time when RDQS is no longer driving from high/low state to Hi-impedance from the last DQ signal crossing (last bit of the Read Data burst).

Procedure:

1 Find the last edge of the RDQS burst found.

2 Find the edge pertaining to RDQS postamble length prior to the edge found in the previous step.

3 Measure the time difference between these two edges.

4 Report the measurement as tRPST.

Expected/ Observable Results: The measured value of tRPST shall be within the conformance limits as per the JESD209-5 specification.

tDQSQ

Availability Condition: **Table 213 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	DQ, RDQS(Diff)

Test ID & References: **Table 214 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tDQSQ	130002	Table 173

Overview: The purpose of this test is to verify the time interval from the RDQS (RDQS rising and falling edges) access time to the associated data (DQ rising and falling) signal.

Procedure:
1 Find all valid rising and falling DQ crossings at VREFDQ level in the specified burst.
2 For all DQ crossings found, locate the nearest RDQS edges.
3 Measure the time difference between these two edges.
4 Report the measurement as tDQSQ.

Expected/ Observable Results: The measured value of tDQSQ shall be within the conformance limits as per the JESD209-5 specification.

tQSH

Availability Condition: **Table 215 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	WCK(Diff), DQ, RDQS(Diff)

Test ID & References: **Table 216 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tQSH	130003	Table 242

Overview: The purpose of this test is to verify the width of the positive pulse of the RDQS signal.

Procedure:
1 Measure tQSH as the time starting from a rising edge of the RDQS positive pulse and ending at the following falling edge.
2 Capture all values of tQSH.
3 Determine the worst result from the set of tQSH measured.

Expected/ Observable Results: The measured value of tQSH shall be within the conformance limits as per the JESD209-5 specification.

tQSL

Availability Condition: **Table 217 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
N/A	N/A	Yes	Yes	Yes	WCK(Diff), DQ, RDQS(Diff)

Test ID & References: **Table 218 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tQSL	130004	Table 242

Overview: The purpose of this test is to verify the width of the negative pulse of the RDQS signal.

Procedure:
1. Measure tQSL as the time starting from a falling edge of the RDQS negative pulse and ending at the following rising edge.
2. Capture all values of tQSL.
3. Determine the worst result from the set of tQSL measured.

Expected/ Observable Results: The measured value of tQSL shall be within the conformance limits as per the JESD209-5 specification.

6 Eye Diagram Tests

RDQS Detect Method for Read Write Separation

RDQS Detect is a read write separation method. This method works when the signal source contains at least an RDQS signal and a WCK signal. In this method, the Read/Write burst data is identified based on the presence of RDQS burst. If WCK burst contains an RDQS burst, then it is a Read burst. If the WCK burst does not contain an RDQS burst, then it is a Write burst.

If you select the RDQS Detect mode as the burst identification method, you must select the length of the WCK Postamble in the WCK Postamble Length section of the LPDDR5 General Setup dialog box.

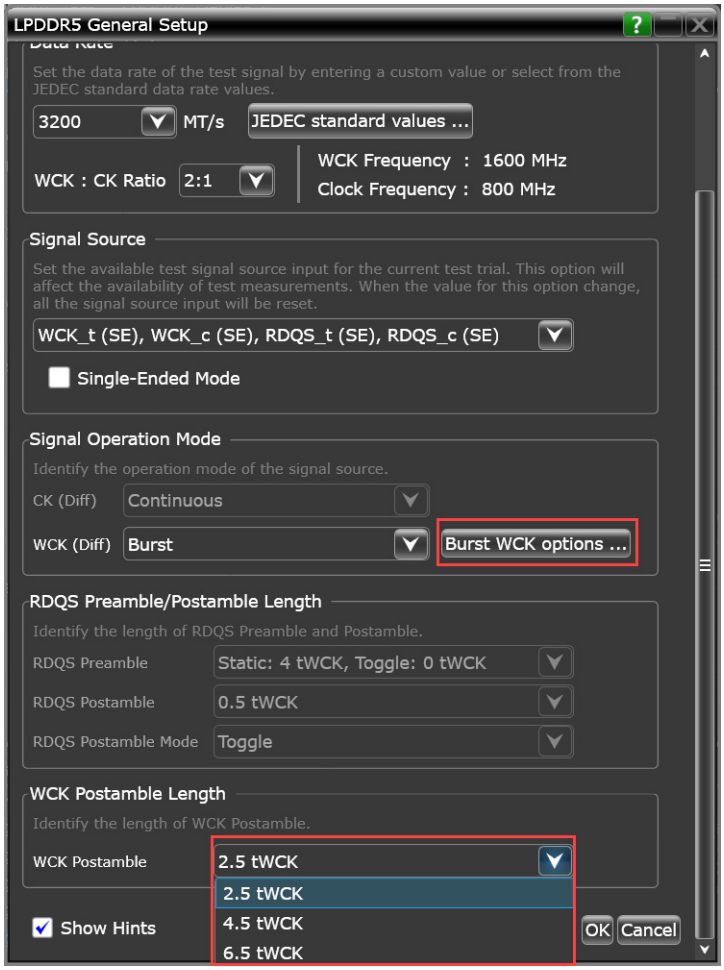

Figure 91 LPDDR5 General Setup Dialog

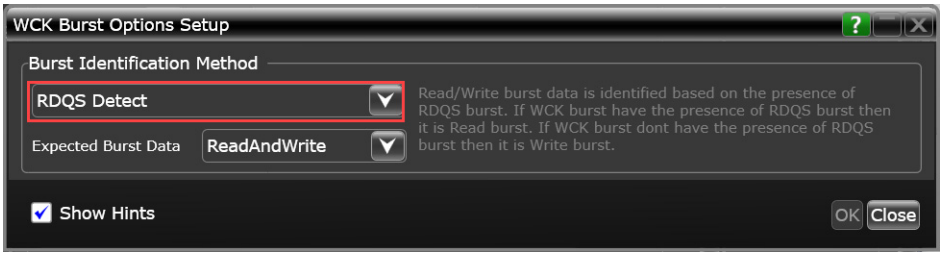

Figure 92 WCK Burst Options Setup Dialog

Tests that support the RDQS Detect Burst Identification Method

The following Eye Diagram tests support the RDQS Burst Identification method:

WRITE Tests

- tDIVW1 Margin
- tDIVW2 Margin
- vDIVW Margin
- tDIPW
- tDIHL
- VDIHL_AC
- tWCK2DQI_HF

READ Tests

- tQW
- tWCK2DQO_HF

Method of Implementation for the RDQS Detect Burst Identification Method

The following are the steps for the method of implementation for the RDQS Detect burst identification method:

1 Populate the burst from WCK signal.

2 Locate FirstWCKRising for the burst.

3 Compute TimeA = FirstWCKRising + tWCKPRE_Toggle_RD * ClockCycleWidth.

4 Compute TimeB = Start of WCK postamble. For example, if tWCKPST=2.5nWCK then TimeB = time of second last rising edge of WCK burst. If tWCKPST=4.5nWCK then TimeB = time of fourth last rising edge of WCK burst.

5 Compute TimeC = 0.5*(TimeA+TimeB)

6 Compute VmaxTimeCWithinUI = Vmax range from (TimeC - 1*UI) to (TimeC + 1*UI)

7 Compute VminTimeCWithinUI = Vmin range from (TimeC - 1*UI) to (TimeC + 1*UI)

8 If [(VmaxTimeCWithinUI > VOHDiff_RDQS) AND (VminTimeCWithinUI < VOLDiff_RDQS)] then the burst will be recognized as a READ burst. Otherwise, the burst will be recognized as a WRITE burst.

9 Repeat steps 2 to 8 for the rest of burst.

References for DQ Rx Voltage and Timing tests

LPDDR5 DQ, DMI, Parity and DBI Rx mask is defined as hexagonal mask as shown in Figure 93. The mask (vDIVW, tDIVW1, tDIVW2) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal.

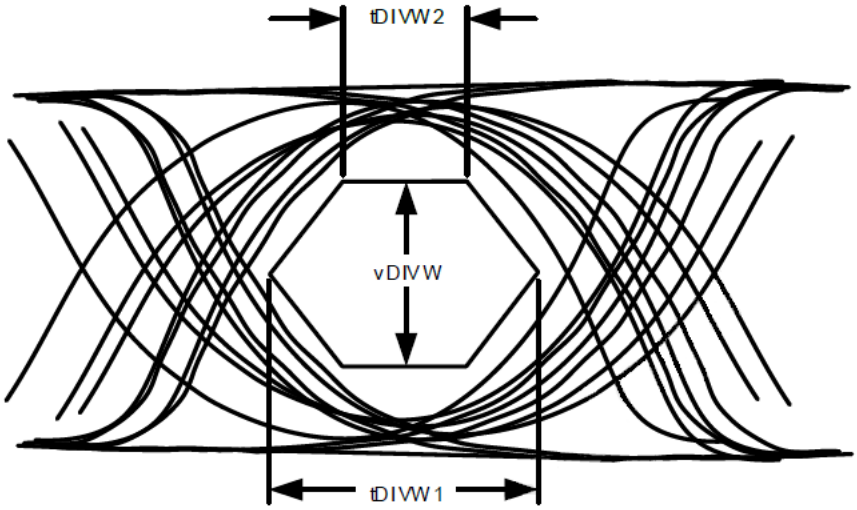

Figure 93 DQ Rx Mask definition

Rx mask voltage vDIVW has to be centered around VrefDQ as shown in Figure 94. DQ single input pulse amplitude into the receiver has to meet or exceed vDIHL_AC at any point over the total UI. vDIHL_AC is the peak to peak voltage centered around VrefDQ such that vDIHL_AC/2 min has to be met both above and below VrefDQ.

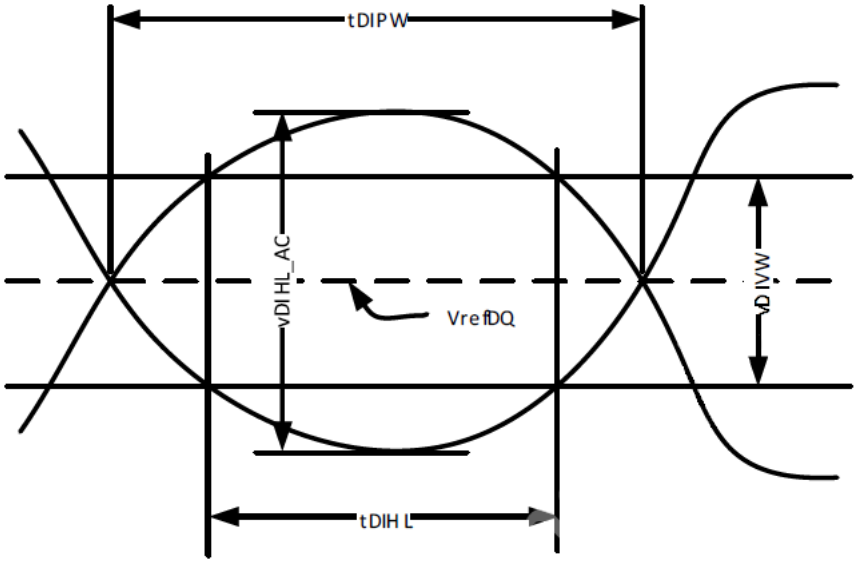

Figure 94 Identifying DQ Rx Mask parameters with respect to VrefDQ

tWCK2DQI is measured at the center (midpoint) of the tDIVW window, as shown in Figure 95. The LPDDR5-SDRAM uses an un-matched WCK-DQ path for lower power, so the WCK must arrive at the SDRAM ball prior to the DQ signal by the amount of tWCKDQI. The WCK must be trained to arrive at the DQ pad center-aligned with the DQ-data.

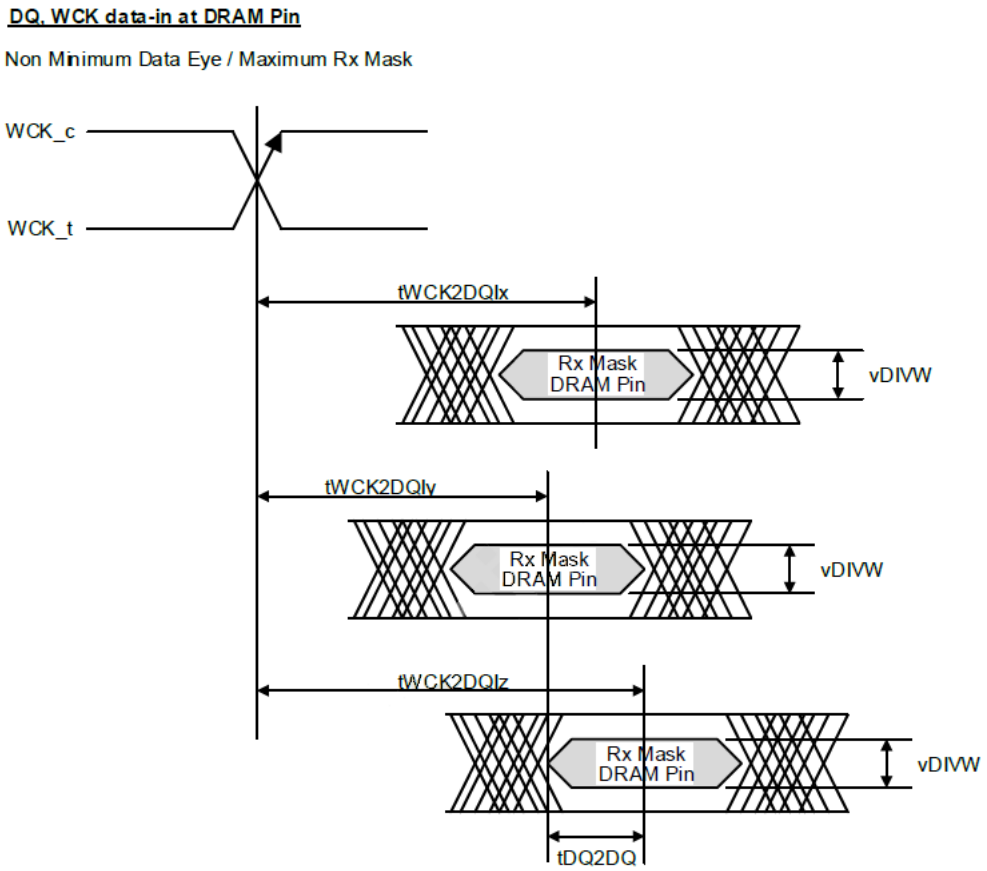

Figure 95 Identifying DQ Rx Mask parameters with respect to WCK

DQ Rx Voltage and Timing (WRITE) tests

tDIVW1 Margin

Availability Condition: **Table 219 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 220 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tDIVW1	141000	Table 355

Overview: The purpose of this test is to measure the minimum tDIVW1 Margin of the WRITE eye diagram generated.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid WCK input test signals by verifying its frequency and amplitude values.

3 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the WCKx channel input.

c Set up fixed vertical scale values for DQx channel and WCKx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered WCK, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

5 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select ‘WidestOpening’ to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the tDIVW1 Margin value for both corners of the Test Mask.
The tDIVW1 Margin for each Test Mask corner is denoted by tDIVW1_m1 and tDIVW1_m2.

8 Find the minimum value between tDIVW1_m1 and tDIVW1_m2. Use the minimum value as the worst time gap.

9 Calculate the margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_time\_gap}) / (\text{Half of mask width})] \times 100\%$$

where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2.

10 Report the worst time gap and margin percentage as test results.

Expected/ Observable Results: The measured tDIVW1 Margin value for the test signal indicates if there is a violation in the mask region.

tDIVW2 Margin

Availability Condition: **Table 221 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 222 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tDIVW2	141001	Table 355

Overview: The purpose of this test is to measure the minimum tDIVW2 Margin of the WRITE eye diagram generated.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid WCK input test signals by verifying its frequency and amplitude values.

3 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
   b Set up measurement threshold values for the DQx channel and the WCKx channel input.
   c Set up fixed vertical scale values for DQx channel and WCKx channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test.
   f Set up Clock Recovery on SDA.

   : Explicit clock, Source = filtered WCK, Rise/Fall Edge
   g Set the Real Time Eye on SDA to ON.
4 Perform Mask Testing:
   a Set the Mask Test Run Until setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
5 Determine and store the Vcent value. To determine the value of Vcent:
   a In the Configure tab of the Test Application, choose Mode as Debug.
   b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
   - Select 'WidestOpening' to use the widest eye opening as vCENT.
   - Select a positive value greater than 0 to specify vCENT.

   To obtain the vCENT value with 'WidestOpening' selected:
      i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
      ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
      iii Use the voltage level at the widest eye opening as the value for Vcent.
6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
7 Use the Histogram feature in the Infiniium Application to measure the tDIVW2 Margin value for all the four corners of the Test Mask.
   The tDIVW2 Margin for each Test Mask corner is denoted by tDIVW2_m1, tDIVW2_m2, tDIVW2_m3 and tDIVW2_m4.
8 Find the minimum value between tDIVW2_m1, tDIVW2_m2, tDIVW2_m3 and tDIVW2_m4. Use the minimum value as the worst time gap.
9 Calculate the margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_time\_gap}) / (\text{Half of mask width})] \times 100\%$$

   where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.
10 Report the worst time gap and margin percentage as test results.

Expected/ Observable Results: The measured tDIVW2 Margin value for the test signal indicates if there is a violation in the mask region.

vDIVW Margin

Availability Condition: **Table 223 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 224 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
vDIVW	141002	Table 355

Overview: The purpose of this test is to measure the minimum vDIVW Margin of the WRITE eye diagram generated.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid WCK input test signals by verifying its frequency and amplitude values.

3 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the WCKx channel input.

c Set up fixed vertical scale values for DQx channel and WCKx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered WCK, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

5 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select ‘WidestOpening’ to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the vDIVW Margin value for the top and the bottom area of the Test Mask.
The measured vDIVW margin is denoted as vDIVW Margin upper and vDIVW Margin lower.

8 Find the minimum value between vDIVW Margin Upper and vDIVW Margin lower. Use this value as the worst voltage gap.

9 Calculate the worst margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_voltage\_gap}) / (\text{Half of mask height})] \times 100\%$$

where, Worst_voltage_gap is the voltage gap between the mask and the eye at the top and bottom.

10 Report the worst voltage gap and the margin percentage as test results.

Expected/ Observable Results: The measured value of vDIVW Margin for the test signal indicates if there is a violation in the mask region.

tDIPW

Availability Condition:

Table 225 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References:

Table 226 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tDIPW	141003	Table 355

Overview: The purpose of this test is to verify the minimum input DQ Rx pulse width defined at the Vcent_DQ.

Procedure:

1 This test requires the following pre-requisite test:

- tDIVW1 Margin (Test ID: 141000)

  Location for Vcent is determined and its value is stored.

2 Acquire and identify the READ and WRITE burst data of the acquired signal.

3 Use all valid WRITE bursts that are found to perform TDIPW measurement.

4 Find all valid rising and falling DQ edges, which are defined as the crossings at Vcent in the WRITE data burst.

5 Measure tDIPW as the time starting from a rising/falling edge of the DQ to the time ending at the following falling/rising edge.

6 Process all valid edges in the WRITE data burst.
7 Collect all tDIPW.
8 Determine the worst result from the set of tDIPW values measured and report it as the final test result.

Expected/ Observable Results: The measured value of tDIPW for the test signal shall be within the conformance limit as per the JESD209-5 specification.

tDIHL

Availability Condition: **Table 227 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 228 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tDIHL	141004	Table 355

Overview: The purpose of this test is to verify the minimum input DQ Rx pulse width above and below vDIVW defined at the Vcent_DQ.

Procedure:
1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
2 Check for valid WCK input test signals by verifying its frequency and amplitude values.
3 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.
   b Set up measurement threshold values for the DQx channel and the WCKx channel input.
   c Set up fixed vertical scale values for DQx channel and WCKx channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test.
   f Set up Clock Recovery on SDA.
   : Explicit clock, Source = filtered WCK, Rise/Fall Edge
   g Set the Real Time Eye on SDA to ON.
4 Perform Mask Testing:
   a Set the Mask Test Run Until setting to ‘Forever’.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.
5 Determine and store the Vcent value. To determine the value of Vcent:
   a In the Configure tab of the Test Application, choose Mode as Debug.
   b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature to measure the width of the eye opening at the top and bottom of the mask.

8 The worst value of the width obtained between the top and bottom is reported as tDIHL.

Expected/ Observable Results: The measured value of tDIHL for the test signal shall be within the conformance limit as per the JESD209-5 specification.

vDIHL_AC

Availability Condition: **Table 229 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 230 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
VDIHL_AC	141005	Table 355

Overview: The purpose of this test is to measure the DQ single input pulse amplitude vDIHL_AC that the pulse must meet or exceed at any point over the total UI.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid WCK input test signals by verifying its frequency and amplitude values.

3 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the WCKx channel input.

c Set up fixed vertical scale values for DQx channel and WCKx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered WCK, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

4 Perform Mask Testing:
   a Set the Mask Test Run Until setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
5 Determine and store the Vcent value. To determine the value of Vcent:
   a In the Configure tab of the Test Application, choose Mode as Debug.
   b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.
   - Select 'WidestOpening' to use the widest eye opening as vCENT.
   - Select a positive value greater than 0 to specify vCENT.

   To obtain the vCENT value with 'WidestOpening' selected:
      i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
      ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
      iii Use the voltage level at the widest eye opening as the value for Vcent.
6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
7 Use the Histogram feature in the Infiniium Application to measure the vDIHL_AC/2 values for the top and the bottom area of the Test Mask.
   The measured vDIHL_AC/2 values is denoted as vDIHL_AC/2_top and vDIHL_AC/2_bottom.
8 Calculate vDIHL_AC using the equation:

$$vDIHL\_AC = [vDIHL\_AC/2\_top] - [vDIHL\_AC/2\_bottom]$$

9 Report the measured vDIHL_AC as test result.

Expected/ Observable Results: The measured value of vDIHL_AC for the test signal shall be within the conformance limit as per the JESD209-5 specification.

tWCK2DQI_HF

Availability Condition: **Table 231 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 232 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCK2DQI_HF	141007	Table 301

Overview: The purpose of this test is to verify the offset between the WCK signal and the start of DQ input pulse / DQ input Rx mask.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid WCK input test signals by verifying its frequency and amplitude values.

3 Set up the oscilloscope:

a Using UDF methodology, separate Write burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the WCKx channel input.

c Set up fixed vertical scale values for DQx channel and WCKx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered WCK, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

4 Realign the eye opening of the first transition DQ bit to the center of the screen:

a Increase the search range on the screen to the range specified in the 'First DQ Transition Search Range (ps)' configuration option in the Configure tab, so that the crossing point of the eye is visible on the screen.

b Use the Histogram feature to find the first crossing point at 'VRefDQ' level horizontally across the screen.

c Realign the center of the eye to the middle time position.

NOTE If the Test Application is unable to find any cross point within the search range, it prompts an error and this test run is aborted.

5 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

6 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

8 Find the mid-point in time at the Vcent level of the eye diagram and denote it as EyeCenterLoc.

9 Determine the location of the filtered WCK rising edges used in the recovered clock and denote it as FilteredWCKLoc.

10 Compute the final test result using the equation:

tWCK2DQI_HF = EyeCenterLoc - FilteredWCKLoc

11 Determine the worst result from the set of tWCK2DQI_HF values measured and report it as the final test result.

Expected/ Observable Results: The measured value of tWCK2DQI_HF for the test signal is considered for 'Information-Only' purpose.

DQ Rx Voltage and Timing (READ) tests

tQW

Availability Condition: **Table 233 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	Yes	Yes	CK(Diff), DQ, RDQS(Diff)

Test ID & References: **Table 234 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tQW	140000	Note: No pass limits defined. However, a Read eye diagram formation indicates that the test has passed.

Overview: The purpose of this test is to verify the tQW parameter by measuring the DQ Read Eye.

Procedure:

1 Calculate initial time scale value based on selected LPDDR5 speed grade options.
2 Check for valid RDQS input test signals by verifying its frequency and amplitude values.
3 Set up the oscilloscope:
   a Using UDF methodology, separate Write burst and return the filtered RDQS signals as recovered clock for eye folding later.
   b Set up measurement threshold values for the DQ channel and the RDQS channel input.
   c Set up vertical scale values for DQ channel and RDQS channel input.
   d Set Color Grade Display option to ON.
   e Set up Mask Test settings.
   f Set up Clock Recovery settings on SDA.

   : Explicit clock, Source = filtered RDQS, Rise/Fall Edge
   g Set Real Time Eye on SDA to ON.
4 Perform Mask Testing:
   a Set the Mask Test Run setting to ‘Forever’.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.
5 Measure the Eye Height and Eye Width.
6 Report the measured Eye Height and Eye Width.

Expected/ Observable Results: The measured tQW value for the test signal is considered for ‘Information-Only’ purpose.

tWCK2DQO_HF

Availability Condition: **Table 235 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	Burst only	No	Yes	Yes	CK(Diff), WCK(Diff), DQ

Test ID & References: **Table 236 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tWCK2DQO_HF	140007	Table 301

Overview: The purpose of this test is to verify the offset between the WCK signal and the start of DQ output pulse / DQ output Rx mask.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid WCK input test signals by verifying its frequency and amplitude values.

3 Set up the oscilloscope:

a Using UDF methodology, separate Read burst and return the filtered WCK signals as Recovered Clock, which is used for eye folding later.

b Set up measurement threshold values for the DQx channel and the WCKx channel input.

c Set up fixed vertical scale values for DQx channel and WCKx channel input.

d Set the Color Grade Display option to ON.

e Set up Mask Test.

f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered WCK, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

4 Realign the eye opening of the first transition DQ bit to the center of the screen:

a Increase the search range on the screen to the range specified in the 'First DQ Transition Search Range (ps)' configuration option in the Configure tab, so that the crossing point of the eye is visible on the screen.

b Use the Histogram feature to find the first crossing point at 'VRefDQ' level horizontally across the screen.

c Realign the center of the eye to the middle time position.

NOTE If the Test Application is unable to find any cross point within the search range, it prompts an error and this test run is aborted.

5 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

6 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to DQ Rx Voltage and Timing tests > WRITE > vCENT DQ mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

7 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

8 Find the mid-point in time at the Vcent level of the eye diagram and denote it as EyeCenterLoc.

9 Determine the location of the filtered WCK rising edges used in the recovered clock and denote it as FilteredWCKLoc.

10 Compute the final test result using the equation:

tWCK2DQO_HF = EyeCenterLoc - FilteredWCKLoc

11 Determine the worst result from the set of tWCK2DQO_HF values measured and report it as the final test result.

Expected/ Observable Results: The measured value of tWCK2DQO_HF for the test signal is considered for 'Information-Only' purpose.

References for CA Rx Voltage and Timing tests

LPDDR5 command and address interface operates from a differential clock (CK_t and CK_c). Commands and addresses are registered single data rate (SDR) at every rising edge of CK. Chip Select (CS) is part of the command code, and is sampled on the rising(falling) edge of CK_t (CK_c). The Read/Write command behavior depends on the bank architecture. The READ and WRITE commands are each initiated with CS, and CA[6:0] asserted to the proper state at the rising and falling edges of CK, as defined by the Command Truth Table (refer to *Table 154* of the *JESD209-5* specification). Command/Address ODT (On-Die Termination) is a feature of the LPDDR5 SDRAM that allows the SDRAM to turn on/off termination resistance for CK_t, CK_c, and CA[6:0] signals.

LPDDR5 CA Rx mask is defined as hexagonal mask shape as shown in Figure 96. All CA signals apply the same compliance mask and operate in double data rate mode. The receiver mask (Rx Mask vCIVW, tCIVW1, tCIVW2) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal. CA Rx mask window center is around CK_t/CK_c cross point (differential mode). Rx mask voltage vCIVWl(max) has to be centered around VrefCA. CA single input pulse signal amplitude into the receiver has to meet or exceed vCIHL_AC at any point over the total UI. vCIHL_AC is the peak to peak voltage centered around VrefCA such that vCIHL_AC/2 min has to be met both above and below VrefCA. vCIHL_AC does not have to be met when no transitions are occurring. tCA2CA is defined fastest CA[x] mask center to slowest CA[y] mask center.

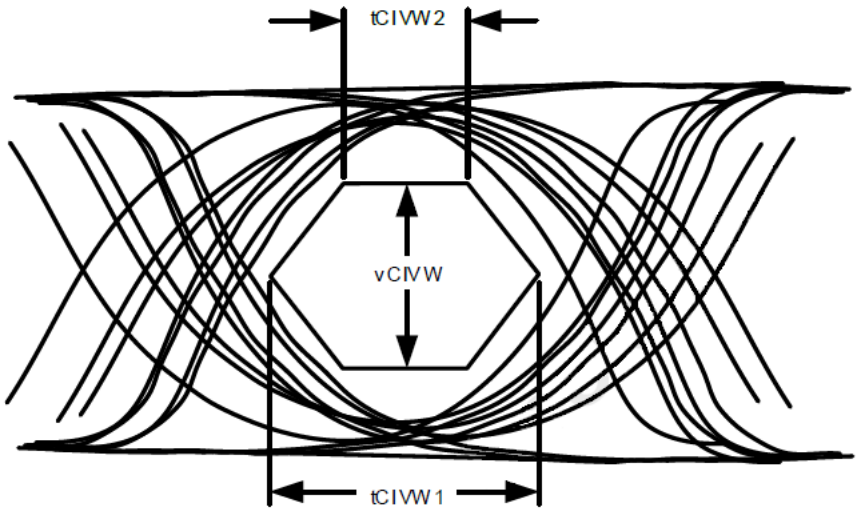

Figure 96 CA Rx Mask Defintion

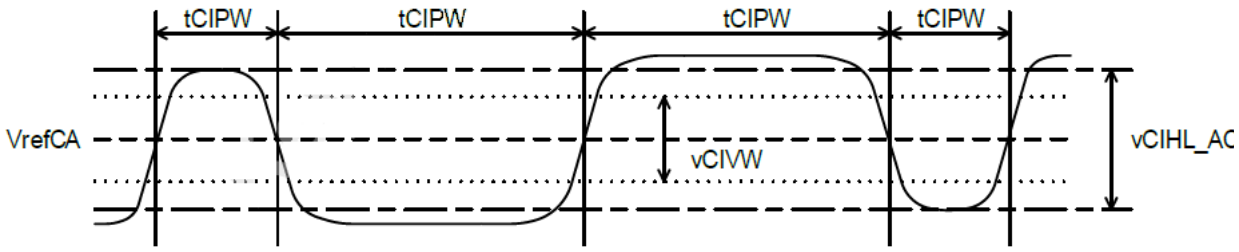

Figure 97 Identifying CA Rx Mask parameters with respect to VrefCA

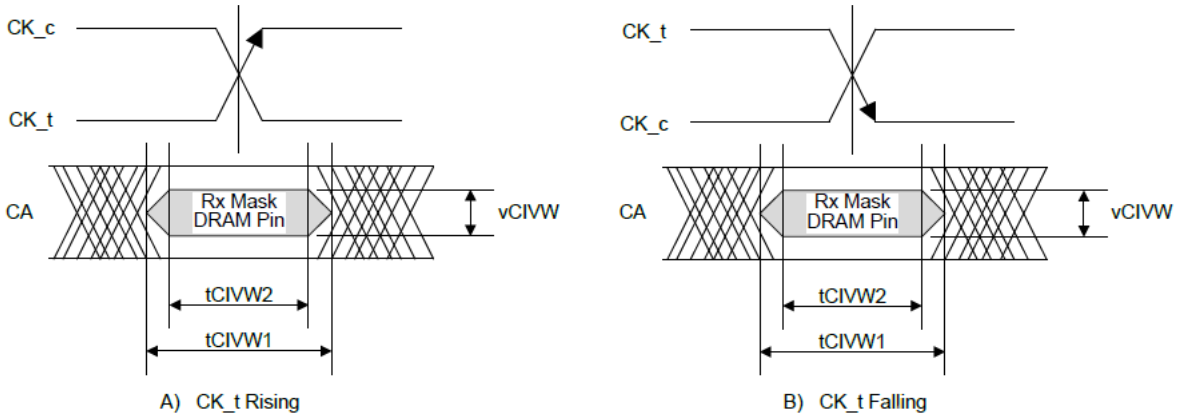

Figure 98 Identifying CA Rx Mask parameters with respect to CK

CA Rx Voltage and Timing tests

tCIVW1 Margin

Availability Condition: **Table 237 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References: **Table 238 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCIVW1	142001	Table 354

Overview: The purpose of this test is to measure the minimum tCIVW1 Margin of the CA eye diagram generated.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CA input test signals by verifying its frequency and amplitude values.

3 On the Oscilloscope:

a Set the Trigger to ‘Auto-Sweep’.

b Set the Sampling Rate of the Oscilloscope to the maximum value.

c Set the Sampling Points to the user defined value configured for the ‘Sampling Points (Pts) for Eye Diagram Tests Only’ configuration option in the Configure tab of the Test Application.

d Set Function 1 to duplicate the CK signal.

e Set the Color Grade Display option to ON.

f Set up Mask Test settings.

g Set up Clock Recovery on SDA.

: Explicit clock, Source = Function 1, Rising Edge

h Set the Real Time Eye on SDA to ON.

i Set up measurement threshold values for Function 1 and CA input signals.

j Change Trigger Source to ‘CA input signal’ on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

5 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the tCIVW1 Margin value for both corners of the Test Mask.
The tCIVW1 Margin for each Test Mask corner is denoted by tCIVW1_m1 and tCIVW1_m2.

8 Find the minimum value between tCIVW1_m1 and tCIVW1_m2. Use the minimum value as the worst time gap.

9 Calculate the margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_time\_gap}) / (\text{Half of mask width})] \times 100\%$$

where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2.

10 Report the worst time gap and margin percentage as test results.

Expected/ Observable Results: The measured tCIVW1 Margin value for the test signal indicates if there is a violation in the mask region.

tCIVW2 Margin

Availability Condition: **Table 239 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References: **Table 240 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCIVW2	142002	Table 354

Overview: The purpose of this test is to measure the minimum tCIVW2 Margin of the CA eye diagram generated.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CA input test signals by verifying its frequency and amplitude values.

3 On the Oscilloscope:
   a Set the Trigger to 'Auto-Sweep'.
   b Set the Sampling Rate of the Oscilloscope to the maximum value.
   c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.
   d Set Function 1 to duplicate the CK signal.
   e Set the Color Grade Display option to ON.
   f Set up Mask Test settings.
   g Set up Clock Recovery on SDA.
   : Explicit clock, Source = Function 1, Rising Edge
   h Set the Real Time Eye on SDA to ON.
   i Set up measurement threshold values for Function 1 and CA input signals.
   j Change Trigger Source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.
4 Perform Mask Testing:
   a Set the Mask Test Run Until setting to 'Forever'.
   b Load the mask file and start the Mask Test.
   c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.
5 Determine and store the Vcent value. To determine the value of Vcent:
   a In the Configure tab of the Test Application, choose Mode as Debug.
   b Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.
   - Select 'WidestOpening' to use the widest eye opening as vCENT.
   - Select a positive value greater than 0 to specify vCENT.

   To obtain the vCENT value with 'WidestOpening' selected:
      i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).
      ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.
      iii Use the voltage level at the widest eye opening as the value for Vcent.
6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.
7 Use the Histogram feature in the Infiniium Application to measure the tCIVW2 Margin value for all the four corners of the Test Mask.
   The tCIVW2 Margin for each Test Mask corner is denoted by tCIVW2_m1, tCIVW2_m2, tCIVW2_m3 and tCIVW2_m4.
8 Find the minimum value between tCIVW2_m1, tCIVW2_m2, tCIVW2_m3 and tCIVW2_m4. Use the minimum value as the worst time gap.
9 Calculate the margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_time\_gap}) / (\text{Half of mask width})] \times 100\%$$

   where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.
10 Report the worst time gap and margin percentage as test results.

Expected/ Observable Results: The measured tCIVW2 Margin value for the test signal indicates if there is a violation in the mask region.

vCIVW Margin

Availability Condition: **Table 241 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References: **Table 242 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
vCIVW	142003	Table 354

Overview: The purpose of this test is to measure the minimum vCIVW Margin of the CA eye diagram generated.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CA input test signals by verifying its frequency and amplitude values.

3 On the Oscilloscope:

a Set the Trigger to 'Auto-Sweep'.

b Set the Sampling Rate of the Oscilloscope to the maximum value.

c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.

d Set Function 1 to duplicate the CK signal.

e Set the Color Grade Display option to ON.

f Set up Mask Test settings.

g Set up Clock Recovery on SDA.

: Explicit clock, Source = Function 1, Rising Edge

h Set the Real Time Eye on SDA to ON.

i Set up measurement threshold values for Function 1 and CA input signals.

j Change Trigger Source to 'CA input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

5 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the vCIVW Margin value for the top and the bottom area of the Test Mask.
The measured vCIVW margin is denoted as vCIVW Margin upper and vCIVW Margin lower.

8 Find the minimum value between vCIVW Margin Upper and vCIVW Margin lower. Use this value as the worst voltage gap.

9 Calculate the worst margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_voltage\_gap}) / (\text{Half of mask height})] \times 100\%$$

where, Worst_voltage_gap is the voltage gap between the mask and the eye at the top and bottom.

10 Report the worst voltage gap and the margin percentage as test results.

Expected/ Observable Results: The measured value of vCIVW Margin for the test signal indicates if there is a violation in the mask region.

tCIPW

Availability Condition:

Table 243 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References:

Table 244 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tCIPW	142004	Table 354

Overview: The purpose of this test is to verify the minimum input CA Rx pulse width defined at the Vcent_CA.

Procedure: 1 This test requires the following pre-requisite test:

- tCIVW1 Margin (Test ID: 142001)
  Location for Vcent is determined and its value is stored.

2 Perform the pulse width on the CA signal:
   a Set to ON the positive pulse width measurement and jitter statistics to measure all the edges.
   b Set the measurement threshold to a hysteresis of ± CA mask height at the threshold level of Vcent_CA.
   c Obtain the minimum result from the measurements as the worst positive pulse width.
   d Repeat steps a to c for negative pulse width and store the minimum result from the measurement as the worst negative pulse width.
3 Compare the minimum values from the positive and negative pulse width results.
4 Measure tDIPW as the time starting from a rising/falling edge of the CA signal to the time ending at the following falling/rising edge.
5 Capture all values of tCIPW.
6 Convert the unit for the values from seconds to UI.
7 Determine the worst result from the set of tCIPW values measured and report it as the final test result.

Expected/ Observable Results: The measured value of tCIPW for the test signal shall be within the conformance limit as per the JESD209-5 specification.

vCIHL_AC

Availability Condition: **Table 245 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA

Test ID & References: **Table 246 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
vCIHL_AC	142005	Table 354

Overview: The purpose of this test is to measure the CA single input pulse amplitude vCIHL_AC that the pulse must meet or exceed at any point over the total UI.

Procedure:
1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
2 Check for valid Clock (CK) and CA input test signals by verifying its frequency and amplitude values.
3 Set up the oscilloscope:
   a Set the Trigger to 'Auto-Sweep'.
   b Set up measurement threshold values for the CAx channel and the CKx channel input.
   c Set up fixed vertical scale values for CAx channel and CKx channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test.
   f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered CK, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

5 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the vCIHL_AC/2 values for the top and the bottom area of the Test Mask.
The measured vCIHL_AC/2 values is denoted as vCIHL_AC/2_top and vCIHL_AC/2_bottom.

8 Calculate vCIHL_AC using the equation:

vCIHL_AC = [vCIHL_AC/2_top] - [vCIHL_AC/2_bottom]

9 Report the measured vCIHL_AC as test result.

Expected/ Observable Results: The measured value of vCIHL_AC for the test signal shall be within the conformance limit as per the JESD209-5 specification.

tCA2CA

Availability Condition:

Table 247 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CA[x], CA[y]

Test ID & References:

Table 248 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tCA2CA	142000	Table 354

Overview: The purpose of this test is to verify the mask offset between the fastest CA[x] mask center to the slowest CA[y] mask center.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK), CA[x] and CA[y] input test signals by verifying its frequency and amplitude values.

3 On the Oscilloscope:

a Set the Trigger to 'Auto-Sweep'.

b Set the Sampling Rate of the Oscilloscope to the maximum value.

c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.

d Enable CK, CA[x] and CA[y] source channels.

e Set the Color Grade Display option to ON.

f Set up Mask Test settings.

g Set up Clock Recovery on SDA.

: Explicit clock, Source = CK source channel, Rising Edge

h Set the Real Time Eye on SDA to ON.

i Set up measurement threshold values for CK, CA[x] & CA[y] input signals.

j Change Trigger Source to 'CA[x] input signal' and 'CA[y] input signal', respectively on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CA bus.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

5 Determine and store the Vcent values for CA[x] and CA[y]. To determine the value of Vcent, perform the following steps for each CA[x] and CA[y] input signals:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to CA Rx Voltage and Timing tests > vCENT CA mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[x] eye, find its midpoint. Denote this value as CA[x]_mid.

7 From the 'WidestOpening' or 'user-defined' Vcent determined for CA[y] eye, find its midpoint. Denote this value as CA[y]_mid.

8 Calculate tCA2CA using the equation:

tCA2CA = CA[x]_mid - CA[y]_mid

9 Report this difference as tCA2CA.

Expected/ Observable Results: The measured value of tCA2CA shall be within the conformance limits as per the JESD209-5 specification.

References for CS Rx Voltage and Timing tests

LPDDR5 CS Rx mask for Synchronous mode is defined as hexagonal mask shape as shown in Figure 219. CS signals apply the same compliance mask and operate in single data rate mode. The receiver mask (Rx Mask vCSIVW, tCSIVW1, tCSIVW2) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal.

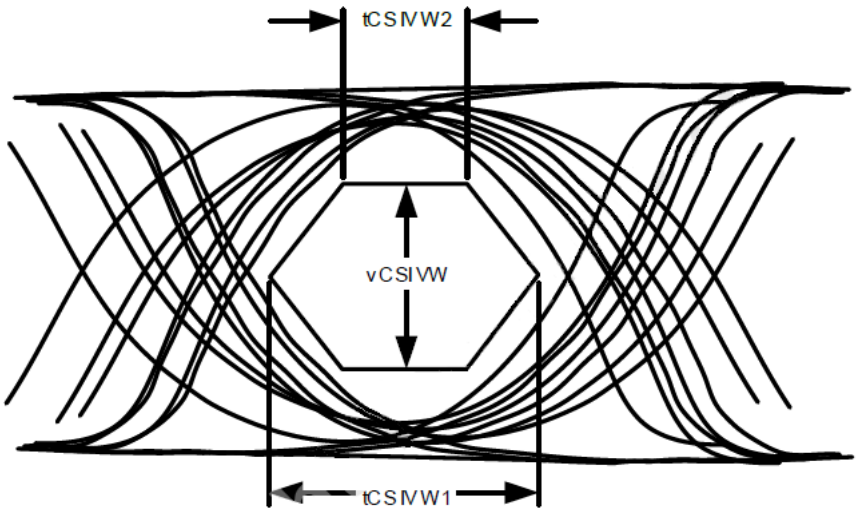

Figure 99 CS Rx Mask definition

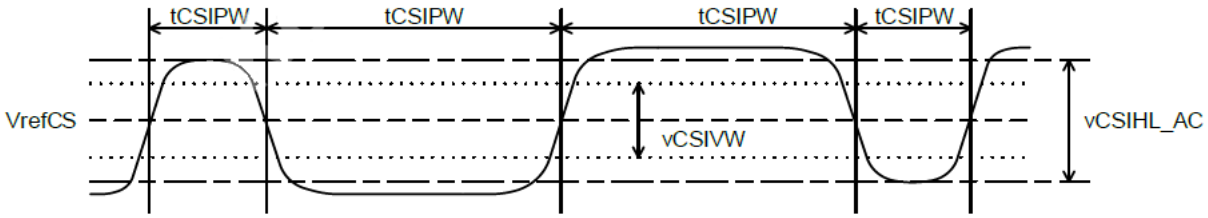

Figure 100 Identifying CS Rx Mask parameters with respect to VrefCS

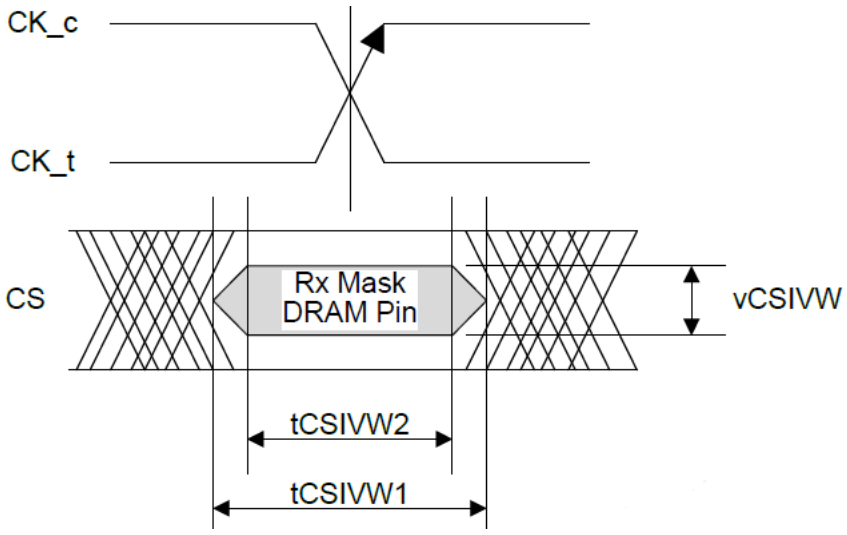

Figure 101 Identifying CS Rx Mask parameters with respect to CK

CS Rx Voltage and Timing tests

tCSIVW1 Margin

Availability Condition: **Table 249 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References: **Table 250 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCSIVW1	142020	Table 353

Overview: The purpose of this test is to measure the minimum tCSIVW1 Margin of the CS eye diagram generated.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CS input test signals by verifying its frequency and amplitude values.

3 On the Oscilloscope:

a Set the Trigger to ‘Auto-Sweep’.

b Set the Sampling Rate of the Oscilloscope to the maximum value.

c Set the Sampling Points to the user defined value configured for the ‘Sampling Points (Pts) for Eye Diagram Tests Only’ configuration option in the Configure tab of the Test Application.

d Set Function 1 to duplicate the CK signal.

e Set the Color Grade Display option to ON.

f Set up Mask Test settings.

g Set up Clock Recovery on SDA.

: Explicit clock, Source = Function 1, Rising Edge

h Set the Real Time Eye on SDA to ON.

i Set up measurement threshold values for Function 1 and CS input signals.

j Change Trigger Source to ‘CS input signal’ on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CS bus.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to ‘Forever’.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for ‘Total Waveforms’ exceeds the number of required waveforms specified in the configuration option ‘Total Waveform’.

5 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to CS Rx Voltage and Timing tests > vCENT CS mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the tCSIVW1 Margin value for both corners of the Test Mask.
The tCSIVW1 Margin for each Test Mask corner is denoted by tCSIVW1_m1 and tCSIVW1_m2.

8 Find the minimum value between tCSIVW1_m1 and tCSIVW1_m2. Use the minimum value as the worst time gap.

9 Calculate the margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_time\_gap}) / (\text{Half of mask width})] \times 100\%$$

where, Worst_time_gap is the time gap between the mask and the eye at corners m1 and m2.

10 Report the worst time gap and margin percentage as test results.

Expected/ Observable Results: The measured tCSIVW1 Margin value for the test signal indicates if there is a violation in the mask region.

tCSIVW2 Margin

Availability Condition: **Table 251 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References: **Table 252 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
tCSIVW2	142021	Table 353

Overview: The purpose of this test is to measure the minimum tCSIVW2 Margin of the CS eye diagram generated.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CS input test signals by verifying its frequency and amplitude values.

3 On the Oscilloscope:

a Set the Trigger to 'Auto-Sweep'.

b Set the Sampling Rate of the Oscilloscope to the maximum value.

c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.

d Set Function 1 to duplicate the CK signal.

e Set the Color Grade Display option to ON.

f Set up Mask Test settings.

g Set up Clock Recovery on SDA.

: Explicit clock, Source = Function 1, Rising Edge

h Set the Real Time Eye on SDA to ON.

i Set up measurement threshold values for Function 1 and CS input signals.

j Change Trigger Source to 'CS input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CS bus.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

5 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to CS Rx Voltage and Timing tests > vCENT CS mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the tCSIVW2 Margin value for all the four corners of the Test Mask.
The tCSIVW2 Margin for each Test Mask corner is denoted by tCSIVW2_m1, tCSIVW2_m2, tCSIVW2_m3 and tCSIVW2_m4.

8 Find the minimum value between tCSIVW2_m1, tCSIVW2_m2, tCSIVW2_m3 and tCSIVW2_m4. Use the minimum value as the worst time gap.

9 Calculate the margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_time\_gap}) / (\text{Half of mask width})] \times 100\%$$

where, Worst_time_gap is the time gap between the mask and the eye at four corners m1, m2, m3, m4.

10 Report the worst time gap and margin percentage as test results.

Expected/ Observable Results: The measured tCSIVW2 Margin value for the test signal indicates if there is a violation in the mask region.

vCSIVW Margin

Availability Condition: **Table 253 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References: **Table 254 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
vCSIVW	142022	Table 353

Overview: The purpose of this test is to measure the minimum vCSIVW Margin of the CS eye diagram generated.

Procedure:

1 Calculate the initial time scale value based on selected speed grade options in the Test Application.

2 Check for valid Clock (CK) and CS input test signals by verifying its frequency and amplitude values.

3 On the Oscilloscope:

a Set the Trigger to 'Auto-Sweep'.

b Set the Sampling Rate of the Oscilloscope to the maximum value.

c Set the Sampling Points to the user defined value configured for the 'Sampling Points (Pts) for Eye Diagram Tests Only' configuration option in the Configure tab of the Test Application.

d Set Function 1 to duplicate the CK signal.

e Set the Color Grade Display option to ON.

f Set up Mask Test settings.

g Set up Clock Recovery on SDA.

: Explicit clock, Source = Function 1, Rising Edge

h Set the Real Time Eye on SDA to ON.

i Set up measurement threshold values for Function 1 and CS input signals.

j Change Trigger Source to 'CS input signal' on both Rising/Falling Edges to prevent timeout for such cases, when there is less activity on CS bus.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

5 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to CS Rx Voltage and Timing tests > vCENT CS mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the vCSIVW Margin value for the top and the bottom area of the Test Mask.
The measured vCIVW margin is denoted as vCSIVW Margin upper and vCSIVW Margin lower.

8 Find the minimum value between vCSIVW Margin Upper and vCSIVW Margin lower. Use this value as the worst voltage gap.

9 Calculate the worst margin (in percentage) using the equation:

$$\text{Margin (\%)} = [(\text{Worst\_voltage\_gap}) / (\text{Half of mask height})] \times 100\%$$

where, Worst_voltage_gap is the voltage gap between the mask and the eye at the top and bottom.

10 Report the worst voltage gap and the margin percentage as test results.

Expected/ Observable Results: The measured value of vCSIVW Margin for the test signal indicates if there is a violation in the mask region.

tCSIPW

Availability Condition:

Table 255 Set Up tab options for availability of tests

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References:

Table 256 LPDDR5 Test References from JESD209-5 specification

Symbol (in Specification)	Test ID	Reference from Specification
tCSIPW	142023	Table 353

Overview: The purpose of this test is to verify the minimum input CS Rx pulse width defined at the Vcent_CS.

Procedure: 1 This test requires the following pre-requisite test:

- tCIVW1 Margin (Test ID: 142020)
  Location for Vcent is determined and its value is stored.

2 Perform the pulse width on the CS signal:
   a Set to ON the positive pulse width measurement and jitter statistics to measure all the edges.
   b Set the measurement threshold to a hysteresis of ±CS mask height at the threshold level of Vcent_CS.
   c Obtain the minimum result from the measurements as the worst positive pulse width.
   d Repeat steps a to c for negative pulse width and store the minimum result from the measurement as the worst negative pulse width.
3 Compare the minimum values from the positive and negative pulse width results.
4 Measure tDIPW as the time starting from a rising/falling edge of the CS signal to the time ending at the following falling/rising edge.
5 Capture all values of tCSIPW.
6 Convert the unit for the values from seconds to UI.
7 Determine the worst result from the set of tCSIPW values measured and report it as the final test result.

Expected/ Observable Results: The measured value of tCSIPW for the test signal shall be within the conformance limit as per the JESD209-5 specification.

vCSIHL_AC

Availability Condition: **Table 257 Set Up tab options for availability of tests**

Supported CK Type	Supported WCK Type	Supports Offline?	R/W Separation needed?	SE Mode?	Required Signals
Burst & Continuous	N/A	No	No	Yes	CK(Diff), CS

Test ID & References: **Table 258 LPDDR5 Test References from JESD209-5 specification**

Symbol (in Specification)	Test ID	Reference from Specification
vCSIHL_AC	142024	Table 353

Overview: The purpose of this test is to measure the CS single input pulse amplitude vCSIHL_AC that the pulse must meet or exceed at any point over the total UI.

Procedure:
1 Calculate the initial time scale value based on selected speed grade options in the Test Application.
2 Check for valid Clock (CK) and CS input test signals by verifying its frequency and amplitude values.
3 Set up the oscilloscope:
   a Set the Trigger to 'Auto-Sweep'.
   b Set up measurement threshold values for the CSx channel and the CKx channel input.
   c Set up fixed vertical scale values for CSx channel and CKx channel input.
   d Set the Color Grade Display option to ON.
   e Set up Mask Test.
   f Set up Clock Recovery on SDA.

: Explicit clock, Source = filtered CK, Rise/Fall Edge

g Set the Real Time Eye on SDA to ON.

4 Perform Mask Testing:

a Set the Mask Test Run Until setting to 'Forever'.

b Load the mask file and start the Mask Test.

c Stop the Mask Test when the counter for 'Total Waveforms' exceeds the number of required waveforms specified in the configuration option 'Total Waveform'.

5 Determine and store the Vcent value. To determine the value of Vcent:

a In the Configure tab of the Test Application, choose Mode as Debug.

b Under Eye Diagram Tests, navigate to CS Rx Voltage and Timing tests > vCENT CS mode (V). This is the level, where the vertical center of the Eye Mask is placed.

- Select 'WidestOpening' to use the widest eye opening as vCENT.
- Select a positive value greater than 0 to specify vCENT.

To obtain the vCENT value with 'WidestOpening' selected:

i The Vcent level search range is from 40% to 60% of the eye amplitude (that is, the eye height measured at the center of the eye diagram).

ii Scan for the widest eye opening at the mentioned search range with a scan resolution of 5mV.

iii Use the voltage level at the widest eye opening as the value for Vcent.

6 Reposition the Test Mask so that it is centered on the Vcent value with the Test Mask width and height set in the Configure tab.

7 Use the Histogram feature in the Infiniium Application to measure the vCSIHL_AC/2 values for the top and the bottom area of the Test Mask.
The measured vCSIHL_AC/2 values is denoted as vCSIHL_AC/2_top and vCSIHL_AC/2_bottom.

8 Calculate vCSIHL_AC using the equation:

$$vCSIHL\_AC = [vCSIHL\_AC/2\_top] - [vCSIHL\_AC/2\_bottom]$$

9 Report the measured vCSIHL_AC as test result.

Expected/ Observable Results: The measured value of vCSIHL_AC for the test signal shall be within the conformance limit as per the JESD209-5 specification.