Overcoming Challenges Characterizing High Speed Power Semiconductors

Introduction

Having trouble obtaining consistent results from your Double-Pulse Test (DPT) setup? You are not alone. As the switching frequency of switch-mode power converters increase into the MHz range, rise/fall times are dropping to 10ns or even single digits of nanoseconds. It is no longer possible to design & measure power converter performance without considering high frequency effects. This article discusses DPT fixture design to obtain repeatable and reliable results from your DPT setup.
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International Electrotechnical Commission (IEC) and JEDEC standards have existed for decades, defining tests to dynamically characterize power semiconductors. The DPT setup is the industry standard used for measuring and extracting most of the key dynamic parameters to characterize these devices (Figure 1).

To investigate the reason for more difficulty in making DPT measurements with faster switching devices, let’s refresh our memory of the mathematical relationship between rise time and bandwidth.

The basic formula relating the bandwidth of a pulse waveform to its rise time is:

\[ f_{\text{rise}} \approx \frac{K}{f_{\text{rise}}} \quad [1] \]

Where:
- \( f_{\text{rise}} \) = pulse rise time (10% – 90%)
- \( f_{\text{rise}} \) = 3 dB bandwidth
- \( K \) = constant of proportionality depending on pulse shape (assume 0.35 for single pole exponential decay)

For determining the impact of the parts of the DPT measurement system (e.g. scope, probe, fixture, and DUT), we use the following formula to determine the risetime that would be displayed on the oscilloscope:

\[ t_{\text{displayed}} = \sqrt{t_{\text{DUT}}^2 + t_{\text{fixture}}^2 + t_{\text{probe}}^2 + t_{\text{scope}}^2} \quad [1] \]

Armed with these relationships, let’s compare two scenarios to illustrate the change in expectation for high frequency consideration.

Scenario #1: Analyze the impact of a 10 kHz switching waveform from a Si power MOSFET with 0.2 \( \mu \)s rise times. Because mid-range oscilloscope bandwidths are typically 500 MHz or more and their associated voltage probes can have bandwidths of 300 MHz, let’s assume these common bandwidths for this scenario. Let’s also assume that DPT fixture was designed with low frequency considerations and provides a 20 MHz bandwidth.

\[ t_{\text{displayed}} = \sqrt{1 \times 10^{-6}^2 + \left( \frac{0.35}{300,000,000} \right)^2 + \left( \frac{0.35}{500,000,000} \right)^2 + \left( \frac{0.35}{500,000,000} \right)^2} \]

\[ t_{\text{displayed}} = 0.2008 \times 10^{-6} \text{ sec} \]

Result: The displayed value on the oscilloscope is very close (< 1% error) to the actual rise time of the MOSFET, with little to no impact from the DPT fixture, probe or oscilloscope.
Scenario #2: Analyze the impact of a 250 kHz switching waveform from a SiC power MOSFET with 10 ns rise times. Let’s assume the same situation above for the oscilloscope (BW = 500 MHz), voltage probe (BW = 300 MHz), and the DPT fixture (BW = 20 MHz).

\[ t_{\text{displayed}} = \sqrt{(10 \times 10^{12})^2 + \left( \frac{0.35}{200,000,000} \right)^2 + \left( \frac{0.35}{500,000,000} \right)^2 + \left( \frac{0.35}{500,000,000} \right)^2} \]

\[ t_{\text{displayed}} = 20.2 \times 10^{-9} \text{ sec} \]

Result: The displayed value on the oscilloscope has slightly more than a 100% error! Let’s run scenario #2 again with a DPT fixture designed for a 200 MHz BW and see how much impact that will have on the result.

\[ t_{\text{displayed}} = \sqrt{(10 \times 10^{12})^2 + \left( \frac{0.35}{200,000,000} \right)^2 + \left( \frac{0.35}{200,000,000} \right)^2 + \left( \frac{0.35}{500,000,000} \right)^2} \]

\[ t_{\text{displayed}} = 10.2 \times 10^{-9} \text{ sec} \]

Result: The displayed value on the oscilloscope has only 2% error. This is a significant improvement in results by designing the fixture for a 200 MHz bandwidth.

Conclusion

Common instruments, like oscilloscopes, are more than capable to support the needs of a high speed DPT system. More significant challenges to provide repeatable and reliable results involve the design of the DPT fixture, including connection of the measurement probes.

NOTE: Because our analysis involves 2 poles, we must consider the relationship between rise time and bandwidth for second-order systems. Simple second-order circuit simulation was performed to approximate the ratio. The graphed result shows the rise time product to be close to 0.35 for (0.5 < \( \zeta < 1.0 \)). And for (0.05 < \( \zeta < 0.5 \)) the ratio only drops to ~0.27. Therefore, our conclusion remains valid for second-order systems. [2]

Considerations for DPT fixture design

Because of the faster rise/fall times (i.e. higher bandwidths) required for newer power semiconductors, analysis of the fixture layout and circuit parasitics are critical to provide repeatable and reliable DPT waveforms. If not, DPT waveforms often have second-order under-damped oscillations of the pulsed waveforms (\( V_{DS, V_{DS, I_{Q}}} \)), making it impossible to extract repeatable dynamic characterization parameters (e.g. \( \theta_{on}, \theta_{off} \)) (Figure 2).

**Figure 2:** Turn off pulses from a GaN device (\( V_{DS}=100V, I_{D}=10A, V_{GS}=12V \)).

Figure 3 shows the DPT setup with the primary parasitics capacitances, inductances, and resistances that need to be considered when designing your DPT fixture. Some of these parasitics are inherent in the power devices themselves (e.g. \( C_{off}, R_{f}, L_{j} \)). Power semiconductor manufacturers continue to develop new packaging materials and designs to minimize the stray parasitics. Once you determine your power semiconductor of choice, the focus is on external parasitics within the fixture.

Figure 3: Primary parasitics needing consideration during DPT switching transients.

There are three loops that are worth considering when analyzing the Double-Pulse waveforms (\( V_{DS}, V_{DS, I_{Q}} \)): the DC-Link Loop, the Gate Loop, and the Power Loop (Figure 3). As always, it is good practice to minimize the area of the loop, which is proportional to the total loop inductance. This can be done practically by routing PCB traces (main and return) close to each other, or by using twisting pairs, if routing the signals through wires.

The DC-Link Loop should be considered when the DC-Link Capacitor, that is charging the load inductor (I), is interrupted (i.e. when the DUT is turned off). When the DUT is turned off, the current charged up in L recirculates through the body diode in the high-side MOSFET. Therefore, there is no current coming from the DC-Link Capacitor and the DC-Link stray inductance (\( L_{DC\text{-}Link} \)) has a large -di/dt. \( L_{DC\text{-}Link} \) resonates with the Decoupling Capacitor in parallel with parasitic output capacitance from the half bridge, developing a voltage surge across \( V_{DC} \) and \( V_{DS} \). This resonant oscillation can be seen on \( V_{DS} \) in Figure 4 during both turn-off events. It can also be seen in Figure 2 as the lower frequency oscillation of \( V_{DS} \). It is next to impossible to eliminate this oscillation, but care needs to be taken to minimize it.

**Figure 4:** Double-Pulse Test Waveforms (SiC MOSFET, 1200V, 40A).
For the Gate Loop, the main parasitics you have control over in your fixture layout are $L_{GL}$ and $L_{PL2}$. It is often not possible to minimize this inductance enough to prevent oscillation, depending on the DUT’s gate resistance ($R_g$). If the oscillation still exists, then an external gate resistor $R_{Q}$ is required to dampen the oscillation to enable repeatable parameter extraction. Unfortunately, the trade-off in adding resistance to the gate, is a slower risetime of the gate voltage.

SiC geometries are typically much smaller than Si, and therefore often have larger internal gate resistance ($R_g$). So, it may not be necessary to add external gate resistance to some SiC devices to dampen the oscillation. While Si MOSFETs may require external dampening, because of the smaller $R_g$, one often finds many different gate resistor values used in DPT systems to accommodate the specific power device being characterized.

The Power Loop parasitics are another source of oscillation in $V_{DS}$ and $I_D$. After ramping the current to the desired value in $L$, during the first of the two pulses, the DUT is turned off. The current in $L$ is recirculated through the body diode. The $dV/dt$ in the power loop inductance ($L_{PL2}$) creates a voltage surge across the drain and source of the DUT. This voltage surge resonates with $C_{DS}$ of the DUT and the parasitic inductance of the Power Loop ($L_{PL1}$), creating a higher frequency oscillation that can be seen in $V_{DS}$ and $I_D$ in Figure 2. Although mechanisms are slightly different from turn-on, $L_{PL1}$ continues to be the key parasitic involved. Additionally, with WBG devices having low $R_{ON}$ values, damping of the Power Loop is minimal. Unfortunately, this often means limiting switching speeds to minimize oscillations.

There is one other mechanism that impacts the switching performance of the DUT. This mechanism is caused by the common parasitics ($C_{GD}$ and $L_{PL2}$) in both the Power Loop and the Gate Loop (Figure 5). For the high $dV/dt$ events (turn-on and turn-off), the common inductance $L_{PL2}$ creates a back EMF, which minimizes the effective $V_{DS}$ in the Gate Loop. It is sometimes possible to see the ringing of the power loop superimposed on the $V_{DS}$ due to this coupling (Figure 2). Similarly, the high $dI/dt$ events (turn-on and turn-off) create a displacement current in the Miller Capacitance ($C_{GD}$) diverting gate current intended to charge $C_{GD}$. This results in negatively impacts the effective $V_{DS}$ and the ability to quickly turn-on the DUT. Both effects impact the consistency and speed of the switching transition of the DUT.

![Figure 5: Power Loop parasitics minimizing Gate Loop drive.](image)

DPT fixture design is quite a challenge, and as we’ve seen, becomes significantly more difficult as risefall times continue to decrease. One needs to consider high frequency effects of multiple second-order circuits (loops) and is often limited in the ability to minimize parasitic inductances and capacitances. Fundamental technology barriers (e.g. low inductance interconnects) exist in designing and constructing DPT systems to characterize newer power semiconductors.

However, the Keysight PD1500A Dynamic Power Device Analyzer/Double-Pulse Tester was developed to solve these tough problems. The PD1500A is a complete DPT system designed for Si and SiC based discrete power semiconductors. The system was architected to be modular and upgradeable as the market evolves to higher voltages and frequencies. Keysight has plans for additional versions to characterize power modules, GaN devices, and to provide some reliability testing (Short Circuit, Avalanche). Just as you’ve come to expect from our B15056A Device Power Analyzers, the PD1500A provides repeatable and reliable results (see typical waveforms in Figure 4).

The PD1500A’s carefully engineered, modular fixture minimizes unwanted parasitics (Figure 6). Multiple gate driver options are provided with some standard resistor values, as well as an option for customer supplied resistors. DUT boards for TO-247 and SMD D2PAK-7 footprints and Si MOSFET, IGBT and SiC devices are also provided. Additional gate driver and DUT board options will be provided in the future.

![Figure 6: PD1500A DPT Modular fixture.](image)

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