CASE STUDY

KIOXIA Accelerates PDK Development by using Keysight Device Modeling Software

In a recent interview, Dr. Sadayuki Yoshitomi, Keysight Certified Expert (KCE), shared the challenges in high-speed NAND flash memory modeling and how KIOXIA accelerates PDK development by using Keysight's device modeling solution.

KIOXIA is a Japanese multinational flash memory manufacturer which spun off from Toshiba in 2018. The main products of KIOXIA are BiCS FLASH™ chips and solid-state drives (SSDs). Yoshitomi-san belongs to KIOXIA's memory development division and is responsible for developing Process Design Kits (PDKs). His team's goal is to provide high-quality PDKs to the design team who work on peripheral CMOS circuits, including logic and analog functional parts inside the memory chip.

In terms of NAND flash memory, the evolution of process technology is aggressive. The need for transistor scaling exceeds Moore's law. Yoshitomi-san's team has to complete the model extraction and PDK generation in a very limited time frame, usually only half the time spent for logic CMOS. Moreover, the IC speed continues to increase with the change from low-speed analog to high-speed CMOS technology. People have to consider the RF components and the increased number of acceptance criteria in PDK quality. Last but not least, Yoshitomi-san's team has to release the first PDK before the first silicon comes out. Releasing a predictive but accurate PDK to the designers is always a challenging task.

To tackle the above issues, Yoshitomi-san and his team established the link between TCAD simulation and SPICE model generation. They implemented a 3D calibration approach to include the high-speed characteristics, noise, and layout-dependent effects (LDEs) in, besides the conventional threshold voltage (Vth) and on-state current (Ion). After TCAD is developed, data flow from TCAD to SPICE modeling tools is also built.

Challenges:

- The very limited time frame for PDK development
- Modeling of the high-speed components
- Release a predictive but accurate model before the first silicon comes out

Solutions:

- Introduction of Design Technology Co-Optimization (DTCO) into PDK development
- End-to-end solution from Keysight

Results:

- 10X modeling efficiency improvement
- The number of modeling iteration is much less than before
- The model accuracy is improved in long-term prediction

KEYSIGHT TECHNOLOGIES

Yoshitomi-san and his team introduced Design Technology Co-Optimization (DTCO) process into the PDK development flow. DTCO here refers to the link between the mass production data and the SPICE model development flow. Iteration is the key part of the DTCO, besides test structure design and high volume measurement. They now have a total solution to access and analyze the big data and realize DTCO.

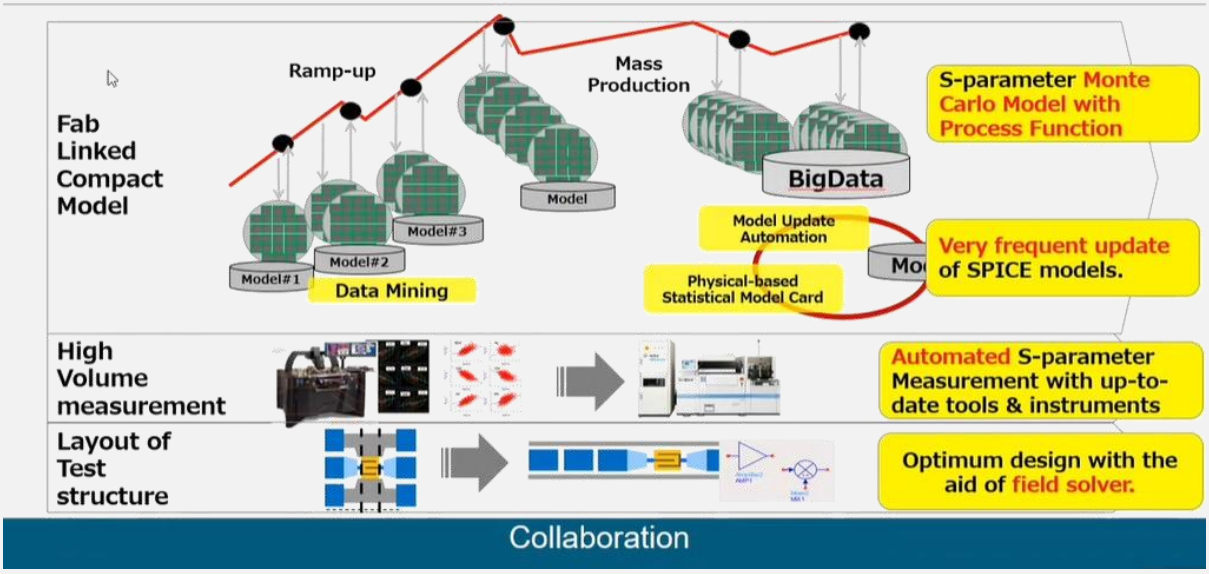

Figure 1. Process design kit (PDK) is Frequently updated by the incoming big data of the production line that cover both DC and RF figures of merit. The compact model should play a key role to directly combine between circuit designer and production

To enable DTCO, KIOXIA adopts the total solution from Keysight for modeling and PDK generation. They are PathWave Advanced Design System (ADS), PathWave WaferPro (WPE), PathWave Model Builder (MBP), PathWave Device Modeling (IC-CAP), PathWave Model QA (MQA), and Advanced Low-Frequency Noise Analyzer (A-LFNA).

ADS is used for the layout design of the test structures dedicated to the DTCO process. After the tape-out, WPE is used to perform the automated on-wafer measurement. “We have a way to collect a huge amount of S-parameter data which helps us to select the golden die of the AC performance. It is very helpful to have a very accurate SPICE model for high-speed circuit design.” said Yoshitomi-san. Next, MBP is used for typical and corner model generation together with WPE and IC-CAP's DataPro, to obtain good parameter fitting. The cycle time of parameter extraction has been improved a lot. IC-CAP is mainly used for the sub-circuit modeling to customized model extraction. “For the scalable model, IC-CAP is very helpful to incorporate LDEs in the compact model. IC-CAP gives modeling engineers more insight on the modeling process rather than simple parameter extraction.” Yoshitomi-san added. MQA is used to check the data consistency in the early measurement QA data stage and the quality of the model library in the later library QA stage.

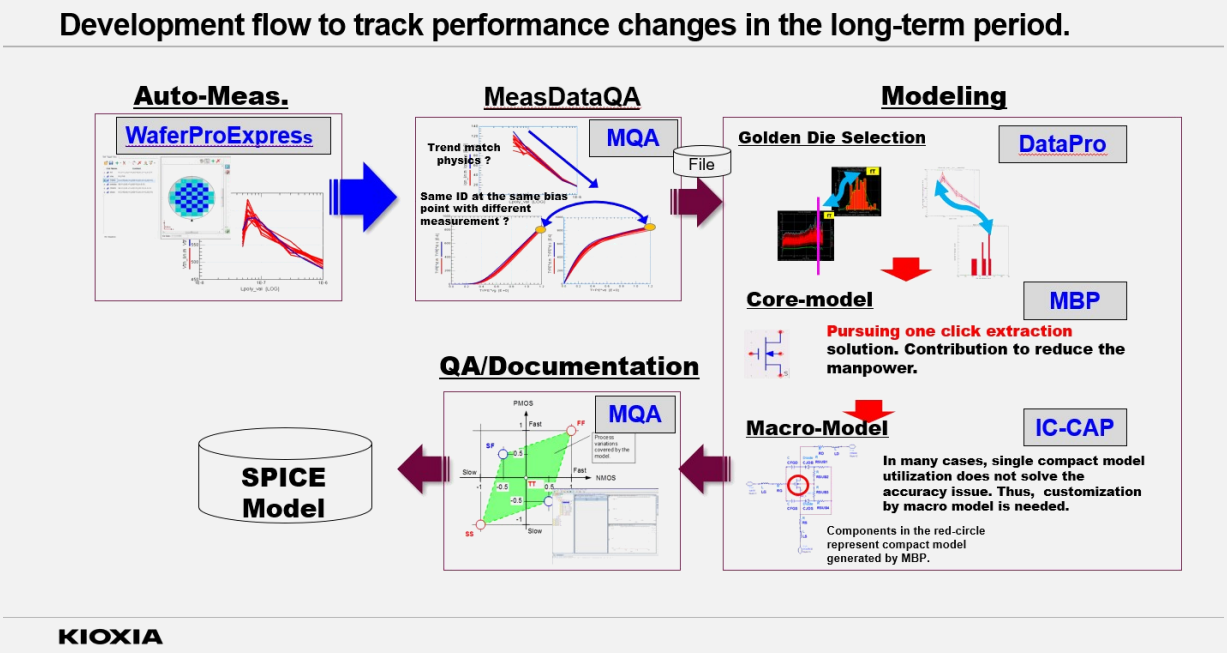

Figure 2. Development flow to track performance changes in a long term period by using Keysight device modeling solution

The characterization of low-frequency noise is also essential for BiCS FLASHTM development since the size of transistors used in the peripheral circuit is small, and the small transistors generate random telegraph noise (RTN). “Thanks to the new A-LFNA (E4727B), we are able to collect data with a large number of time steps. This is a great help to distinguish and visualize the RTN signal automatically.” said Yoshitomi-san.

As a result, the number of modeling iteration is much less than before. The time spent on measurement is reduced. And the seamless data flow from WPE and MBP helps to reduce the working hours. “The total modeling efficiency is improved 10X,” said Yoshitomi-san, “And in terms of long-term prediction, the model accuracy is much better than before.”

Reference

- Sadayuki Yoshitomi, RF CMOS Compact modelling technologies past and future, MOS-AK 2018 Q3 Meeting, 2018.
- Sadayuki Yoshitomi, Combination of Transistors' compact model and Big Data For successful Smart Factory, International Symposium on Devices, Circuits and Systems (ISDCS), 2020.

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