PathWave ADS Memory Designer
A complete design and test platform for next-generation memory

Challenges of Memory Design and Next-Generation Memory Standards

Have you spent hours setting up your memory simulations? Remember individually wiring each connection for an entire data bus?

Are you worried about the requirements of next-generation memory, such as DDR5, and LPDDR5?

Have you ever worried that crosstalk isn’t being captured accurately enough in your simulations?

Do you want to explore design constraints for your memory channel with vias and transmission lines, optimized for your substrate stack-up, early in your design cycle?

Designing a DDR memory system is already a very challenging and complicating task. It may take hours to setup your simulation, including wiring, setting up IBIS and channel models, as well as design parameters (if you are still using legacy tools and flows). As design margins continue to shrink, and complexity increases, the memory design workflow also need to evolve. With emerging new standards, such as DDR5/LPDDR5, there are new simulation requirements and methodologies to consider. DDR5, as an example, compared to previous generations of DDR standards, now requires equalization at the receiver. This brings the need for accurate IBIS-AMI models for the receiver. Additionally, since project timelines are now tighter than ever, it is essential to design your DDR system in the most predictive and productive manner, reaching design sign-off with the utmost confidence.

DDR5 and LPDDR5 are disruptive technologies:

- Data rate is increased to 3200 – 6400 MT/s (with a view to 8600 MT/s)
- Equalization (including CTLE and DFE) is utilized in both memory controller and DRAM to mitigate ISI (inter-symbol interference)
- Timing and voltage margins are specified at an extremely low BER
Simulation Workflows Need to Evolve for DDR5 and LPDDR5

1. Design Margins are Shrinking

As speed grades continue to increase, the unit intervals (UI) we need to work with are continuing to shrink. This leads to jitter eating up a greater portion of your design margin, and we need to carefully handle the cross talk to minimize eye closure. So much so, that at DDR5 speeds, after the long channel, looking at the package pins of the DRAM, the eye may be completely closed. Therefore, equalization to open the eye both at the driver and receiver may be unavoidable. Additionally, design specifications are becoming more bit error rate focused, moving away from traditional setup and hold timing measurements.

This means your simulation must predict eye closure due to random jitter all the way down to BER 1E-16 in a practical amount of simulation time.

2. Design Complexity is Increasing

With DDR5 and LPDDR5, it is the first time to have decision feedback equalization (DFE) on the DRAM. Traditionally, the DDR specification was at the balls of the DRAM package. With DDR5, probing at the package, the eye can be closed, meaning the receiver specification must move inside the die (after the equalizer). Typical equalization in memory systems are 3 tap pre-emphasis, feed forward equalization for the transmitter, and CTLE, VGA, and DFE for the receiver.

For an accurate prediction of signal integrity, IBIS-AMI models for single ended signals have emerged as a leading technology for DDR5/LPDDR5.

3. Project Timelines are Tighter than Ever

It is necessary to have a predictive and productive design flow to minimize the risk of design failure in the first prototype. By reducing design iterations, you can get your product to market as fast as possible.

Additionally, you can increase your confidence in the design sign-off by performing an automated DDR compliance test, powered by Keysight’s industry proven compliance test solutions and measurement science.

Keysight is the technology leader and has a complete DDR5 design and test workflow; your best partner to accelerate your project to success.
**DDR5 and LPDDR5 Jitter Tracking**

Since IBIS-AMI was developed for differential signaling, the first challenge for the adoption of AMI to DDR was how to handle single ended signaling. Additionally, the single ended DDR signals have asymmetric rising and falling edges as well as forwarded clocking. This common mode issue was resolved by IBIS BIRD 197.7 with the introduction of the new parameter, DC_Offset. The asymmetric edges in single ended signals is addressed accurately by applying two impulse responses for each rising and falling edge, rather than taking the average. The forward clocking can be accurately modeled by GetWave2. GetWave2 enables finding the optimum DFE clocking and jitter tracking which are key design parameters for DDR5 and LPDDR5.

![DDR5 AMI Jitter Tracking](image)

Jitter tracking for uncorrelated jitter between data and strobe signals.

The **BIRD204** document describes the details of different AMI clocking options and the table below, summarizes the differences.

<table>
<thead>
<tr>
<th>Effect to model</th>
<th>GetWave2</th>
<th>GetWave with clock time input</th>
<th>GetWave with internal CDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock forwarding and DQ-DQS jitter tracking</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>DQ slicer sensitivity in terms of DQS slew rate</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Power Integrity output delay nonlinearity and discretization</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>DQS correlated voltage noise</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>DQS jitter amplification by Power Integrity</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>
**Advanced Challenges Covered by PathWave ADS Memory Designer**

<table>
<thead>
<tr>
<th>Predict eye closure due to crosstalk</th>
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<tbody>
<tr>
<td>Equalization modeling</td>
<td>Yes</td>
</tr>
<tr>
<td>Single Ended Signals: Asymmetric eye shape</td>
<td>Yes</td>
</tr>
<tr>
<td>Single Ended Signals: DC offset</td>
<td>Yes</td>
</tr>
<tr>
<td>DQ to DQS clocking (jitter tracking)</td>
<td>Yes</td>
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<tr>
<td>Multiple Tx and Rx simultaneously</td>
<td>Yes</td>
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<tr>
<td>Write-leveling</td>
<td>Yes</td>
</tr>
<tr>
<td>Compliance Reporting</td>
<td>Yes</td>
</tr>
<tr>
<td>Transient Convolution, DDR Bus Simulation (Bit-By-Bit &amp; Statistical)</td>
<td>Yes</td>
</tr>
<tr>
<td>IBIS-AMI model generation</td>
<td>Yes</td>
</tr>
<tr>
<td>Flexible components (SPICE netlist, IBIS models, Ideal Tx / Rx, S-Parameters)</td>
<td>Yes</td>
</tr>
<tr>
<td>Unmatched IO* (Can represent multiple UI skew between Data &amp; Strobe)</td>
<td>Yes</td>
</tr>
<tr>
<td>Power Aware Simulation (SSO/SSN)</td>
<td>Yes</td>
</tr>
</tbody>
</table>

*Inside a DRAM devices there can be multiple UI’s skew between signals and their clock. The jitter relationship can be maintained IBIS AMI modeling if two waveforms are input into the model.*
Introducing the PathWave ADS Memory Designer Workflow

Traditional workflow:

[Diagram of traditional workflow]

Significantly reduce clicks and setup time using the smart components and bus-wire in Memory Designer

Memory designer workflow: new, faster, simpler setup

[Diagram of new workflow]

Key Productivity Benefits with PathWave ADS Memory Designer:

- Reduce setup time from hours to minutes
- One schematic for both DDR Bus simulation and Transient simulation
- One schematic for read and write cycle
- Apply IBIS models for groups of signals as one (reduce clicks)
- Simple smart bus-wiring to automatically match and connect components
- IBIS and non-IBIS flow (including jitter and equalization)
- Design-and-Test solution with compliance applications, invoked within ADS
Utilizing the smart component “memory probe” enables you to access Keysight’s compliance test applications with industry proven measurement science, all automated from within ADS.
**PCB Channel Models**

Memory Designer provides a comprehensive and simple workflow for both pre-layout design exploration, and post-layout EM verification for a smooth flow. EM verification can be provided from your EM simulation of choice (e.g. SIPro). Memory Designer enables total flexibility where there are no limits in the schematic from using models from: HSPICE, S-parameters, other cells of SIPro PCB models. Automatically detect through-paths for S-parameters to help matching up pins and utilize the build in write leveling calculation to compensate for signal skews. In your post-layout verification stage of your design, utilize Keysight’s accurate EM extractions.

Easier than using a 3rd party tool kit, Keysight’s accuracy and integrated ADS flow will ensure a passing design in the shortest amount of time.

PathWave ADS provides a cohesive workflow with electromagnetic (EM) extraction. Via Designer creates accurate models for via arrays for pre-layout designs. SIPro extracts an entire memory data bus at once with accurate crosstalk effects.
PathWave ADS SIPro (W3033E) is available as a separate element, and in bundles that include Memory Designer. SIPro’s unique extraction technology captures crosstalk in the signal traces and in the signal vias. Via Designer is included in all new PathWave Signal Integrity bundles.

**PathWave ADS Memory Designer Key Feature List:**

<table>
<thead>
<tr>
<th>Key feature</th>
<th>Description</th>
</tr>
</thead>
</table>
| Smart Bus Wire | Connect multiple wires (e.g. data bus or command address bus) with a single mouse click  
- Automatic signal identification & matches  
- Automatic connection of wires |
## Memory Controller Component

**Smart controller component for fast model setup**
- Supports IBIS, EBD, IBIS-AMI models, and built-in model if no IBIS model exists
- Supports package models, write-leveling, & power aware simulations
- Configure single or multiple drivers
- Supports both transient and DDR bus simulation
- Allows pin-based model and equalization setting
- Parameterize IBIS model corner cases and model selector

## Memory Probe

**Configure memory measurements including, design exploration and automated compliance test**
- Organizes measurements by signal group and type of measurements
- Computes write-leveling and write out the delay file for automatic compensations
- Generate design exploration report for pass/fail against design specification
- Generates compliance test report (PDF)

## PCB Component

**Smart, configurable PCB component**
- Supports touchstone s-parameter data
- Automatic recognition of signal properties
- Automatic recognition of signal properties by reading directly from SIPro EM models
- Allows custom editing of signal IDs
- Enables termination of unused ports

## Memory Component

**Smart memory component for fast model setup**
- Can represent single DRAM, multiple DRAM dies within a single package, or multiple DRAM chips on a DIMM
- Allows pin-based model and equalization settings
- Parameterize IBIS model corner cases
- Supports IBIS, EBD, IBIS-AMI models, and built-in model if no IBIS exists
- Can configure single or multiple drivers
- Supports:
  - Package Models
• Write-Leveling
• Power-aware simulations
• Transient & DDR Bus Simulation

Types of Measurements
Includes many important DDR measurements including:
• Eye
• Eye height & width
• Bathtub
• Bathtub Plots
• BER Contour
• Height & Width at targeted BER
• Skew
• Strobed Eye
• Mask Margin
• Rx BER Mask Margin

Pre-layout Component
Smart configurable pre-layout component
• Supports existing ADS designs & HSPICE netlist
• Allows easy setup for signal property tables by reading in .csv file
• Supports design parameters for batch/sweep simulations
### Design Exploration Solution

See pass / fail of your design in one report
- Automatically generate batch simulation
- Sweeps based upon selected variables and values
- Select custom limits for typical measurements
- Generates excel file with pass/fail results

### Simulations

One schematic for multiple simulation types

### Transient

Handle non-linear time varying effects (SSN)
- Spice Simulation – uses individual points

### DDR Bus Simulation Statistical Mode

A Fast simulator that can predict eye closure down to low BERs
- Provides an eye diagram, and predicts how closed the eye will be after a large number of bits

### DDR Single-Ended IBIS-AMI Bit-By-Bit Simulation

- Fast
- For DDR5/LPDDR5 and above
- GDDR6

### AMI modeling

- Supports IBIS BIRD 204
- AMI model to receive 2 waveforms as input (ex: DQ & DQs waveforms)
- Supports DC offsets and Vref information
- Support BCI (Back Channel Interface)
- Memory Interface AMI Model Builder
- SystemVue AMI Modeling
# Product Ordering Information

<table>
<thead>
<tr>
<th>Model number</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>W3626B</td>
<td>PathWave ADS Core, EM Design, Layout, HSD Circuit Sim, SIPro, PIPro, Memory Designer</td>
<td></td>
</tr>
<tr>
<td>W3622B</td>
<td>PathWave ADS Core, EM Design, HSD Circuit Sim, Memory Designer</td>
<td>Includes the Memory Designer workflow and DDR Bus Simulator DDR5, LPDDR5 AMI Model Builder</td>
</tr>
<tr>
<td>W3025E</td>
<td>PathWave Memory Designer Element</td>
<td>Includes the Memory Designer workflow and DDR Bus Simulator (does not include SIPro) DDR5, LPDDR5, AMI Model Builder</td>
</tr>
<tr>
<td>W3033E</td>
<td>PathWave SIPro</td>
<td>Includes Memory Designer workflow</td>
</tr>
<tr>
<td>W4810B</td>
<td>PathWave System Design Core + AMI</td>
<td>Customized SerDes and DDR IBIS-AMI model generation environment</td>
</tr>
<tr>
<td>W3024E</td>
<td>PathWave HSD Circuit Sim Element</td>
<td>ViaDesigner which is included in all new PathWave Signal Integrity bundles</td>
</tr>
</tbody>
</table>
Conclusion

Next-generation memories are a disruptive technology, and both simulation technologies and workflows need to adapt. Keysight is your number one partner for a complete design and test workflow for DDR, to shorten the design cycle and reduce project delays.

Keysight PathWave ADS Memory Designer is a predictive, productive, and insightful platform to enable you to easily simulate your DDR designs. Reduce clicks, get accurate results and avoid board failures using Keysight – your best partner with solutions in all DDR5 touchpoints.

Resources:


https://www.youtube.com/playlist?list=PLtq84kH8xZ9Ft7jMfxBCu6lIS92zZAL5

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at:

www.keysight.com/find/contactus