CASE STUDY

Developing an X-Band Hybrid Beamformer Digital Twin

Virtual platform enables accurate simulation of configurations with hundreds of phased array elements

KEYSIGHT

PATHWAVE

Breaking the Limits of Hardware Prototyping

Organization

- Analog Devices

Challenges

- X-band phased array systems for aerospace, defense, and weather radar applications driving for higher performance arrays
- Prototyping thousand element phased array systems in hardware is cost prohibitive. ADI enablement platforms allow the ability to create smaller arrays representative of end systems for proof of concept designs

Solutions

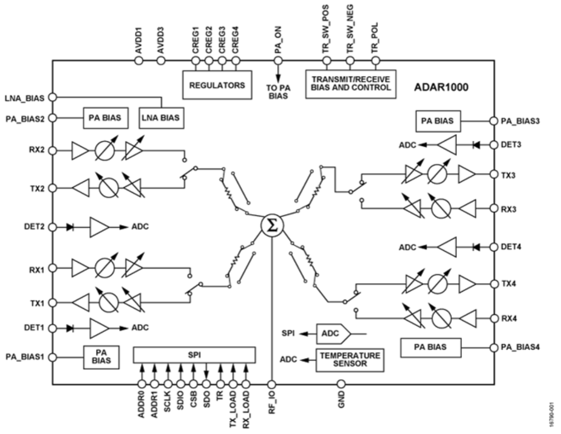
- Create a digital twin for X-band phased array hybrid beamformer prototyping and design
- PathWave RFPro provides 3D electromagnetic simulation of antenna array
- PathWave System Design integrates with PathWave ADS, MATLAB blocks, ADI Sys-parameters, and S-parameters for modeling and co-simulation

Results

- Digital twin scales to much larger phased array sizes than basic 4x8 configuration of the hardware enablement platform – up to hundreds of elements
- Baseline simulations run in around 25 minutes and provide highly accurate results
- Potential savings of a year or two to reach program “technology readiness” milestones

Analog Devices, Inc., based in Wilmington, Massachusetts, is a long-time industry leader in analog signal-processing semiconductor technology. X-band (8 to 12 GHz) radar uses techniques like phased antenna arrays for hybrid beamforming, and aerospace, defense, and weather radar design teams turn to Analog Devices (ADI) for critical RF components in the signal chain. ADI offers customers a hardware enablement platform for X-band hybrid beamforming based on its ADAR1000 beamformer and AD9081 MxFE® chipsets.

In a two-year project, three to five ADI engineers, plus added experience and assistance from Keysight Field Solutions Engineering Fellow Murthy Upmaka, set out to create a digital twin of this X-band hybrid beamformer system. This digital twin uses Keysight PathWave System Design to quickly adapt to various phased array configurations and newer ADI components as they become available.



Challenge: From components to system-level models

Hardware provides a level of comfort for RF engineers. Teams can take measurements in a lab, in an anechoic chamber, or in the field with a hardware prototype. But RF hardware also provides a fixed set of boundaries, some based on the architecture of the implementation and some based on the physical realization of the elements involved.

Figure 1 shows a photo of the ADI hardware enablement platform for an X-band phased array hybrid beamformer depicted in the block diagram from the introduction. “These platforms scale to some degree, and there is interchangeability in the signal chain by upgrading boards to newer versions if available,” says Sam Ringwood, Systems Platforms Application Engineer at ADI. Still, the Stingray board (far left) implements one configuration: four subarrays of eight elements each. “X-band phased array radar designs now run into hundreds and even thousands of elements,” continues Ringwood. Physical interconnects between the hardware are crucial in a beamforming application. What might appear to be simple coaxial cabling is a phase-matched set of cables between each board or module; if one breaks, the repair or replacement must maintain phase stability or performance changes.

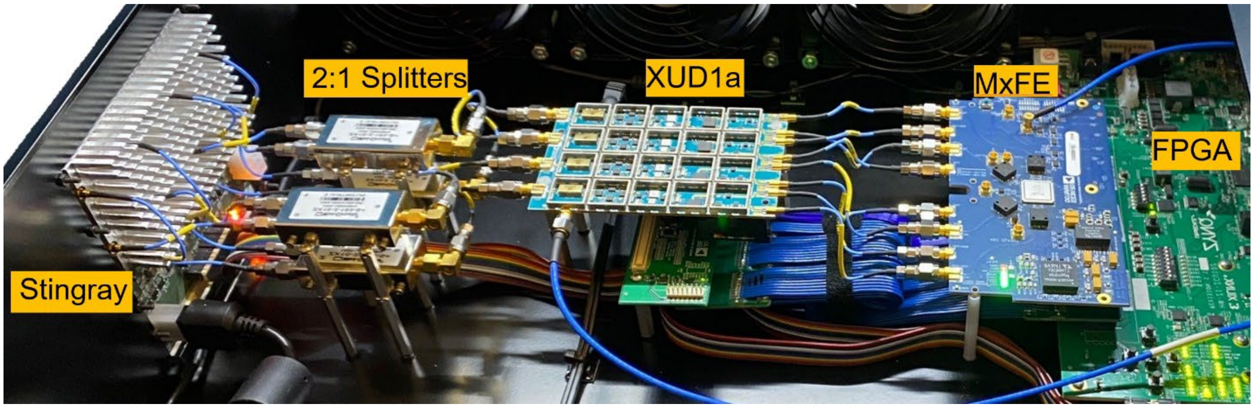


Figure 1. Photo of the X-band phased array hybrid beamformer hardware enablement platform

ADI application teams wanted a platform that could quickly scale to many more array configurations while still providing flexibility to interchange any parts in the signal chain. “Moving to a digital twin provides a reference design that would work for more customers, including those designing with legacy ADI parts, new ADI parts before an evaluation board is available, or other commercially available components to fit a particular aspect of a beamforming application,” observes Ringwood. “We’d then be able to validate our digital twin performance against a basic configuration, then scale it to a larger array configuration.”

The first step ADI took in moving to its digital twin was getting comfortable with the PathWave System Design environment and discovering how to leverage its capabilities. “We’d used RF Link for simple signal chain cascade analysis, and stepping up to PathWave System Design for a more comprehensive cross-domain simulation environment with data flow analysis was a bit of a learning curve,” shares Ringwood. ADI also has some homegrown spreadsheets, again for simple cascade analysis. A realization emerged: they needed better model fidelity for the more powerful solvers in PathWave System Design if its simulations were to provide results close to the hardware.

Pieces of modeling existed, but significant gaps remained. Many ADI RF components have Sys-parameters, measurement-based characterizations of mixers and power amplifiers describing linear and non-linear behavior such as P1dB, IP3, gain, noise figure, return loss, and more. Where Sys-parameter models didn't exist, S-parameter models would work, especially since wideband analysis wouldn't be required in an X-band system. Teams also had some groundwork in MATLAB models for ADI data converters, mixed-signal components with analog and digital properties. All three model types integrate with PathWave System Design. "Things got much easier once we figured out how to drop MATLAB blocks within the system model as code," Ringwood offers with perceptible relief.

Ultimately, the challenge ADI faced was architecting a virtual system model representing the performance of its existing hardware enablement platform in the 4x8 array configuration. At first, the team thought they would need an exact 1:1 match for the hardware. "Our definition is based on perspective," says Ringwood. "You can avoid overcomplicating the model while still achieving accuracy representative of the system." Abstracting the model allowed the team to break the relationship between the features of a specific chip and the capability needed in the beamforming system.

Solution: A simpler, scalable digital twin

A digital twin is a detailed virtual representation of a system made from measurement-based or predictive behavioral models, incorporating real-world effects and delivering fast, accurate simulation results close to system hardware measurements. It can become an instance of the physical system it represents with feedback on actual measurements made under operating conditions and any maintenance performed.

In a more straightforward prototyping context, ADI's digital twin seeks to provide a faster path to a proof-of-concept for an X-band hybrid phased array beamformer, delivering equivalent performance to the 4x8 hardware enablement platform and, by extension, different and larger configurations. Figure 2 shows the block diagram for the X-Band hybrid beamforming enablement platform (pictured in Figure 1) used initially to guide the digital twin system design and gauge its performance.

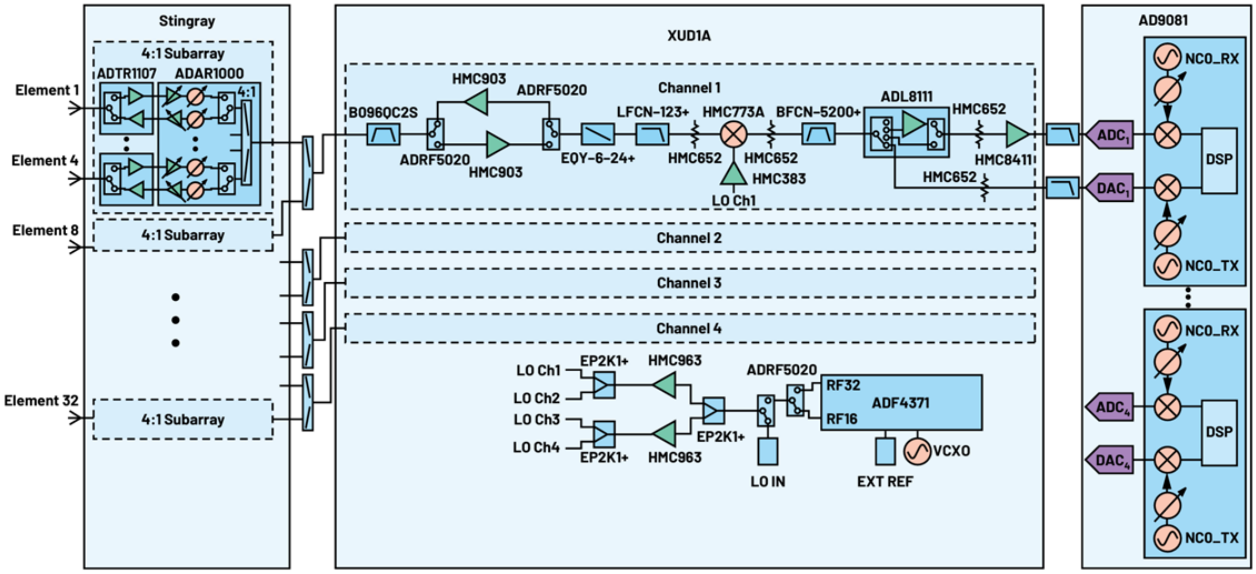


Figure 2. Block diagram of the X-band phased array hybrid beamformer hardware enablement platform

PathWave System Design was an easy choice for hosting the X-band hybrid beamforming digital twin. Existing users across ADI design groups forged prior relationships with Keysight, resulting in a library of Sys-parameter models and reference designs for signal chains with ADI components ready to use in PathWave System Design. Site licensing provided a low barrier of entry for Ringwood’s team. MATLAB was the alternative for hosting since the ADI data converter models and system-level control toolboxes existed. The team considered creating MATLAB behavioral models for everything else in the system. Ultimately, the ability to integrate MATLAB blocks into PathWave System Design cinched their decision.

The new workflow quickly revealed advantages. “The phased array toolbox within PathWave System Design is attractive,” says Ringwood. “It enabled us to take a ‘simple’ signal chain as a line-up of components, fully modeled, and replicate it hundreds of times without cluttering the workspace.” PathWave System Design also has phased array radar waveforms and measurement routine libraries to simplify simulation. ADI adapted simple continuous-wave stimuli for their digital twin instead of porting more complex waveforms from MATLAB.

Starting from Sys-parameter component behavioral models, which stem directly from ADI measurements, provided a solid foundation. S-parameter models were added for specific components without Sys-parameter models and, importantly, all board-level interconnects with precise phase matching. “We do over-the-air beam pattern measurements in our anechoic chamber,” says Ringwood. “We found that every piece of hardware – down to one-inch cables – needs to be in the digital twin for simulations to align with measurements.” ADI uses Keysight test equipment for validating single-channel and single-subarray performance measurements. PathWave System Design uses the exact Keysight measurement science in its analysis routines, helping a digital twin attain the same results as physical hardware with high-fidelity models in place.

Figure 3 shows the PathWave System Design system-level view of the hybrid beamformer, with each box exploding into more details. The most interesting are the antenna array, the analog beamforming model, and the imported MATLAB model for the data converter within the digital beamformer model.

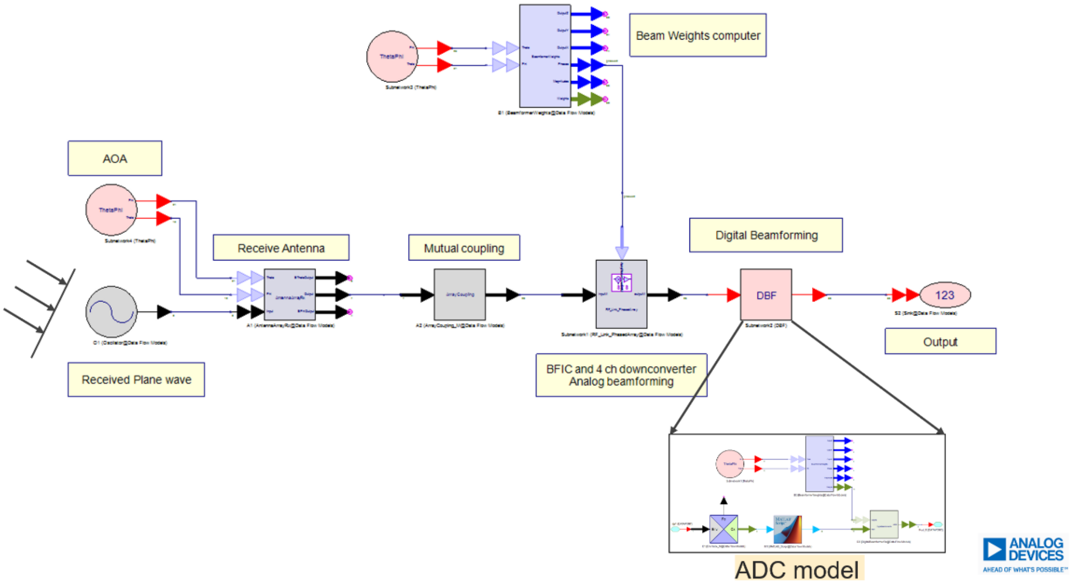
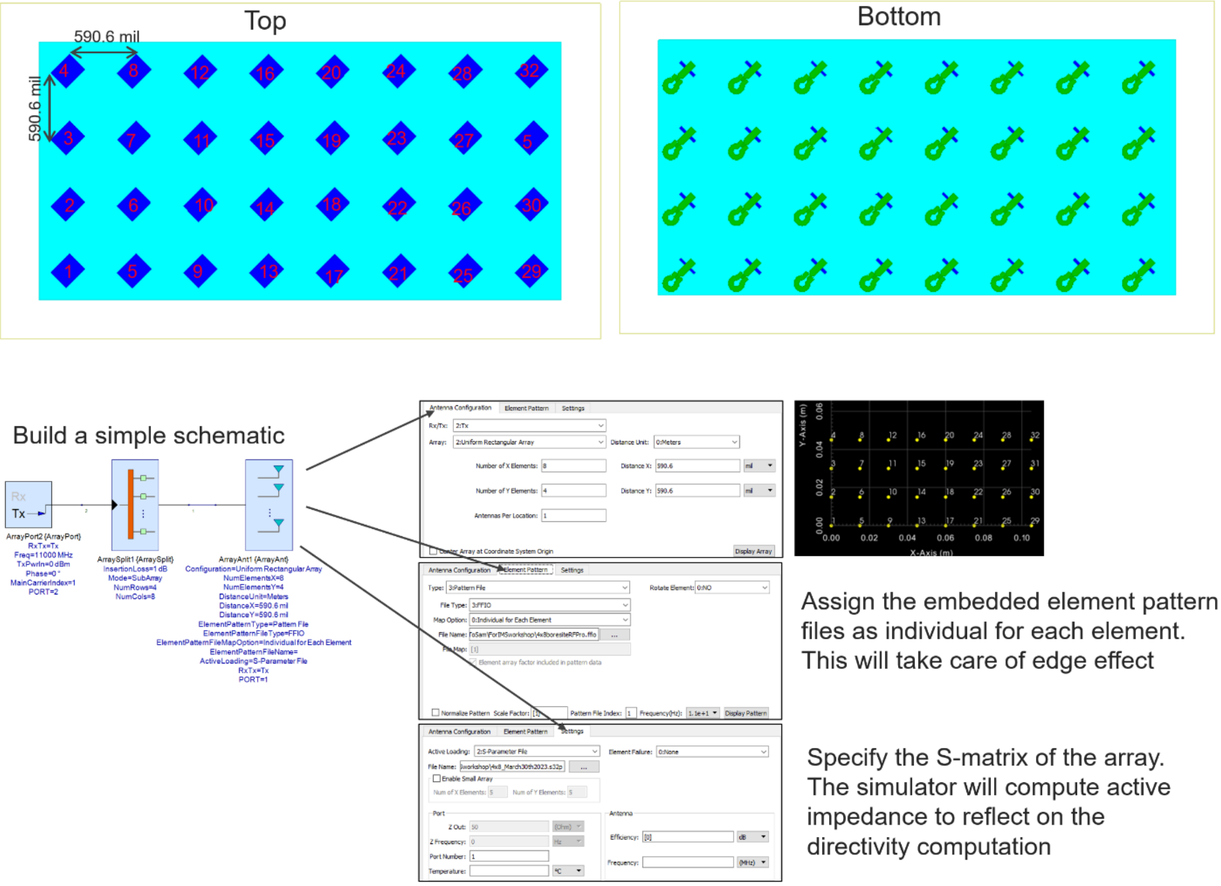


Figure 3. The high-level view of the hybrid beamformer digital twin in PathWave System Design

“We saw we could move from board layouts to co-simulation easily in RFPro and PathWave System Design, giving us a recipe for array scaling,” shares Ringwood. Layouts for several hardware enablement platform boards were in Cadence Allegro. A layout of the 32 antenna array elements in the basic 4x8 configuration moved from Allegro to Keysight PathWave Advanced Design System (ADS), then into Keysight PathWave RFPro for 3D electromagnetic (EM) simulation. Three pieces of information flow to PathWave System Design from that EM simulation, illustrated in Figure 4:

- A mapping of element locations in PathWave System Design to the ports in RFPro,
- Embedded element beam patterns, represented in a .ffio file,
- An S-parameter matrix for the array.



Build a simple schematic

ArrayPort2 {ArrayPort}
RxTx=Tx
Freq=11000 MHz
TxPwrIn=0 dBm
Phase=0 °
MainCarrierIndex=1
PORT=2

ArraySplit1 {ArraySplit}
InsertionLoss=1 dB
Mode=SubArray
NumRows=4
NumCols=8

ArrayAnt1 {ArrayAnt}
Configuration=Uniform Rectangular Array
NumElementsX=8
NumElementsY=4
DistanceUnit=Meters
DistanceX=590.6 mil
DistanceY=590.6 mil
ElementPatternType=Pattern File
ElementPatternFileType=FFIO
ElementPatternFileMapOption=Individual for Each Element
ElementPatternFileName=
ActiveLoading=S-Parameter File
RxTx=Tx
PORT=1

Antenna Configuration | Element Pattern | Settings

Rx/Tx: 2:Tx
Array: 2:Uniform Rectangular Array
Distance Unit: 0:Meters
Number of X Elements: 8
Distance X: 590.6 mil
Number of Y Elements: 4
Distance Y: 590.6 mil
Antennas Per Location: 1
☐ Center Array at Coordinate System Origin
Display Array

Type: 3:Pattern File
Rotate Element: 0:NO
File Type: 3:FFIO
Map Option: 0:Individual for Each Element
File Name: ToSam\ForIMSworkshop\4x8boresiteRFPro.ffio
File Map: [1]
☑ Element array factor included in pattern data
☐ Normalize Pattern
Scale Factor: [1]
Pattern File Index: 1
Frequency(Hz): 1.1e+1
Display Pattern

Assign the embedded element pattern files as individual for each element. This will take care of edge effect

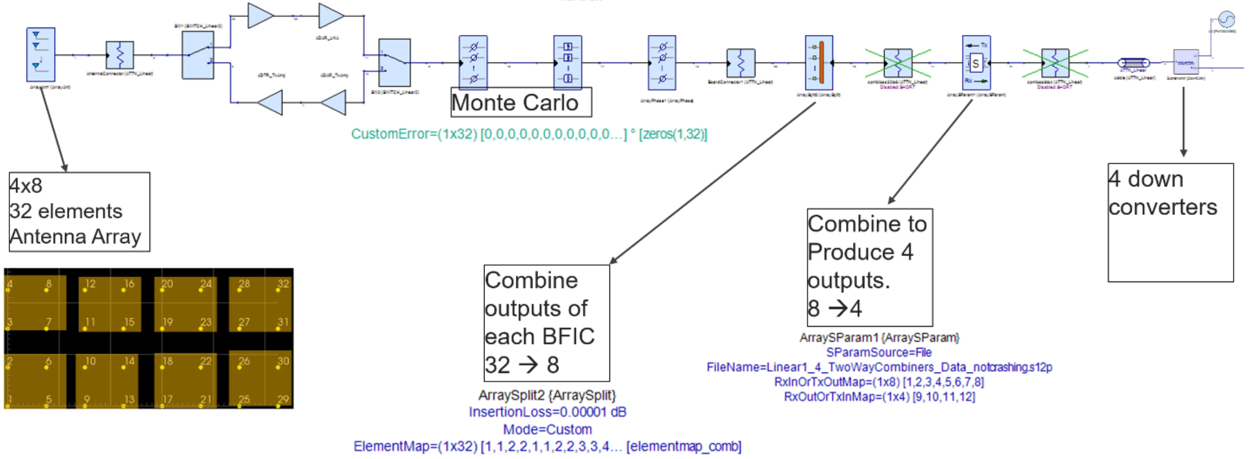
Active Loading: 2:S-Parameter File
Element Failure: 0:None
File Name: 5workshop\4x8_March30th2023.s32p
☐ Enable Small Array
Num of X Elements: 5
Num of Y Elements: 5
Port
Z Out: 50 (Ohm)
Z Frequency: 0 Hz
Port Number: 1
Temperature: °C
Antenna
Efficiency: [0] dB
Frequency: (MHz)

Specify the S-matrix of the array. The simulator will compute active impedance to reflect on the directivity computation

Figure 4. Array element locations, directivity patterns, and S-parameters compose a behavioral model of an array

Building and simulating an array this way in RFPro makes it straightforward to replace the model for the physical 4x8 array with any array configuration. This scalability is a primary goal for the digital twin.

The analog beamforming model shown in Figure 5 depicts the abstraction of the signal processing chain. Rather than track a 1:1 model of the exact chip (BFIC = beamforming integrated circuit) and board configurations, the model is decomposed into functional blocks accurately representing what the hardware does, lined up in a signal chain.



CustomError=(1x32) [0,0,0,0,0,0,0,0,0,0,0...] ° [zeros(1,32)]

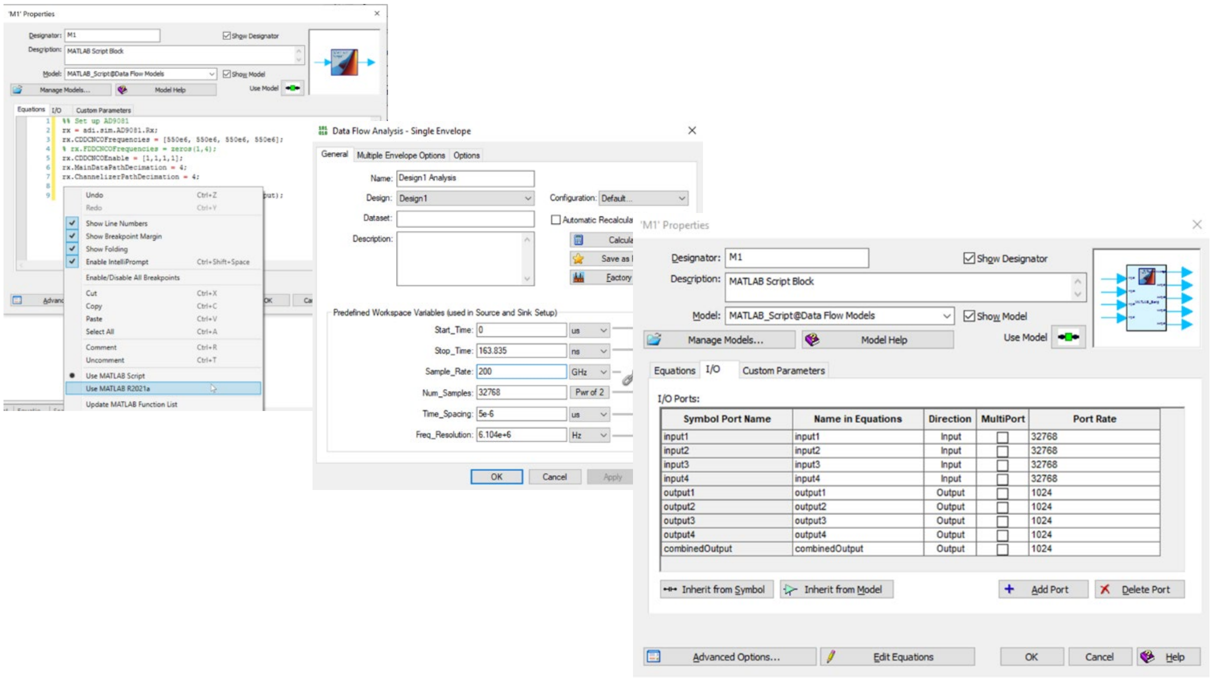
ArraySplit2 {ArraySplit}
InsertionLoss=0.00001 dB
Mode=Custom
ElementMap=(1x32) [1,1,2,2,1,1,2,2,3,3,4... [elementmap_comb]

ArraySParam1 {ArraySParam}
SParamSource=File
FileName=Linear1_4_TwoWayCombiners_Data_notcrashing.s12p
RxInOrTxOutMap=(1x8) [1,2,3,4,5,6,7,8]
RxOutOrTxInMap=(1x4) [9,10,11,12]

Figure 5. Analog beamforming signal chain represented in PathWave System Design

Again, the digital twin starts with a baseline for the 4x8 array configuration, with the signal chain line-up easily replicated and reconfigured for more array inputs. “Every time we considered a decision, simpler was better for scalability, and ultimately for customer experience with the digital twin,” shares Ringwood.

One of those decisions was pulling in the MATLAB model for the data converter, which accepts real input from RF Link and custom sampling data using ADI’s High-Speed Converter Toolbox for MATLAB. PathWave System Design can implement a MATLAB script block, invoking MATLAB in the background during simulation. The designer sees everything needed to run the code within the PathWave System Design environment, including properties shown in Figure 6.



Designator: M1
☑ Show Designator
Description: MATLAB Script Block
Model: MATLAB_Script@Data Flow Models
☑ Show Model

```
%% Set up AD9081
rx = adi.sim.AD9081.Rx;
rx.CDDCNCOFrequencies = [550e6, 550e6, 550e6, 550e6];
% rx.FDDCNCOFrequencies = zeros(1,4);
rx.CDDCNCOEnable = [1,1,1,1];
rx.MainDataPathDecimation = 4;
rx.ChannelizerPathDecimation = 4;

                                                   put);
```

Name: Design1 Analysis
Design: Design1
Configuration: Default...
Dataset:
Description:
☐ Automatic Recalcula

Predefined Workspace Variables (used in Source and Sink Setup)
Start_Time: 0 us
Stop_Time: 163.835 ns
Sample_Rate: 200 GHz
Num_Samples: 32768 Pwr of 2
Time_Spacing: 5e-6 us
Freq_Resolution: 6.104e+6 Hz

I/O Ports:

Symbol Port Name	Name in Equations	Direction	MultiPort	Port Rate
input1	input1	Input	☐	32768
input2	input2	Input	☐	32768
input3	input3	Input	☐	32768
input4	input4	Input	☐	32768
output1	output1	Output	☐	1024
output2	output2	Output	☐	1024
output3	output3	Output	☐	1024
output4	output4	Output	☐	1024
combinedOutput	combinedOutput	Output	☐	1024

Figure 6. Property settings for MATLAB code integration in PathWave System Design

Results: Good matching, a surprise, and time savings

Metrics for the digital twin break into two categories. First are antenna-related metrics, such as beam pattern directivity. Overlapping pattern alignment between measurements and simulations is critical within a ±30° beam window. Figure 7 shows a plot of measured versus simulated directivity distribution for the 4x8 configuration with a near-perfect overlap in the desired window.

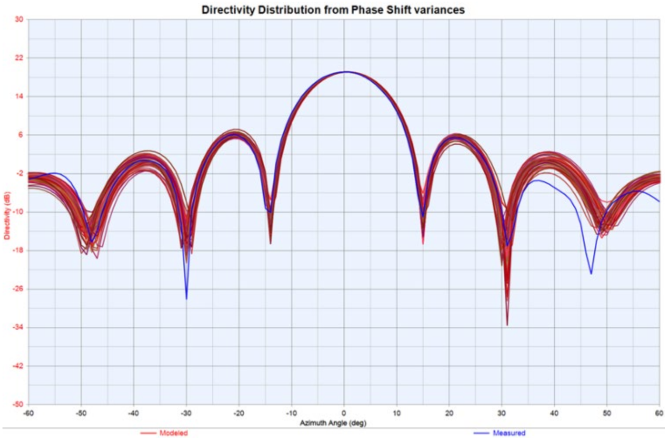


Figure 7. Comparing directivity distribution of 4x8 configuration physical measurements versus the digital twin

Second are receiver-related metrics, like performance per channel, per subarray, and the total array in gain, noise spectral density, and intermodulation products. A good rule of thumb for these metrics is simulations being within ±1dB of measurements; Figure 8 shows the digital twin achieves this.

		Gain (dB)	NSD (dBm/Hz)	IIP3 (dBm)
Full Array	Simulated	49.97	-136	-29.5
	Measured	49.81	-136	-29.84
Subarray	Simulated	49.96	-130	-26.9
	Measured	49.8	-129.3	-29.09
Channel	Simulated	31.07	-138.5	-25.2
	Measured	31.26	-137.6	-22.87

Figure 8. Gain, noise spectral density, and intermodulation products in the digital twin match measurements

Also important is matching simulation results between the layout level with ADS and RFPro and the system level with PathWave System Design. "Creating accurate system-level models makes a digital twin very attractive," says Upmaka. Figure 9 shows a near-exact match for antenna simulations on a 30° scan.

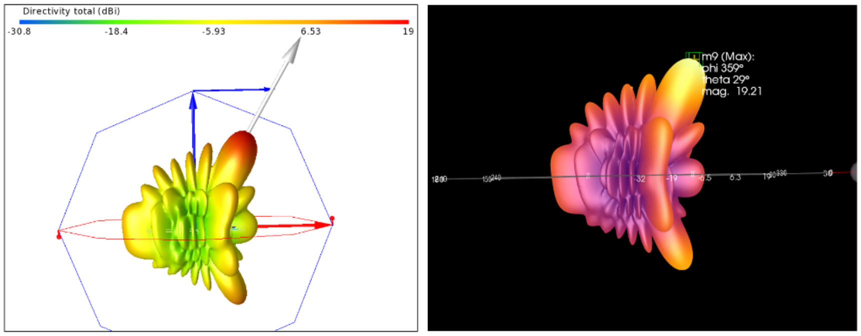


Figure 9. Beam lobe patterns simulated in RFPro (left) and PathWave System Design (right)

A surprising result came from converting to an ADS layout and running RFPro EM simulations on the Stingray (ADAR1000EVAL1Z) board with the antenna elements. “We noticed some unusual transmit mode resonance, and our first thought was the simulation was unstable,” relates Ringwood. “Investigation showed the physical hardware had cavity resonances under the heat sink. We used the digital twin to drill down into a subset model focused on reproducing the effect. That led to adding eight RF absorbers under the heat sink in the physical design and the same absorbers in the model, suppressing the resonance.”

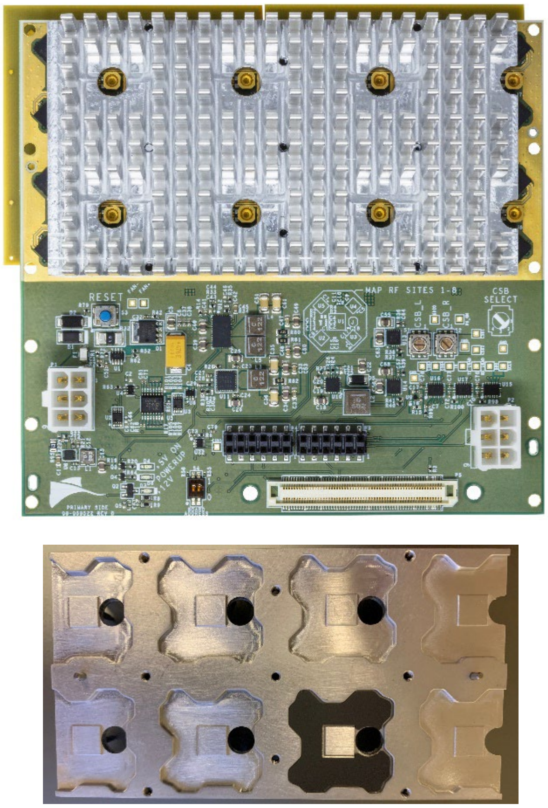


Figure 10. Stingray board with heatsink (top) and heatsink underside with one of eight RF absorbers inserted (bottom)

Customer experience is also essential. “Our goal was to get customers self-sufficient with the digital twin workspace,” says Ringwood. His simulation of the 4x8 configuration with the array pointing in one direction takes around 25 minutes on a mid-range Intel Core i7 laptop. Increasing array sizes into the hundreds and adding additional beam angles would suggest using a high-performance computing (HPC) environment for PathWave System Design, supported in its 2023 release, to lower simulation times.

The big win from the digital twin is design time reduction. Customers can purchase the hardware enablement platform, set it up, and evaluate their algorithms. They can then jump into the digital twin and establish their phased array configuration – reaching “technology readiness” milestones without a hardware redesign effort. Based on ADI’s findings, Ringwood guesses the digital twin can save as much as a year or two in a program that might take five to seven years in a hardware-centric development approach. The ability to explore virtually also reduces risk. A digital twin demonstrating a proof-of-concept may be the difference between securing program funding or missing an opportunity.

> “Moving to a digital twin provides a reference design that would work for more customers, including those designing with legacy ADI parts, new ADI parts before an evaluation board is available, or other commercially available components to fit a particular aspect of a beamforming application.”
>
> **Sam Ringwood, Systems Platforms Application Engineer, Analog Devices**

A pro tip Ringwood offers in deploying and using PathWave System Design: stay organized in the workspace as design complexity increases. Having a plan for file structures, data structures, annotations, and more helps reduce hunting around for vital information in a design.

Looking ahead: Expanding modeling capability

With high-fidelity models being absolutely crucial to the success of a digital twin project, Ringwood has three suggestions for expanding modeling capability in PathWave System Design. Adding complexity to component modeling, such as the model for the ADAR4000 time delay unit, requires application engineering insight – an opportunity for ADI and other component manufacturers. More Sys-parameter models of components like switches would also help customers. Improving ways to represent data converters in PathWave System Design is also something to consider; the MATLAB integration is good, but direct manipulation of properties and behaviors in one environment would be ideal.

Learn more about Analog Devices and its X-band beamforming solutions at:

X-Band Phased Array Platform

X-Band Phased Array Development Platform User Guide

For more information on these Keysight RF EDA solutions, please visit:

PathWave System Design

PathWave Advanced Design System (ADS)

PathWave RFPro

All figures courtesy of Analog Devices, Inc.

KEYSIGHT

Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.

Published in USA, September 21, 2023, 3123-1726.EN