

Keysight Technologies U4431A Protocol Analyzer for MIPI™ M-PHY Interfaces

Product Fact Sheet

Industries and Applications

- High-resolution cameras
- High-speed peripherals
- Advanced graphics adapters
- Massive memory buffers

Designers and Validators of

- M-PHY
- IP
- Application processors
- Memory/chipsets
- Mobile devices
- Mobile embedded systems



Product Description

Deep insight to help you win the race to M-PHY

The MIPI™ M-PHY standards are the backbone of next-generation mobile computing designs. Because these designs are replacing desktop PCs in many applications, these architectures are much faster and more complex than in the past. The increasing demand for bandwidth has driven the expansion of the M-PHY specification to include four-lane, 6.0-Gbs options. The U4431A offers up to 16 GB of analysis memory on each lane, allowing designers to capture tens of seconds of system traffic, even at these high speeds.

In addition, the Keysight U4431A offers “Raw Mode,” a feature that lets designers see the time-correlated 8b/10b data that underlies each protocol. These states can be displayed as a waveform or listing, providing insight into how a packet is formed at the physical layer.

Main Features and Benefits

Power to meet the needs of today’s and tomorrow’s designs

- Up to gear 3 HS data rates
- Up to 16 GB trace depth
- Up to 4 data lanes

Complete insight into complex designs

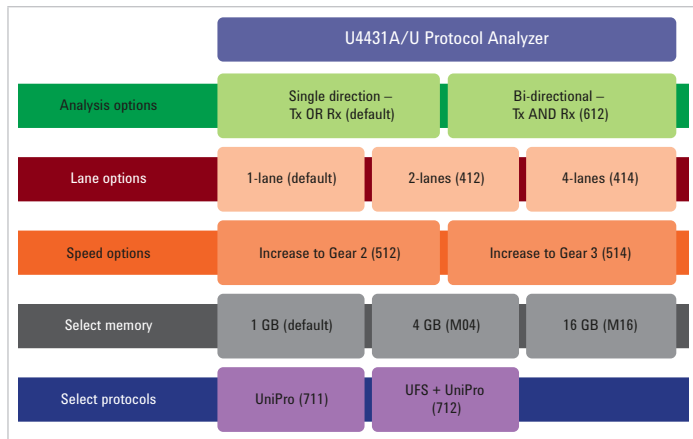
- Track multiple M-PHY busses from the PHY to the application layer
- Raw Mode 8b/10b data views
- Infiniium Oscilloscope integration
- Powerful interface that allows unlimited customization of system views

Powerful triggers

- N-way if/then/else trigger branching with AND/OR logic
- Over 50 triggering macros
- PHY and protocol error triggers
- Event counters, flags, and timers

Flexible probing

Module Configuration



Specifications

Electrical	
Minimum Vdiff	100 mV
Input impedance (DC)	
U4433A probe + N5246A ZIF tips	700 Ω, typical
U4432A SMA harness	128 Ω, typical
Topological	
Lane width	Up to 4 with option 414. Analyze 1, 2, 3, or 4-lane systems
Clocking architecture	Type I
Analysis direction	Tx or Rx (Both Tx and Rx with option 612)
Lane remapping	User-selectable
Lane polarity	User-selectable
Multiple blade support	Up to 5 time-correlated blades in one frame (configured as up to 3 separate busses), multiple frames can be correlated
Performance	
HS Modes supported	G1 to G3
PWM Modes supported	G0 to G7 (subject to limitations of individual protocol)
Rate Series supported (HS and PWM)	A and B
Symbol lock time (subject to protocol spec limit)	
Fast (HS-G1)	1 symbol, typical
Slow (HS-G2, HS-G3)	< 128 symbols
Auto speed detection and tracking	Supported (with no RSE-PO-TX support)
Memory	
	User allocated (shared among analyzer and raw mode)
Standard	1 GB
Option M04	4 GB
Option M16	16 GB

Chassis and Probing Configuration

Chassis options

M9502A	2-slots
M9505A	5-slots
M9502A-020	USB 2.0 host connection for either chassis
M9505A-020	Lower-speed alternative to PC control options, not recommended for > 1 GB memory

PC control options

M9536A	Embedded PC module (no cables or adapters needed)
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Connecting via PCIe to a desktop PC

M9047A	PCIe desktop adapter
Y1202A	PCIe cable (x8 to x8)

Connecting via PCIe to a laptop PC

M9045A	ExpressCard adapter
Y1200B	PCIe cable (x4 to x8)

Analyzer probes

U4433A 1	Probe, ZIF flying leads, MIPI M-PHY (one probe for both directions)
U4432A	SMA cable, MIPI, M-PHY (one probe for both directions)
N5426A	ZIF Tip, 12 GHz InfiniiMax – Kit of 10

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