SOLUTION BRIEF

Your Pathway to PCIe® 6.0

KEYSIGHT

Keysight's Complete and Scalable PCIe® Test Solutions – From Simulation to Protocol

PCI Express®, short for Peripheral Component Interconnect Express, is a high-performance and high-bandwidth serial communication interconnect standard. First proposed by Intel and further developed by the Peripheral Component Interconnect Special Interest Group (PCI-SIG) in replacement of bus-based communication architecture, such as PCI, PCI Extended (PCI-X), and Accelerated Graphics Port (AGP).

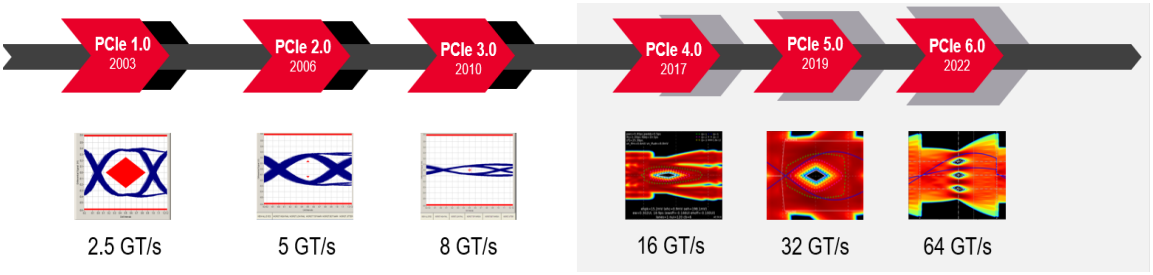

Figure 1. Development of the PCIe standard. PCIe 6.0 is moving to speeds up to 64 GT/s and PAM4 modulation.

PCIe 5.0 brings 512 Gb/s of throughput across 16 lanes, doubling the performance of PCIe 4.0. The specification is backward compatible with all previous PCIe generations and offers new features, including electrical changes to improve signal integrity and backward-compatible card electromechanical (CEM) connectors for add-in cards.

PCIe 6.0 will double the bandwidth of PCIe 5.0 to 1024 Gb/s among the same maximum number of lanes, 16. The data transfer rate will hit 64 GT/s per pin, up from PCIe 5.0's 32 GT/s. A move from NRZ to PAM4 signals brings new challenges. PCIe 6.0 is also backward compatible with previous PCIe generations.

PCIe technology is deployed in a diverse array of products spanning high-performance computing, hyper scale datacenter infrastructure, artificial intelligence systems, desktop computing, automotive applications, and mobile.

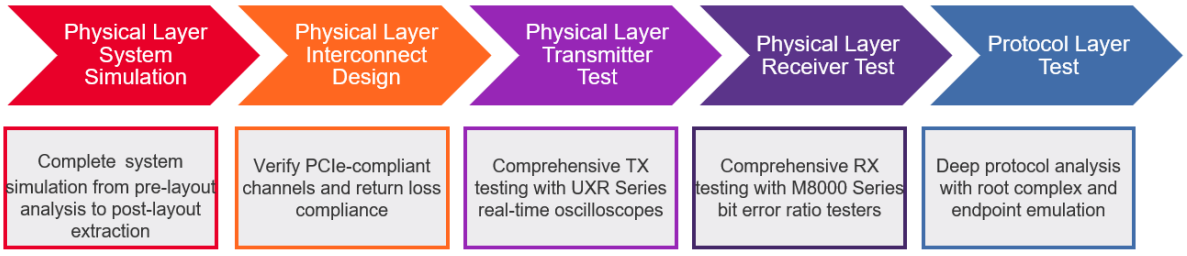

Figure 2. Keysight PCIe solution along the entire design cycle.

Single-vendor Solution for PCIe 5.0 and 6.0 throughout the Entire Design Cycle

With Keysight you get a complete solution along the entire design cycle and (across OSI layers) from one vendor. Keysight has been engaged with PCI Express® (and related technologies) at many levels including having a representative on the PCI-SIG® Board of Directors and others as major participants in the key working groups that define the future of PCI Express. This close involvement allows Keysight to develop the leading-edge tools that ensure the integrity of your PCIe measurements. These tools, coupled with the deep insight of our worldwide support network, improve your time to market and streamline your path to PCIe success.

Keysight recently extended its PCIe solution offering to address PCIe 6.0 protocol test needs with a new PCIe 6.0 protocol analyzer and exerciser in a new compact form factor and CXL 1.1 / 2.0 protocol test. PCIe 6.0 and CXL powerful visualization and analysis tools help to debug the most complex and difficult aspects of these protocols.

Regardless of which generation of the PCIe specification you are working on, you need a test solution approved by PCI-SIG to ensure that your products comply with the standard and get to market faster. Keysight provides a total solution approach to test all generations of the PCIe specification, so you can focus on your next design, rather than spending time learning the details of the test procedures and requirements.

Physical Layer – System Simulation

Keysight PathWave Advanced Design System (ADS) offers integrated design guidance via templates to help you get started faster. Extensive component libraries make it easy to find the part you want. Automatic synchronization with layout allows you to visualize the physical layout while making schematic designs.

Pathwave ADS allows you to characterize and analyze the performance of your design early in the design cycle where errors can be quickly addressed before build-out, saving you both time and money and giving you more confidence in your end design. With Pathwave ADS you can simulate the effects of your channel on your PAM4 design while also applying your silicon-specific, adaptive equalization capabilities. In addition, you can use the power of Pathwave ADS to simulate full channel effects of your PCIe 6.0 channel elements combined with your transmitter and receiver models.

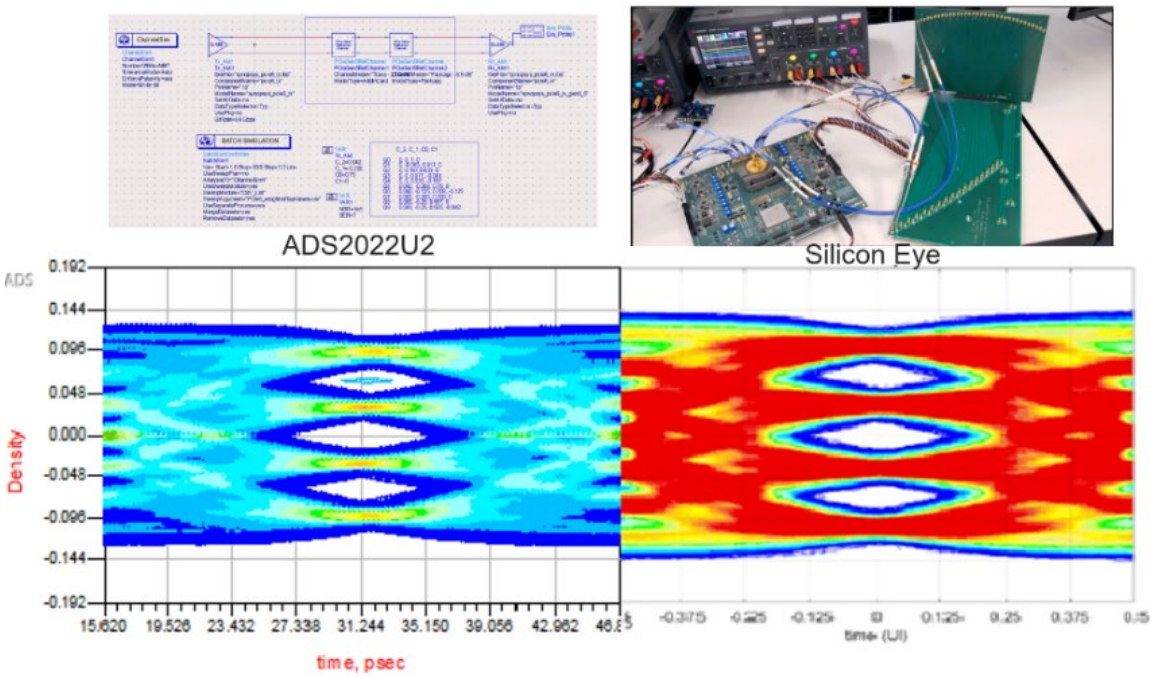

Figure 3. PCIe 6.0 simulation to measurement correlation

Physical Layer – Interconnect Design

The N19301 Physical Layer Test System (PLTS) software is a convenient tool to perform multi-domain characterization of PCIe 6.0 interconnect. Looking at a PCIe 6.0 strip line transmission line structure between two vias below, we can create a test template specific to the important performance parameters such as impedance profile (time-domain reflectometry), near-end crosstalk (NEXT), and far-end crosstalk (FEXT) in both time and frequency domain horizontal axes, mode conversion, and PAM4 eye diagram. The eye diagram analysis is particularly helpful to gain insight because the design engineer can immediately see results of various stimulus/response scenarios. These PAM4 eye diagrams have 32 & 64 Gbaud (64 & 128 Gbps) data rates with 4 taps of decision feedback equalization (DFE). Color-grade-histogram mode is utilized for the 32Gbaud eye in the first case. This is accomplished through a multi-channel simulator built directly into the PLTS tool without forcing the user to create time-consuming simulation schematics. This cuts the development of PCIe 6.0 interconnect by a factor of 4 times and enables a much more efficient design cycle.

Characterization of the most susceptible channels within the PCIe 6.0 interconnect can be done with a 16-channel M937xA vector network analyzer and PLTS software.

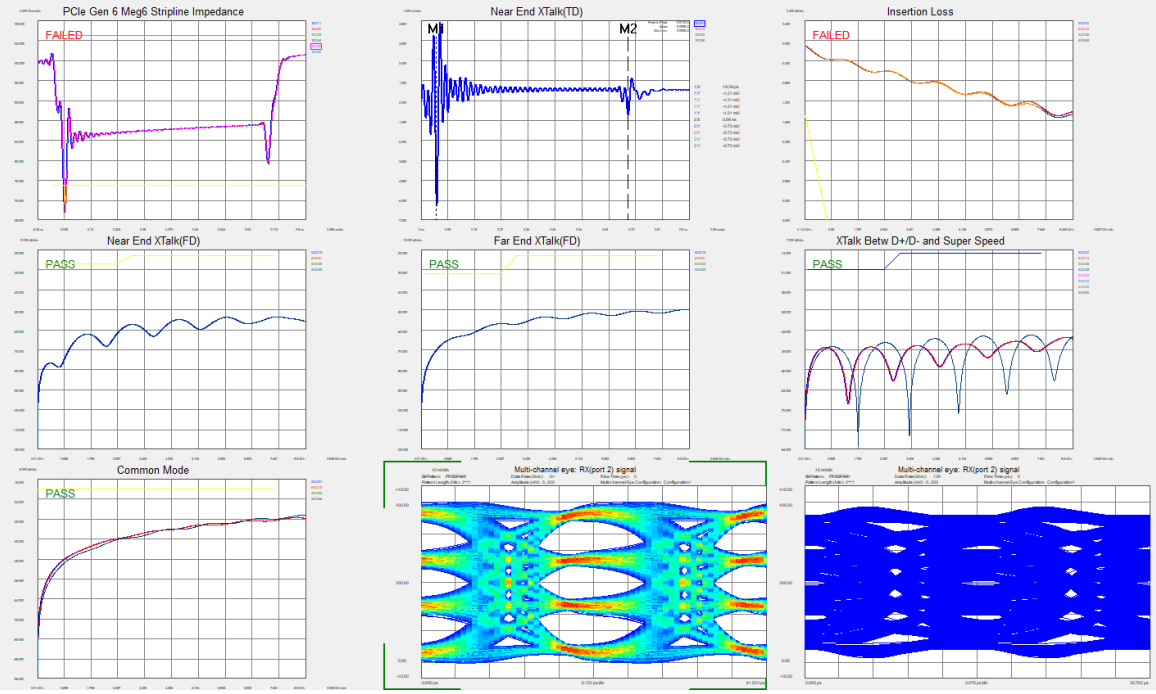

Figure 4. PCIe 6.0 stripline transmission line structure between two vias, characterized with the PLTS software

Physical Layer – Transmitter Test

To help you characterize your transmitter at both the silicon level and at the system level, Keysight offers an automated transmitter test solution based on the class leading UXR family of oscilloscopes with bandwidths of up to 110 GHz. As PCI Express® speeds increase, channel loss also has a greater impact on your device's signal-to-noise ratio (SNR). With PCIe 6.0 moving to PAM4 signal encoding, the impact on your measurements forces you to accommodate an additional decrease in SNR of 9dB. The UXR series oscilloscopes have an intrinsic noise floor that is up to half of that of any other oscilloscope ever offered. This was done with standards like the PCI Express 6.0 specification in mind and the UXR is able to make the most accurate transmitter measurements compared to any other real-time oscilloscope.

Keysight offers **automated transmitter compliance test tools** for PCI Express along with other high performance serial bus standards. The D9050PCIC PCI Express 5.0 electrical performance and compliance test software provides you with a fast and straightforward way to verify and debug your PCIe Express 5.0 design for both silicon validation (per the PCIe 5.0 BASE specification) as well as for PCIe 5.0 add-in cards and motherboard systems.

PCIe 6.0 transmitter test tools are included in the SW00PCIE PCI Express Validation License Suite. SW00PCIE and its accompanying SW02PCIE support transmitter testing under the PCIe® 6.0 BASE specification at 64, 32, 16, 8, 5, and 2.5 GT/s. SW02PCIE includes licenses for D9040PCIC (PCIe 4.0 Tx test software), D9050PCIC, and D9010PCIP advanced PCIe protocol decode/trigger software for PCIe generations 1 through 4.

Figure 5. Low-noise UXR real-time oscilloscopes with up to 110 GHz bandwidth for most accurate PCIe TX test.

The PCI Express D9050PCIC test software allows you to automatically execute PCI Express electrical transmitter tests, and it displays the results in a flexible report format. In addition to the measurement data, the report provides a margin analysis that shows how closely your device passed or failed each test. PCIe 6.0 TX app is expected in late summer 2022.

Receiver and Link Equalization Testing for PCI Express 5.0 and 6.0

The M8040A 64 GBaud high-performance BERT is approved for LinkEQ Gold Suite testing for 8 GT/s and 16 GT/s and is used at PCI-SIG workshops covering 32 GT/s. It was also used for pathfinding for PCIe 6.0 64 GT/s. The perfect oscilloscope for a M8040A-based PCIe RX and LinkEQ test bench is a UXR0594A Infiniium UXR-Series oscilloscope. The very good intrinsic noise performance of the UXR-Series and the M8040A's coverage of baud rates beyond 32 GBaud combined with its NRZ and PAM4 coding capabilities make this combination the ideal choice for users with PCIe 6.0 testing needs on the horizon.

Test automation software is available for PCIe 5.0 Base specification (N5991PB5A) and CEM form factor (N5991PC5A), as well as for PCIe 6.0 for Base specification (N5991PB6A).

The M8040A system capabilities can be extended when the need arises. The pattern generator and error detector starting configurations are for NRZ and 32 GBaud. PAM4 capabilities can be upgraded.

Designed for NRZ and PAM4 receiver testing with baud rates exceeding 32 GBaud, the M8040A 64 GBaud High-performance BERT is Keysight's answer for PCI Express receiver and LinkEQ testing needs for transfer rates from 2.5 GT/s to 64 GT/s.

Figure 6. Keysight M8040A 64 GBaud High Performance BERT for PCIe 5.0 and 6.0 receiver testing.

Protocol Layer Test – The Next Generation

PCIe 6.0 Protocol Test – New Form Factor, More Uptime

Keysight has launched the new PCIe 6.0 Protocol Analyzer and Exerciser to meet the current demand in PCIe 6.0 Protocol test solutions. The capability to link train at 64 GT/s is now made possible with Keysight's innovative CEM Card form factor of the Analyzer. Engineers will be able to link up instantly at 6.0 data rates and start link training, without having to deal with cables with conventional protocol test solutions in the market today. Get ready for more up-time with **Keysight's new PCIe 6.0 Protocol Test Solution.**

Figure 7. Keysight's P5570A PCIe 6.0 Protocol Analyzer and P5573A PCIe 6.0 Protocol Exerciser

The **P5570A PCIe 6.0 Protocol Analyzer** enables deep protocol analysis of PCIe DUTs (devices under test) and systems in a form factor that is easy to deploy on the lab bench and offers unparalleled signal integrity. It is backward compatible with all previous generations of PCIe and the cableless design moves away from the conventional traditional setup, which means, no more cable mess. In addition to not having the need for a cumbersome external analyzer chassis, setup and versatility are improved and in addition, the small footprint for the full setup.

The **P5573A PCIe 6.0 Protocol Exerciser** supports protocol traffic analysis from 2.5 GT/s, PCIe 1.0 through 64 GT/s, PCIe 6.0 with lane width support of x1 to x16. The tool includes over 100 built-in LTSSM test cases, error insertion capability and a protocol checker platform. **RAS (Reliability, Accessibility and Serviceability)** testing is also available as an option for system and server environment tests.

CXL 1.1 / 2.0 Protocol Test

Compute Express Link (CXL) is an industry supported, high-speed interconnect standard that enables coherenet memory accesses between a host and an end-point device, such as memory expansion and hardware accelerators. CXL technology enables a more efficent use of resources for datacenters by sharing or pooling these resources to achieve higher performance, better workload balance, and optimal utilization of server resources.

CXL leverages the dependability and performance of the PCIe physical layer and uses a flexible processor port to auto-negotiation whether the link will commuicate using the standard PCIe protocol or the supported alternate CXL transaction protocol. CXL defines three sub-protocols CXL.io, CXL.mem, and CXL.cache that are used for initialization and link-up, and to facilitate the coherent sharing of memory between computing devices.

P5561CXLA CXL 1.1 / 2.0 Protocol Exerciser Software supports protocol traffic generation for all CXL 1.1 and 2.0 supported speeds and lane widths from x1 to x16. The CXL exerciser can emulate a root port or endpoint, generate FLIT traffic, and includes built-in LTSSM test cases, error insertion, and a protocol checker. The P5561CXLA software is used with the P5573A protocol exerciser hardware for an integrated, CEM add-in-card design which greatly simplifies the connection to the CXL device.

P5562CXLA CXL 1.1 / 2.0 Protocol Analyzer Software enables comprehensive analysis and visualization capabilities for CXL.io, CXL.mem, and CXL.cache. The protocol analyzer sits between the root port and endpoint to capture and decode the transactions on the CXL bus. The P5562CXLA software is used with the P5570A protocol analyzer hardware and offers a cableless CEM form factor for a robust and reliable setup that is easy to deploy on the lab bench and offers unparalleled signal integrity.

Your Pathway to PCIe 6.0

Keysight helps define the future of PCI Express as a representative on the PCI-SIG Board of Directors and a major participant in working groups. We provide the most complete and scalable PCIe testing solution showing the true performance of your design, improving your time to market, and streamlining your path to PCIe success. With Keysight you have excellent investment protection supporting your progress in the PCI Express Ecosystem from PCIe 4.0 (16GT/s) to PCIe 5.0 (32GT/s) to PCIe 6.0 (64GT/s). All these generations of PCIe technology can be supported with the same hardware platform.

Subscription bundles: Keysight offers subscription bundles on technology, rather than the generation of technology. All updates and future generations are included in the subscription. The model also offers the flexibility to stop, pause, or add subscription at annual intervals.

For more information: www.keysight.com/find/pcie