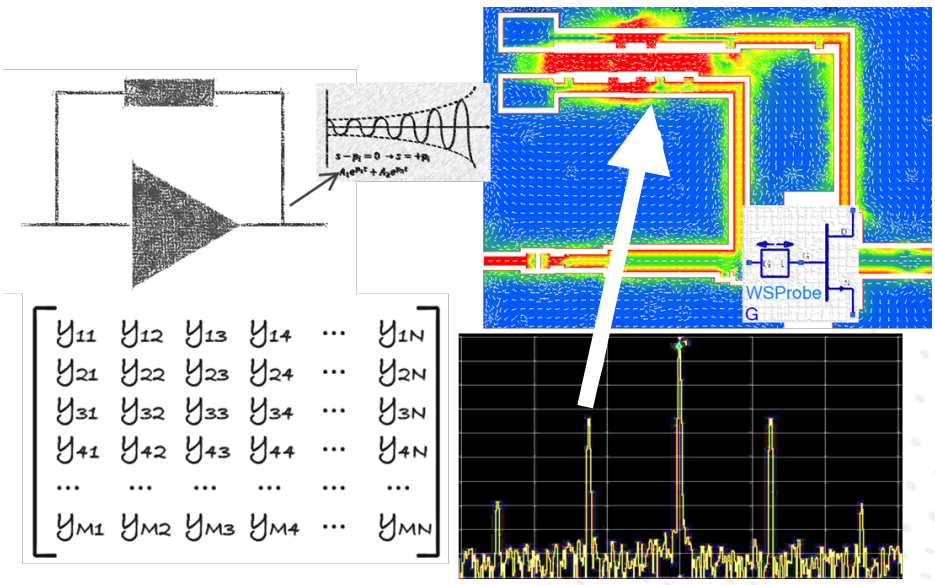
APPLICATION NOTE

Designing for Stability in High Frequency Circuits

PATHWAVE

This application note will help engineers understand how instabilities fundamentally arise in their circuit and illustrate how to troubleshoot and resolve these issues up front in the design process before manufacturing. This not only requires an understanding of classic theory and techniques, but also practical knowledge to apply these efficiently using modern design tools such as a novel new impedance probe called the WS-Probe.



KEYSIGHT TECHNOLOGIES

Abstract

Why should high frequency circuit designers consider stability early on in the design process? Isn't there enough to worry about just making the circuit function at the fundamental frequency? In the past, Microwave Engineers used to solve stability problems in the lab, perhaps adding bypassing or loss in a strategic location to stabilize their circuits. Stability was viewed as too complicated to model or predict, and the problems were usually easy enough to solve in the lab anyway. But things are changing. Across the entire wireless communications industry, standards are moving higher in frequency and systems are getting more complex. Instability arises from a combination of gain and feedback. In today's circuits, gain is higher due to increasing device f_T's, and feedback is more prevalent because features are more compact and resonate more easily with signals that have smaller wavelengths. At the same time, advanced packaging technologies make the internals of the circuit less accessible than in the past, meaning things are harder to fix after the fact in the lab, even with the most apt technicians.

To make circuits which meet the needs of modern communications systems, designers need to master stability by truly understanding the root causes of problems in the circuit before building a design. The problem: stability is a very complex topic. Most high frequency design engineers use only the classic "Rollett stability factor" to assess circuits, but this technique is based on assumptions which may not be valid for modern circuits. Besides, K-factor only applies to a two-port network at the external I/O's, while the circuit inside could be very complex and hinder visibility from the outside. There are many alternative techniques in the literature, but they are sometimes difficult to apply correctly, and furthermore it's not clear which one is best for any given application.

This Application Note will help designers understand how instabilities fundamentally arise in their circuit and illustrate how to troubleshoot and resolve these issues up front in the design process before manufacturing. This requires not only an understanding of theory and classic techniques, but also a practical knowledge of how to apply these techniques efficiently using modern design tools. This paper starts by reviewing the theory, discussing concepts like loop gain, return difference, and driving point impedance, and then expands to build a framework for applying these techniques to modern circuit design. The key is to use a new probe, called the WS-Probe, which has recently become available in Keysight's PathWave Advanced Design System (ADS), to derive the necessary stability measures quickly and efficiently. The probe allows application of multiple stability analysis techniques to the circuit post-simulation for both small and large signal analysis in a non-invasive manner. Multiple examples illustrate how to use the probe on real life circuits. After reading this Application Note, you'll look at stability in an entirely different way and the circuits you design will reflect that.

About the Author

Matthew Ozalas received his BSEE from Penn State University in 2001 and his MSEE and MBA from Arizona State University in 2010. From 2001 to 2005, he worked at the MITRE Corporation where he designed high frequency circuits for a variety of applications. From 2005-2013, he worked at Skyworks Solutions in the Santa Rosa Design Center, where he designed and developed multiband power amplifier and front-end modules for high volume wireless handsets. He joined Keysight in 2013, where he is currently working as an Application Developer and Product Owner for Advanced Design System. Matt admits that he has designed plenty of unstable amplifiers throughout his career and has spent months in the lab trying to figure out the root causes of stability problems in his circuits.

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Acknowledgement

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Introduction

Stability in modern wireless design: the perfect storm

Wireless technology is advancing faster than ever before. Whether you're working in Aerospace / Defense / Satcom, Commercial Wireless, or Automotive, the trends that are driving these businesses forward are twofold.

First, frequencies are increasing. Think about your car: a few years back, the highest frequency hardware might have been the FM radio. Now, most cars have some form of millimeter wave radar or sensors built in. Consider commercial cellular; frequencies increased very modestly between each new standard upgrade, about 1.4X over 17 years. Now, going from 4G to 5G, frequency increases by a factor of 38 – in just 12 years!

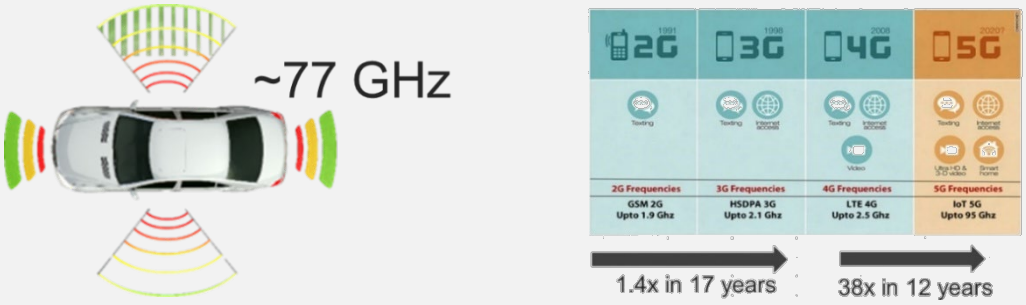
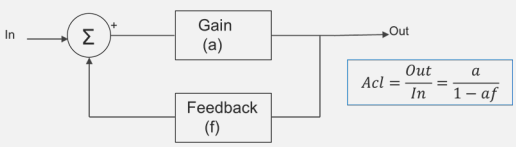


Figure 1. Millimeter Wave Radar on a car (left) and frequency increase between cellular standard upgrades (right).

Second, wireless communication systems are becoming very complex. For example, Aerospace/ Defense hardware designers cannot just build high performance, single functioning systems anymore. The systems also need to be flexible and reconfigurable, which leads to dense heterogenous integration. These heterogeneous designs are orders of magnitude more complicated than their traditional chip and board predecessors. At the same time, 5G cellular and automotive communications increasingly require MIMO (Multi-In-Multi-Out) configurations, which imply the need for beam steering phased arrays. These advanced systems used to be developed exclusively by defense companies – now they are being produced commercially at high volumes.

Both trends lead to many hardware design challenges; new circuit topologies are needed, antennas must be co-designed, digital and wireless blocks must co-exist in smaller spaces – but one unexpected nemesis could throw a wrench into all of this: amplifier stability is becoming a major problem with high frequency, tightly integrated circuits and systems. At first glance, this may seem a little surprising – stability has always been a circuit design challenge, but one that was manageable with best practices, basic simulation, and a little handiwork in the lab. Why is stability poised to become such an issue now?

To understand this, look no further than any college circuits textbook. In my old textbook [1], I found a great refresher on how instability arises from a combination of gain and feedback, illustrated in Figure 2.



A closed loop network is unstable when loop gain (af) is equal to 1

$$1 - af = 0 \Rightarrow af = 1$$

Figure 2. Gain / Feedback systems and the condition for instability.

Let's apply this understanding to the trends described above. First, frequency is increasing; among other things, this demands devices with higher gain. The reason is simple, gain tends to roll off at higher frequencies, so to get any gain at say 28 GHz, you'll need a lot of gain at lower frequencies to compensate the roll off. As frequency increases, wavelengths also get smaller and that means antennas get smaller too. That's great if you're building a phased array, but it implies that small structures on a chip or package can now start to look like antennas. Let's throw in the second trend – systems are getting complex, which means engineers must design more tightly integrated circuits to achieve the required functionality. Smaller resonant structures and tighter integration all but guarantees that the coupling will increase significantly in modern high frequency circuit designs.

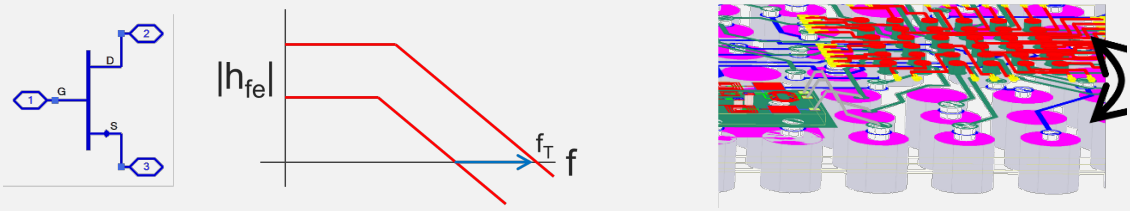


Figure 3. A combination of high transistor gain and integrated hardware increases potential for instability.

This knowledge together with the most basic understanding of stability in gain-feedback systems shows how the recent trends in the wireless space are leading to a perfect storm for stability problems in circuit design. Briefly, higher frequency devices have more gain and more feedback exacerbated by high levels of integration in modern systems. More gain plus more feedback … well, you get the idea. To make matters worse, advances in technology like Wafer Scale Chip Packaging implies that the circuit nodes which used to be accessible for cutting and soldering are no longer available for such freeform lab experiments, even with the most sure-handed technicians. So, it's necessary to understand stability problems up front, in the design phase, rather than solving them later in the lab as an afterthought. To do that, designers need new tools and techniques at their disposal. Why not just rely on traditional K-factor? Well, that may have been good enough in the past when you could mop up simulation inaccuracy in the lab, but it's no longer good enough today.

The Trouble with “K-Factor”

Rollett’s stability (K)-factor was originally a two-port measurement technique. These days, it’s often misapplied to CAD based simulation, which didn’t exist in any true form when John Rollett wrote his famous paper. Referring to the original work, you’ll find a short and often overlooked paragraph in this paper which states the following (now known as Rollett’s proviso):

“…provided also that the characteristic frequencies of the two port with ideal terminations (infinite immittances, i.e., open or short circuits, as appropriate) lie in the left half plane. This last condition will be assumed to hold in what follows…“[2].

In other words, K-factor analysis is valid if the network itself is known to be stable when ideally terminated. For measurement, this is a given; it’s not possible to consistently measure an unstable network. In simulation however, this is not true – a network with RHP poles inside will often converge and simulate just fine away from the unstable region. In the 1990’s, Struble and Platzker gave an example of such a network – a ring oscillator which has a very stable K-factor yet can be shown to oscillate [3]. Figure 4 shows the circuit and results.

Another problem with K-factor is that it applies only to two port linear networks, which is fine for a simple amplifier, but gets harder to justify in today’s world of multi-stage, coupled complexity. The K-factor says nothing about the stability of what’s inside the network – it only provides a view from outside, which can obscure the true stability of the internal nodes within the two-port network. For example, loss between an input port and an internal node may obscure an internal negative resistance buried inside the circuit.

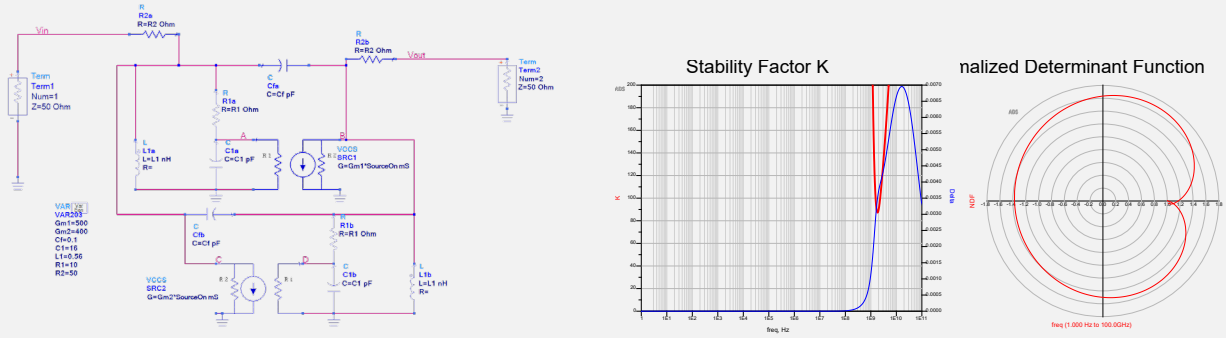


Figure 4. Struble and Platzker’s Classic Ring Oscillator, showing stable K-factor but unstable Normalized Determinant

To be clear, the above discussion is not meant to imply that K-factor is useless, rather, it’s simply pointing out some reasons why this measure may not be entirely sufficient for today’s hardware designers. When designers understand and manage the limitations, K-factor is a great tool to quickly assess stability across both frequency and load value. Sometimes though, it’s just not possible to know for sure whether the K-factor is valid, which makes double checking the network with different approaches wise. What other techniques could validate the proviso or at least scrutinize the network to understand if the K-factor result is likely accurate? Fortunately, there are many stability techniques to choose from. Unfortunately, it’s not always easy to understand or set up different simulation testbenches to try out each one. In the next section, we’ll review a few classic techniques to analyze stability.

Background

Feedback Theory

Returning to the classic Amplifier/Feedback example from my college textbook (Figure 2), it's easy to derive the transfer function by following the signal through the amplifier then through the feedback network and back to the input. The transfer function takes the following form:

$$Acl = \frac{Out}{In} = \frac{a}{1-af} \quad \text{(Eq 1)}$$

Since both the numerator and denominator terms are S-domain equations, it's possible to factor them into roots, which represent zeros in the numerator and poles in the denominator. The denominator terms are separated using partial fraction expansion, leading to an S-domain equation with the form as follows:

$$Acl(s) = \frac{A(s)}{1-A(s)F(s)} = \frac{(s-z1)(s-z2)\ldots}{(s-p1)(s-p2)\ldots} = \frac{A_1}{(s-p_1)} + \frac{A_2}{(s-p_2)} \quad \text{(Eq 2)}$$

If you didn't memorize your Laplace transform table, here's a brief refresher. Equations with the form "A/(s-p)" in the S-domain map to an exponential term in the time domain which either grows or shrinks depending on the sign of the exponent. Poles with positive S-domain values result in positive exponential terms which are of course unstable because they grow to infinity.

$$\frac{A_1}{(s-p_1)} + \frac{A_2}{(s-p_2)} \Leftrightarrow A_1 e^{p_1 t} + A_2 e^{p_2 t} \quad \text{(Eq 3)}$$

Plotting these positive-valued poles in the complex S-domain indicates they end up in the right half of the S-plane, which means the system is unstable (Figure 5). The right half plane is real estate to avoid if you're an amplifier designer.

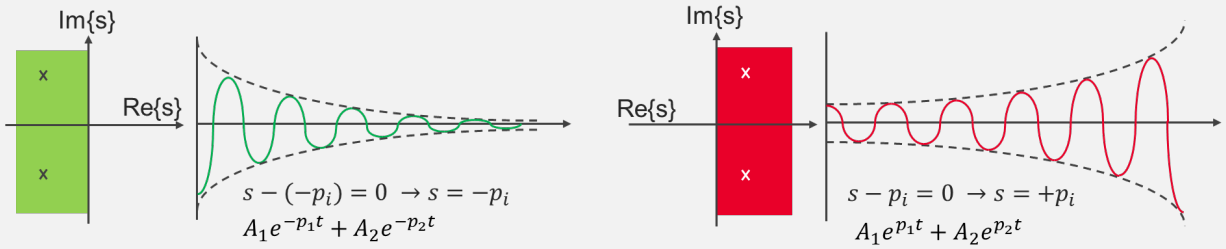


Figure 5. Time domain response for systems with poles in left half plane vs. right half plane.

To detect zeros or poles in an arbitrary system, engineers often take advantage of *Cauchy's Argument Principle*. This states that values along a closed contour on the S-plane passed through a transfer function will have an output which circles the origin clockwise equal to the difference between the number of poles and zeros contained in that contour. Figure 6 illustrates the principle.

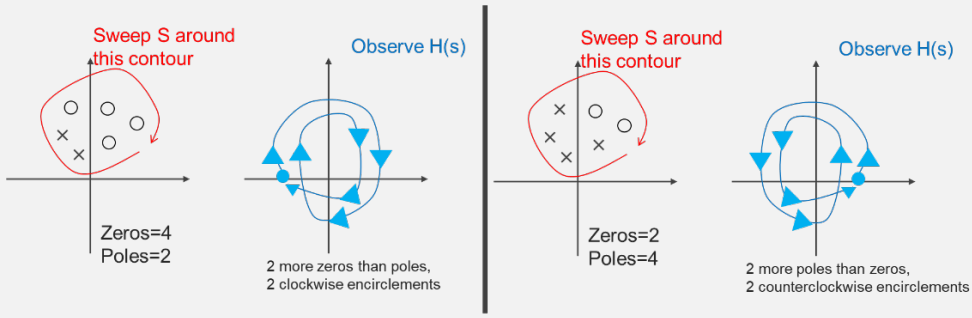


Figure 6. Cauchy's Argument Principle: send an S-domain contour through a transfer function, observe encirclements

It's possible to create a contour which covers the entire right half of the S-Plane by simply sweeping frequency from negative infinity to infinity for a given transfer function (the details of how that works are widely documented, but beyond the scope of this paper). To evaluate the gain-feedback-network transfer function described above for RHP poles, engineers often look at the denominator to find zeros, which are poles in the overall transfer function. Since the loop gain term "af" is in the denominator, it's easy to simulate or measure that term over frequency, plot it on the S-plane, and look for clockwise encirclements. This analysis is referred to as a Nyquist plot. It's worth noting that some engineers prefer to plot the entire denominator, 1-af, which would encircle the origin point (0,0), while others prefer to simply plot loop gain af, in which case they look for encirclements of (1,0) on the complex S-Plane.

$$Acl(s) = \frac{A(s)}{1 - A(s)F(s)}$$

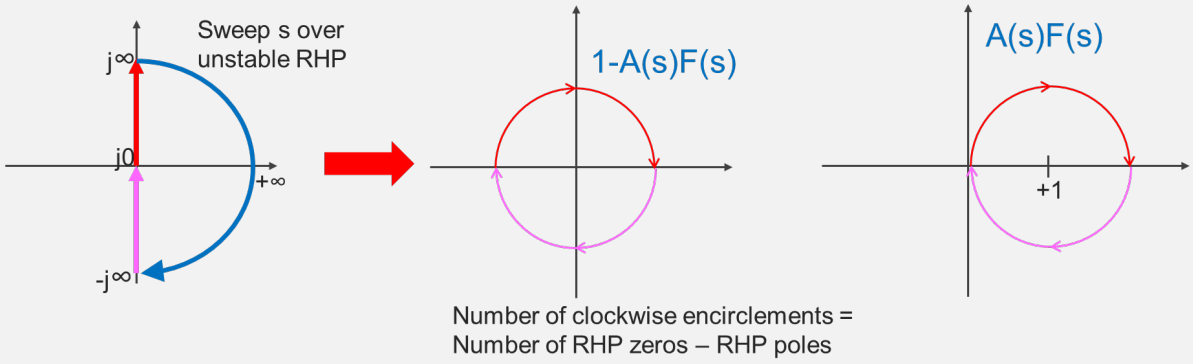


Figure 7. Evaluating a transfer function by sweeping the Right Half Plane and observing encirclements.

Techniques to compute loop gain

In the most basic sense, computing loop gain simply involves breaking the loop, injecting a test signal, and observing the return, either by analyzing gain and phase margin (Bode plot), or clockwise encirclements on a polar plot (Nyquist Plot). However, there are lots of fine details which make doing this a considerable challenge, especially for high frequency circuits.

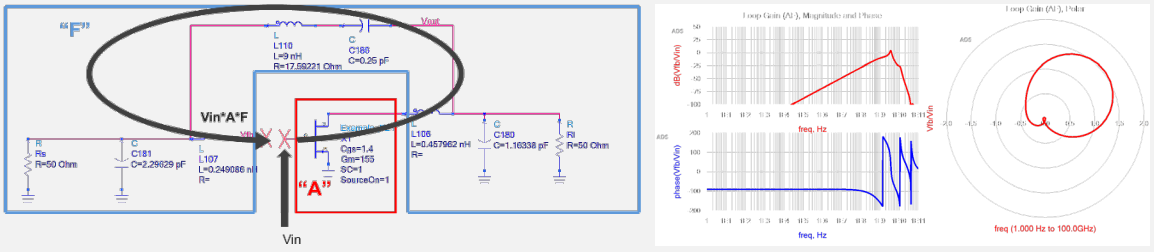


Figure 8. Measuring Loop Gain in a simple circuit.

'Osctest' is the first technique we'll cover – this is a classic oscillator stability analysis tool which is probably the most widely used loop gain technique applied to high frequency circuits. First, the loop is broken, and a circulator is placed inside the break along with a termination, as shown in Figure 9. The circulator configuration is such that the incident wave from the termination is directed into the loop, while the return signal at the other side of the loop break is directed back to the original termination emulating the reflected wave. In this manner, the single port S-parameter from the termination represents the entirety of loop gain, which is a compact way to represent it. There are two main sources of inaccuracy with Osctest. First, the termination applied is arbitrary and does not represent the actual closed loop impedance seen by the return signal. This means that the loop gain is sensitive to break location and termination impedance. Second, the circulator forces the signal to flow in only one direction: in reality, signals flow bidirectionally.

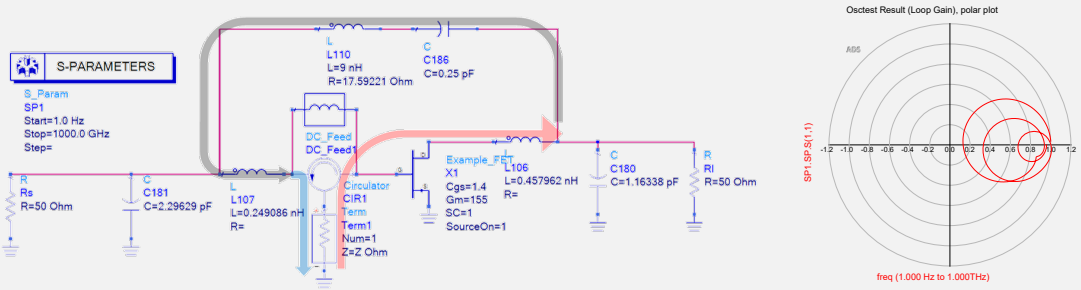


Figure 9. The classic "Osctest" method to derive loop gain

In the 1970's, Dr. Middlebrook came up with a technique to make the loop gain measurement insensitive to break location by using a dual voltage and current injection which self-compensates for impedance variation [4]. However, Middlebrook's technique still suffers from the assumption that the signal flow is unilateral. The approach can be emulated in simulation using an AC voltage and current source and processing the return values using equations (Figure 10).

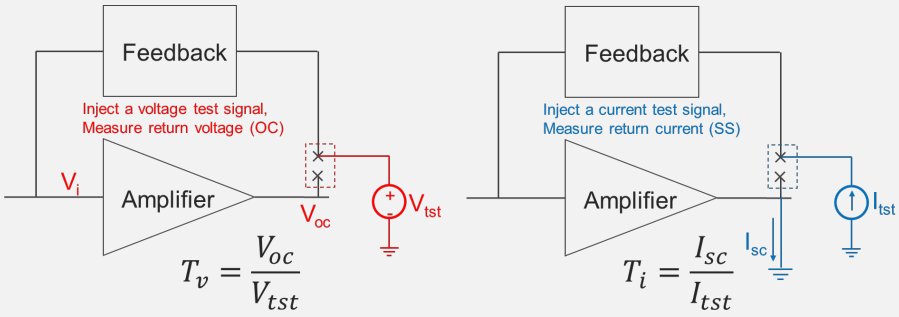


Figure 10. Middlebrook's Null Double Injection Loop Gain technique (adapted for simulation environment).

In the 1990's, Dr. Hurst presented a technique to account for bilateral signal flow by representing the amplifier and feedback blocks as separate Y-parameter networks, then cleverly combining the forward and reverse flow terms in parallel to derive the resulting bilateral loop gain [5], (Figure 11). This provided an easy way to compute bilateral loop gain, however, the simplification of a transistor or amplifier into a single grounded admittance block can lead to significant errors for more realistic cases. It's worth nothing that Hurst was actually pointing out the shortcomings of the loop gain techniques in general, and the need for a more fundamental approach to ultimately determine the stability of an amplifier, rather than seeking to provide a perfect technique for computing loop gain.

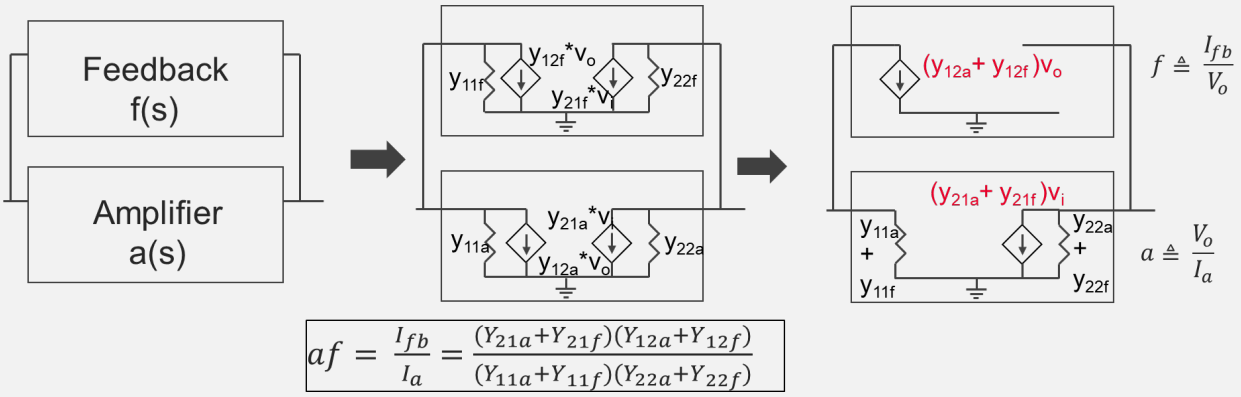


Figure 11. Hurst's computation of loop gain combining Y-parameters of gain and feedback networks.

In the early 2000's, Dr. Tian revisited Middlebrook's earlier work and extended the loop gain computation to the bilateral signal flow case [6]. While the computation was rather detailed, the result was represented in simple terms based on the Y-parameters of the amplifier, or combined amplifier-feedback network, shown in Figure 12. The advantage of this approach is that it is both insensitive to impedance variation along the loop thanks to the dual injection approach, and it also considers signal flow in both directions. However, as with Hurst's loop gain, the representation of a complex transistor or amplifier model with an ideally grounded admittance network is an oversimplification which can lead to practical inaccuracies for cases where the dependent source is ungrounded.

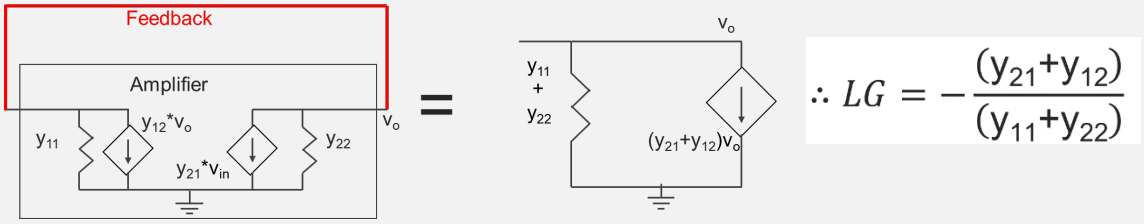


Figure 12. Tian's extension of Middlebrook's Loop Gain to make it bilateral.

Each of the loop gain techniques described so far were applied to a simple test circuit consisting of a transistor with passive feedback across the I/O terminals, along with input and output matching networks, as shown in Figure 13. The feedback network was configured to make the amplifier close to instability, so that each technique could be evaluated for the marginally stable case. The "transistor model" consists of both a controlled current source for the gain and a set of surrounding parasitics. Often, designers are not able to access this internal level of the model, so they are inclined to treat the entire device as the amplifier, even though the parasitics are technically part of the feedback network. Similarly, it may be tempting to consider the feedback to be only the direct connected passive elements across the transistor I/O terminals. However, to represent the circuit in the classic "amplifier-feedback" block topology, everything not designated as the amplifier is by definition the feedback network. So, the feedback network must also technically include the input and output matching and terminations. For this case, the entire transistor is treated as the amplifier (pretending as though the internal nodes were not accessible) and the loop was broken at the transistor's external gate input.

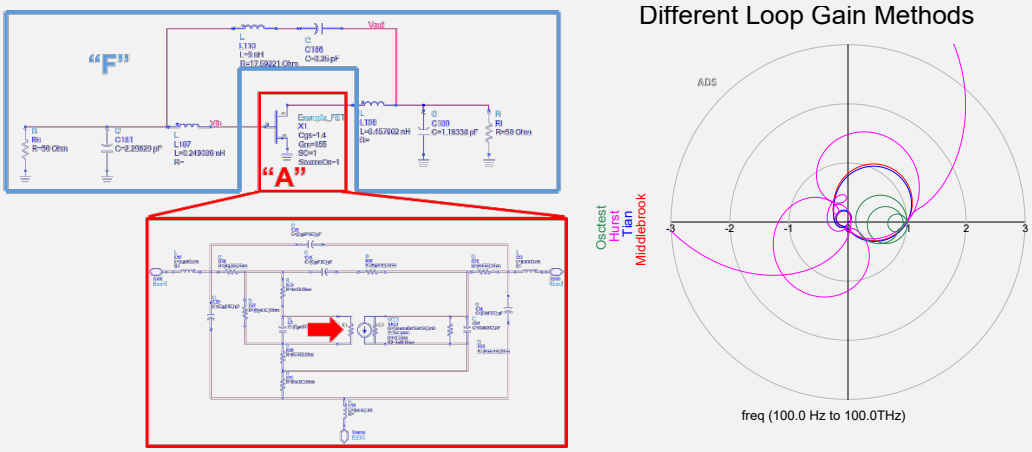


Figure 13. Four different loop gain methods applied to a simple transistor-feedback circuit. Which result is correct?

The results from each of the loop gain techniques applied at the input to the transistor were plotted in Figure 13, and the result observed for clockwise encirclements around the point (1,0), which indicate RHP poles in the full transfer function (or alternatively, zeros in the denominator of the transfer function). Note that each technique gives a different result on a polar plot. Even though there is some relative convergence near the point of instability, (1,0), the different techniques do give contradictory results on whether this circuit is stable. The natural question to ask: “which result is correct?”.

Besides the nonidealities already described so far, there are two more reasons why loop gain approaches can be flawed. The first reason is visibility. Loop gain analysis will only work if you are inside an unstable loop. It’s possible that another loop outside of the loop under analysis will be unstable, and you may not be able to observe that instability without breaking the unstable loop itself. This is a big problem for microwave transistors because the internal parasitics could have multiple self-contained loops which are entirely inaccessible to the end user. For example, if a user cannot access the network inside the red box in Figure 13**,** they will not be able to break and observe the loop gains through the transistor parasitics, which may cause instability. The second reason goes back to the idea that encirclements represent the *difference* between poles and zeros in each transfer function rather than the absolute value. Perhaps in the loop gain term, there are RHP poles which cancel out RHP zeros. If that is the case, there could be no encirclements observed even for an unstable system. Put another way, there are two unknowns (i.e. RHP poles, zeros), and only one equation (i.e. encirclements = poles - zeros).

As before with K-factor, all of this may leave you feeling a little uneasy about relying on classic loop gain techniques. At this point, you might ask: “if this is not rigorous, what is?”. Let’s explore that concept.

Rigorous Stability Analysis Techniques

To understand what it takes to achieve a rigorous answer to stability, it helps to study Dr. Bode's 1943 work: "Network Analysis and Feedback Amplifier Design" [7]. First, some historical context: the amplifier-feedback model described earlier was introduced in the 1930's by Harold Black and had already been around for some time before Bode's breakthrough work [8]. In fact, Bill Hewlett was even using some of these feedback techniques in 1939 to design early measurement test equipment [18], some of which is currently on display at Keysight's Santa Rosa headquarters [19]. Bode grappled with the same challenges regarding stability that were described in the last section and sought to develop a general definition of feedback to "avoid the ambiguities and uncertainties which appear if we rely exclusively upon an analysis in terms of separate u and B <gain and feedback> circuits". Bode examined in his work how instabilities manifest into a system. He described two views of a system: first, as a set of nodal equations, and alternatively, as a gain-feedback transfer function similar to the ones covered in the prior section. For each view, he derived a fundamental, rigorous measure to characterize the system; for the nodal network, "Driving Point Impedance" and for the transfer function network, "Return Difference".

In the first paradigm, Bode described a circuit as defined by a set of nodal equations. The solution to these equations is the steady state response of the overall system, as in Figure 14. When analyzing a node, it's helpful to view the surrounding circuit as providing a stimulus to, or "driving", this node by way of a voltage or current. Then, the node responds to this stimulus as predicted through the set of equations. But what if there is some nontrivial condition where a node under analysis does not respond to the normal drive from the circuit? It means the node has a steady state solution independent from the rest of the circuit, it's oscillating. That happens when the impedance is infinite because any current added does not change the voltage. Or, it happens if the node's impedance is negative, because such a node responds by outputting more energy than the surrounding circuit puts in, thereby acting as a source.

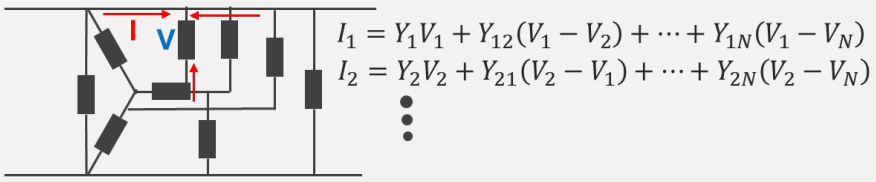


Figure 14. A circuit is defined by a set of nodal equations. Each internal node is "driven" by the rest of the circuit.

Mathematically, Bode defined the driving impedance as the ratio of the network determinant to the same determinant with the node removed entirely from the matrix. For example, in Equation 4 below, k refers to the kth node of the network matrix. Therefore, it's possible to compute driving point impedance for any node in any given network.

$$Z_{dp(k)} = \frac{\Delta}{\Delta_{kk}} \qquad \text{(Eq 4)}$$

Also, the inverse of the driving point impedance (the “driving point admittance”) is valid to consider and is in some cases more useful to analyze. But first, what does it mean to remove a node from a matrix? Let’s consider the previous amplifier-feedback circuit to analyze the driving point admittance of the input node. In the circuit simulation, a simple set of two port parameters is used to derive the Z-or Y matrix, for example from terminations applied to the I/O’s. The determinant of the resulting 2x2 matrix is computed trivially as:

$$[Y] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \rightarrow \Delta = y_{11}y_{22} - y_{21}y_{12} \qquad \text{(Eq 5)}$$

To “remove” node 1 from this matrix (the input), exclude both the row and column containing it. So, the first row and the first column are removed from the matrix, leaving behind only one term: Y_{22}. The determinant of a one element matrix is just the element itself, so that is the denominator in the Equation 4 (the Δ_{11} term):

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \rightarrow [y_{22}] \qquad \therefore y_{dp(1)} = \frac{y_{11}y_{22} - y_{21}y_{12}}{y_{22}} \qquad \text{(Eq 6)}$$

A more practical way to compute driving point impedance in modern software tools is to stimulate a node with non-perturbative auxiliary generator, which can be either a voltage or current source [9]. It’s important that this source does not disturb or load the existing circuit in any way. Conveniently, this feature exists in most modern simulators, which can perform such an operation as a matter of course. Performing a source frequency sweep allows for observation of both the injected term (i.e. current) and the response term (i.e. voltage). From there, its trivial to compute driving point impedance or admittance from these results, as shown in Figure 15.

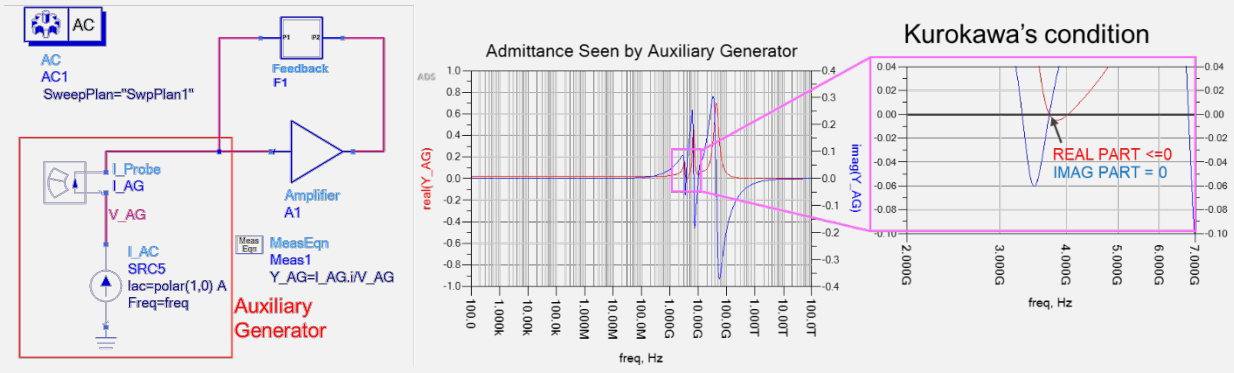


Figure 15. Computing Driving Point Admittance using an auxiliary generator and monitoring for Kurokawa’s condition.

It's possible to analyze driving point admittance to extract specific unstable poles and zeros using custom software tools [16], but it's also just as easy to search for response points which meet Kurokawa's condition for autonomous (self-starting) oscillation. This condition is: zero or negative real part with zero imaginary part, where the slope of the imaginary term is increasing with respect to frequency as required by Foster's theorem. Practically speaking, the reason to use admittance instead of impedance when looking for instability is the admittance detection searches for zero, while the impedance detection searches for infinity. Figure 15 shows the driving point admittance for the input node of the test circuit, plotted vs. frequency. Note that Kurokawa's condition occurs at about 3.7 GHz.

An alternative view put forth by Bode presented a system as a gain-feedback style transfer function, which should already be familiar from the preceding discussion. Bode introduced two fundamental terms which parallel the transfer function denominator ("Return Difference") and loop gain ("Return Ratio").

The difference between Bode's definitions and the prior loop gain terms resides in the fact that Bode performed the analysis directly at the *ideal active transconductance element* in the circuit. Analyzing the circuit at the dependent source takes care of one of the problems discussed earlier: by operating at the internal active node, the analysis accounts for all possible feedback loops, including through device parasitics, and therefore provides the rigor missed in the earlier loop gain analysis. Essentially, Bode's Return Ratio is the negative loop gain across the ideal generator internal to the active device; the negative value is a convention defined by Bode.

In addition to the circuit definition, Bode also described the Return Difference for a network mathematically as a ratio of determinants. Return Difference is the network determinant divided by the same determinant but with the active elements removed from the matrix, as described in equations 7,8.

$$F = \frac{\Delta}{\Delta_0} \qquad \text{Return Difference} \quad \sim (1\text{-af}) \tag{Eq 7}$$

$$-T = 1 - F \qquad \text{Return Ratio} \quad \sim \text{af ("Loop Gain")} \tag{Eq 8}$$

What does it mean to remove active elements? It's possible to do this in the example circuit discussed earlier by simply setting the dependent gain term to zero. Practically, the dependent source contains a toggle variable, "On". If this variable is set to 1, the source behaves as normal; when it's set to 0, the active gain term is off. High impedance terminations are placed at the four ports of the active source to avoid loading the network, and an admittance matrix is derived based on these terminations. From there, it's possible to compute the determinant for the condition when the source is on and divide by the determinant for the condition when the source is off, as illustrated in Figure 16.

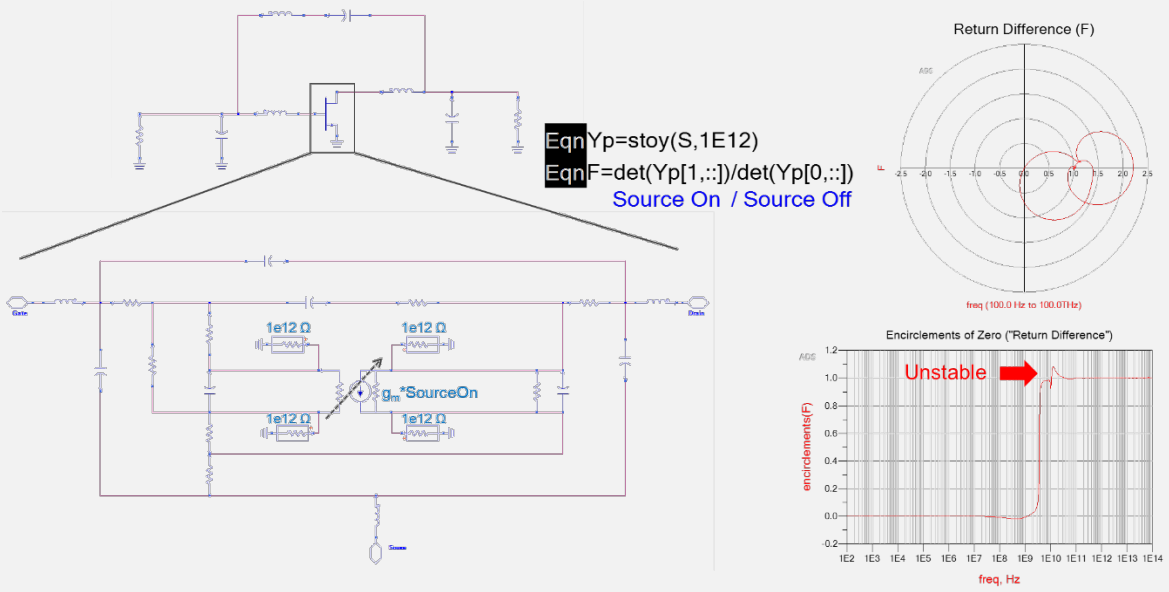


Figure 16. Computing Return Difference by going inside the transistor and toggling the active source on and off.

Figure 16 also shows a plot of encirclements from the computed Return Difference. It's worth noting that the same result can be obtained from a different simulation where the input connection to the dependent source is broken, an AC source is connected to the active generator input, and the loop gain is computed based on the return voltage across the generator input, as shown in Figure 17. So, the internal loop gain style method when applied across the active generator is equivalent to the determinant method.

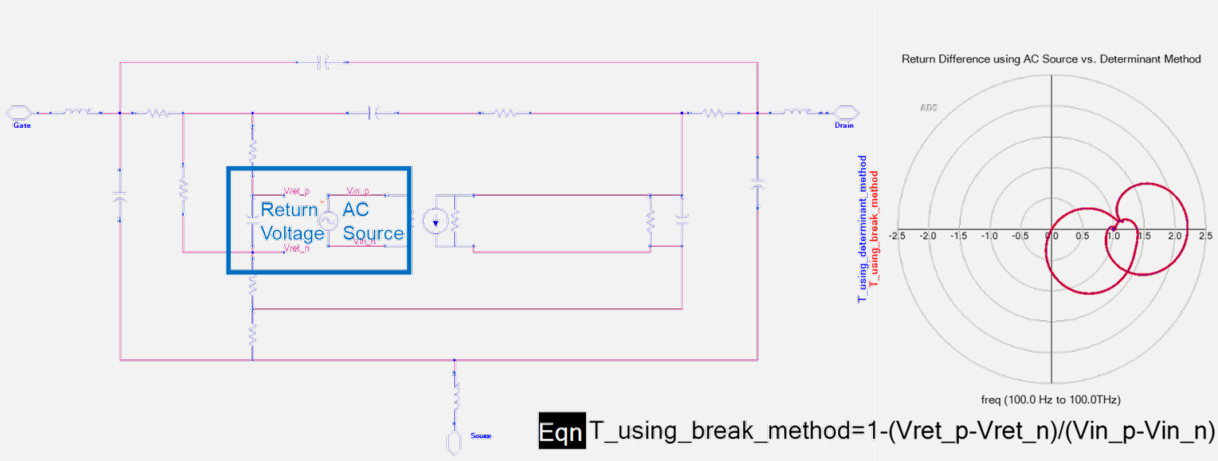


Figure 17. Computing Return Difference by breaking the active source input, applying an AC source, and observing the return control voltage. These results match the prior computation of return difference using network determinants (the blue curve on the polar plot).

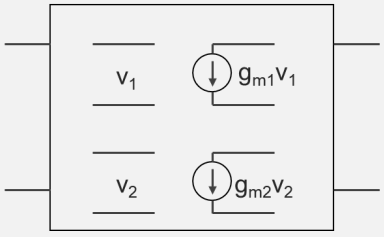
The mathematical definition of Return Difference (Equation 7) contains the secret to its rigor. Recall from Cauchy's Argument Principle that loop gain encirclements represent the *difference* between RHP zeros and poles. Without knowing the number of poles, one cannot know the exact number of zeros. However, the mathematical definition of Return Difference which Bode derived ensures that *no poles can exist in the function denominator* because there is no active element, thereby guaranteeing a stable denominator. As a result, unlike loop gain, observing encirclements for Return Difference is a *rigorous* way to account for the true number of RHP zeros in the transfer function denominator. The encirclements observed will exactly match the number of RHP zeros. This was indeed a profound realization.

Modern Implementations

One problem with applying Bode's original work on Return Difference to today's designs is that most modern circuits have many active sources, in fact, sometimes there are even multiple active sources inside the same transistor. In the 1990's, Struble and Platzker presented a methodology to apply Bode's original Return Difference concept to networks containing multiple active sources, termed "Normalized Determinant Function", or NDF [10]. Briefly, Struble and Platzker showed how to decompose an arbitrary network with multiple sources into the product of individual Return Ratios for each source. In aggregate, this produces a set of network determinants where the numerator contains all the active source terms and the denominator removes all the active terms, ensuring a similar rigor to Bode's original Return Difference computation, but extended to an arbitrarily large network (Figure 18).

$$NDF = \frac{\Delta}{\Delta_{0N}} = (RR_1 + 1)(RR_2 + 1)(RR_3 + 1) \ldots (RR_N + 1)$$

Accounts for multiple sources



$$\begin{bmatrix} y_{11} & y_{12} & y_{13} & y_{14} & \cdots & y_{1N} \\ y_{21} & y_{22} & y_{23} & y_{24} & \cdots & y_{2N} \\ y_{31} & y_{32} & y_{33} & y_{34} & \cdots & y_{3N} \\ y_{41} & y_{42} & y_{43} & y_{44} & \cdots & y_{4N} \\ \cdots & \cdots & \cdots & \cdots & \cdots & \cdots \\ y_{N1} & y_{N2} & y_{N3} & y_{N4} & \cdots & y_{NN} \end{bmatrix}$$

Figure 18. Expanding Return Difference to Normalized Determinant Function by considering multiple active sources.

The circuit example described earlier, modified to contain a *parallel* set of transistor amplifiers, illustrates practical computation of the Normalized Determinant Function (Figure 19). In this case, the active source toggles on/off for both transistors, with terminations placed across each active generator. This results in an 8x8 admittance matrix (double the size of the single transistor case) for both the on and off condition. The ratio of determinants is polar plotted to observe clockwise encirclements as before. One final note: it's necessary to preserve the DC bias conditions when the source is off to maintain accuracy in the computation; this is a detail which engineers often miss.

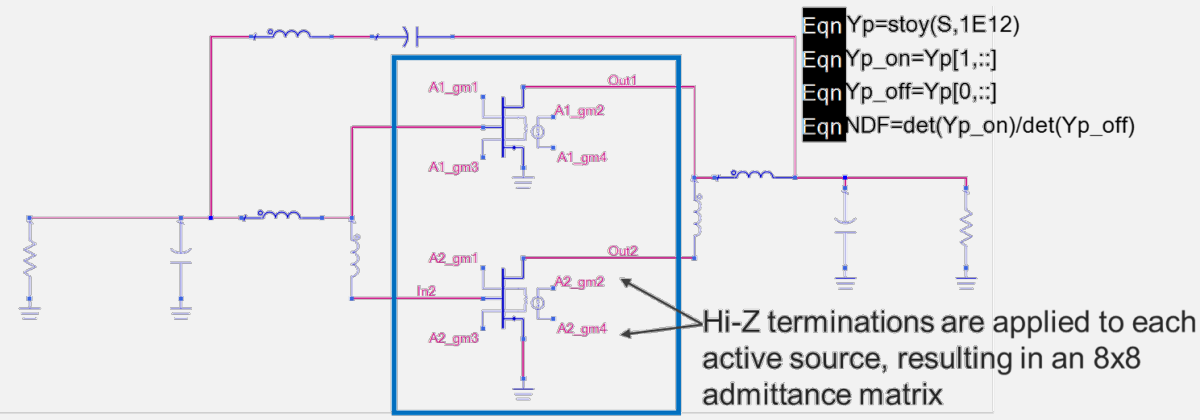


Figure 19. NDF for example circuit with two transistors, where the active sources are toggled on and off together.

The Normalized Determinant method is elegant in the sense that it is rigorous and potentially global in scope, however there are still some practical challenges to implementing NDF on modern designs. The biggest challenge is the need to both access and toggle off the embedded sources in each circuit. In many cases, designers are using encrypted models provided by a foundry, or even black box models such as X-parameters, and it is just not possible to access or turn off the internal sources for these devices. Attempts to cancel or estimate the “turn off” condition in other ways have been proposed, however, these may be prone to large errors if done incorrectly. The second practical challenge comes down to the matrix math itself: some circuits have many transistors, resulting in a very large matrix whose determinant may take a long time to compute. This is obviously improving with better processing speed and algorithms, however, at the same time, circuits are also becoming larger and more complex leading to even larger matrices. A third challenge revolves around the need to sweep frequency over a wide range to properly observe encirclements: from very low frequencies up to 100+GHz, so that the functions can stabilize properly. This becomes an issue when electromagnetic blocks are part of the circuit analysis, because the EM simulation frequency must also extend over the range of the NDF computation. Practically, this means designers need to run EM sweeps far beyond the typical passband of the circuit, which can add considerable time and complexity to the analysis.

Because of these limitations, most designers do not compute NDF in the manner described above. For models where the internal nodes are not accessible, but the source is togglable, it makes sense to apply high impedance probes at the *external* transistor I/O ports as close to the intrinsic sources as practical. For the circuit in Figure 19, applying terminations at the *external* gate and drain nodes, as shown in Figure 20, accomplishes this. Since the sources are ground, it’s not possible to probe the negative terminal in any meaningful way, so the matrix size in Figure 20 reduces to 4x4 rather than 8x8 for the earlier internally accessible case (Figure 19). The resulting NDF does show the instability, however, the curve *does not* match the original NDF derived across the internal current generator. This is due to removing the negative terminals entirely from the matrix. So, it’s possible to lose information and therefore some of the rigor by simplifying the matrix to include only the externally accessible nodes.

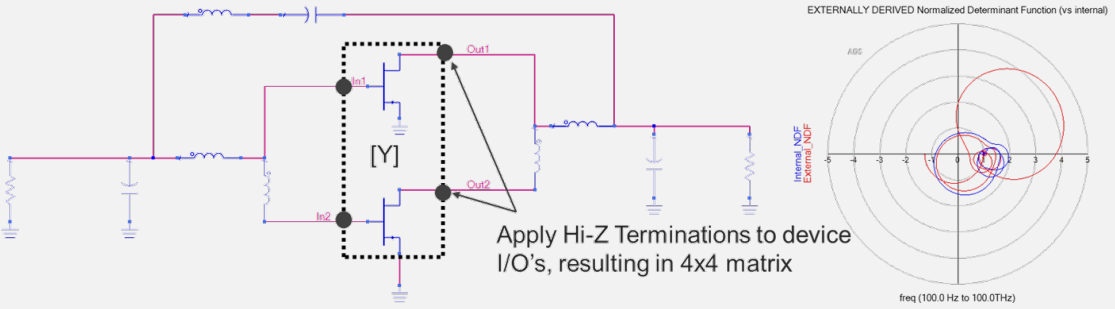


Figure 20. Approximating NDF by probing external transistor I/O nodes. The result does predict instability correctly but does not match the NDF derived internally. The matrix size reduces due to inaccessible device nodes.

Even with the simplification for cases with only external nodes accessible, Normalized Determinant is still the "gold standard" of stability analysis because it can catch an instability which arises anywhere inside a circuit. If you can toggle or accurately cancel the active source, this is typically the best way to verify that your complete design is in fact stable.

Active-Passive Circuit Bifurcation

An alternate approach described in the 1990's by Dr. Ohtomo allows for a similar type of global, rigorous stability analysis without needing to access or shut off the intrinsic elements or compute a large determinant [11]. In Ohtomo's method, the circuit bifurcates into two networks: one contains the passive elements and other contains the active elements (Figure 21). Next, circulators and isolators are applied in an iterative manner to each of the *interface nodes* which connect the active and passive networks together, resulting in a type of loop gain response. Analysis of the complete set of loop gains for all interface nodes determines the overall stability of the combined network by observing encirclements.

This technique was shown to be rigorous if each of the two network halves are independently stable, which makes it practically applicable to cases where well-behaved transistors are used as part of a larger, more complex circuit design with many potential feedback loops.

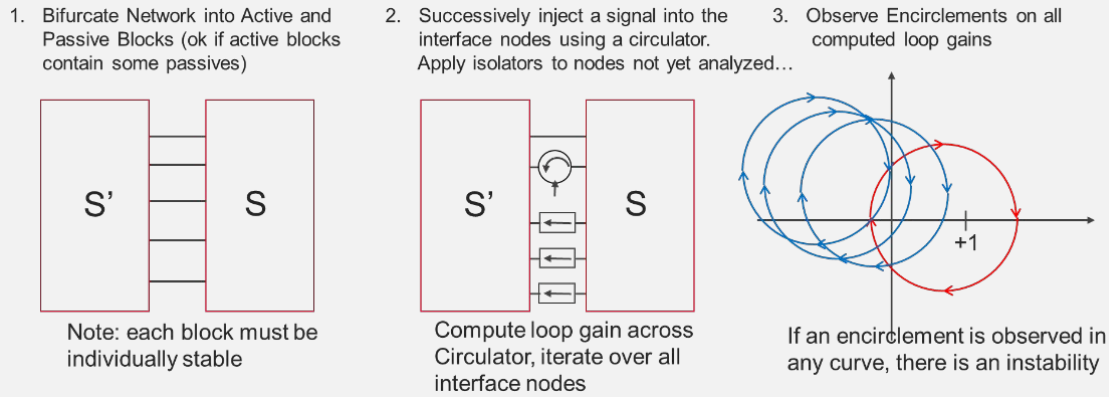


Figure 21. Bifurcation of circuit into active and passive imbedding network, iteratively analyzing loop gain at interface.

Let's analyze the previous two-transistor circuit (Figure 20) using Ohtomo's method in Figure 22. Since there are two transistors, there are four interface points: the gates and drains for both devices. It's necessary to run one simulation per interface. In the first simulation, the input to the gate of the top transistor is cut and a circulator and termination are added to compute loop gain in a manner identical to the Osctest method described earlier. For the second simulation, an isolator replaces the input circulator and a new circulator and termination connect to the top transistor's drain (interface 2), pointing towards the active element. Consistency is important here: if the first circulator points towards the active network, all subsequent circulators and isolators must do the same. For the third simulation, another isolator replaces the previous circulator, and new a circulator/termination connects to the bottom transistor's gate. And finally, the process repeats for the drain of the fourth transistor. Analysis of the four separate loop gains computed from the set of simulations (these are the S-parameter terms) indicates instability through encirclements of (1,0). The third interface node shows instability, agreeing with the previous NDF assessment.

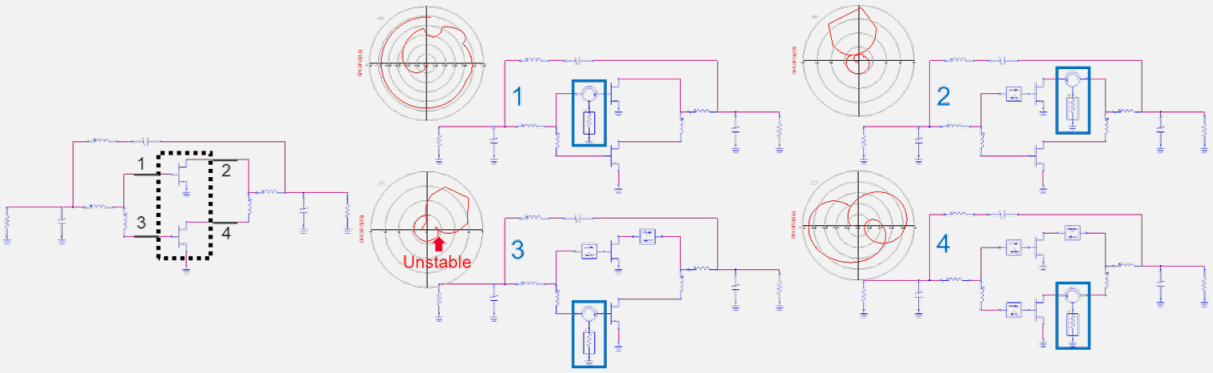


Figure 22. Bifurcation analysis at interface nodes on a test circuit, with circulators and isolators added. Loop gain is analyzed for encirclements.

Besides the need for individually stable subnetworks, the disadvantages to this method are that the iteration is tedious, and you need multiple simulations or copies of the original circuit to make the analysis. This may be the reason why Ohtomo's method never gained wide adoption across the industry, despite its potentially significant advantages over other techniques.

Summary of Techniques

So far, we've studied K-factor, several loop gain techniques, driving point admittance, return difference / NDF, and active/passive bifurcation for stability analysis. K-factor and loop gain are useful, but not rigorous. Driving point admittance is rigorous for a given node and easy to compute, but it's not global. Normalized Determinant is rigorous and global, but access and computation can be problematic. Network Bifurcation is rigorous and global, but the individual active block must be stable, and the iterative method is tedious to implement. If you're wondering why there are many stability analysis techniques out there, the short answer is that no one technique is perfect for every situation. There are clear pros and cons to each approach.

Even though some designers will swear on one "tried and true" method, the reality is that when viewed in aggregate, the techniques are actually quite complementary to one another (Figure 23). For example, loop gains are not rigorous, but the results are easy to understand and make troubleshooting straightforward (i.e. just reduce the gain response). Driving point analysis is easy to implement on a suspect node and is rigorous, but it gets more complex when you consider applying this technique to multiple nodes. NDF is global and works well as a final "verification" step for a complex design, but it doesn't give much root-cause insight, and also there are practical challenges to implementation. Finally, Network Bifurcation is a nice way to get a global analysis for situations where NDF is not feasible, but it's tedious to compute and the blocks must be individually stable. But what about combining techniques? For example, pairing loop gain with driving point admittance provides the rigor of Bode's technique with the design intuition that comes from minimizing loop gain resonances. Going a step further, adding NDF or Network Bifurcation gives a more global view. And, if validated by other means, K-factor includes all viable external source and load combinations in one easy sweep.

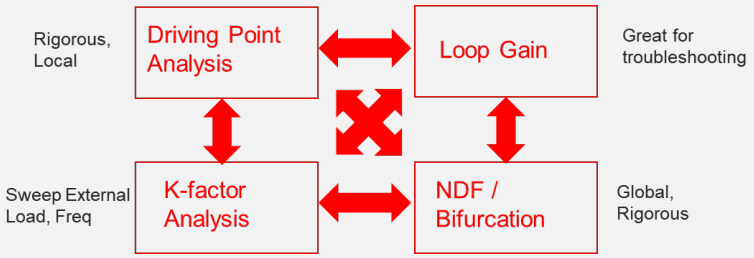


Figure 23. Stability analysis techniques are complementary to one another.

The only problem with using the techniques together (or perhaps a good argument for picking only one technique) is that each requires a different approach, resulting in a separate simulation testbench to derive the results. For example, to compute loop gain, it might be necessary to break a loop or inject voltage and current. Driving point analysis requires adding an auxiliary generator. NDF or Return Difference requires probe terminations and a source toggle sweep. Network Bifurcation requires analysis at each interface node. There are plenty of opportunities for error in this manual simulation paradigm. Speaking from experience, just setting up the proper testbenches can take hours. But circuits are becoming more prone to stability problems, so perhaps a more modern automation approach can help. While some tools offer to automate one or two specific techniques, none so far have demonstrated a true ability to automate many techniques at once in a simple enough manner to be usable to modern circuit designers.

A Modern Approach to Stability Analysis

Unifying Stability Analysis Techniques: The WS-Probe

It may not seem likely, but the key to solving the huge challenge described in the last section starts with a simple, mostly forgotten probe that microwave designers have used on matching networks for many years. But before we get there, it's helpful to ponder what, if anything, the stability techniques in the prior section have in common? The answer is admittance networks – the same networks which Bode manipulated to derive his rigorous figures of merit back in the 1940's. After all, Bode eloquently described Return Difference not just in terms of circuit manipulation, but rather in admittance network determinants. Similarly, although modern simulation tools use an auxiliary generator to compute Driving Point Admittance, admittance network determinants were the terms used in the original derivation. Ohtomo's method uses a bifurcation based on S-Parameters, but it's just as easy to convert these to admittance matrices for mathematical purposes. Even the loop gain techniques such as Hurst's approach were straightforward manipulations of gain and feedback admittance blocks. In fact, just about every stability metric described so far can be arrived upon by clever manipulation of admittance matrices.

The question now becomes "how can one accurately produce the proper admittances to compute these figures of merit?". The most simplistic approach would be to break apart the node in question, apply terminations to both sides, and compute the "bidirectional" S or Y parameters from the two terminations. The problem is that breaking the circuit and terminating each side of the split results in an unrealistic and inaccurate operating condition. A much better approach, described in the 1980's by Campbell and Brown [12], is to use a noninvasive probe based on a set of ideal sources to perform an "in-situ" bidirectional S-parameter computation. This probe is still in use today, commonly referred to as the "S-Probe". The S-probe was originally proposed as a stability analysis tool, but these days, it's used mostly for matching network design and not stability analysis. Why?

The problem, forgotten and rediscovered throughout the years, is that the S-probe is simply not accurate in the presence of feedback. Anyone with a simple understanding of stability can appreciate why this is a huge problem. Stability arises from feedback systems, so a probe which loses accuracy in the presence of feedback is of little value for real life stability analysis. I've worked with several designers who knew this intuitively but could never quite pinpoint the exact problem with the S-Probe, it just never seemed to catch the instability we were looking for. Dr. Winslow, currently a Senior Fellow of Technology at MACOM, described it concisely using a simple passive circuit with capacitive feedback around a central S-probe [13], shown in Figure 24.

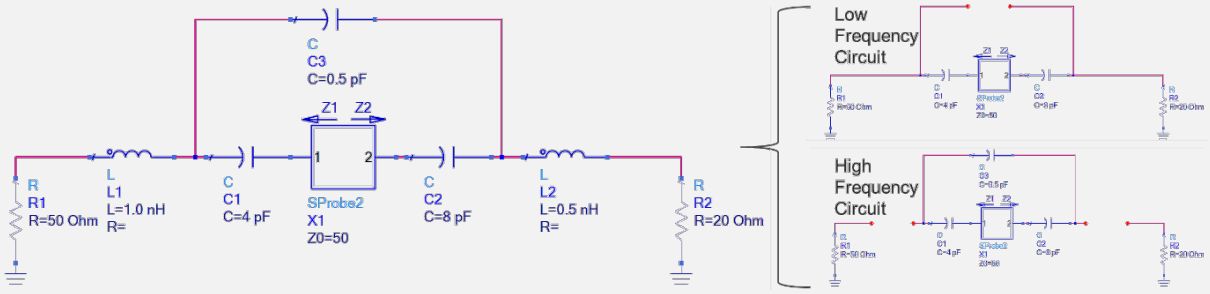


Figure 24. S-Probe applied to a simple passive circuit with feedback. At low frequencies, the feedback is open, and each port sees a series RC combination. At high frequencies, the resistors are blocked, and each port sees a set of feedback capacitors.

With such a straightforward example, it's possible to analyze the expected behavior of the circuit at low and high frequencies by inspection. At low frequencies, the feedback capacitance is an open circuit and the inductors are shorts, leading to a set of series RC terminations on either side of the probe. At high frequencies, the inductors act as open circuits, leading to a chain of three capacitors in series around the probe. To analyze the simulation results from the classic S-Probe, shown in Figure 25, we can break the outputs into series R and C elements. At low frequencies, where feedback is minimal, the probe is quite accurate giving series R and C values which match expectation. However, at high frequencies, the feedback is more substantial, and the S-probe gives a nonsensical result – a negative resistor and a negative capacitor. Clearly this is incorrect when compared with the visual inspection of the circuit. So, put simply, the classic S-probe may be useful for matching network design, but its inaccuracy in the presence of feedback means it is not a viable tool to use for stability analysis.

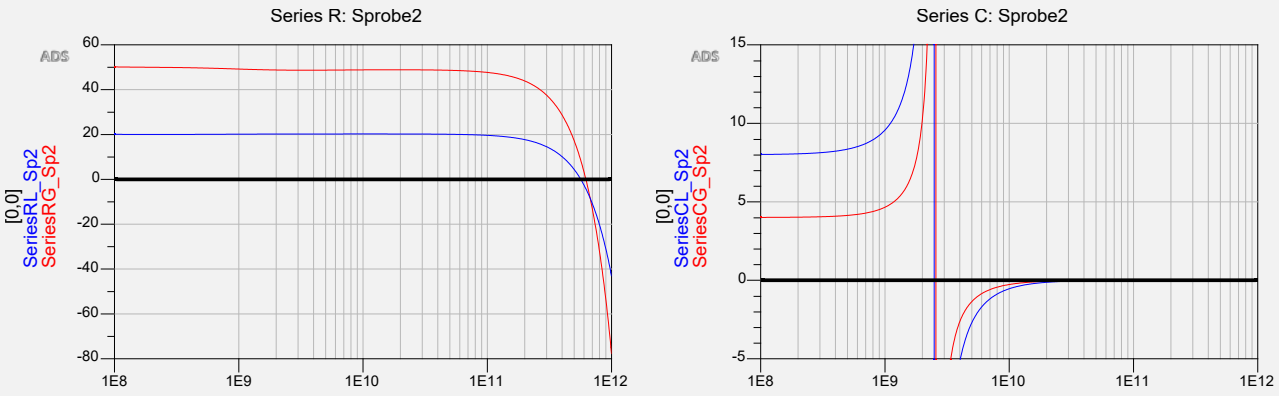


Figure 25. Impedances for passive circuit from S-Probe, decomposed into Series R and Series C elements.

This problem is solvable though implementation of a non-perturbative dual stimulus probe which retains accuracy in the presence of feedback, called the WS-Probe (nicknamed the “Winslow Probe” after its inventor) [13]. This probe is now available in Keysight’s PathWave Advanced Design System. Applying the WS-Probe to the passive circuit from Figure 24 allows for comparison with the classic S-probe in Figure 26. It’s clear from the analysis that the S-probe and WS-probe both agree on the RC values when there’s no feedback. However, in the presence of feedback, the WS-Probe diverges from the S-probe and produces a sensible result: zero resistance, with capacitive parts adding up to the series total of the three components in the circuit. This small update to an old probe unlocks tremendous power in the design tools and can change the way designers approach stability in modern circuits. The addition of WS-Probes to any circuit can facilitate easy computation of multiple stability metrics without perturbing or altering the fundamental analysis.

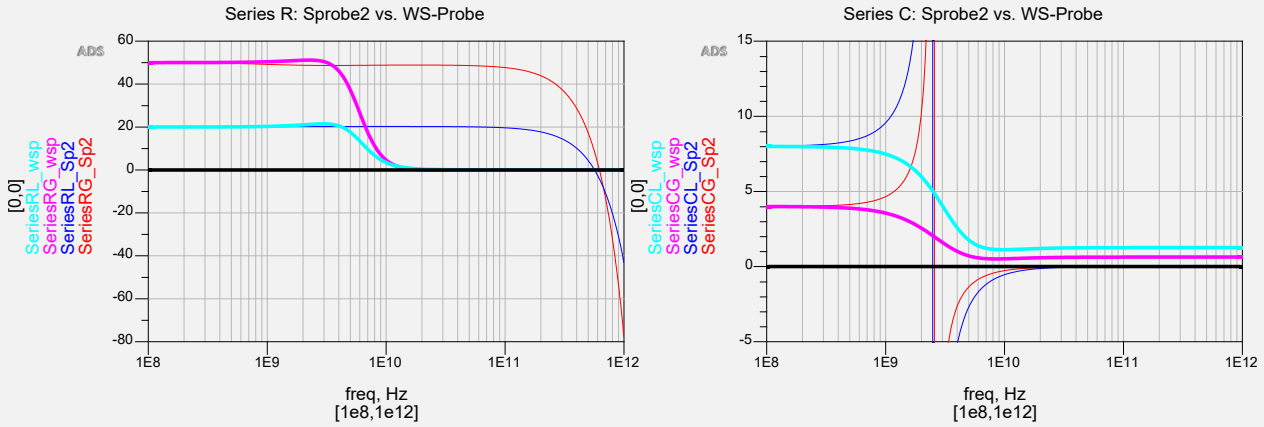


Figure 26. WS-Probe results added to the Figure 25 plots, showing agreement with visual circuit expectation at both low and high frequencies. At high frequencies, the S-Probe results are inaccurate due to the presence of feedback.

The WS-Probe in action

To understand the power of having accurate admittance parameters for stability analysis, let's consider the simple amplifier-feedback circuit test case analyzed throughout this paper. As shown in Figure 27, WS-Probes can be applied at the external transistor gate and drain, as well as internally across the active source. Next, an S-Parameter simulation runs with frequency swept from 100 Hz to 100 THz on a logarithmic scale. It's possible to use the results from this one simulation to compute every one of the stability metrics meticulously derived by circuit manipulation earlier in this paper.

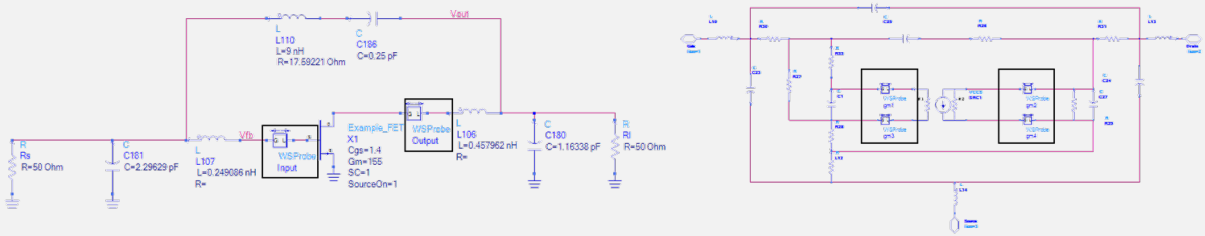


Figure 27. WS-Probes applied to amplifier-feedback example circuit used throughout this paper.

First, let's use the probes to derive Rollett's Stability Factor, shown in Figure 28. Equations can process the WS-Probe outputs to generate an admittance matrix for a *high impedance termination condition* across the transistor I/O's, similar to NDF. This matrix converts to an S-matrix which computes K-factor. Figure 28 shows equations used in this computation. The results from the probe match results derived from a standalone simulation with *high impedance terminations* placed in the circuit at the same location as the probes (Figure 28, right). This scenario simply illustrates the potential the probes have to perform a versatile set of computations in an accurate manner on any circuit under analysis. In this case, the result is more academic than practical: typically, such a computation is performed at the external R_s and R_L under nominal termination conditions rather than the transistor.

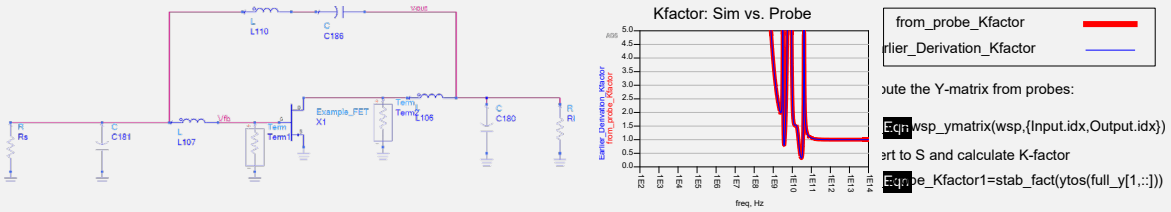


Figure 28. K-factor derived from the circuit with terminations (blue) vs. computed from WS-Probe (red). Placing probes at the outside terminations can also match the K-factor derived from the entire network.

Next, in Figure 29, we'll compute a few different loop gains. Data Display equations process the same WS-Probe outputs to compute Osctest, Middlebrook, Hurst and Tian style loop gains for the transistor Input / Output nodes on the circuit in Figure 27. The WS-Probe curves exactly match the manual circuit-based derivations for each type of loop gain (originally computed for each approach in Figure 13).

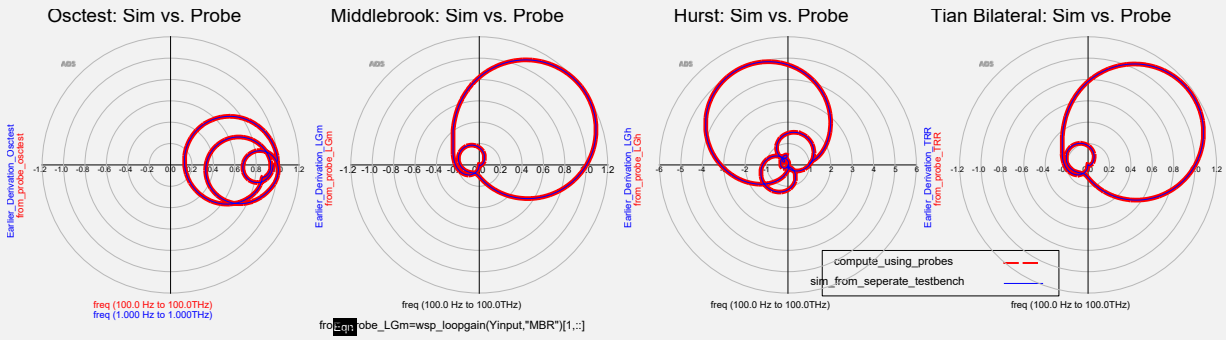


Figure 29. Osctest, Middlebrook, Hurst, Tian loop gain, simulated w/ separate testbenches vs. computed from probes

The same simulation can also derive Bode's Return Difference across the internal current source, as shown in Figure 30, left. This computation uses the probes instead of explicit terminations across the current generator to derive the Y-matrix for the on and off swept conditions with the normal circuit operation still unperturbed. This result matches the manual simulation originally shown in Figure 16. For Normalized Determinant (Figure 30, left center), the results were computed at the external transistor I/O's, similar to the approach in Figure 19. For this comparison however, the circuit topology used was the one from Figure 26 with only one transistor. For Driving Point Admittance (Figure 30, right center), the probe results were compared to the auxiliary generator simulation originally shown in Figure 15. Again, results match perfectly across a wide frequency. Finally, for the Ohtomo Network Bifurcation, (Figure 30, right) results were derived from the same probe simulation in Figure 27, using an equation which replaces the manual application of circulators and isolators. These curves are compared to a set of results which were derived manually using circulators and isolators at the two non-grounded interface nodes of Figure 26. All in all, adding the WS-Probe to this simple circuit can replace 16 separate manual simulations to derive just the metrics shown in Figures 28-30. Keep in mind, that number is for a simple circuit – as the complexity of the circuit increases, the amount of effort saved by using the probes also increases dramatically.

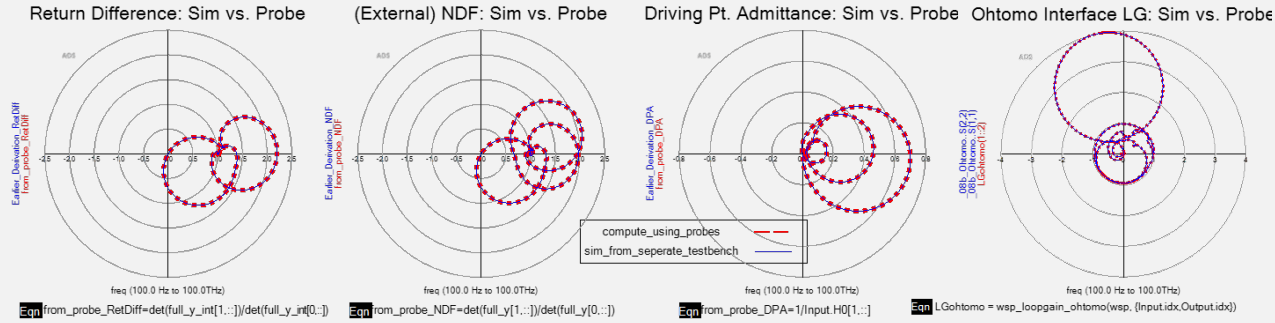


Figure 30. Return Difference (internal), NDF (external), Driving Point Admittance and Ohtomo Loop Gain, simulated from separate testbenches vs. computed from probes.

Using WS-Probes to Compute a “Virtual Load Pull”

Most of the stability analysis techniques described so far only provide results at a *single* impedance condition: the loaded state of the circuit. In some cases, designers want to sweep an external source or load over high VSWR and derive the resulting stability inside the circuit under these mismatched conditions. This is straightforward enough to do for any of the above metrics by running an explicit source and load sweep in the simulator, but for some applications, it’s desirable to perform the analysis *computationally* rather than using brute force, for example, when attempting to optimize stability for individual devices inside a multistage MMIC amplifier [15]. The challenge: it’s not always straightforward to mathematically derive the effects that varying external impedances will have on nodes buried inside an active circuit with multiple gain stages. This limits the type of analysis. For example, impedance dependent functions have been derived for Normalized Determinant, which is mathematically straightforward [14], and voltage loop gain across a FET [15], which relies on a specific type of open circuit loop gain methodology to derive the necessary dependent function.

It would be nice to add Driving Point Admittance to the list of techniques having load-dependent stability functions. The result of such an analysis could enable optimization of individual devices like the ‘loop gain envelope’ approach [15], but with the added benefit that Driving Point analysis is fully rigorous for a given node (unlike an externally derived loop gain). The computed result could holistically determine if any of the derived curves meet or approach Kurokawa’s condition. It turns out that computing such a “virtual loadpull” *is possible* to do simply and effectively on the Driving Point result using WS-Probes, because by design, the probes can mathematically bifurcate circuits. Probe-based bifurcation enables a setup whereby three embedded WS-Probes divide a circuit into two cascaded network blocks. Then, a single simulation run at a nominal 50-ohm condition can derive the internal effect on the network which results from applying a nonideal reflection coefficient to the external ports. From here, the two results combine to compute the full Driving Point Admittance at any internal node.

The procedure, shown in Figure 31, is as follows: place WS-Probes externally at the source and load connections of any nominally loaded circuit, and add one additional WS-Probe inside the circuit (for example, at the gate of the output stage transistor in a MMIC amplifier). A small signal S-parameter simulation sweeps frequency. From this nominal, static result, it’s now possible to entirely compute the effects at the internal node which result from varying the external VSWR. It takes one equation to process the three probe outputs (external source probe, external load probe, internal probe in the circuit).

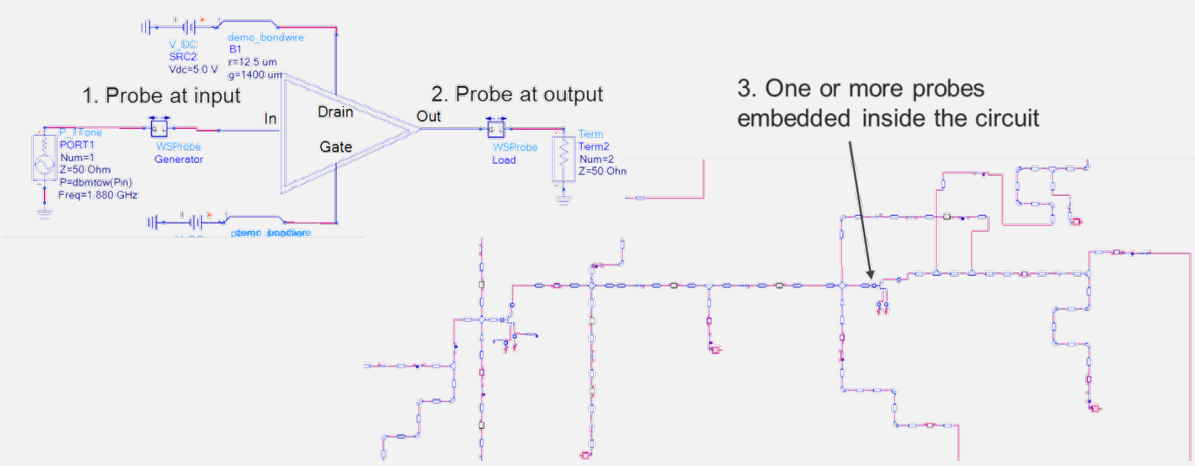


Figure 31. Setup configuration required to virtually vary external source and load impedance using WS-probes.

The probe outputs pass into a custom function built into PathWave ADS 2022 along with a set of arbitrary user-specified gamma and phase points. The function derives the family of driving point admittance curves at the internal node resulting from the arbitrary external source and load VSWR conditions. These curves are analyzed to find Kurokawa frequencies across any loaded state. The functions return indices for source/load combinations where instabilities are found to occur, as illustrated in Figure 32. In this example, source and load combinations which are unstable are marked with red X's. Conversely, external source and load points marked with black dots produced stable Driving Point Admittance responses at the internal gate node. In this manner, designers can understand the sensitivity of their circuit or devices to external loading conditions without needing to perform a brute force sweep.

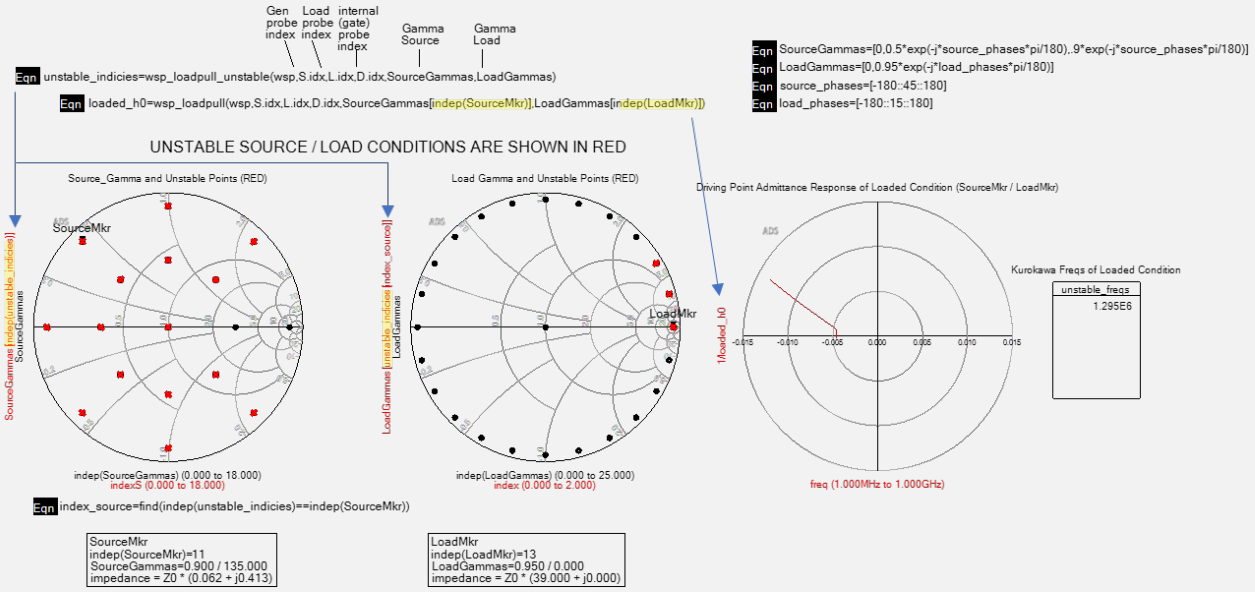


Figure 32. Family of Driving Point Admittance curves for source and load gammas shown, mathematically derived from three WS-Probes (Source, Load, Internal) using equations. The function wsp_loadpull() can compute loaded sets of H0 curves, while wsp_loadpull_unstable() evaluates all the source / load combinations for instability. The curve on the right shows the Driving Point Admittance plotted for the selected arbitrary source and load markers computed by the function rather than simulated, while the red X's are combinations of external source and load impedances which result in unstable Driving Point Admittances per the computed response.

The results from the virtual loadpull computation are straightforward to verify by applying the same source and load combination to the amplifier and simulating the Driving Point Admittance at the internal node in this loaded state. From there, it's straightforward to compare this simulated result to the computed admittance curve based the nominally loaded (50Ω) amplifier, as shown in Figure 33 for two different high VSWR source / load combinations. The curves match well for the external load conditions, indicating the function produces accurate results. Other load combinations were verified in a similar manner.

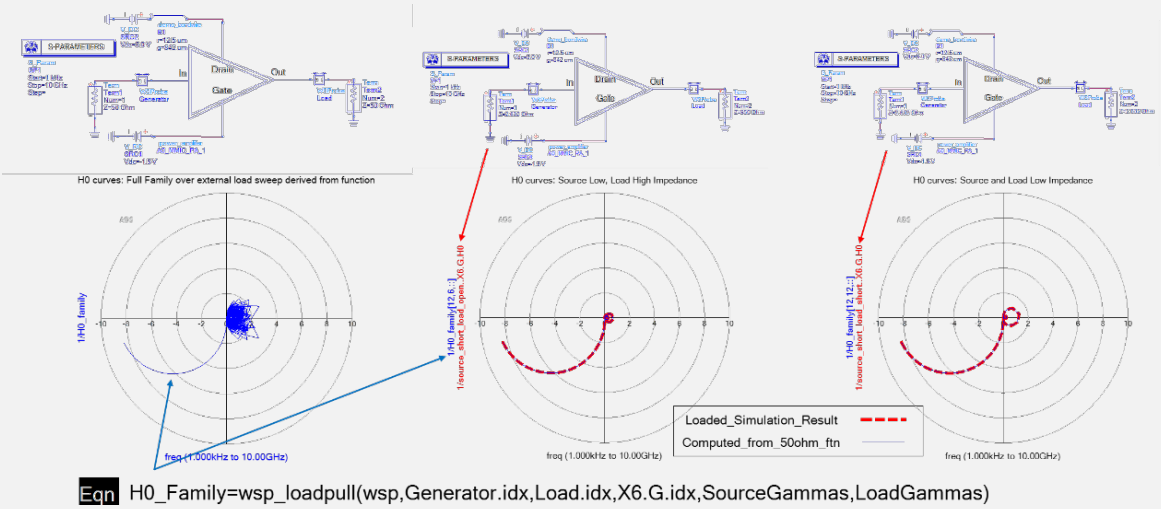


Figure 33. Comparison between Driving Point Admittance response under two different externally loaded VSWR conditions (red) and the response computed from the static 50 ohm externally loaded condition, using three WS-Probes and a basic function (blue).

Fast and efficient optimization is also possible using a virtual loadpull function. One simple approach is to use a modified computation which analyzes external load states and returns only the *number* of unstable source/load combinations, rather than the indices or family of curves. For example, if there are 9 source points and 9 load points passed to the function, there are 81 possible loading combinations. If all source / load combinations are unstable, the function returns 81. If all are stable, the function returns 0. The optimizer now drives the node into stability by minimizing the absolute number of unstable loads. This is possible to do for multiple devices simultaneously while also optimizing other performance parameters. For example, Figure 34 shows results of a 25-run random optimization using a "count" expression for both the driver and output stages. In addition to stability over VSWR, the optimizer also drives gain and input return loss to specified goals across the fundamental frequency band. The four "count" expressions (2 stages, gate and drain) added about 0.5 sec to the ~23 sec S-parameter simulation with 300 points.

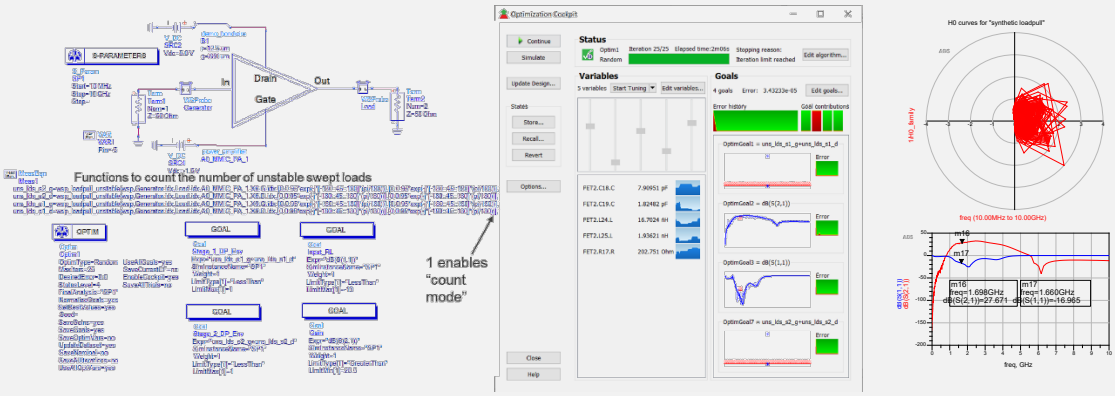


Figure 34. Optimization of a two stage MMIC for varying loads (using "count" method), plus gain and input return loss. Goal was to drive the unstable load count to zero and achieve in band performance. Post run results are on right.

The "count unstable loads" approach to Driving Point Admittance optimization is fast and rigorous, but it only tells the designer if there are unstable load points or not. Sometimes, it's desirable to have an indication of relative stability as well. To get a sense as to the relative stability of the Driving Point Admittance curve (or set of curves on a polar plot) one technique is to offset the curves in the negative resistance direction to determine if such a shift incurs additional unstable frequencies per Kurokawa's condition. For example, if the gate admittance curve shown in Figure 35 (in red) shifts left along the real axis by a factor of 0.1 (blue), then 4 additional unstable frequencies will appear. The equations to perform the shift for the admittance curve are on the top right. The scale factor is the absolute value shifting the real part of driving point admittance. Performing an optimization to stabilize a *shifted* Driving Point Admittance set can potentially produce an additional stability margin for a given design.

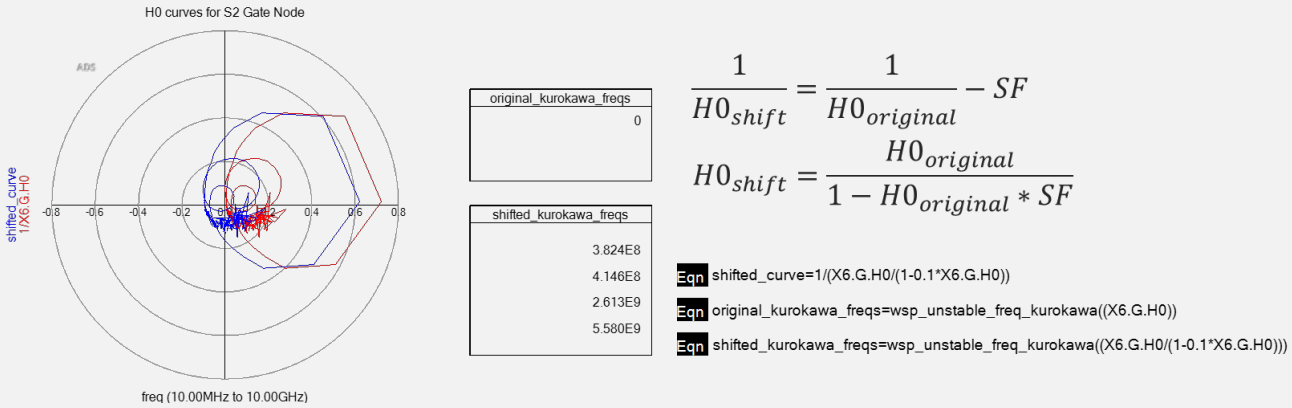


Figure 35. Shifting the Driving Point Admittance curve left along the real axis to give an indication of relative stabiltiy.

This virtual loadpull approach using WS-Probes has many advantages over other techniques. First, the analysis is rigorous for the internal node because it's based on Bode's Driving Point Admittance. It's also possible to simultaneously analyze and optimize multiple nodes from just one simulation by applying the same function repeatedly. Finally, there is no need to remove gain stages between the internal node and the swept external impedance because the computation is accurate even for multi-stage designs. You'll get a chance to see this stability technique in action later in the "Examples" section of this paper.

Stability under Large Signal Drive

The stability metrics and results described so far derive entirely from small signal analysis conditions. How well do these techniques extend to large signal, nonlinear cases? To illustrate, the circuit used throughout this paper can act as a large signal amplifier with the addition of diodes to either side of the controlled source to model a "turn on" and "knee" voltage. As the signal increases, the output diode begins to conduct and the gain curve compresses, much like a real transistor. It's instructive to examine the modifications needed to adjust only one small signal analysis technique, the "Osctest" loop gain, to give accurate results for a such large signal circuit. To assess stability under large signal conditions, a small signal sweep typically runs concurrently with a harmonic balance simulation.

Recall from Figure 9 that under small signal conditions, the Osctest loop gain is very easy to derive: it consists of a circulator and a termination along with a DC feed. However, to account for the additional complexity that arises in large signal analysis, the circuit needs modifications, as shown in Figure 36.

First, it's necessary to configure a harmonic balance analysis with a small signal frequency sweep around the large signal carrier (this is set in the "Small Signal" tab of the Harmonic Balance controller). To facilitate this sweep, one must replace the termination used in the small signal Osctest configuration with a separate AC source and load, requiring an additional circulator (Figure 36, center). However, there's another problem: the small signal tone will pass through the circulators and around the loop properly, but the large signal *also* must pass through the circulator component unhindered. The large signal needs to compress the amplifier for the small signal swept analysis to be valid under the specified input drive conditions. Figure 36 shows plots of the waveforms at the device output, lower right, illustrating the clipping effects which are necessary to induce for an accurate analysis. To facilitate this simultaneous small and large signal operation, an ideal bandpass filter is added to the thru path of the component so the large signal can bypass the circulator, while a bandstop filter is added to the small signal path to prevent the large signal from leaking onto the loop-return termination. Still this is not enough: the clipped waveforms contain harmonics, so the filters also need to pass or block *multiple* harmonics to maintain the needed level of accuracy. In this case, the filters pass the first five harmonics, but more may be required.

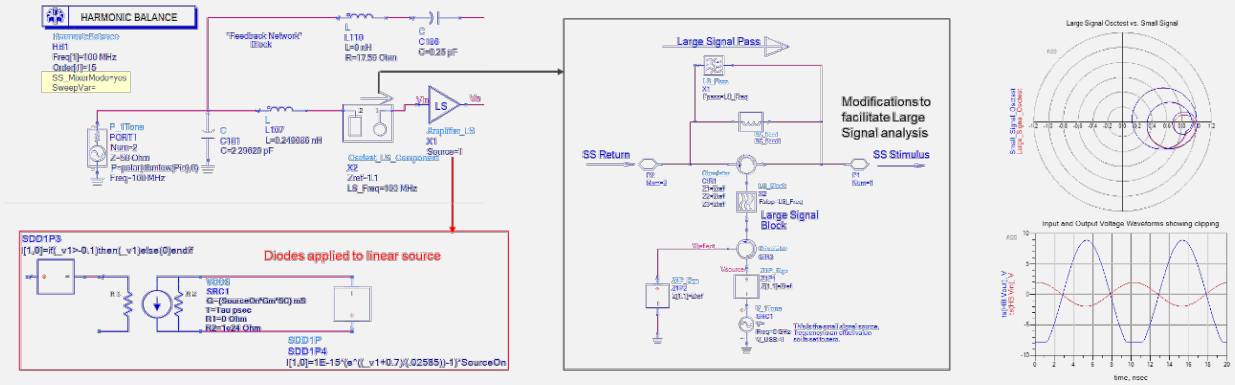


Figure 36. Modifying the Osctest loop gain method to work for large signal is not trivial because the large signal must pass through the component while the small signal must flow around the loop. It's also necessary to index the proper Harmonic Balance mixing terms.

Finally, the simulation runs, but still the results are tricky to process. It's necessary to properly index the Harmonic Balance mixing terms in the computation to specify the *small signal frequency sweep terms*, as opposed to the large signal terms. Finding the correct index values may require some trial and error, and the index may change for simulations which have a different number of harmonics. Figure 36 (top right) plots the loop gain with the small signal terms indexed properly, showing a slight shift in the response due to the diode conducting across the generator output. This is a lot of complexity to derive one response!

The point is that for this one simple loop gain derivation, the setup, testbench, and results became much more complex and nuanced under large signal drive than they were for small signal operation. It's fair to say that other small signal stability techniques will encounter some similar changes in setup when extending to large signal cases. This additional complexity can be a big challenge for circuit designers. Often, designers do not consider stability at all under large signal operation because the setup required to get accurate results is just too complicated. Ignoring the large signal cases might be a fatal oversight in some situations because large signal instability can often be hard to pinpoint in the lab.

Extending WS-Probe Analysis to Large Signal

The bidirectional impedance derivation which the WS-Probe is based on easily extends to large signal analysis. To illustrate, WS-Probes were added to the various I/O nodes of the circuit described in the previous section, as shown in Figure 37, with input power adjusted to the 1 dB gain compression point. To enable the probe analysis, simply configure an option in the Harmonic Balance control (Perform Stability Analysis checkbox / HBSS_WSP=1), and the simulation runs as normal, sweeping a small signal tone around the large signal input. The probe output variables for the large signal simulation are the same as they were for the earlier small signal simulation, meaning that all the prior analyses and equations (Figures 28-30) are reusable for the large signal case. The plots in Figure 37 compare the large signal stability results (red) with the previously derived small signal results on the same circuit (blue). The shift observed between the small signal and large signal results is expected: for example, as the circuit compresses, loop gain typically decreases. Similar to the small signal case, this WS-Probe based simulation bench can replace a set of equivalent large signal testbenches needed to perform a stability analysis. In some cases, such as the Osctest loop gain example, these benches are even more complex than the configurations needed for the small signal analysis. The ability to seamlessly switch between large and small signal stability analysis with the same circuit topology is a big advantage to the admittance-based probe technique.

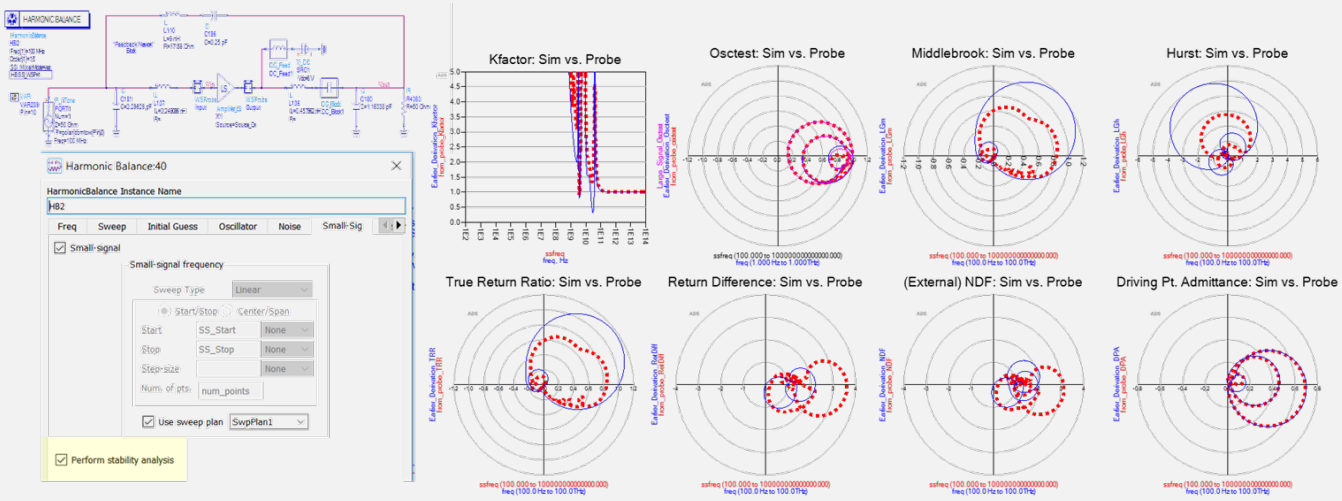


Figure 37. Modifying the small signal WS-Probe simulation to work under large signal conditions is as easy as checking a box in the controller. All the probe outputs are the same and the equations are also the same for large or small signal. The plots are showing the WS-Probe results under large signal drive (red) compared to the earlier small signal results (blue). Difference in the plots are due to the transistor compressing under high input drive.

Practical Application Examples

This section will examine three practical high frequency circuit examples in detail with a focus on answering common questions and dealing with challenges that designers run into when analyzing stability using the WS-Probes for the first time. Along the way, you'll learn some new techniques, understand how to apply the probes to real life circuits, and even uncover a few mistakes to avoid when analyzing and troubleshooting your own stability problems.

The first example applies the probes to a potentially unstable transistor. Many times, when designers begin working with the probes, they start with a seemingly well understood circuit consisting only of a transistor and bias tee. Seeing a positive valued return loss and a K-factor less than one, they believe that the transistor is unstable, then expect the probe results to validate this. However, sometimes the probe results imply the opposite conclusion; that the circuit is in fact stable, which can be confusing. This section goes into detail on what exactly the results mean and how to validate conclusions made from the probe metrics. There's also an opportunity to discuss situations where common assumptions and rules of thumb can be misleading. Upon further investigation, the metrics from the probe do in fact agree with the earlier K-factor results, but a number of subtle details make this hard to recognize at first glance.

The second example examines a two-stage high frequency MMIC amplifier. In this circuit, if the designer adds a bondwire to one of the bias lines, this creates an unintended instability. This is a good opportunity to go into more detail on how to apply the probes to a complex circuit and also how to choose and validate the stability metrics given the practical limitations of the models. It's also an interesting case study because the instability initially appears to be related to feedback or loop gain, but upon further inspection, it's due to an unstable loading condition on the device. This example also shows a few great tips and tricks for troubleshooting and solving complex stability problems in your own designs.

The third scenario studies a single stage GaN Power Amplifier which is based on a commercially available transistor and model. In this case, the circuit initially appears to be stable, but when the designer includes EM effects, the circuit oscillates. The problem is, it's not so easy to track down the source of the instability when the dominant feedback is occurring somewhere on a large physical structure. This example will describe a new and novel technique to find the root cause of such a problem. It uses results from the WS-Probe to drive a targeted circuit simulation which physically excites the Electromagnetic structure to pinpoint the instability. This allows the designer to graphically visualize the precise location of feedback paths on the layout which are causing the circuit to oscillate.

Example 1: Using the Probes on a Transistor

Figure 38 shows the first application circuit; this is nothing more than a transistor with a bias tee. An S-parameter simulation reveals some potential concerns: S22 is greater than 0 dB at low frequencies, and the Rollett stability factor is less than 1 from very low frequencies up to 1 GHz. Most high frequency designers would expect this circuit to oscillate. Certainly, it would be difficult for an engineer to get through a design review with these results.

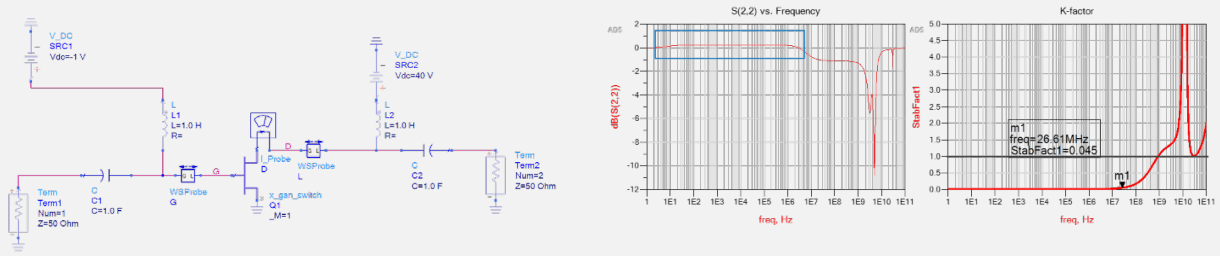


Figure 38. Simple transistor test circuit showing a suspected instability due to positive S22, stability factor <1.

This seems like a good circuit to use for validating the WS-Probes because it's 'obviously' unstable. The expectation is that the probes will show this instability through all of the various metrics. So, the designer adds WS-Probes to the gate and drain and simulates. The probe results are shown in Figure 39 for Loop Gain (Tian-bilateral), Network Bifurcation (Ohtomo), and Driving Point Admittance, with Kurokawa frequencies computed. Perhaps surprisingly, the results from the probe do not indicate any instability. The bilateral loop gain response is very low, essentially zero. The Network Bifurcation (Ohtomo) interface node loop gains do not encircle (1,0). The Driving Point Admittance response does not have any Kurokawa condition – this is obvious because the real part of the response never goes below zero. An engineer in this situation could be forgiven for concluding these metrics are not accurate, or the probes are not working properly. However, such a conclusion would be erroneous. Let's dig a little deeper to test the stability of the circuit with a few other measurements and techniques.

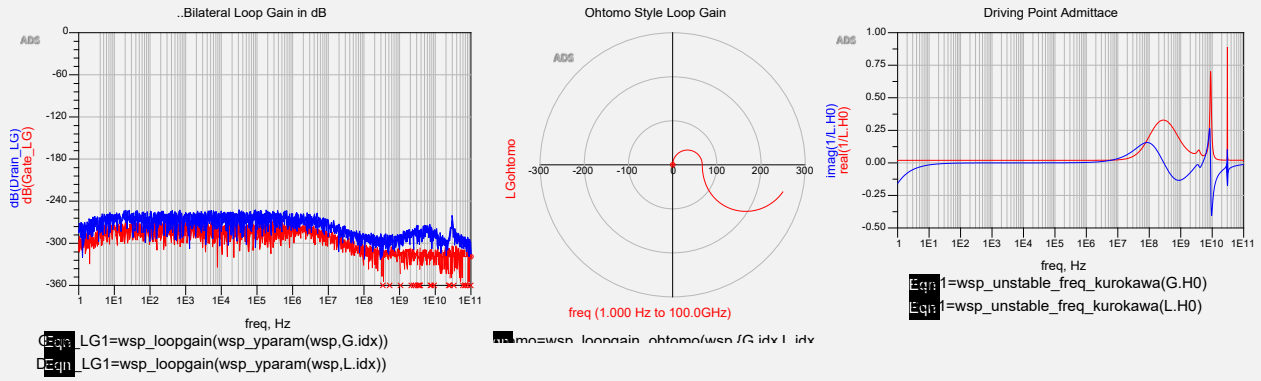


Figure 39. Results from applying WS-Probe to transistor I/O's. Bilateral loop gain (left) is zero, all Ohtomo loop gains are stable (middle), and driving point admittance shows no Kurokawa conditions on the Gate or Drain (right).

In this case, the transistor has static parasitics which are explicitly placed in the circuit along with a model card which gives access to all the device parameters, as shown in Figure 40. This is of course a rare and unusual situation, but it helps to illustrate some useful concepts. First, access to the nodes which are inside the parasitics allows us to compute loop gain and other metrics inside of the device itself, which may shed more light on feedback which cannot be accessed from outside of the transistor. To measure this feedback, additional probes are placed at internal Gate, Drain and Source nodes (gi, di, si).

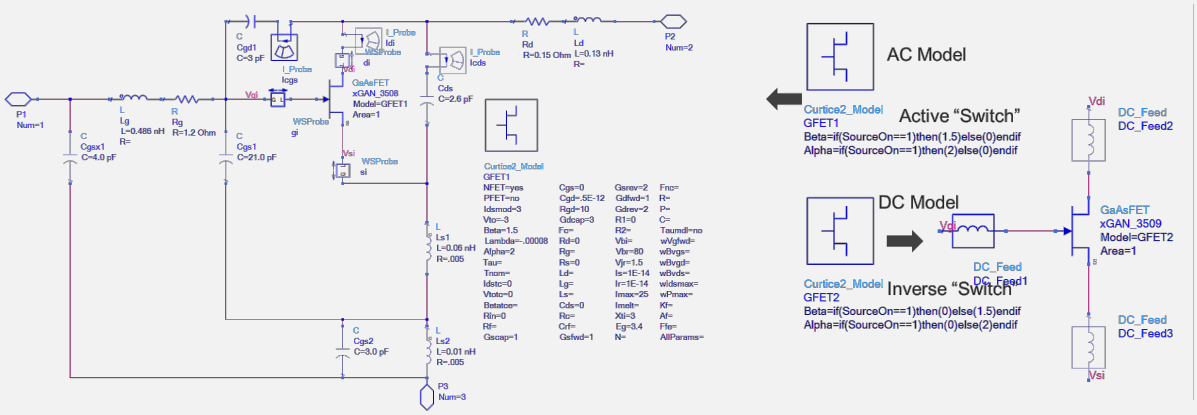


Figure 40. Transistor model internals, with parasitics and model card, configured to perform Normalized Determinant

These internal probes can also be used to derive an additional stability metric with some clever manipulation of the circuit model card. The Curtice2 transistor model has active parameters as follows: Beta =1.5 and Alpha =2. If these parameters are set to zero, this essentially makes the device passive. Having a passive version of the model allows us to compute the Normalized Determinant Function to validate or discredit the other stability metrics reviewed so far. To implement a 'switchable' model, an if-then-else statement is used on the Beta and Alpha terms based on a higher level input called 'SourceOn', shown on the right of Figure 40. When the switch term equals one, the Beta and Alpha are set to their normal values; when the switch term equals zero, the Beta and Alpha terms are explicitly set to zero. There is one additional requirement to compute an accurate NDF: the DC state of the circuit must be maintained in the "off" analysis. To facilitate this, an additional DC coupled transistor is placed in parallel with the original transistor, and it points to a model card which is the inverse of the AC model. In other words, when the AC model is on, the DC model is off, and vice-versa. In this manner, the nonlinear device is able to turn the active source off while preserving the DC operating point.

With the internal probes and switches in place, let's return to the circuit analysis. First, consider the previous bilateral loop gain result, which showed essentially a zero value (~-260 dB). Let's compare this gate node loop gain with the one derived from a probe placed inside the parasitics at the internal gate input, shown in Figure 41. Comparing the red external loop gain to the blue *internal* loop gain in Figure 41 is quite insightful. Clearly, there is significant feedback, it just exists entirely *inside* of the device and it's not visible from a node location outside.

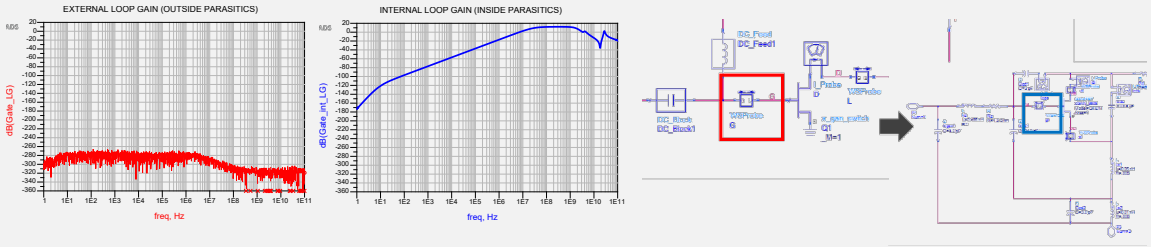


Figure 41. Loop Gain with WS-Probes applied outside the parasitics (red) vs. inside the parasitics (blue).

This is a point designers often miss: you need to be inside of a loop to measure any meaningful loop gain. In the *external* circuit with Bias-T's and ideal grounds, no such loop exists. All of the possible paths terminate in a supply or in an ideal ground. There's simply no way for a signal to traverse from the output of a probe through the circuit and back to the input of the same probe. Therefore, the zero external loop gain response is expected and makes perfect sense. Inside of the transistor model's parasitics, however, it's a different story. For the internal probe (gi – Figure 40), it is straightforward to trace a path from output of the probe through one or more the parasitic capacitors (Cgd or Cds+Cgs) and back to the input of the same probe. Consequently, the relatively high value of loop gain shown in the blue trace in Figure 41 is also expected and makes sense. This internal / external visibility paradigm is one of the challenges with relying on loop gain to measure stability, as discussed earlier in this paper. From outside the transistor, you could never tell there is feedback which could impact the stability of the circuit.

Next, let's look at the other metric which this unusual device modeling situation affords: direct measurement of the Normalized Determinant Function. Using the switch implemented earlier combined with the probes placed inside of the device parasitics, a swept S-parameter analysis is run with the device switch toggled off then on. Then, an admittance matrix is derived from the internal probes (gi,di,si) and the determinant for both the on and off states is used to compute the NDF, as shown in Figure 42.

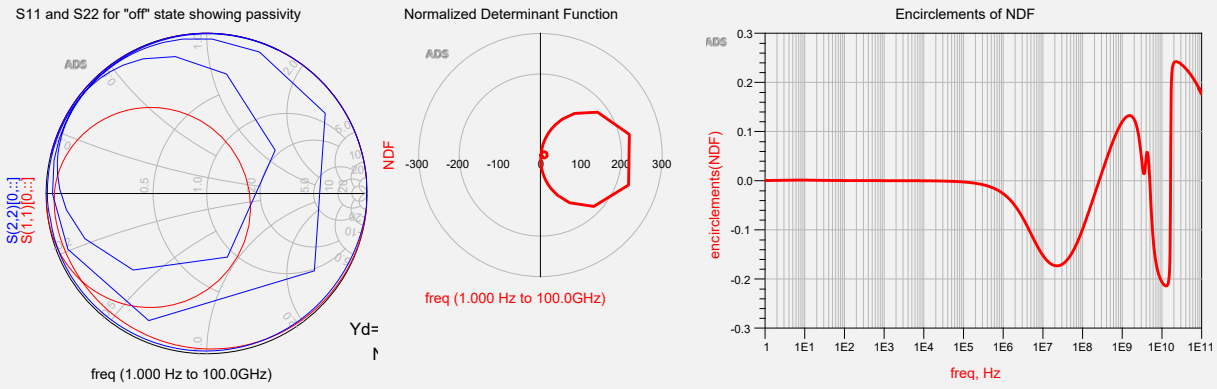


Figure 42. S11 and S22 for transistor in the "off" state (right), Normalized Determinant Function (center), encirclements (right).

First, it's a good idea to validate that the off state is truly passive. To do that, we can measure the reflection coefficients at the input and output, and also the forward and reverse gain terms. For the off state, Figure 42 shows the input and output return losses are now entirely inside of the Smith Chart, and the gain terms (not shown) are also well below zero. This is of course expected and indicates a passive state for the "off" circuit. Perhaps it's not surprising at this point, but the NDF result agrees with all the other metrics because it indicates that the circuit is stable. This is unfortunately at odds with the designer's intuition based on the positive valued S11 and the K-factor. As more data becomes available, it seems that perhaps the initial set of assumptions regarding instability based solely on S22 and K-factor may have been the thing which was flawed in this particular situation.

As a final data point, let's perform a transient analysis which is a particularly effective way of verifying that a suspected oscillation is real. The analysis itself is straightforward to set up; just apply a step or impulse at the input and watch for oscillations to grow out of the noise floor at suspect nodes such as the output. There are, however, a few important details to doing this analysis properly. First, it's a good idea to set up the time scale at roughly the same order of magnitude as the timescale which the oscillation is expected to occur at. If you are sweeping a nanosecond scale but trying to observe a microsecond oscillation, the sweep will likely be too short to catch even one cycle of the problem. Conversely, if a microsecond scale is used to induce a nanosecond oscillation, the pulse may be too slow and convergence might be very challenging. Along those lines, the second consideration to be aware of is that transient analysis can have convergence problems when a circuit is very unstable because the results tend towards infinity. So, if you run into convergence issues along the way, its helpful to decrease the stop time and the step. Even so, in some situations the circuit just may not converge no matter what. Finally, it's important to note that transient analysis does not work for explicitly reactive terminations (i.e. 50+j*50), because these terminations are valid only at one frequency, which has no meaning for a time-based analysis scale. Instead, to achieve a reactive load, you'll need to use transmission lines, inductors or capacitors to get the proper reactance, which of course will only occur at one frequency.

The transient analysis for the transistor circuit is shown in Figure 43. The goal is to induce an oscillation in the MHz region (indicated by the K-factor), so a step function is applied at the microsecond timescale and the resulting node voltages and currents are plotted. No oscillation is found; both the input and output nodes are flat after the step response. These results validate the other stability metrics from WS-Probe indicating fundamental stability, and are again at odds with the S-parameter and K-factor intuition which the designer had. This might end up being a lengthy design review!

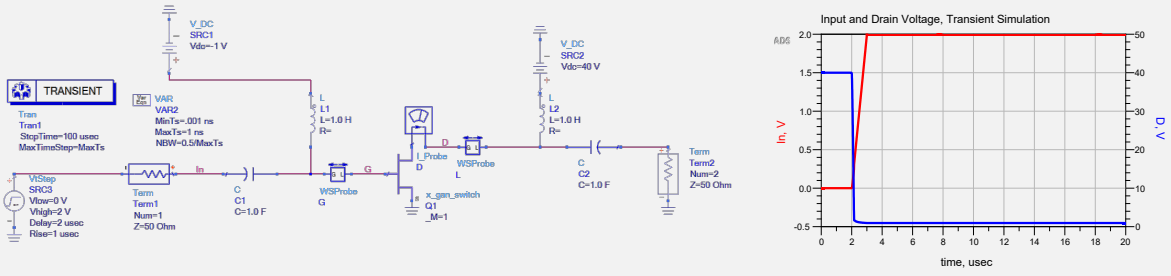


Figure 43. Transient analysis for the Example #1 circuit with a pulse applied to the input, showing no oscillations.

To summarize, intuition may have indicated that the circuit should be unstable because the output return ‘loss’ was actually a small gain, and the K-factor was well below unity at lower frequencies. However, not a single stability metric nor a transient simulation was able to show an autonomous oscillation. Simply put, the only reasonable conclusion to draw here is that the circuit is not oscillating. The lesson is, ‘don’t throw away the stability metrics too early!’.

Going back to K-factor, a closer inspection would have provided reason for a designer to be suspicious. Recall that for Rollett’s stability factor to be valid, the absolute value of the S-matrix determinant must be *less than unity*. This determinant is often >1 cases where the reflection coefficients are >0 dB, and that’s the case here too, as shown in Figure 44. The K-factor is rarely valid when the nominally-loaded input / output impedances go outside of the Smith Chart.

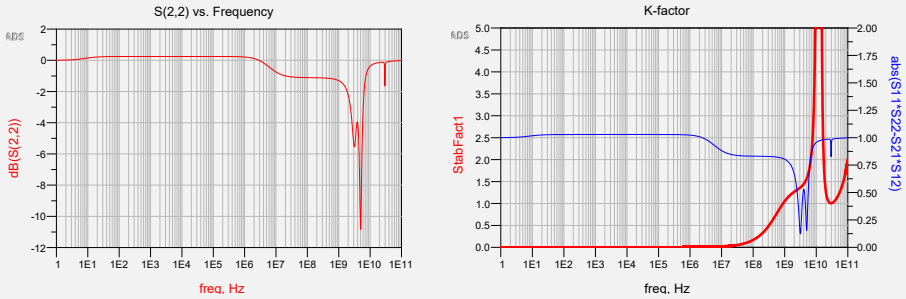


Figure 44. Stability factor is often invalid for cases where a reflected S-parameter is >0, because the matrix determinant is >1.

Even so, for this circuit, there is still a considerable region from ~10 MHz to ~1 GHz where the K-factor is <1 *and* the determinant is also <1. However, it’s not clear what conclusion to draw here. If you think about the way instability manifests, self-starting oscillations occur as a result of poles in the right half plane. Those poles are usually at single frequencies, or perhaps conjugate pairs of frequencies, but they rarely exist continuously, for example over a frequency range from 10 MHz – 1 GHz. That would be a very large set of poles indeed! So, interpreting K-factor as showing broad regions of instability may not be entirely accurate. Perhaps a better way to interpret K-factor is that it shows where the circuit is unconditionally *stable*, instead of unstable. This distinction can be important when designing real circuits.

Another concept worth mentioning is that K-factor by definition considers loads across the *entire* Smith Chart. However, the individual stability metrics studied here only consider the loaded state of the circuit as it currently exists. So, to accurately compare K-factor to other metrics, technically we should sweep these metrics over the entire Smith Chart. Fortunately, this is now easy to do for Driving Point Admittance using the WS-Probe “virtual loadpull” computation technique described earlier. Again, these results are computed in post process, so it’s not necessary to do an additional simulation sweep of the external loads. Figure 45 shows such an analysis for the circuit in question; an external source and load sweep were applied virtually using the “wsp_loadpull” functions, and the internal drain node was monitored for instability. The results from Figure 45 indicate that there *are* unstable regions on the edge of the Smith Chart where this circuit should oscillate, they just occur at a different load state than the original analysis.

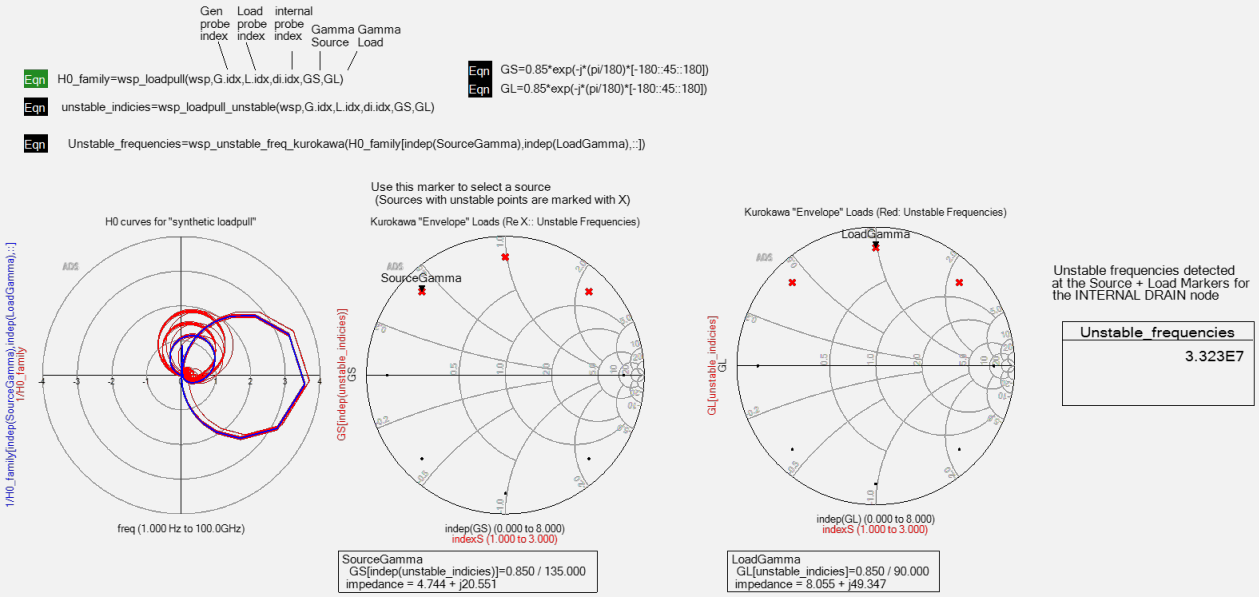


Figure 45. Driving Point Analysis of the circuit with source and load virtually swept, showing several unstable loads (red X).

Let's validate this virtual loadpull result using a transient simulation. To do that, reactive loads must be applied using inductors and terminations near the Kurokawa frequency (33 MHz). Then, a transient analysis can run based on a step function at the input. The timestep for the oscillation is expected to be about 30 ns, therefore an appropriate rise time and stop time were configured to be 5 ns and 500 ns, as shown in Figure 46. The results clearly show the oscillation on both the input and output nodes, and visual inspection puts the time scale of the response at roughly the same frequency as the Kurokawa condition occurred in the virtual loadpull analysis.

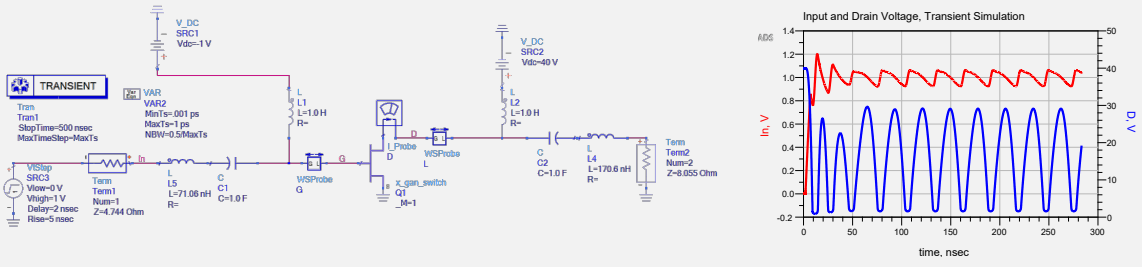


Figure 46. Transient simulation of circuit with reactive loads to match the unstable conditions in the driving point analysis. The circuit is now shown to oscillate.

Plots comparing the unstable loads from the virtual loadpull analysis to the traditional source and load stability circles near the Kurokawa frequency are shown in Figure 47. There is clearly a general agreement between the circles and the unstable loads, but this should be taken with a small grain of salt. One difference is the loadpull analysis flags one frequency point corresponding to a RHP pole. However, the stability circles exist over a broad frequency range, which can be misinterpreted as indicating the circuit has many RHP poles (not true). Also, in this case the Kurokawa frequency was fairly consistent in the loadpull analysis, but in some cases the oscillation frequency may actually change based on the external loading. Nonetheless, the comparison in Figure 44 does inspire some confidence that maybe the metrics are not in such disagreement after all.

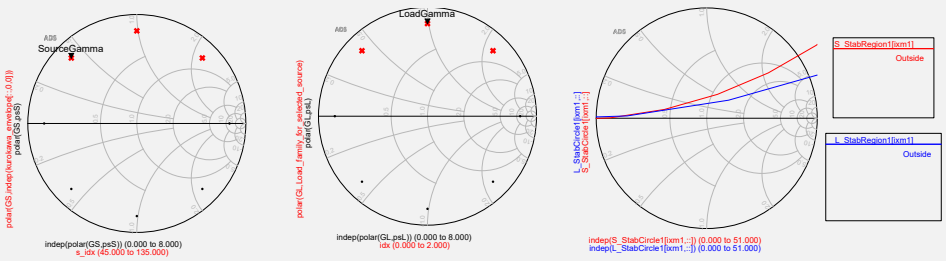


Figure 47. Source and Load conditions where the circuit was unstable per Driving Point Analysis (left, center) compared with source and load stability circles at the unstable frequency, around 33 MHz (right).

Going back to the original circuit, you may have noticed that the bias tee had values of 1 Henry and 1 Farad. When is the last time you used a 1 Farad capacitor in the lab? Just like in the lab, the selection of bias tees in simulation can have a considerable impact on the stability of the device being measured. That is to say using an unrealistic bias tee can lead to… unrealistic results! This is a common mistake that even experienced design engineers make: assuming that an ideally large choke or feed minimizes the loading effects that the bias components have on the circuit. In reality, it's the opposite: having idealized chokes or feeds can often load the circuit in such an unrealistic way that they obscure stability problems. Let's return to the original circuit and redo the simulation with slightly more realistic bias tee values. In this case, 1 uH and 1 uF were arbitrarily chosen, although the Q-factor was still not modeled. Let's see if different bias tee values change the stability results of the circuit.

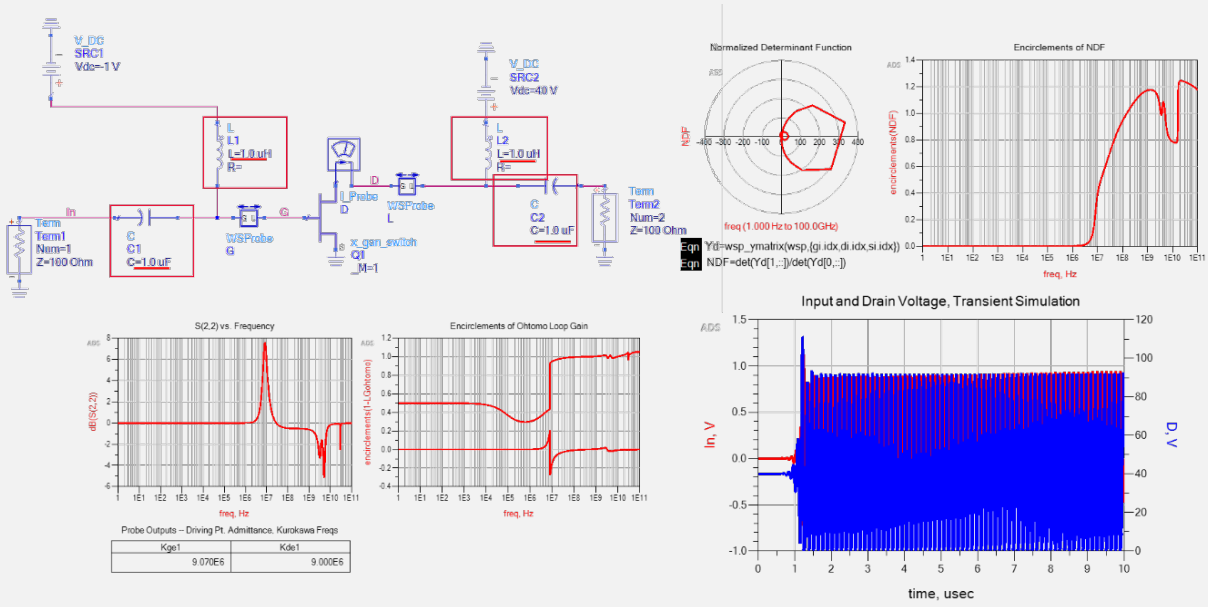


Figure 48. Applying non-ideal bias tee networks to the circuit shows instability with 100-ohm terminations, all of the stability measures agree for this case.

The circuit with modified bias tees along with the results are shown in Figure 48. Perhaps surprisingly, at the 50 ohm condition, the stability metrics still show the circuit to be stable even with a big spike in S22! However, a small adjustment to increase the resistive Z_0 value to 100Ω causes the circuit to oscillate. All the stability metrics are in good agreement with the return loss intuition here, and a transient simulation confirms it in Figure 48. In fact, it's not even necessary to pulse the input, notice that the transient oscillation starts before the step function goes high. The noise modeled in the circuit is enough to induce an oscillation in this particular case.

This example showed how using multiple stability techniques and approaches together can give confidence in the stability (or instability) of the circuit. If one technique disagrees with another, further investigation is often warranted to figure out which is correct. This is the benefit of using multiple approaches – sometimes intuition is wrong, or an approach like K-factor does not reveal the whole story. In other cases, one measure like Network Bifurcation may disagree with another like Driving Point Admittance –additional work is often required in these situations to resolve the conflict. A transient analysis was introduced as a good technique to break a tie or validate a suspicious oscillation. If you can produce a transient simulation showing an oscillation, it's real. We also learned that techniques like Driving Point Admittance or NDF are only valid for the current loaded state of the circuit, while K-factor or virtual loadpull analysis considers broader sections of the Smith Chart. Finally, when analyzing any network, it's still important to be realistic in the component values chosen for the simulation – any external component can have a big impact on the overall stability of a circuit, even "ideal" bias tees.

Example 2: Using WS-Probes in a Multistage MMIC Amplifier

The second example will illustrate how to use the probes in a more complicated circuit: a two stage MMIC Power Amplifier based on the Nonlinear Process Design Kit (PDK) which ships with Advanced Design System. To find it from the ADS main window, go to File→Open→Example and search for "MMIC Power Amplifier". The sub-circuit consists of an input match, driver stage, interstate match, output stage, and an output match. The original design was modified for this work to include bondwires in both the gate and drain DC supply lines to emulate packaging effects, as highlighted in Figure 49. For reference, this is the same example described earlier in the section on virtual loadpull analysis.

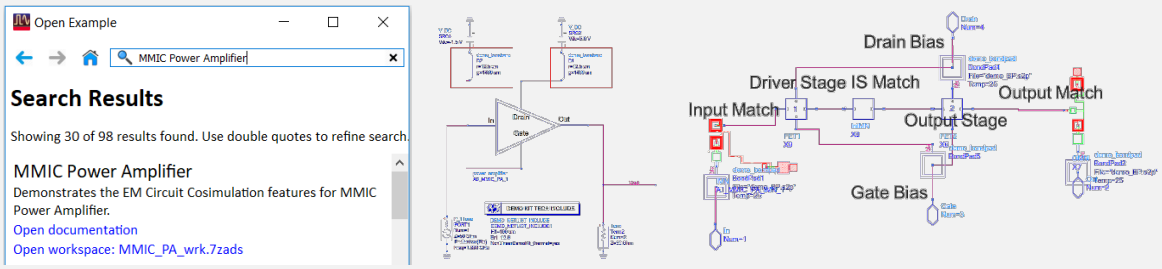


Figure 49. Stability analysis of two stage MMIC amplifier. Bondwires were added to the bias lines.

S-parameter results (Figure 50) show that the bondwires make the K-factor drop below zero from about 1 MHz to 1 GHz, and also causes a suspicious gain spike in the S(2,1) response around 330 MHz As in the previous example, the WS-Probes can be used to provide clarity and validate these initial results.

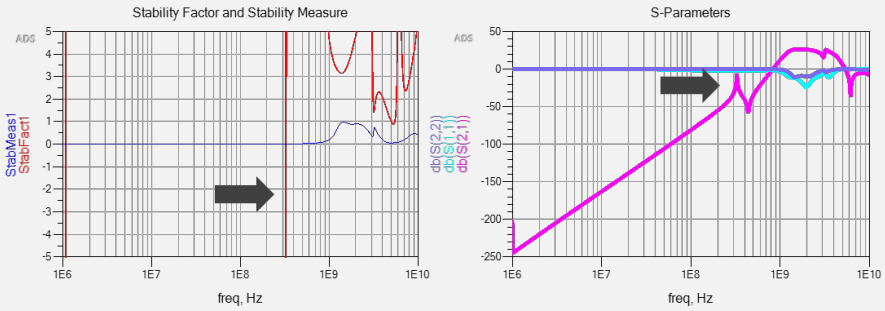


Figure 50. Adding a bondwire to the bias causes K-factor to drop with negative Stability Measure (left), resulting in a corresponding spike seen in the S(2,1) response (right).

The first question designers often ask when using the probes in a complex circuit is: "where should I put them"? While it may seem necessary to place probes everywhere in the circuit*, it's usually enough to probe only the active device I/O's to capture instability*. In this case, there are two transistors: a driver and an output stage, so it's necessary to place probes around these active device interfaces for all non-grounded nodes, as shown in Figure 51.

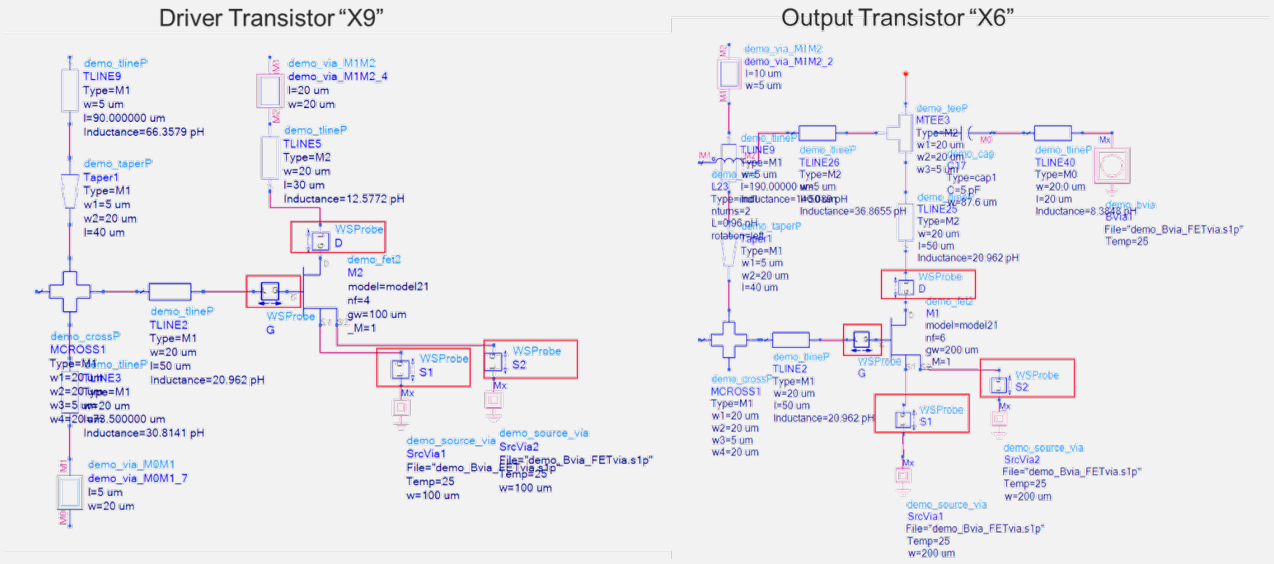
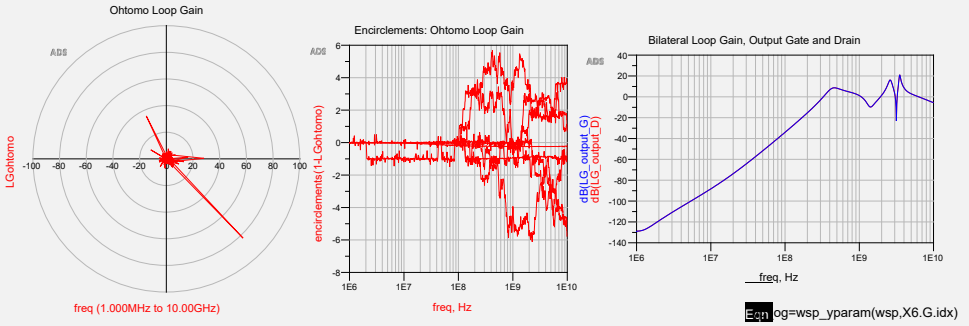


Figure 51. Applying WS-Probes at active device I/O’s for both driver and output stages. Probes have the “G” side facing the active elements to correctly perform Ohtomo’s Bifurcation analysis.

The next question is: “Which metrics?” Normalized Determinant is not practical here because the transistors are part of an encrypted design kit; there is no way to get inside the model to probe the internal node or shut off the active sources. Ohtomo’s Network Bifurcation analysis could be valid *assuming the devices are stable*. To facilitate this analysis, it’s necessary to configure the probes with the *“G” nodes consistently pointing towards the active devices* (Figure 51). The other metrics worth considering are Driving Point Admittance and Loop Gain. Figure 52 plots results from the probe.



Driving Point Admittance - Kurokawa Conditions

Kur_oG	Kur_oD	Kur_oS1	Kur_dS1	Kur_dD	Kur_dG
3.284E8	3.279E8	0	0	0	0

Eqn oG=wsp_unstable_freq_kurokawa(X6.G.H0)
Eqn dD=wsp_unstable_freq_kurokawa(X9.D.H0)
Eqn oD=wsp_unstable_freq_kurokawa(X6.D.H0)
Eqn dS1=wsp_unstable_freq_kurokawa(X9.S1.H0)
Eqn oS1=wsp_unstable_freq_kurokawa(X6.S1.H0)

Figure 52. Ohtomo’s loop gain and encirclements (top left, center), bilateral loop gain (top right), and Driving Point Admittance Kurokawa frequencies for all probes (bottom). Ohtomo’s loop gain computation is noisy due to very low impedance source nodes in the analysis (see discussion), while unstable DPA frequencies generally agree with the K-factor / S(2,1) intuition.

The first thing that sticks out in Figure 52 is the Ohtomo loop gain curves are noisy and difficult to interpret. Nonetheless, the Driving Point Admittances conclusively show an oscillation at 328 MHz for the output stage, seeming to agree with the earlier K-factor result. The Bilateral Loop gain for the output stage shows positive gain from ~300 MHz to 1 GHz, also backing up the potential for feedback induced oscillation in this frequency range.

Let's go back to the Network Bifurcation result. Why is Ohtomo loop gain so noisy? This is a common problem. In situations where there are low impedance nodes in the analysis (like transistor source nodes), the probe results for Network Bifurcation Loop Gain can be sensitive to rounding errors in the resulting admittance matrix. In general, it's easy to remedy this "noisy Ohtomo response" by placing *high value resistors in parallel with the low impedance nodes*. This tends to stabilize the admittance matrix without changing the fundamental circuit performance.

Correspondingly, high value resistors were added to the source nodes of both devices, as shown in Figure 53. Now, the bifurcated loop gain becomes much more conclusive, agreeing with the Driving Point Analysis, showing instability at around 330 MHz It's possible to further validate this instability with a transient simulation, that exercise is left to the reader.

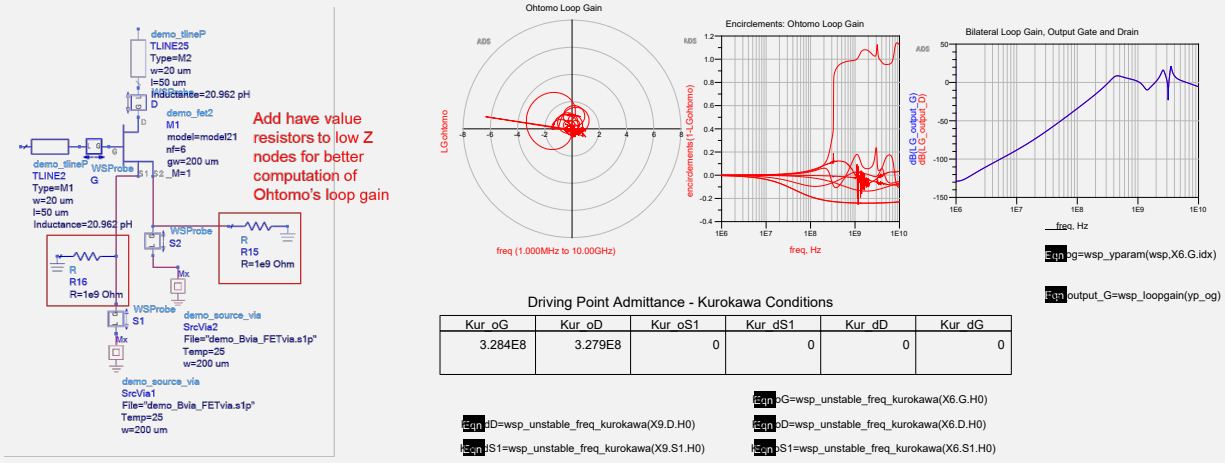


Figure 53. Adding high value resistors (left) in parallel with low impedance nodes improves the accuracy of the Ohtomo loop gain computation. All the other metrics are unaffected by this change.

With the addition of the high value resistors to the source nodes, the metrics now agree that there is an instability around 330 MHz To fix the problem, we need to understand the root cause. The first obvious suspect is unstable feedback loops. It's straightforward to analyze the loops contained in this design though process of elimination because this circuit is simple which makes it easy to break the loop connections. Just cut the wire on the loop manually, and then re-simulate the circuit for the case with the loop removed. Then, reanalyze stability based on the new results. Note that when breaking loops, it's always necessary to retain the original DC state of the circuit. For example, when breaking the Drain Bias loop, apply a separate DC source to the driver stage to maintain the same operating point. There are three main loops in this design, as shown in Figure 54. Figure 54 also illustrates the stability results for the case where each loop is individually removed from the circuit, thereby removing the feedback contribution from the Driving Point Admittance.

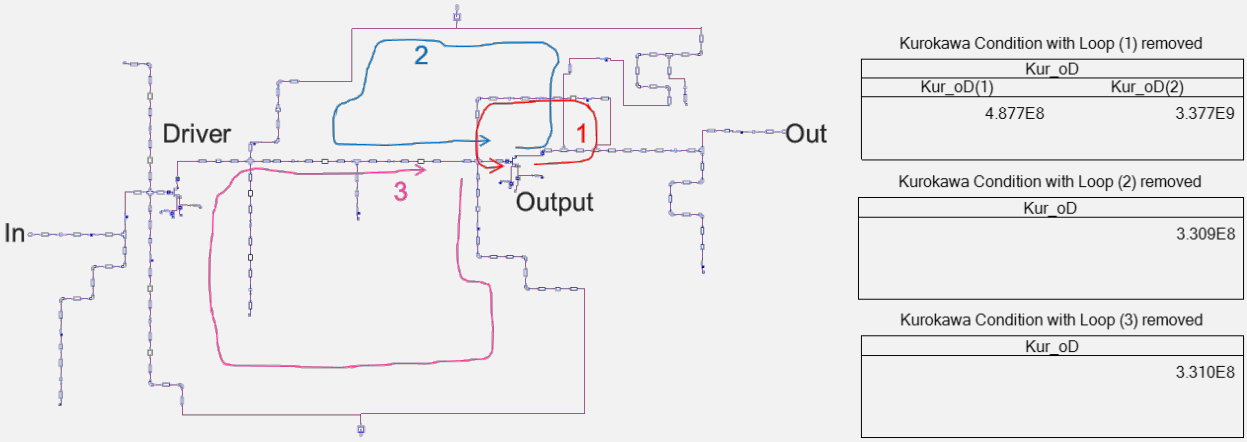


Figure 54. Three feedback loops in the circuit. On the right, Driving Point Admittance Kurokawa frequencies are shown after removing each of the loops individually from the design. All cases are unstable, but removing loop 1 has the biggest impact, making the circuit even more unstable and shifting the oscillation frequency.

The loop elimination results in Figure 54 are perhaps confusing at first glance because the circuit still oscillates for every case. The bias line loops (2&3) seem to have no impact on the oscillation whatsoever. The RLC feedback around the output stage (1) shows a different story: removing this connection causes the oscillation frequency to shift while another higher frequency oscillation appears. One question to ask is whether this shift in the main oscillation frequency (from 330 MHz to 488 MHz) is due to a change in feedback, or something else? Figure 55 shows the loop gain curve around the output stage drain node with (red) and without (blue) the feedback loop in the circuit. As the blue curve shows, removing the feedback (loop 1) does attenuate the loop gain around the output device as expected. Overall, this plot calls into question whether "external" feedback (outside of the transistor parasitics) is the main contributor to the 328/484 MHz oscillation, because removing the loop generally attenuates the gain in that region by over 10 dB. If the loop gain were the cause of the oscillation, this effect would likely dampen the instability, which does not appear to be the case. So, it seems that external feedback induced loop gain may not be the sole culprit of the oscillation after all.

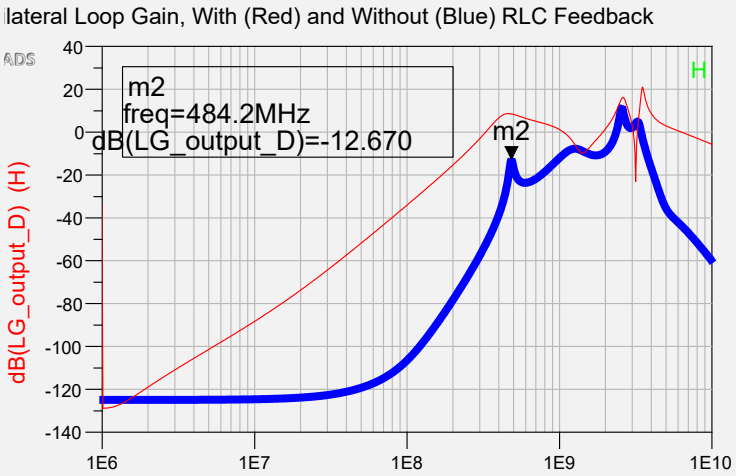


Figure 55. Bilateral loop gain effects from removing Loop 1 (the feedback around the transistor) shown in blue compared with the red trace which is the original response. Removing the feedback loop lowers the magnitude of the response across a broad frequency range from 1 MHz to 1 GHz, indicating that direct feedback is probably not causing the stability problem.

In addition to providing feedback, the network between the gate and drain also *loads* the output transistor, which can certainly impact stability. One way to study the loading effects of the feedback loop is to look at the in-situ impedances which are provided by the WS-Probes, plotted in Figure 56. The left plot shows the impedance as seen looking back into the interstate matching from the gate node, and the right-hand plot shows the impedance looking into the output matching network from the drain node. Now we can analyze the loading effects of removing the feedback.

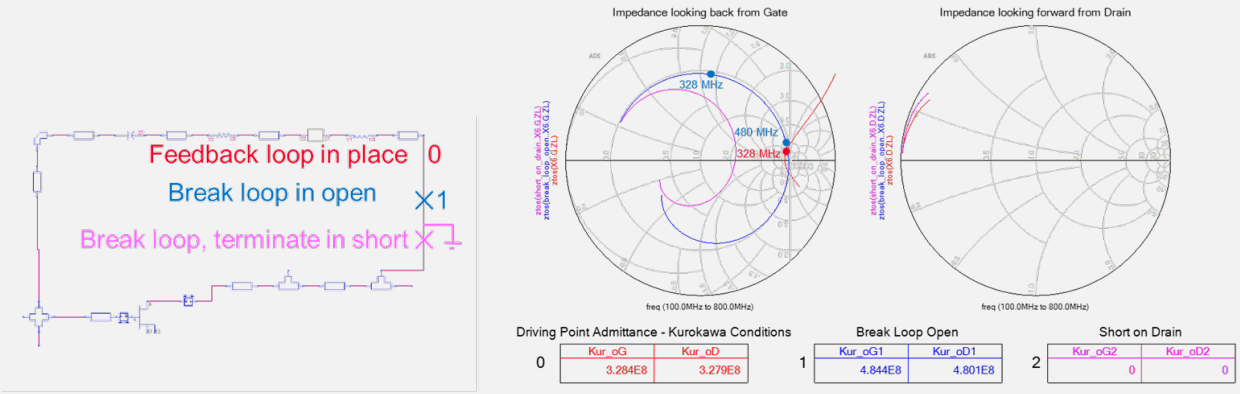


Figure 56. In-situ impedance looking away from the output transistor's gate and drain for three distinct feedback conditions. The red curve shows the results with the loop in place, indicating an open circuit at the gate near the oscillation frequency. The blue curve is the result where the loop is broken with an open circuit, which shifts the unstable frequency to ~480 MHz, notably this is the frequency of the open circuit impedance on the gate. The pink curve shows the loop terminated in a short at the drain, which stabilizes the amplifier and shifts the entire gate impedance loading curve towards the center of the Smith Chart, away from the open circuit. On the right, the drain node loading shows little impact as a result of these feedback changes.

Figure 56 considers the impedances at the gate and drain for three cases. First, consider the case where the feedback loop is in place (shown in red). The gate node's negative impedance may seem alarming, but really this means the RLC feedback is sourcing energy from the output node to the gate. When the impedance is inside the Smith Chart, it means the effect from the feedback is minimal. It is notable that for the red curve, the unstable frequency appears where the feedback is minimal, near the open side of the Smith Chart. If the loop is broken (with an "open" – meaning it's simply cut), then the unstable frequency shifts to 487 MHz (blue curve). Note that the impedance presented to the gate node at this frequency is now very close to the open region of the Smith Chart. At the same time, the previously unstable frequency (328 MHz, blue curve) now moves northwest to an inductive impedance away from the open, and the circuit no longer oscillates there. Finally, when the feedback loop terminates in a short on the drain side, the gate side impedance moves towards the center of the Smith Chart, away from the open, and the amplifier becomes stable with this loading condition. This seems to point to a transistor loading condition being the root cause of the oscillation, which may be due to internal parasitic feedback.

To further validate, it's helpful to look at the output stage transistor by itself with a bias tee, similar to Example #1 in this Application Note. This output transistor can go into its own testbench, biased with 100 uH / 100 uF tee. These values were chosen because they provided no load pulling for frequencies above a few MHz Next, a simple 50-ohm S-parameter simulation was run with the WS-Probes in place, and a "virtual loadpull" analysis was used to look at the effects of source and load impedance on the stability of the device itself. Figure 57 shows the results of the analysis.

In Figure 57, the left-hand chart is source gamma, the right-hand chart is load gamma. The black points are the loading inputs to the equation, selected to match the gate and drain loading the transistor sees in the circuit. Red-X's indicate external loading combinations where the transistor is unstable. A marker specifies a source gamma, and then stability analysis runs for that source plus all swept loads. A gamma point near the open applied to the gate is unstable when combined with a low impedance inductive loading on the drain. The frequency of oscillation very closely matches the frequency seen in the full circuit with the feedback loop removed. This implies that the oscillation seen in the amplifier is probably due to an adverse loading condition applied to the output device's gate and drain. This could stem from an internal feedback loop or some other effect taking place inside of the transistor. Since we can't access the inside of the device model, there's no way to be sure.

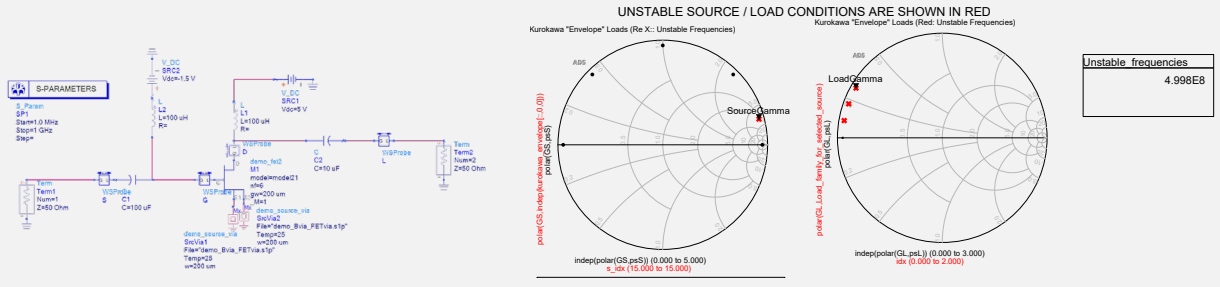


Figure 57. Driving point loadpull analysis, which virtually pulls the source and load conditions, is applied to the output stage transistor. The source pull on the gate with inductive loading on the drain confirms instability as seen in the real circuit. This indicates that the oscillation in the amplifier is due to the gate loading impedance presented to the output stage transistor instead of an internal feedback loop.

To validate in the full circuit, let's configure a block which will terminate the gate impedance below 1 GHz in a resistive value while acting like an open above 1 GHz to pass the fundamental signal. This was implemented using an equation-based S-parameter element with an if-then-else switch on frequency, as shown in Figure 58. When the amplifier simulation includes the ideal filter / termination, the results show the circuit is indeed stable. Note that the effect of this frequency dependent termination is to pull the gate impedance towards the middle of the Smith Chart between 100 MHz and 1 GHz, as shown in Figure 51 center. The WS-Probes already in the circuit can output this data. There are no Kurokawa conditions found. At this point, there are multiple approaches to fixing the stability problem in the circuit. The easiest may be to use the virtual loadpull optimization technique described earlier to optimize the driver and output devices for stability under all possible external loading conditions including those at high VSWR, while also including fundamental circuit performance goals as part of the optimization.

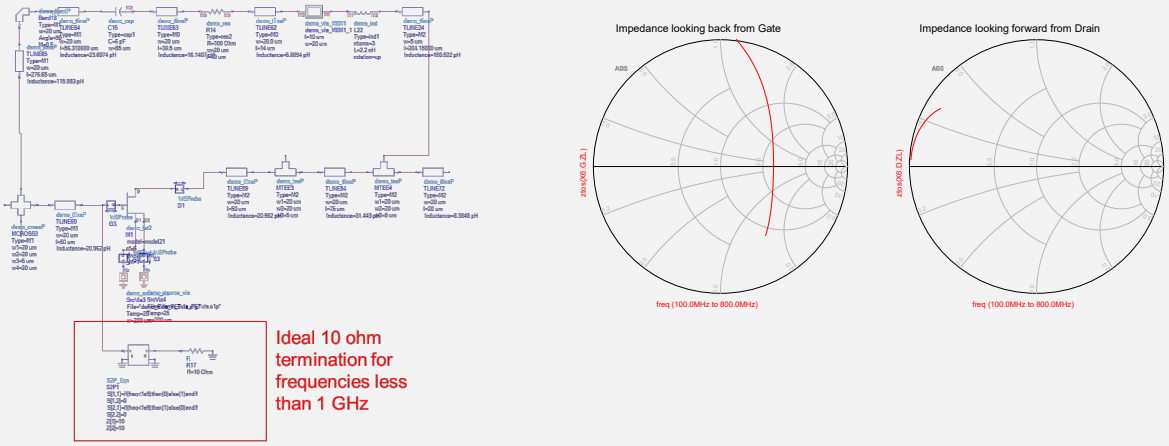


Figure 58. Applying an explicit controlled termination to the gate node stabilizes the circuit, confirming that the problem is related to the in-situ loading condition on the gate of the output stage transistor.

Hopefully this example illustrates the tremendous amount of insight that gained by applying the techniques described throughout this paper in a complementary fashion. K-factor may have been almost enough to infer an instability, but it still wasn't clear as to the root cause. Driving Point Admittance analysis combined with a virtual loadpull on the output device was able to give a clear indication of the root cause of the problem. Incidentally, while Ohtomo's Network Bifurcation technique was generally in agreement with the Driving Point Admittance result here, it's probably wise to discount this result for further analyses. The active network was shown to be unstable, which as described earlier, violates an underlying assumption that's made in the Ohtomo technique. So, even though NDF was not practical, and even though Network Bifurcation was probably not valid, we were *still* able to figure out the underlying cause of the problem using Driving Point Admittance. That's the power of having so many techniques and approaches readily accessible through the WS-Probe.

This example introduced lots of new concepts and techniques. First, it's best to place the probes around all of the active devices in a complex circuit. Second, to do Ohtomo Network Bifurcation accurately, you need to place the probe terminals pointing consistently towards the active device. Also, if the circuit analysis contains low impedance nodes, you may need to add a parallel high value resistor to improve the Ohtomo loop gain computation. While the problem here initially seemed to point to a feedback issue in the amplifier itself, a "Sesame-street" style analysis to individually cut the feedback loops did not result in the circuit becoming stable, which was a little surprising. Analysis done on the impedance of the individual device showed that the loading condition of the circuit at the gate node seemed to be causing the instability. Finally, a clever simulation trick with an equation-based S-parameter block validated the device level analysis, stabilizing the amplifier circuit by altering the low frequency transistor termination. All of these tests and techniques are useful in many types of circuits, not just this one.

Example 3: Using EM Simulation to Visualize Instability

The final example will explore a novel methodology for visualizing areas of instability due to feedback on a physical design. The test circuit is a Power Amplifier built using the Qorvo QPD1015, which is a packaged GaN device with a nonlinear model provided by Modelithics [20]. The PA uses a Class AB bias and as such, it's necessary to consider the stability under large signal input drive. Figures 59 and 60 show the circuit and in-band performance at 1 GHz, indicating ~20 dB gain and peak efficiency of ~60% with Pout >40 dBm. The internal impedances and load line are also viewable at the intrinsic current source of the device (these indicate a Class J loading condition), but as usual, it's not possible to shut this current source off in the device model itself.

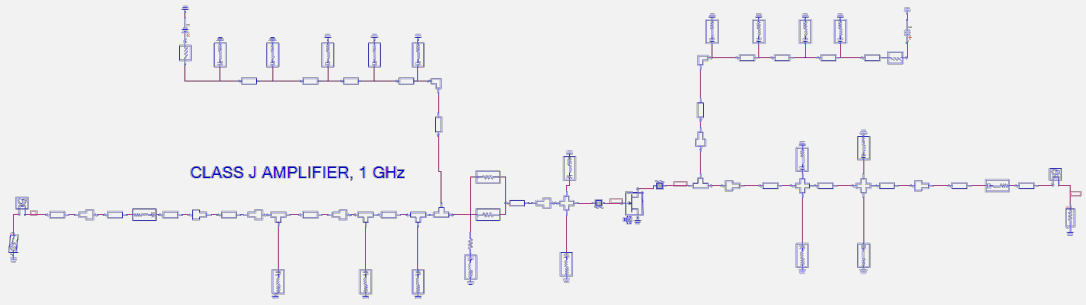


Figure 59. Class J GaN Power Amplifier at 1 GHz, designed using Qorvo's QPD1015

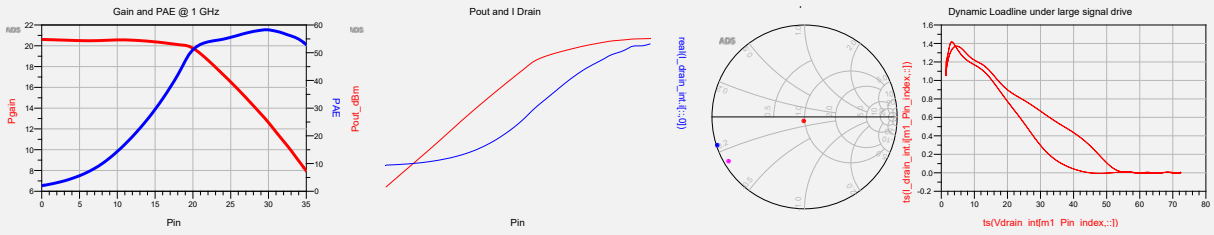


Figure 60. Large signal results for the PA: Gain, efficiency, power, current, generator impedance, and load line.

To assess stability, the designer adds WS-Probes to the input and output of the transistor (the source is ideally grounded). A Harmonic Balance simulation is set up at an input power near gain compression. The stability analysis is straightforward to configure with the WS-Probe by checking the box in the Small Signal tab of the Harmonic Balance Simulation controller. Again, this device model, like most commercially available models, does *not* offer access to turn off the internal current generator to compute Normalized Determinant, therefore, it's necessary to use other stability methods in the analysis.

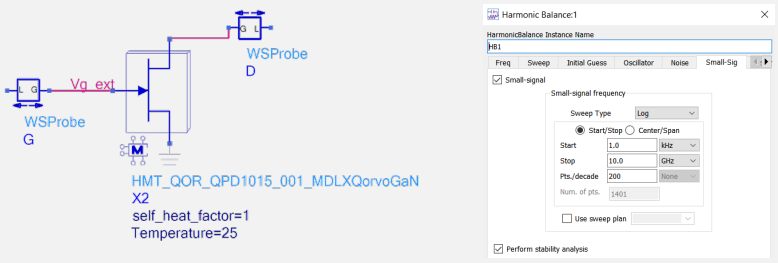


Figure 61. Like most practical situations, the device model does not have card-level access to turn off the active generator, so one cannot compute NDF directly for the large signal case.

Three stability results are worth considering in this case: Ohtomo's Network Bifurcation, Driving Point Admittance, and Tian's Bilateral Loop Gain. Figure 62 shows the results for the large signal simulation with a small signal stability sweep around the carrier tone. Analysis was performed at both the gate and drain nodes of the device.

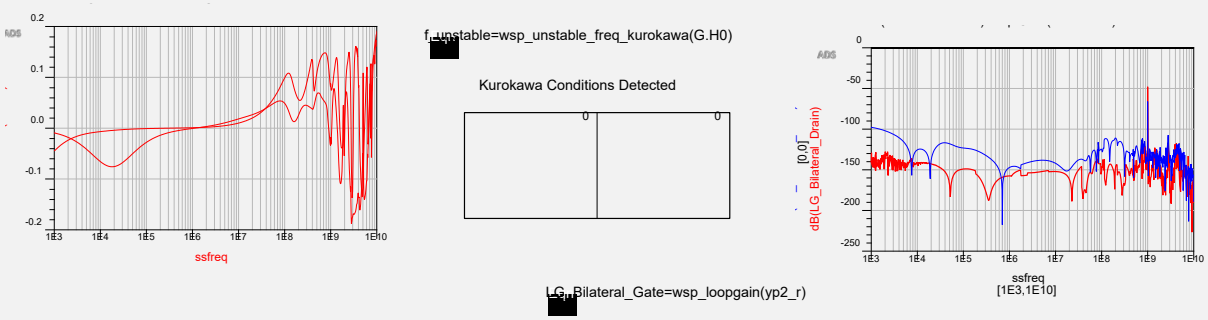


Figure 62. Large signal stability results: Ohtomo's loop gain, driving point admittance and bilateral loop gain all indicate stability.

Clearly from Figure 62, the stability assessment for this amplifier is encouraging. Ohtomo's Network Bifurcation loop gain at the two interface nodes shows no encirclements and there are no Kurokawa conditions detected in the Driving Point Admittance response. Also, perhaps suspiciously, the loop gain is very low. Of course, these results are too good to be true! Indeed, just as in the earlier example, the problem is that the circuit contains no loops! Try it yourself: go back to the earlier schematic and trace a line from the output of a probe through the circuit and back to the input of the same probe. It's not possible: every path ends in an ideal ground symbol! This perhaps the most common problem designers run into when using the probes: feedback loops are not properly modeled!

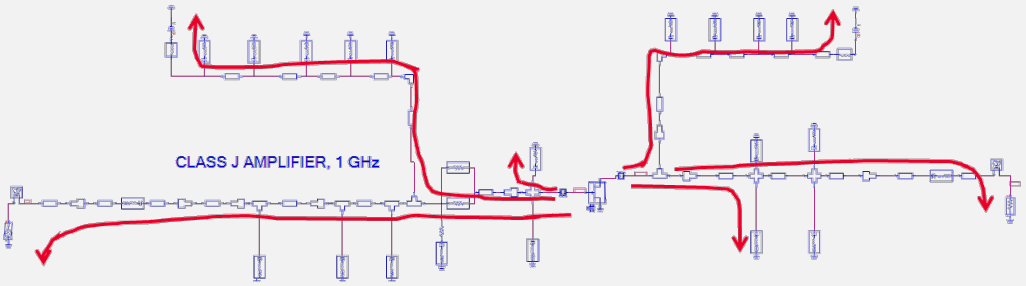


Figure 63. Visual inspection reveals the reason for the stability results: there are no loops modeled in this ideal circuit!

As rudimentary as it might look to an experienced engineer, it is all too common in industry to see such loops go completely unaccounted for in simulation models. In fact, the in-band performance for this amplifier with this component-based schematic, and that may lead designers to wrap up the simulation work and move on. At 1 GHz, perhaps performance will match measured results if the in-band modeling is accurate. However, the out of band coupling and feedback is certainly not accounted for in the circuit analysis. Modeling these other paths and loops out of band is tremendously critical for stability, even if it doesn't impact fundamental performance. After all, a circuit which is oscillating at some other frequency outside of the fundamental will not be easy to measure in the lab, even if the fundamental frequency path is well modeled and expertly designed!

To model these coupling effects properly, it's necessary to perform an Electromagnetic simulation of the physical layout. Then, the designer should combine the EM model with the large signal circuit simulation that includes sources, SMD components, and the transistor itself. In this example, Keysight's PathWave RF Pro performs the EM simulation, allowing the designer to take a "snapshot" of the layout, apply ports automatically, and run an EM analysis using multiple simulation engines. Then, it's easy to return the results back to the circuit simulation environment for large signal modeling of the amplifier combined with the physical layout structure. Performing this task alone can take hours of setup and manual labor to import the layout, configure the EM analysis, and transfer the results back to the circuit tool. RF Pro made this step easy, almost trivial. All in all, it took less than 5 minutes to configure the EM simulation and transfer the results back to the schematic. The EM analysis itself took about 30 minutes to run.

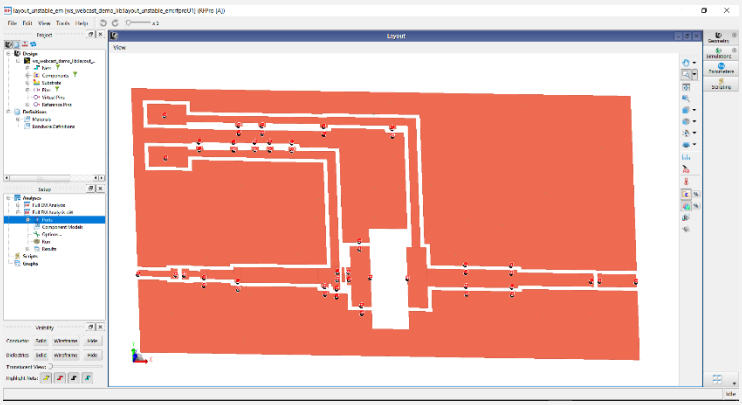


Figure 64. EM / Momentum Simulation of the physical layout performed using Keysight's RF Pro.

The circuit is re-analyzed with the EM model from RF Pro, with stability results shown in Figure 65.

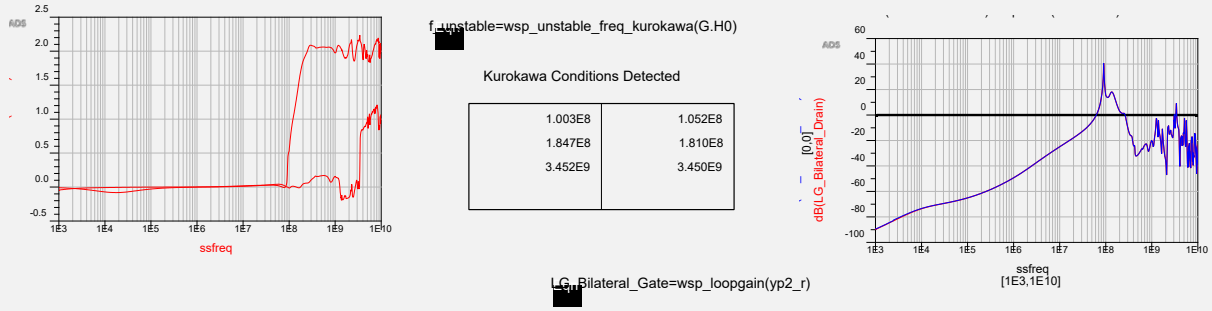


Figure 65. Incorporating EM results back to the circuit, instability is now obvious in all three metrics.

With EM effects included, both Ohtomo's Network Bifurcation and the Driving Point Admittance show multiple stability problems. The instabilities occur both below and above the passband of 1 GHz. The bilateral loop gain response also shows spikes in these areas, which indicates that the problem may be feedback related. Obviously, several feedback loops have appeared in the EM analysis which were not part of the idealized circuit. The problem is, it's not always trivial to find such subtle feedback paths when dealing with a complex physical design. In situations where feedback is the suspected culprit, it's helpful to analyze the Kurokawa frequencies directly on the loop gain plot, as shown in Figure 66.

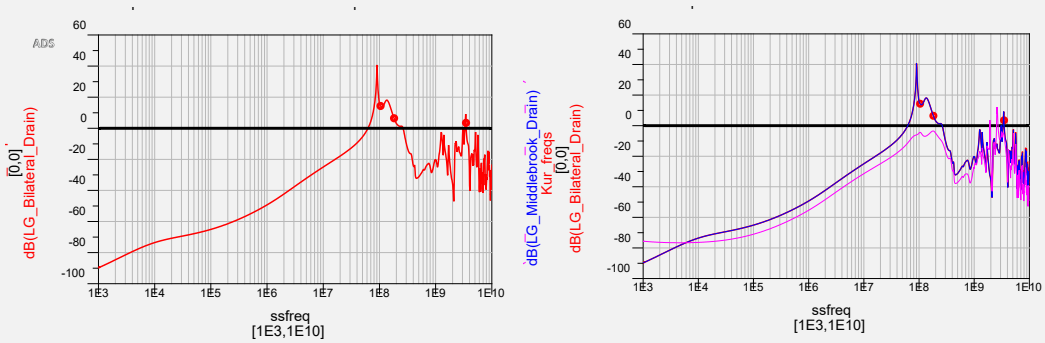


Figure 66. Kurokawa frequencies plotted on top of bilateral loop gain (left), indicating that instability occurs in regions of high loop gain. On the right, bilateral loop gain plotted vs. forward and reverse unilateral loop gain (Middlebrook). This indicates that the dominant direction for the low frequency loop is output-input, but the dominant direction for the high frequency loop is less obvious.

Figure 66 shows that all three of the unstable frequencies occur in regions where the loop gain is greater than zero. Using different loop gain techniques, it's even possible to infer the dominant direction of the feedback, which can shed additional light on the root cause of the problem. Let's look at how to do such an analysis.

Recall from the earlier discussion that the Bilateral loop gain derived by Tian was really an extension of Middlebrook's unilateral dual-injection technique. So, by comparing the bilateral loop gain with the forward and reverse Middlebrook loop gains, a designer can get a good sense for the directionality of the problematic feedback. The plot on the right-hand side of Figure 66 shows the forward and reverse unidirectional Middlebrook loop gains (blue, pink) superimposed on top of the bilateral loop gain (red).

The fact that the forward unilateral loop gain closely matches the bilateral case is not surprising, as it indicates most of the coupling is in the forward direction, from output to input. This means the feedback path is traveling forward through the transistor, which is not surprising as the transistor has a much higher S21 than S12. But the reverse unilateral loop gain curve *does* show some coupling in the opposite direction as well, especially at high frequencies. In fact, there are a few frequencies where the reverse direction gain is higher than the forward gain (Figure 59 right, 2-3 GHz region). So, while the output-input direction clearly dominates lower frequency loop gain, the higher frequency loop gains appear to couple almost equally in both directions: output to input and input to output. This information can be extremely useful when trying to fix a feedback problem in a complex design.

So, the circuit is unstable, and this instability is probably due to feedback around the active device. The problem is, tracking down feedback loops in a physical layout is not easy. We cannot just physically break loops by cutting schematic wires as in the previous example. It's necessary to take a different approach.

The methodology that follows can greatly simplify the process of finding physical locations of feedback which causes instability. The key is to use a new simulation technique called EM-circuit excitation. EM-circuit excitation uses the nodal voltage and current derived from a circuit simulation to stimulate an electromagnetic structure, allowing for visualization of current density or radiation patterns as they would occur when combining an active circuit with a physical layout. Normally, finding a stability problem using

EM visualization is like looking for a needle in a haystack because the coupling changes based on stimulus and frequency. However, when the circuit itself stimulates the structure, and when the analysis focuses on frequencies that are known to have instability with high loop gain, it potentially enables a direct visualization of the coupling problems on the layout.

This excitation is tricky to do with a Harmonic Balance analysis because you need to stimulate both the fundamental and the unstable frequency to visualize the coupling, i.e. the frequencies would need to be harmonics of one another. However, if one uses an AC analysis instead, it's possible to apply the stimulus to the input or bias lines at *any frequency*. For example, in this case, the circuit operates at 1 GHz, but there is an instability at 100 MHz. Applying an AC signal to the input at 100 MHz will cause most of the input to reflect off the first mismatch discontinuity. However, a small portion of that signal will traverse through the circuit and resonate internally. So, by adjusting the visual scale for current density and ignoring the strong reflected signal at the input, it's possible to visualize coupling paths contained *inside* of the circuit.

To illustrate, let's consider the circuit from Figure 67, consisting of an EM block, a transistor model, and passive SMD components. Now, instead of running a Harmonic Balance simulation at the fundamental frequency, let's use a simple AC sweep instead. Figure 67 shows how this simulation generates a dataset later used to stimulate the EM structure itself.

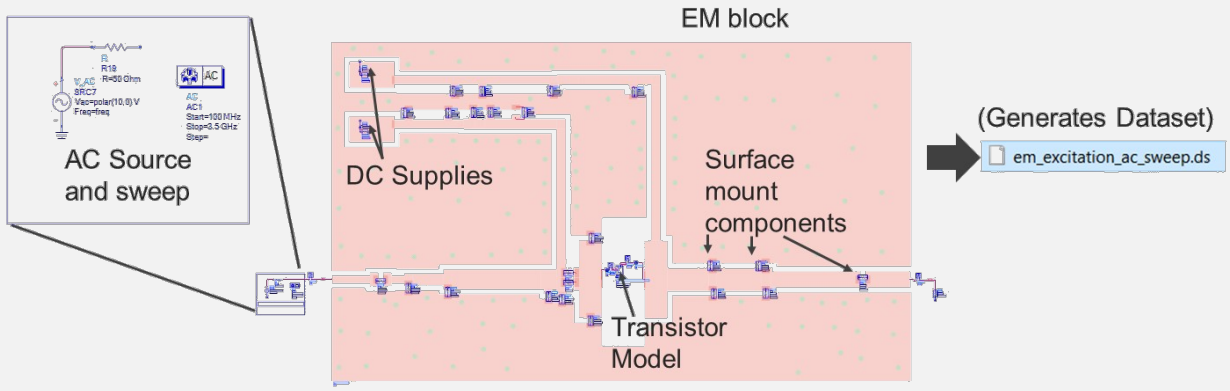


Figure 67. Using an AC simulation to create a dataset used to stimulate the physical EM structure.

Next, configure the previously performed EM simulation to visualize current density in RF Pro. Instead of using a generic single port voltage or current stimulus, the dataset generated from the AC simulation stimulates the physical layout, as shown in Figure 68.

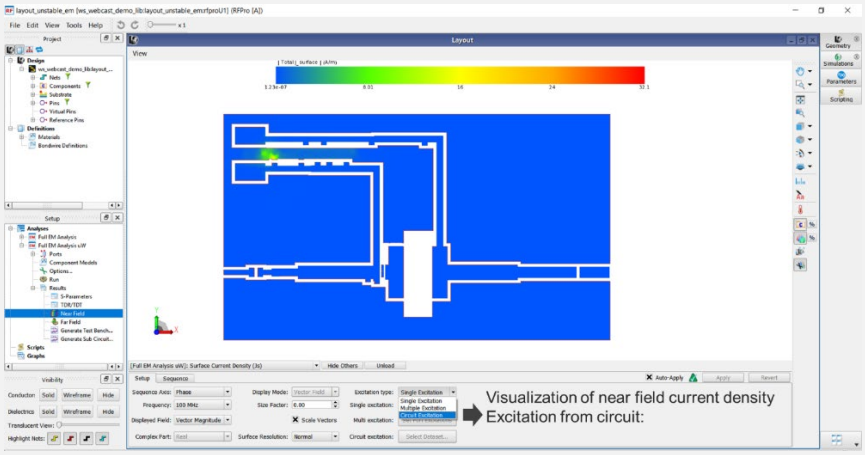


Figure 68. Visualizing the excitation from the AC circuit on the physical EM structure in the form of current density.

Now, the designer can directly visualize unstable frequencies, with the color scale adjusted to show internal circuit current density. Figure 69 shows the EM structure's current density visualized at three points: at the low frequency oscillation (~100 MHz), at the fundamental frequency (1 GHz), and at the high frequency oscillation (~3.4 GHz). At both oscillation frequencies, the current density clearly shows the feedback loop which is causing the problem.

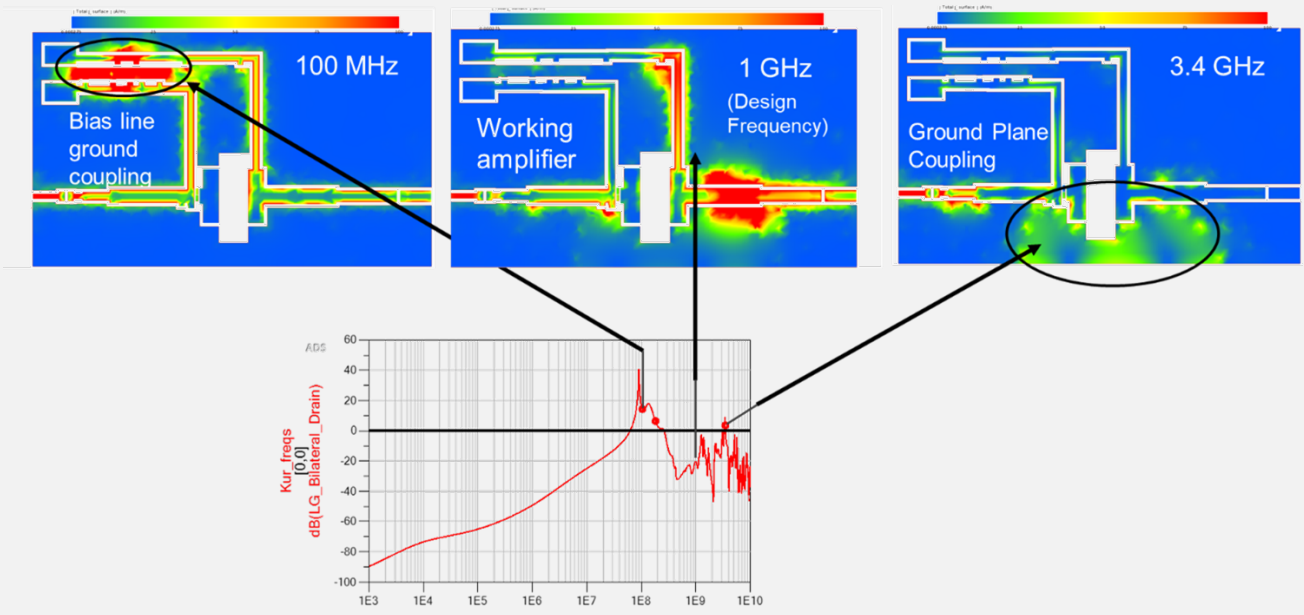


Figure 69. EM-circuit excitation results at each of the unstable frequencies (left/right) along with the fundamental frequency (center). At low frequencies (left), the dominant feedback mechanism is through the bias lines. At the center frequency (center), most of the energy is directed to the thru path. At higher frequencies (right), the dominant feedback mechanism is through the ground plane near the transistor.

At 100 MHz, the bias lines and their associated grounds light up – this indicates that the signal is feeding back from the output DC bias line to the input bias line and through the transistor. It's even possible to infer the direction from the earlier loop gain analysis in Figure 66. In contrast, at 3.4 GHz, above the design frequency, the bias lines are cold, but the *ground plane* around the transistor has a relatively high amount of current. Combining this data with the directional loop gain analysis discussed earlier implies that the signal is coupling through the ground plane between output and input, and vice-versa. The fundamental frequency analysis (shown for comparison) indicates that the circuit is indeed working as expected (it's an amplifier!) – note the DC lines block most of the signal from coupling to the supply and the ground is also well isolated. The amplifier clearly boosts the output signal before it's sent through the matching network to the antenna. By applying EM circuit-visualization specifically to frequencies where we knew there would be stability problems, it became easy to see the offending coupling path in the physical design.

With such a powerful visualization, it's not too difficult to fix the coupling problems on the layout. At low frequencies, physically separating the bias lines from one another is enough to reduce the loop gain substantially. At high frequencies, additional VIAs can be added to the ground plane to improve the isolation. The result is a stable circuit with significantly lower loop gain, shown in Figure 70.

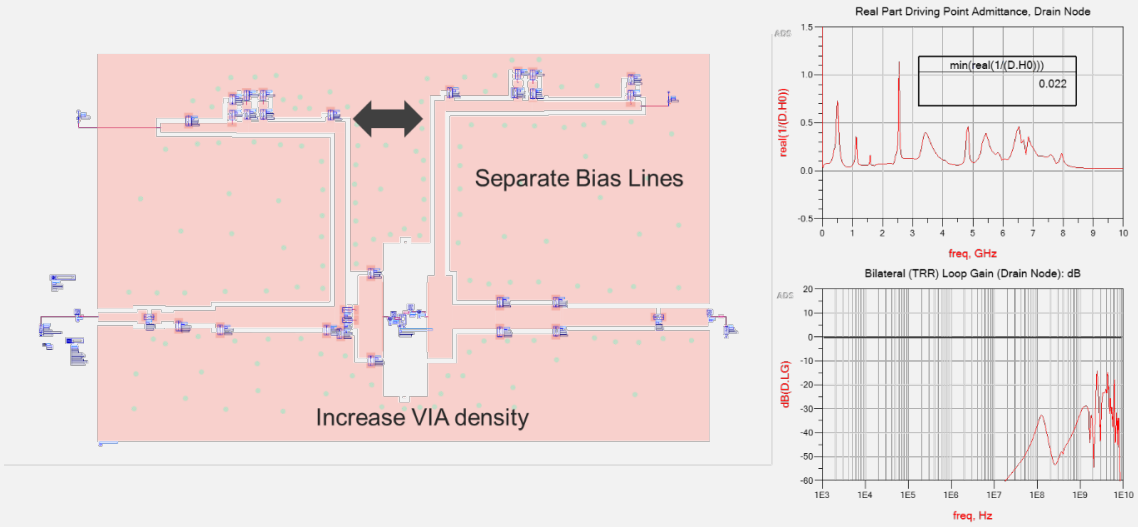


Figure 70. Layout modified to improve stability, based on the insights found using EM-circuit excitation. The bias lines are physically separated and the VIA density on the ground plane is increased. The circuit is now stable as indicated by Driving Point Admittance at the drain (real part positive for all frequencies), with loop gain attenuated.

To close, the reason visualization is so effective on this circuit is because the instabilities are directly related to high loop gain, or feedback. If you think back to the previous example, even though loop gain was high, the problem was transistor loading, not external feedback. For that case, this visualization technique would have been less effective. Also, although the swept AC signal was applied to the input, you can see from Figure 66 that most of this signal is reflected out of band because the input side is red. However, some small amount of energy is transferred inside of the circuit and that energy revealed the dominant coupling mechanisms. So, the scale for the visualization might need adjustment to show the smaller current inside the circuit instead of the larger current reflected at the input. For complex multi-stage circuits, it's also valid to inject the signal into the bias lines or even a component ground. The important thing is to terminate the rest of the circuit in its normal operating state, with capacitors and transistors etc. populated. Finally, the feedback mechanism for this analysis must have at least some energy in the form of current. In a few circuits, it may be more effective to look at the E-Fields from the EM analysis instead of the current density. That would be a similar approach with a slightly different visualization.

This example showed how it's possible to apply advanced simulation techniques along with the right combination of tools to design high frequency circuits which are first-pass stable. In fact, making high frequency circuits stable out of the box is not just a time saver, it's becoming a necessity as frequencies go up and systems become increasingly complex.

Summary

This paper described how to apply classic stability techniques to modern high frequency circuits in a simple and efficient manner. First, we considered the traditional Rollett stability (or K) factor. While this approach is simple and covers the entire Smith Chart, it assumes that the network itself is stable in the unloaded sense, a condition which may not always be valid. As shown later, for some practical cases, the S-matrix determinant being greater than unity invalidates the K-factor, particularly for situations where the return losses are greater than 0 dB. In these circumstances, the result of the analysis is undetermined.

With K-factor being potentially problematic, we considered a number of loop gain techniques: Osctest, Middlebrook, Hurst, and Tian's method were all studied. While these techniques are very insightful, none are rigorous because due to Cauchy's Principle, their encirclements only reveal the *difference* in unstable poles and zeros, rather than the absolute number of zeros. Also, many of the loop gain techniques make assumptions in derivation which can invalidate the results, for example, some techniques only consider unilateral signal flow, while others are based on an ideally grounded admittance network which is not realistic for most high frequency transistors.

From there, we focused on fundamental, rigorous measures of stability as derived by Bode; these are Return Difference and Driving Point Impedance. The key to the rigor of these metrics is that the derivations are performed using the network determinant. For Return Difference, removing the active elements from the determinant based computation guarantees a stable denominator, so encirclements are known to contain only RHP zeros. For Driving Point Admittance, the classic "Kurokawa" oscillator condition determines instability from the response. There are also modern implementations which extend the classical methods: applying Normalized Determinant and Active-Passive Network Bifurcation are more effective for today's complex, multi-transistor circuits. Still, there are disadvantages to these

modern techniques: NDF requires intrinsic access to turn off the active sources inside of the device model, and Network Bifurcation requires the blocks to be independently stable for a valid analysis.

Because every technique has pros and cons, it's more practical to have the ability to apply multiple techniques to any given circuit; in fact, the various techniques are quite complementary when used together. The problem is each stability metric is difficult to derive and requires a different set of circuit manipulations to get the needed result. Therefore, it's necessary to use multiple simulation testbenches, along with manual manipulation of the circuit. There have been previous attempts to unify stability analysis techniques using an impedance probe called the S-probe, however this tool suffered from inaccuracy under high feedback conditions, the very conditions that produce instability!

This Application Note described a new analysis technique which is based on an impedance probe called the WS-Probe. The WS-Probe outputs bidirectional impedances in an accurate way even under high levels of feedback. With this probe, it's possible to derive all the stability metrics discussed mathematically in post-process from one setup, eliminating the need for dozens of additional simulations. In fact, the probe can even mathematically sweep the external loading conditions of the circuit and derive stability at some arbitrary point inside the circuit through "virtual loadpull" functions. The probe results are also extendable to large signal situations with no additional difficultly in deriving the various metrics.

Armed with the WS-Probe, three real life circuit examples were analyzed: a simple biased transistor with probe results compared to K-factor results, a two stage MMIC amplifier which used an unstable transistor, and a packaged GaN based Power Amplifier with instability caused by feedback through the physical layout of the circuit. In working through each of these examples, we gained a unique set of insights by having convenient access to all the stability metrics and techniques stemming from one single circuit simulation. The WS-Probes allow designers to access techniques which would otherwise be prohibitive to set up manually. Having this set of tools at a high frequency circuit designer's disposal truly allows them to master stability up front in the design phase, rather than having to struggle later on in the lab.

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