

Welcome

# Innovations in EDA Webcast Series

August 2, 2012



**IC, Laminate, Package  
Multi-Technology  
PA Module  
Design Methodology**

**Free 1-hour Webcast**  
August 2 - 10 AM (Pacific Time)

Microwave  
**Journal**

**Jack Sifri**  
MMIC Design Flow Specialist

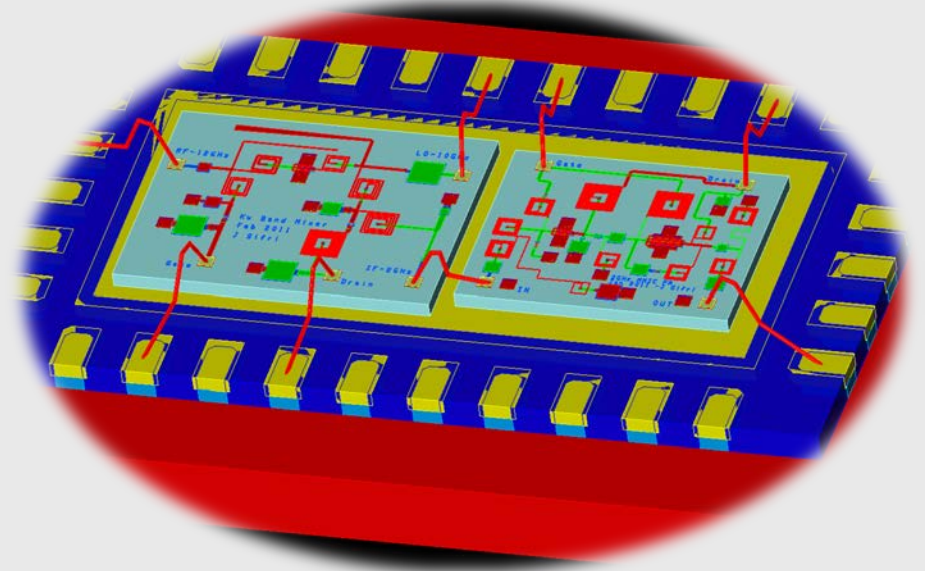


# IC, Laminate, Package Multi-Technology PA Module Design Methodology

Realizing the Multi-Technology Vision within a  
fully integrated design flow in ADS

Jack Sifri  
MMIC Design Flow Specialist

August 2nd, 2012



# IC, Laminate, Package Multi Technology PA Module Design

## Agenda

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
  - Single chip module
  - Multi chip module
  - Flip chip /solder bumps module
  - Transceiver module
  - Electro thermal simulation
5. Conclusion

# IC, Laminate, Package Multi Technology PA Module Design

Typical Example:

Complex ICs in multi-chip RF modules:

The New iPad

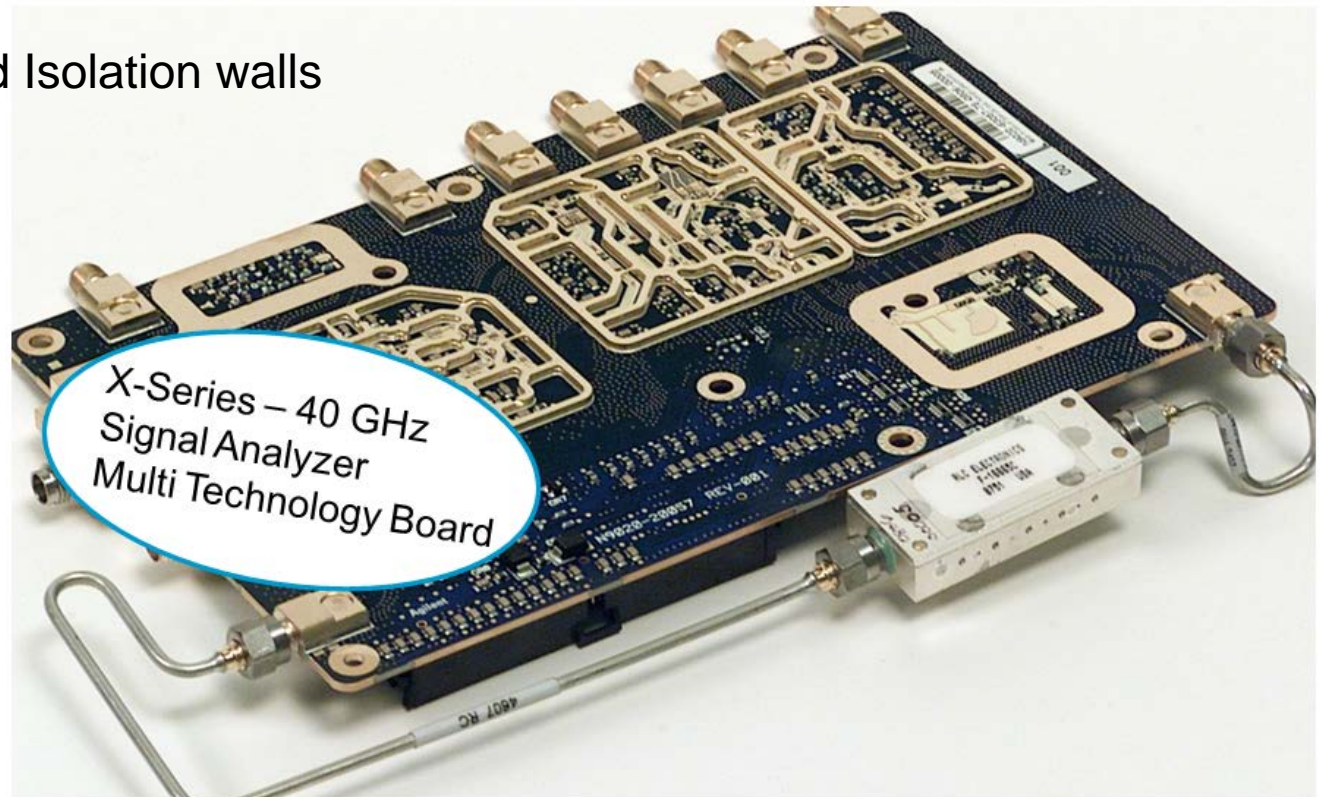
# IC, Laminate, Package Multi Technology PA Module Design

Typical Example:

Agilent's X-Series 40 GHz Signal Analyzer Multi  
Technology Board

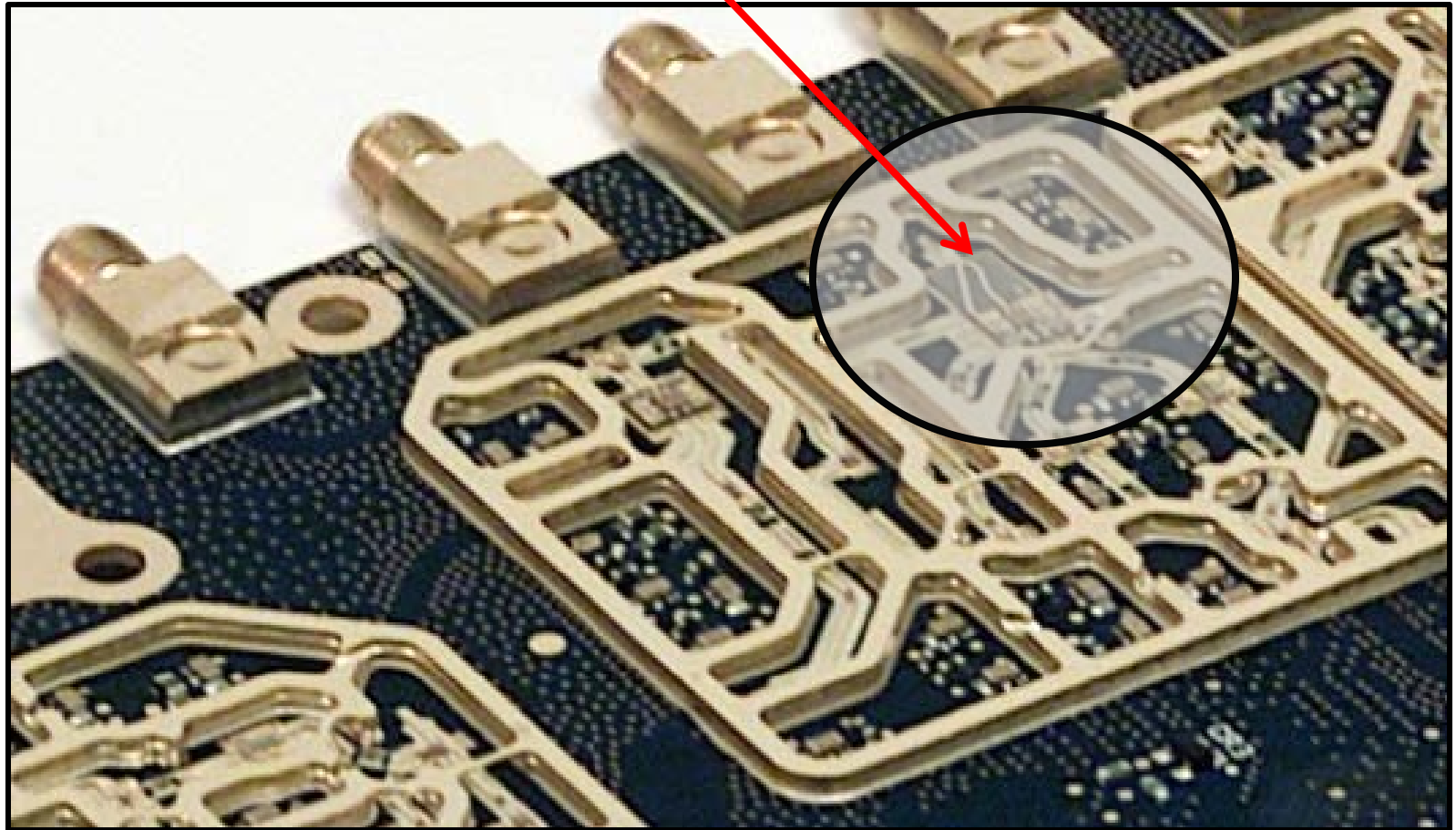
# Multi Technology Example (Agilent EMG)

- Stripline Filter on PC Board
- Designs with SMT packages and bare die components (wire bonded)
- Integrated Circuits Designs and Thin Film Circuit Designs
- Shielding and Isolation walls



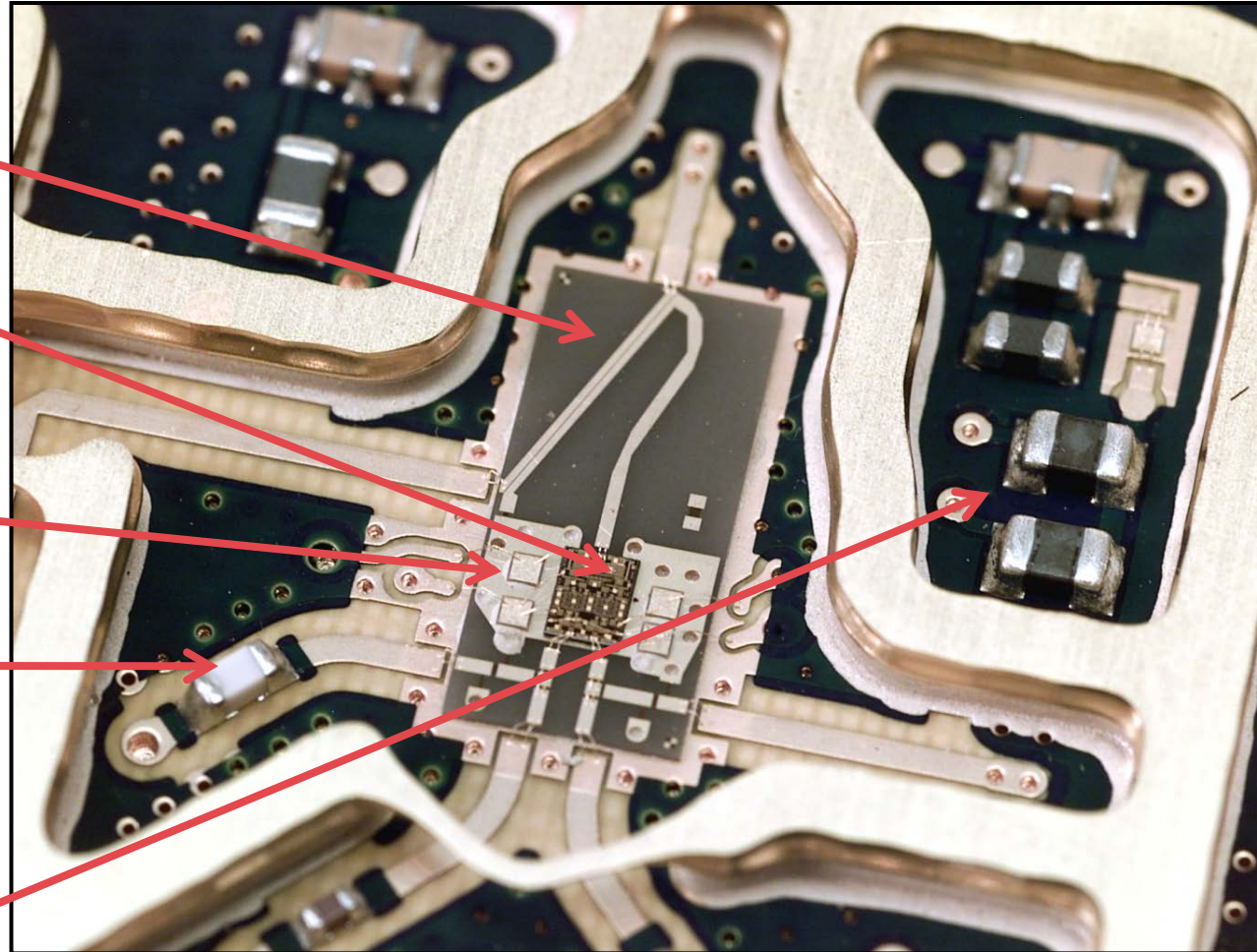
# Zooming on the Thin Film IC Interface

Wide Band LO Distributing Amp



# Thin Film Coupler / LO Distributing Amp Interface

- 6 Layers Rogers Board
- Octave wideband coupler
- GaAs LO distributing amp
- Bond wired and epoxy SMT Caps (DC)
- Blocking Capacitor - to Edge connector
- available LO for testing mixers
- Filtering DC Lines

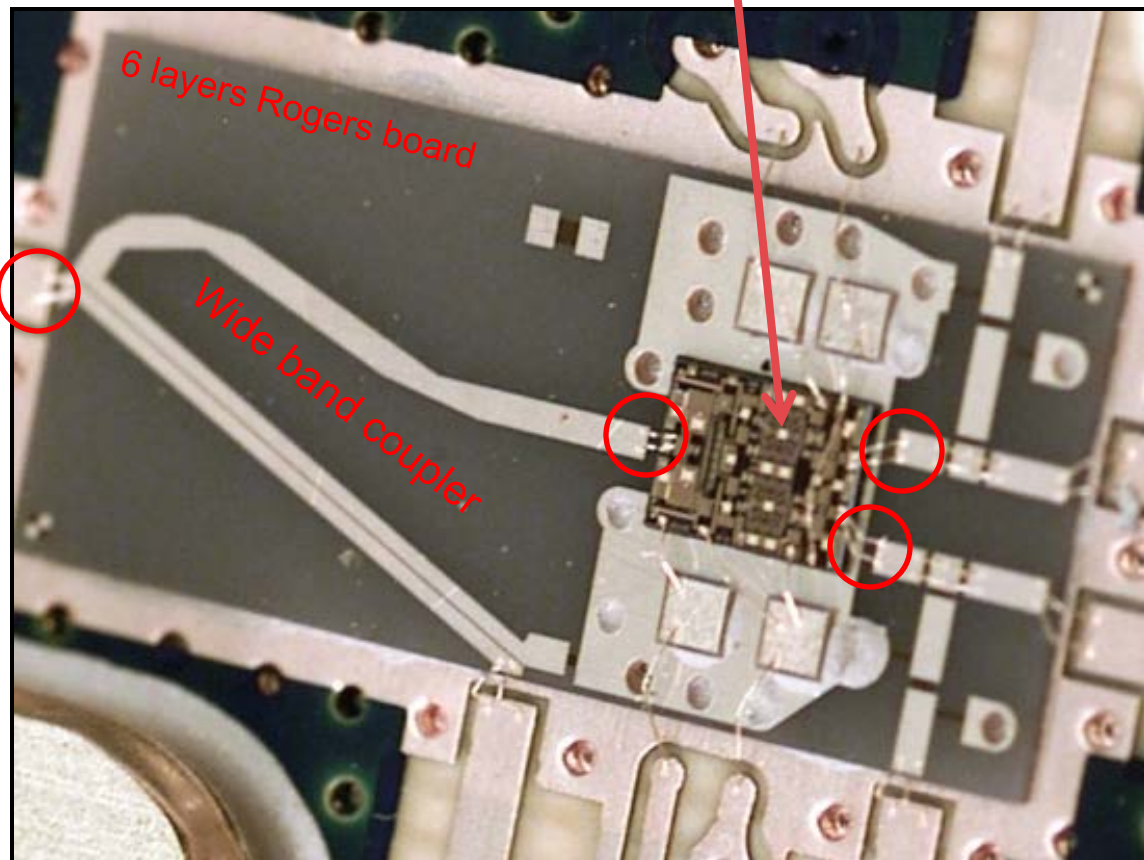




# Board / Laminate / IC/ SMT / Bondwires

A multi-technology module example requires Full 3D FEM Simulation

Wide band LO distributing amp swept for use at different bands



Bond wires / coupler / IC interface caused unlevelled ripple in the wide band output signal

# IC, Laminate, Package Multi Technology PA Module Design

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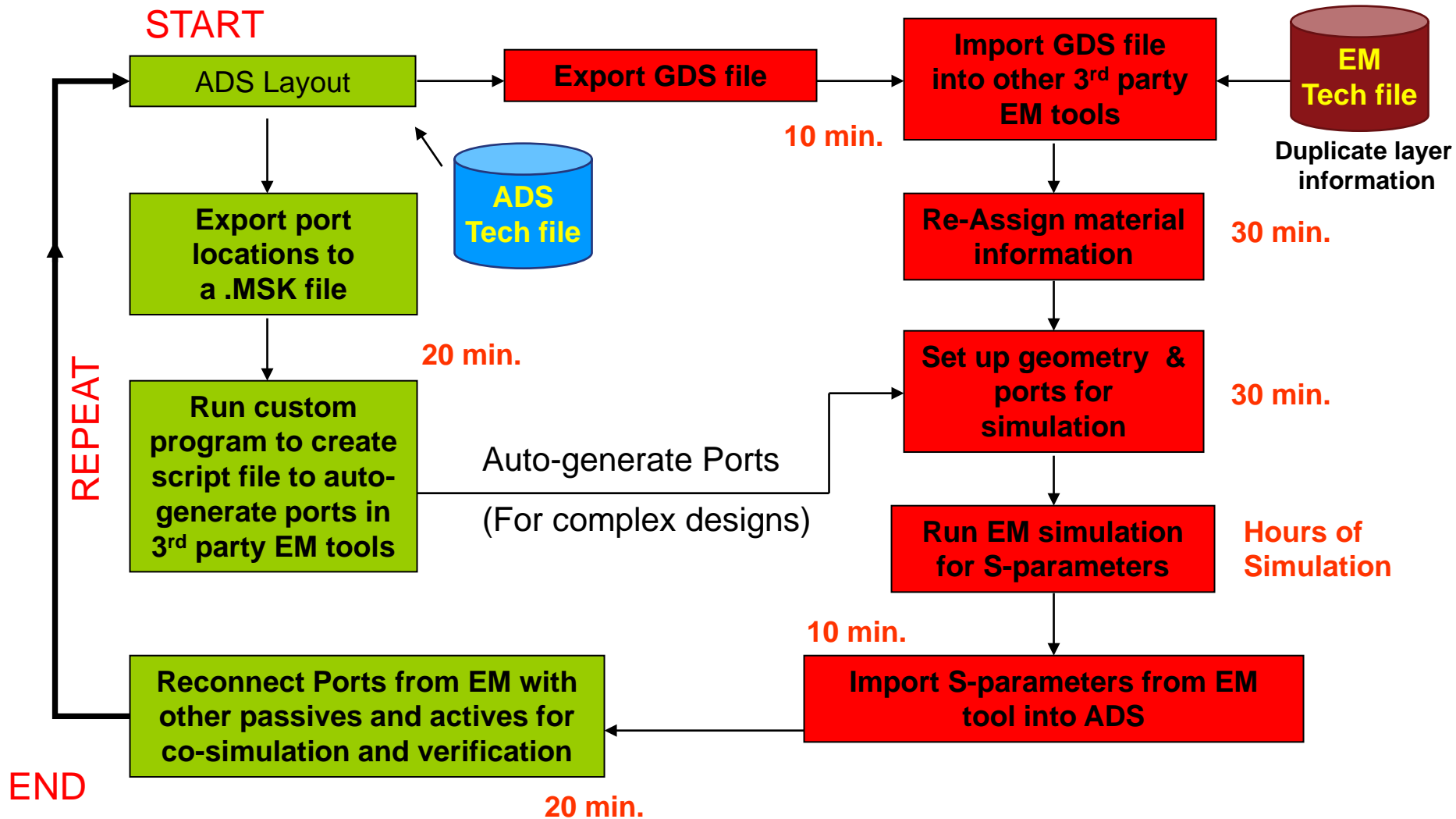
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# IC, Laminate, Package Multi Technology Module Design Challenges

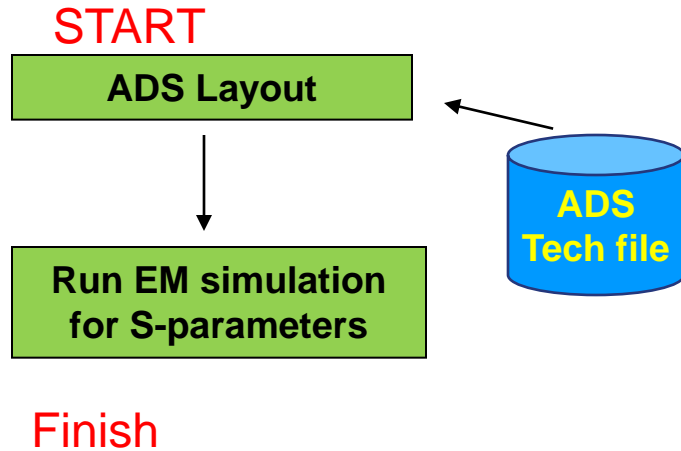
## Design flows are not able to address multiple technology designs

- IC, laminate, package, and PCB need to be designed together
- EM interactions between substrates need to be modeled and accounted for
- The need to move from disjointed tools design flows to simplified integrated flows

# EM Modeling Process in a Disjointed Design Flow



# EM Modeling Process in an Integrated Design Flow

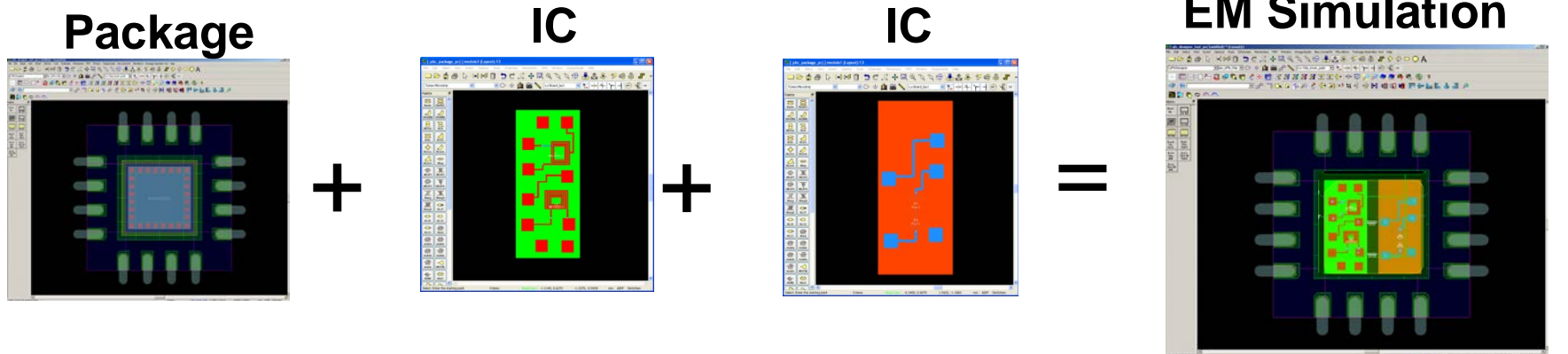


# IC, Laminate, Package Multi Technology PA Module Design

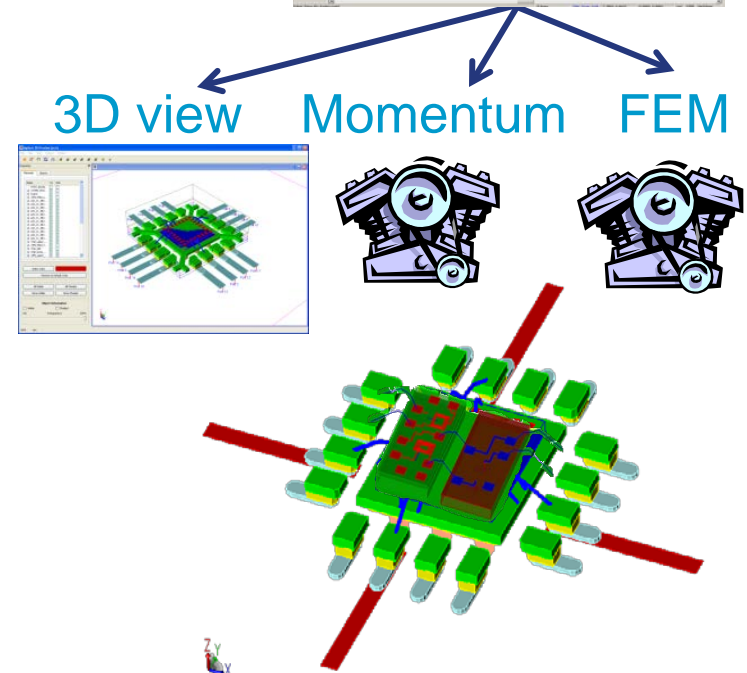
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# Multi-Technology Design Methodology



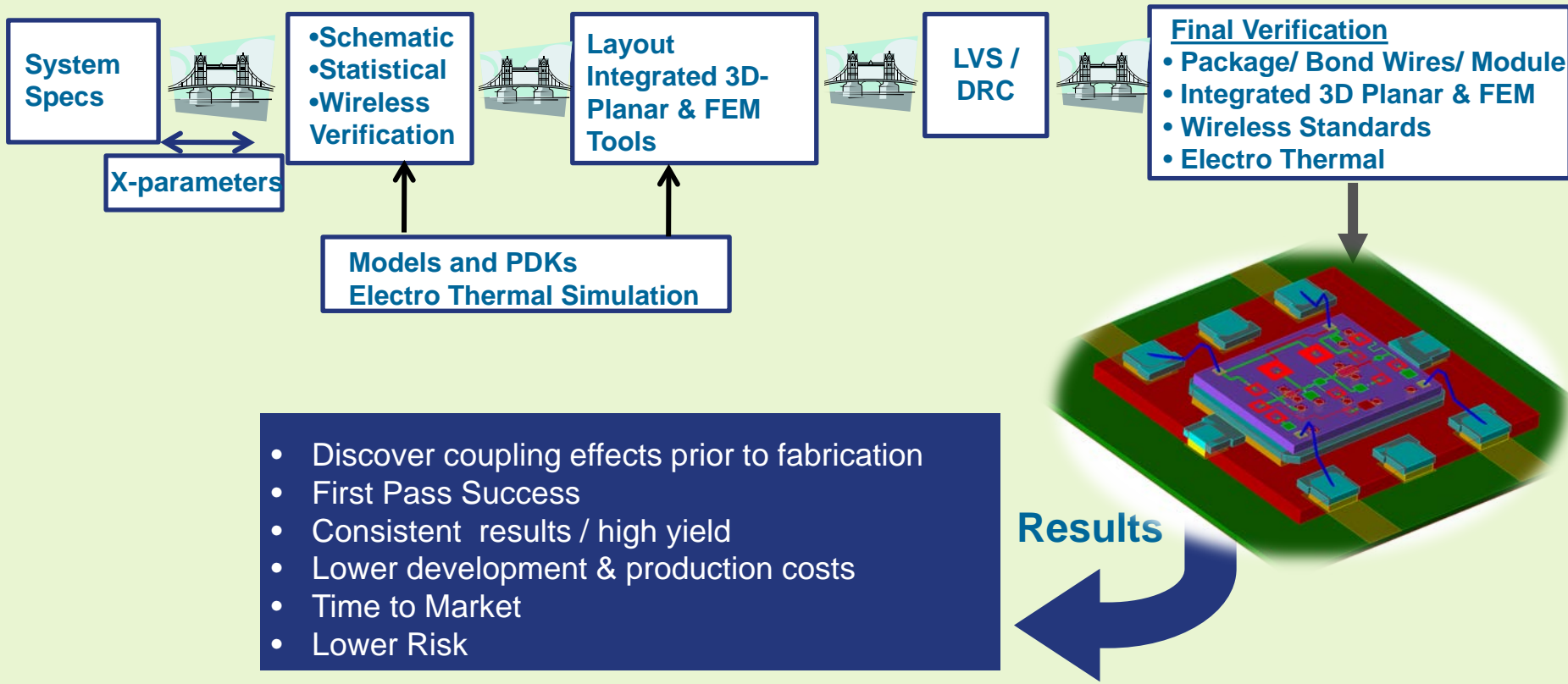
- Discover coupling efforts prior to fabrication
- More effectively optimize design elements for final packaging
- More easily make design trade-offs
- Help diagnose and solve performance problems



# Fully Integrated Design Flow in ADS 2011 and 2012

System; Circuit; Physical; Thermal; Planar/3D EM; Wireless Verification

## ADS Multi Technology Integrated Design Environment



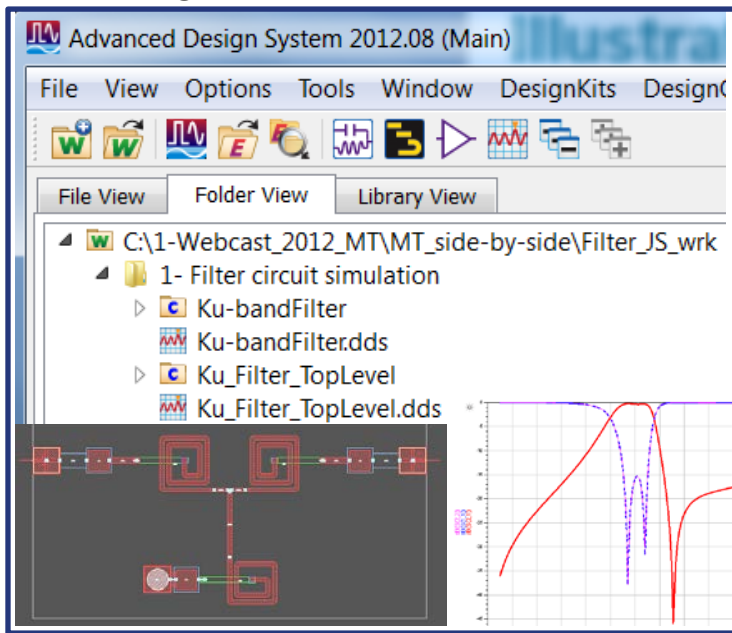
No Walls and no loops in this design process; Fully Integrated Flow;

**One designer completes and verifies the full design all in one design environment**

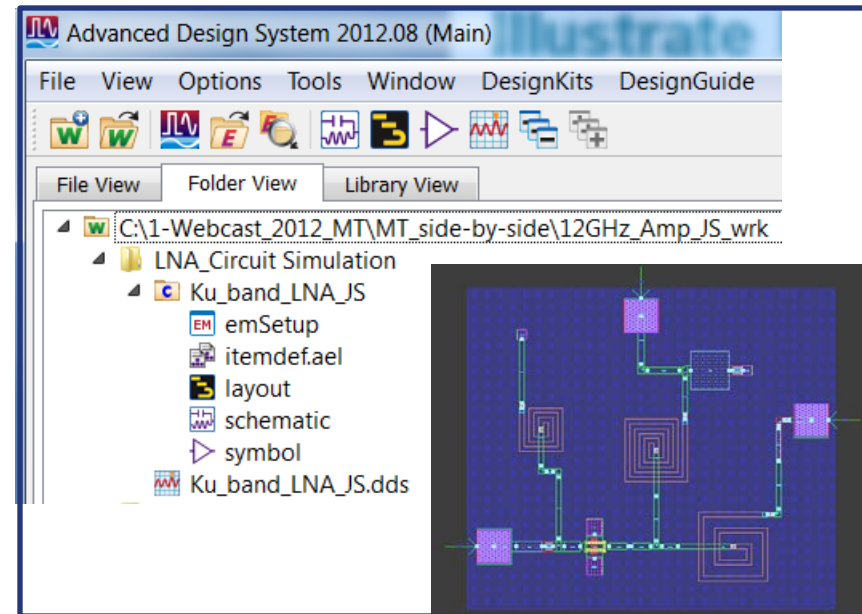


# Multi-Technology Design Methodology

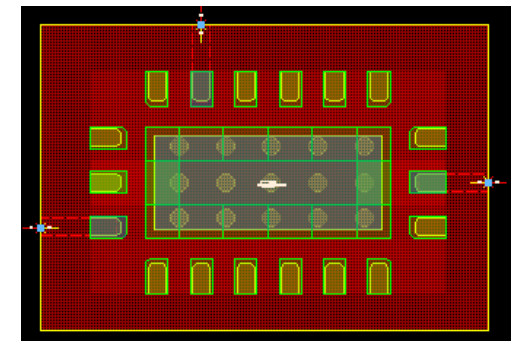
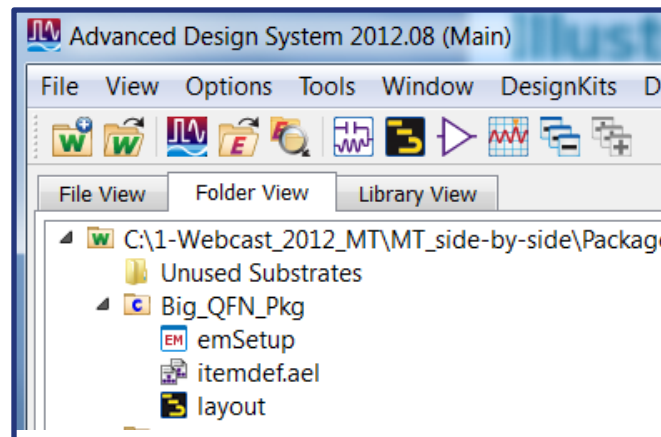
Design IC #1 (IPD – Filter)



Design IC #2 (LNA)

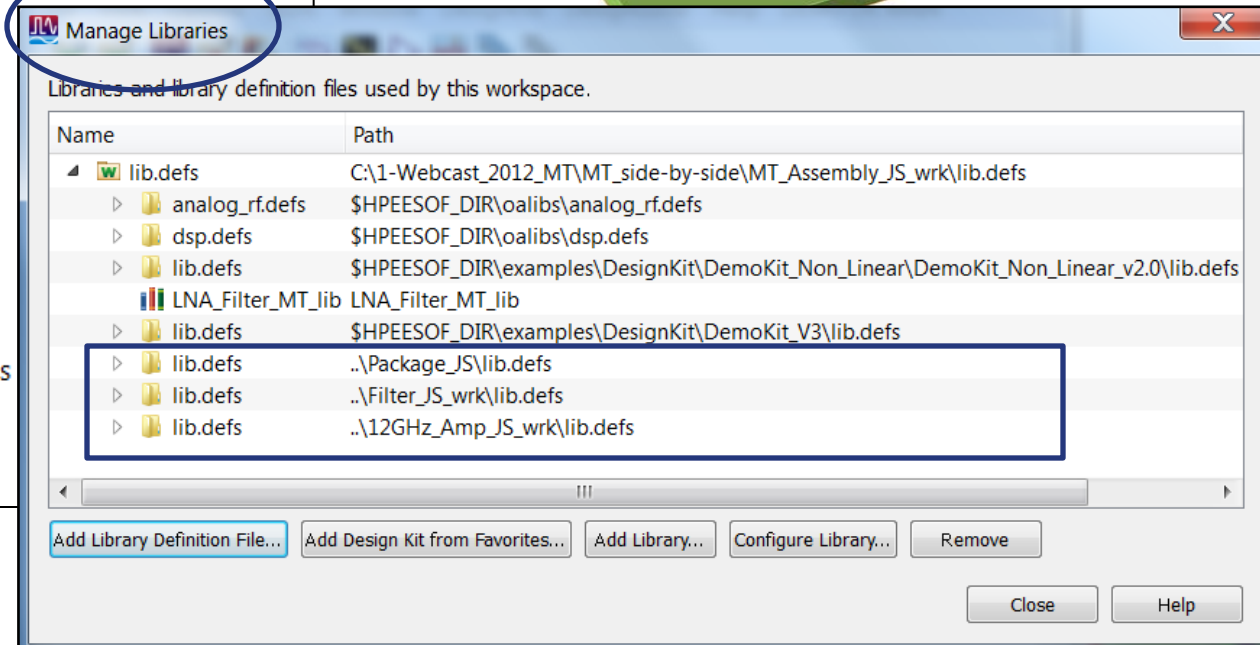
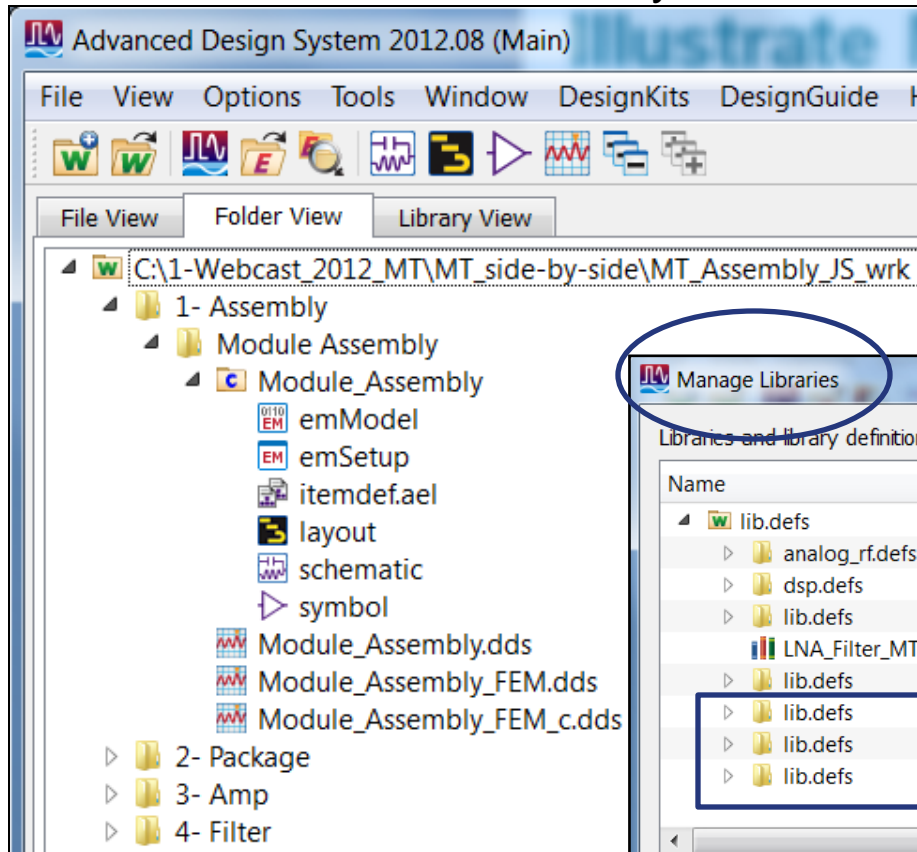
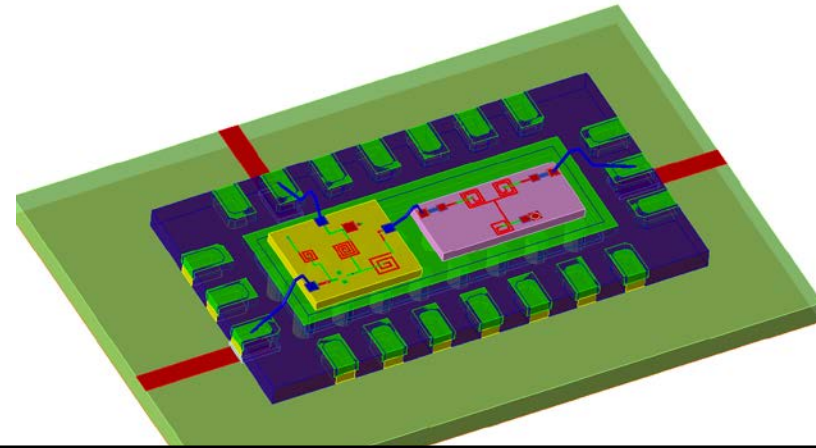


Design Package/Laminate



# Multi-Technology Design Methodology

Bring in all the libraries together  
and build the whole assembly



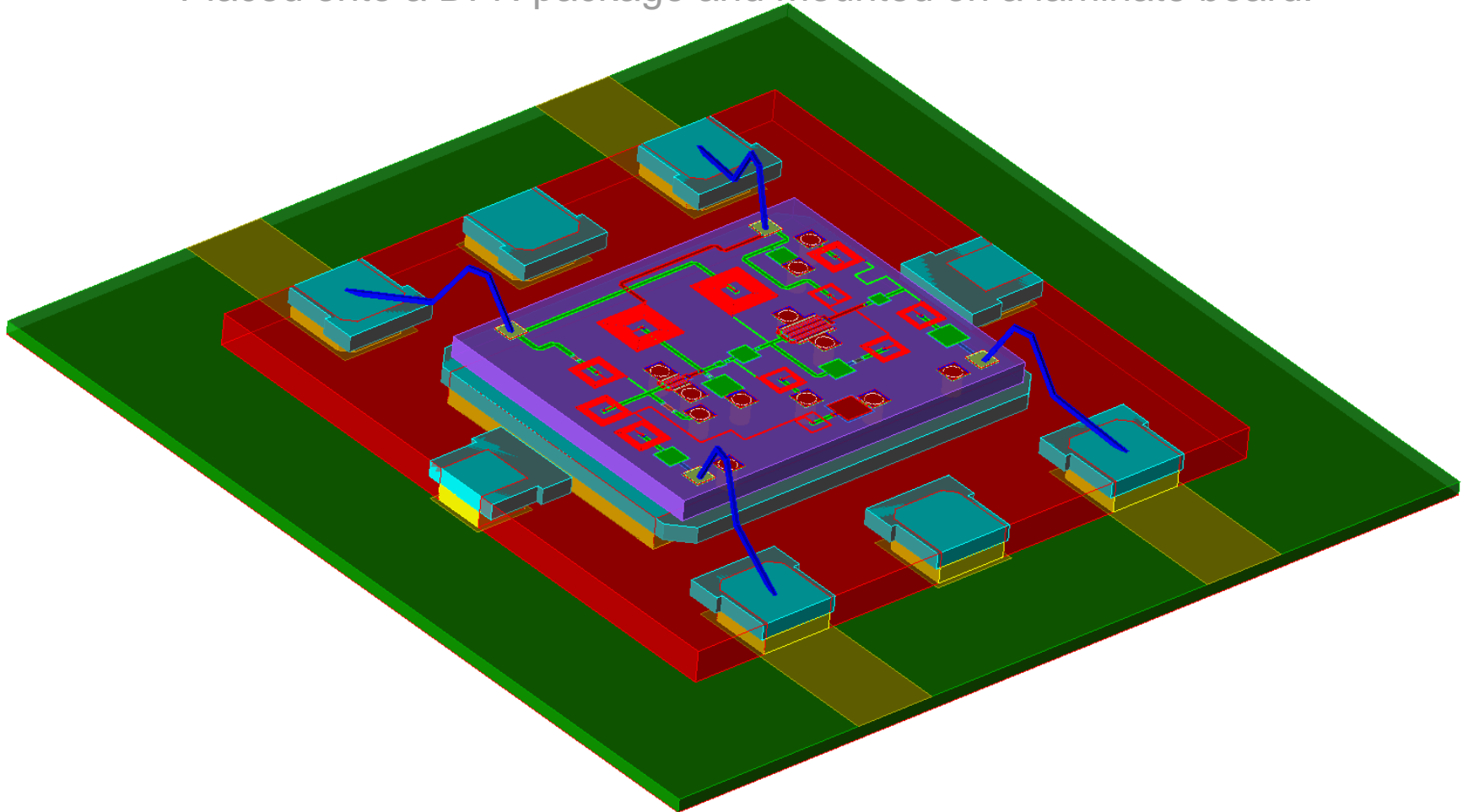
# IC, Laminate, Package Multi Technology PA Module Design

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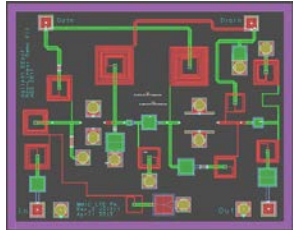
# Example: Packaged LTE PA on Laminate

- Two Stage LTE PA built on a GaAs substrate
  - Placed onto a DFN package and mounted on a laminate board.



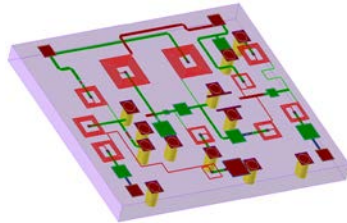
# Packaged MMIC PA Design Example

## Case 1



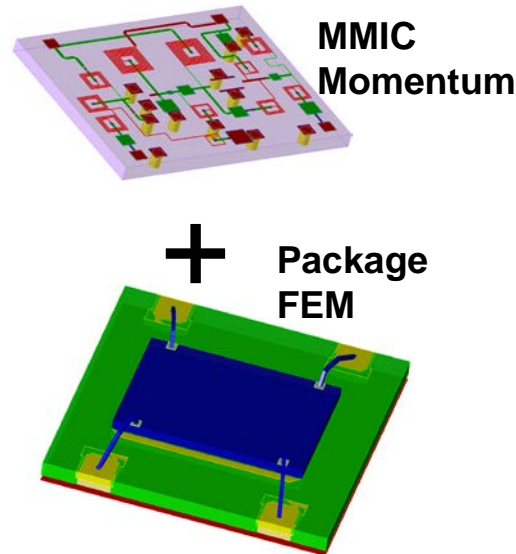
Circuit

## Case 2



Momentum

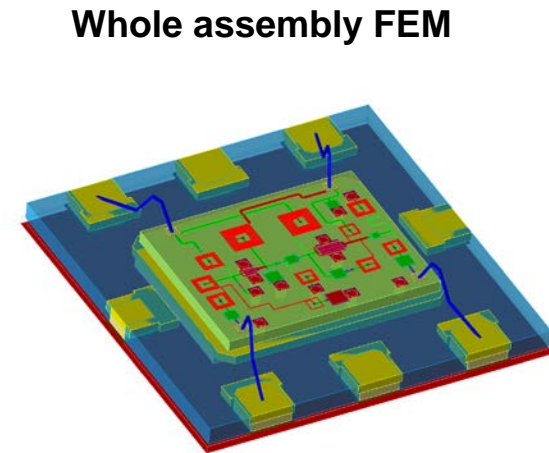
## Case 3



MMIC  
Momentum

+ Package  
FEM

## Case 4



Whole assembly FEM

**Case 1:** MMIC PA - Circuit models Simulation

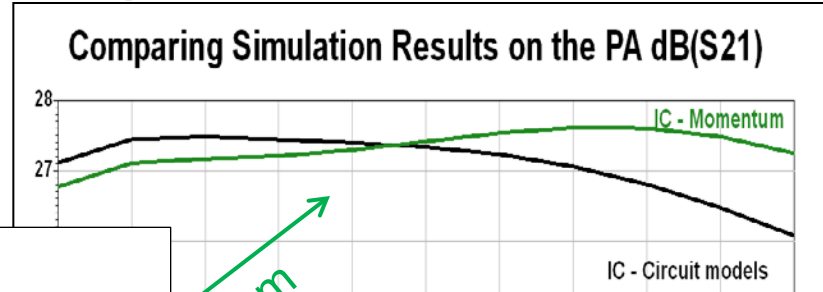
**Case 2:** MMIC PA – Momentum Simulation

**Case 3:** Combine MMIC Momentum & FEM of Package

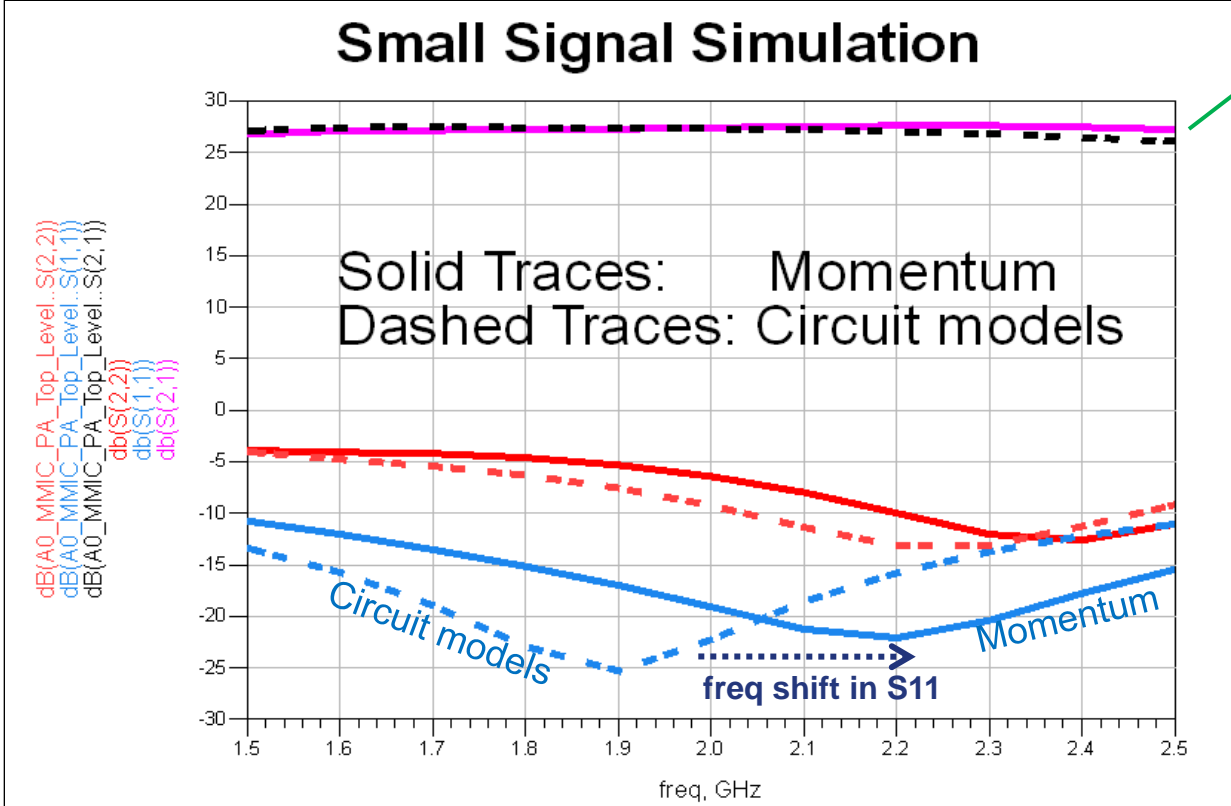
**Case 4:** FEM on the Whole Module

# Packaged MMIC PA Design Example

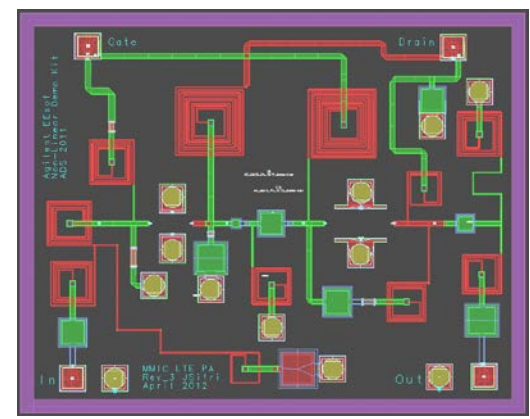
## Cases 1 & 2 on MMIC chip



### Small Signal Simulation



Zoom



Input Matching Network is shown to exhibit coupling effects (freq shift)

# Packaged MMIC PA - Results

Four different simulation results (case 1-4)

## MMIC

**Black:** Circuit Model

**Green:** Momentum

## MMIC + Package

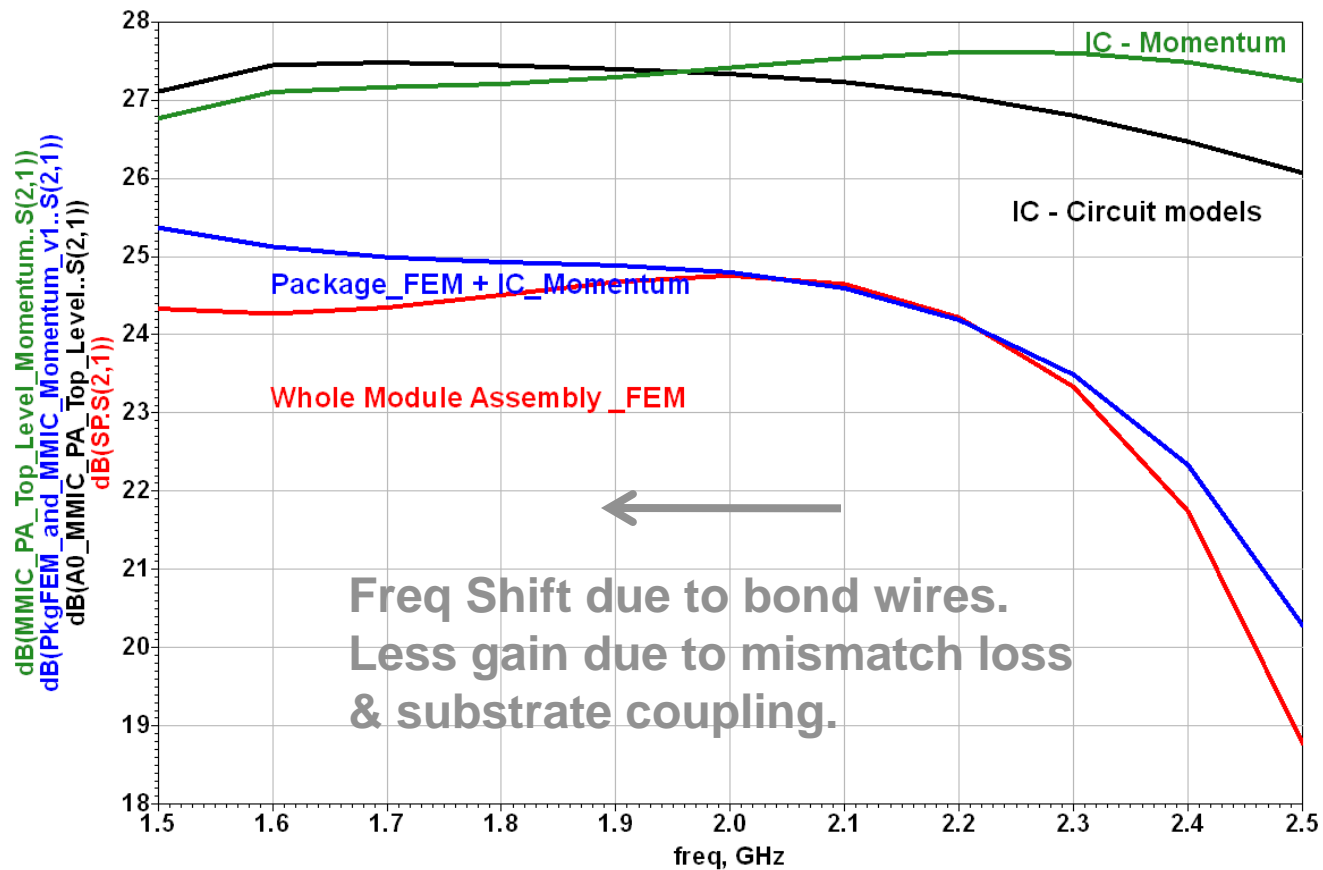
**Blue**

**IC\_Mom + Pkg\_FEM**

**Red**

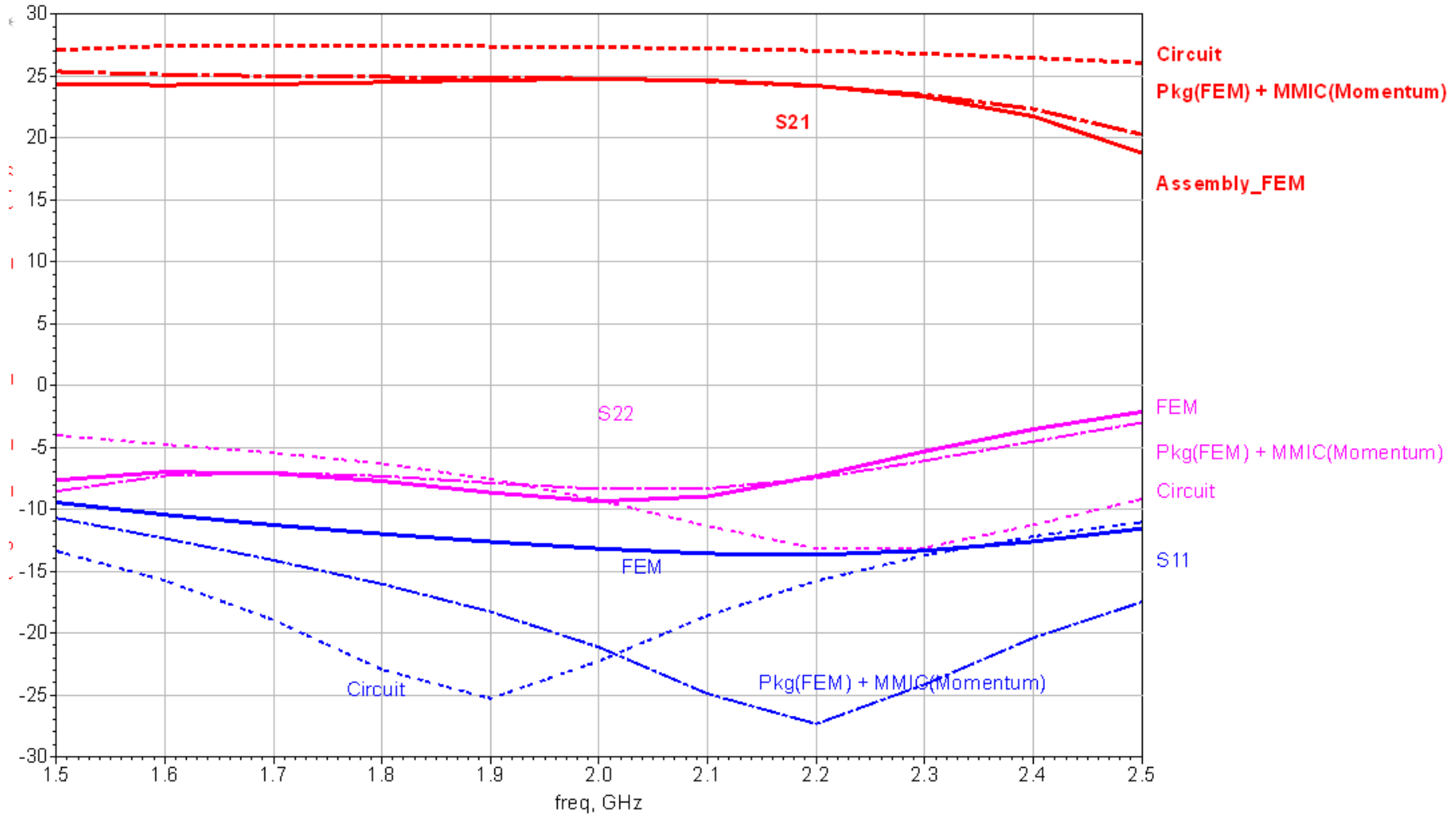
**Whole Module\_FEM**

### Comparing Simulation Results on the PA dB(S21)



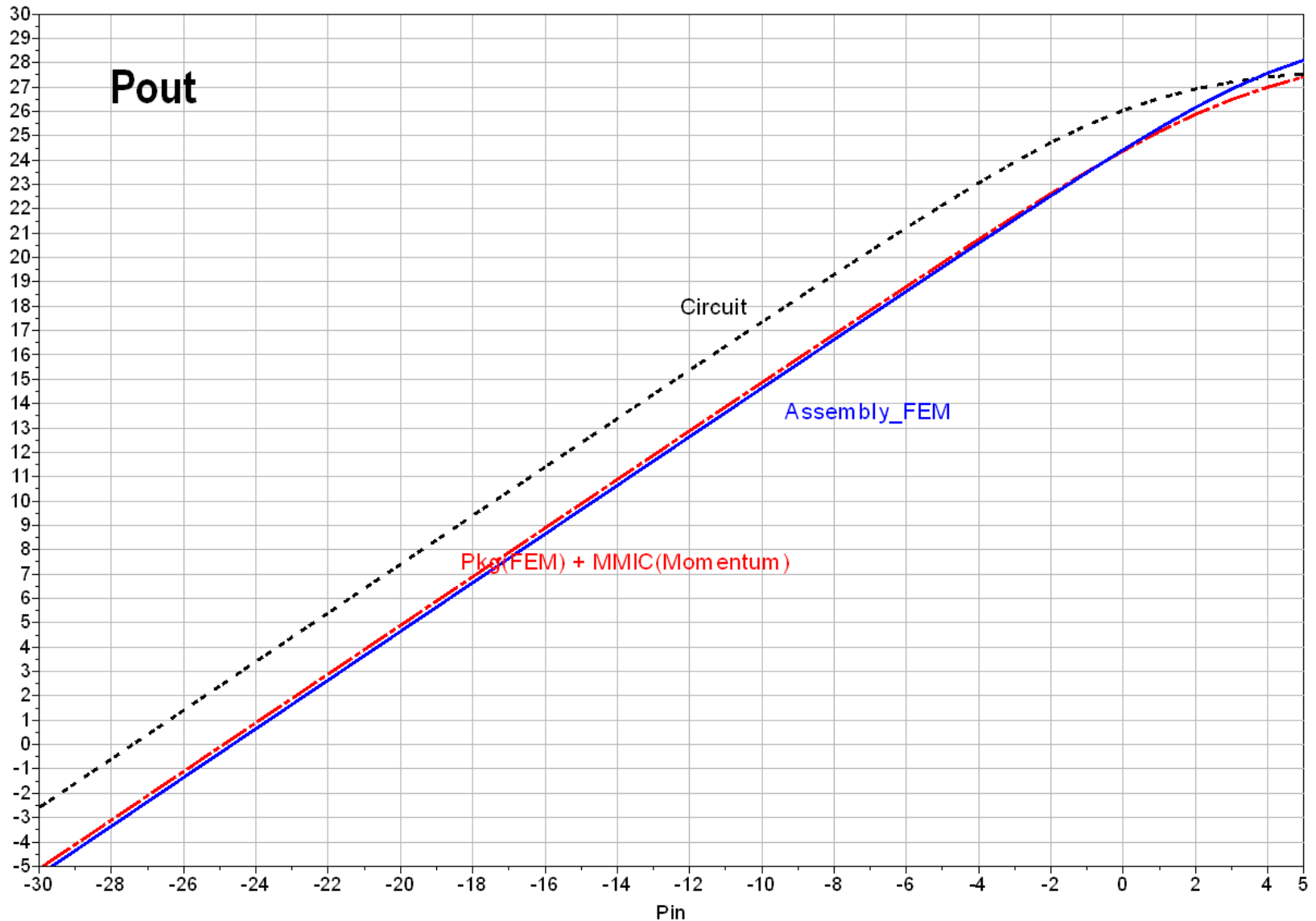
Cases: 1-4

### Compare Module FEM Results with (Pkg\_FEM + MMIC\_Momentum) and with Circuit simulation results



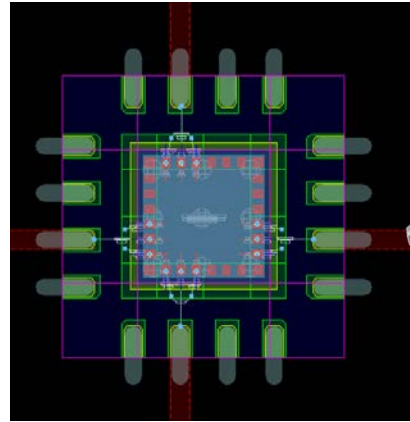
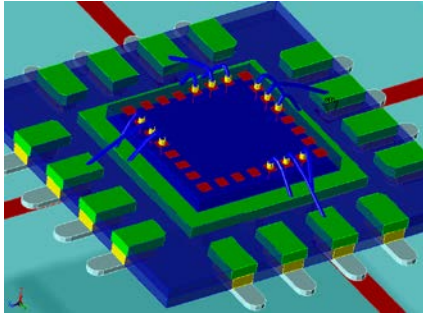


# Packaged MMIC PA Design Example Results

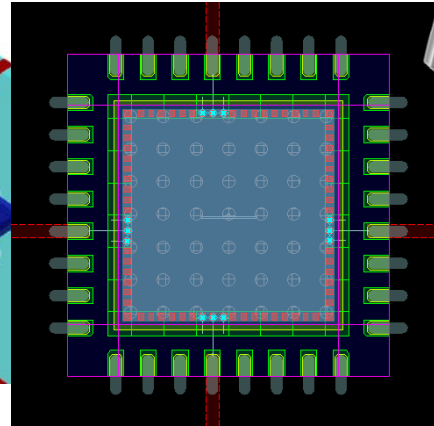
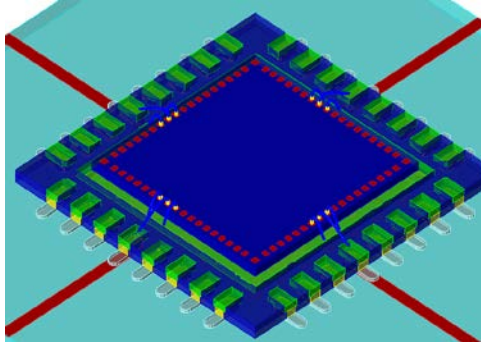
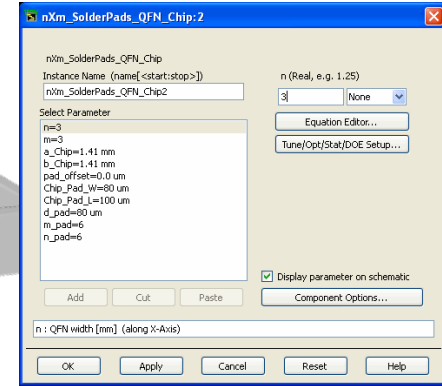


# QFN Designer in ADS

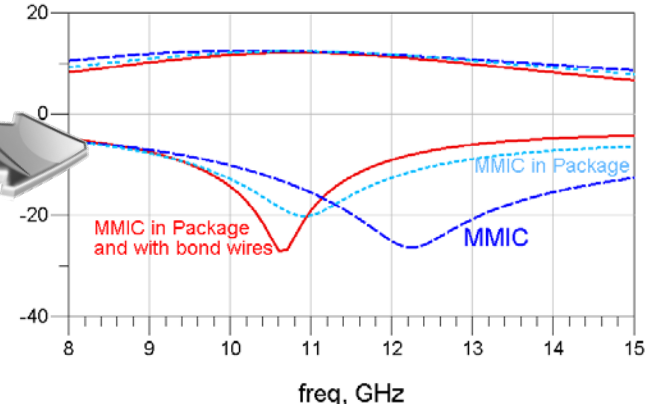
## Predict Packaged Performance in Minutes



### Configure QFN package



### Accurately predict real performance

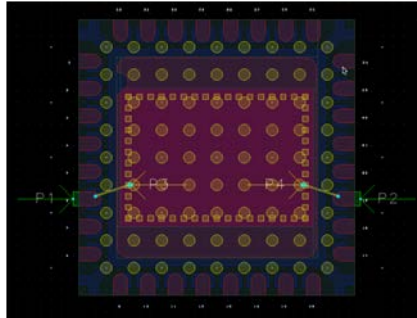
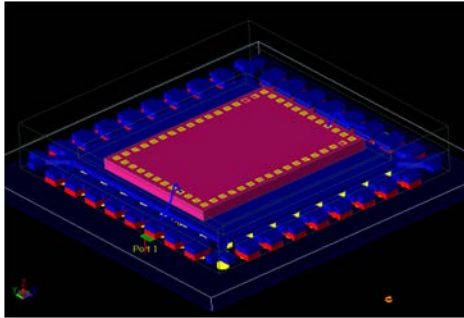
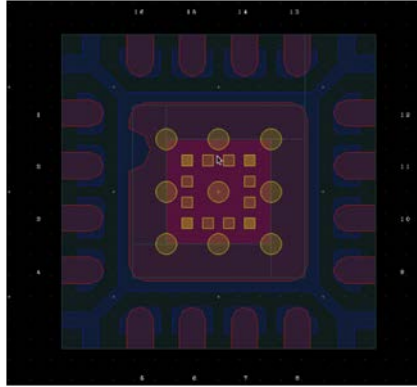
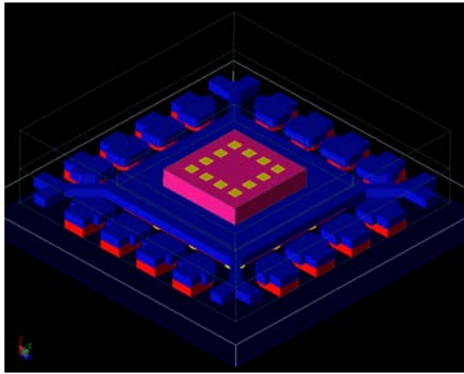


Quickly synthesize complex package, combine with IC & PCB data

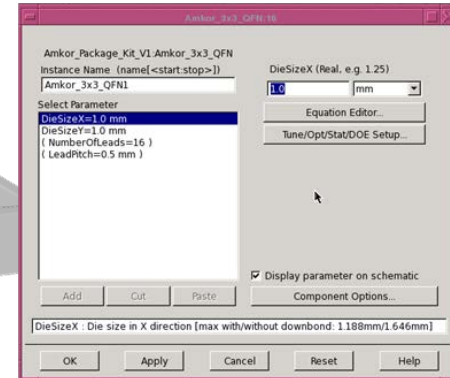
Performance w/ & w/o package

# Amkor Package Design Kit for ADS

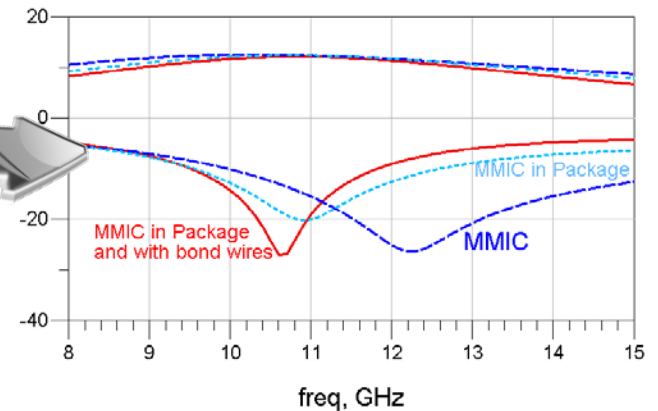
## Predict Packaged Performance in Minutes



### Configure QFN package



### Accurately predict real performance



Performance w/ & w/o package

Quickly synthesize complex package,  
combine with IC & PCB data

# IC, Laminate, Package Multi Technology PA Module Design

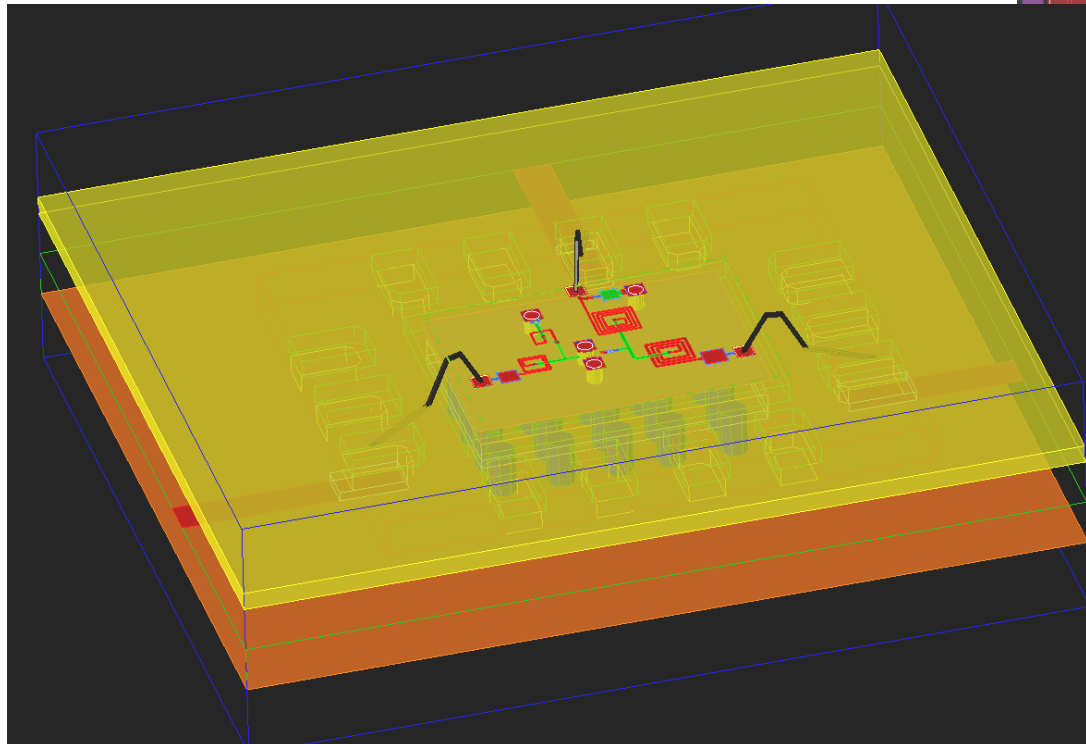
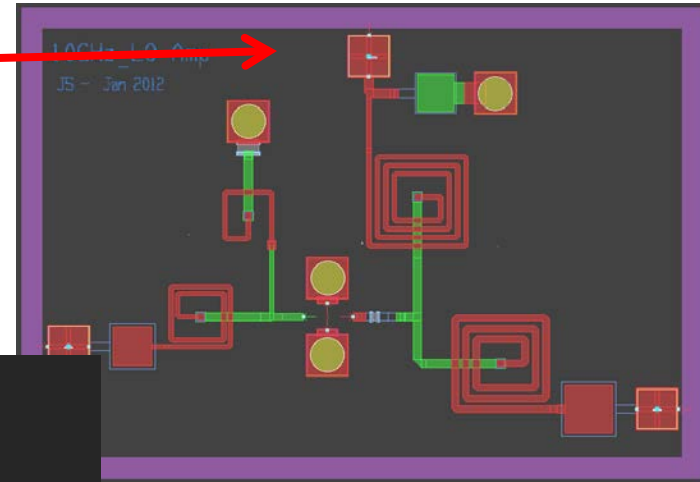
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# Bounding the IC within the Package/ Laminate Assembly

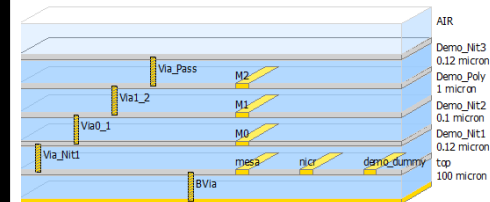
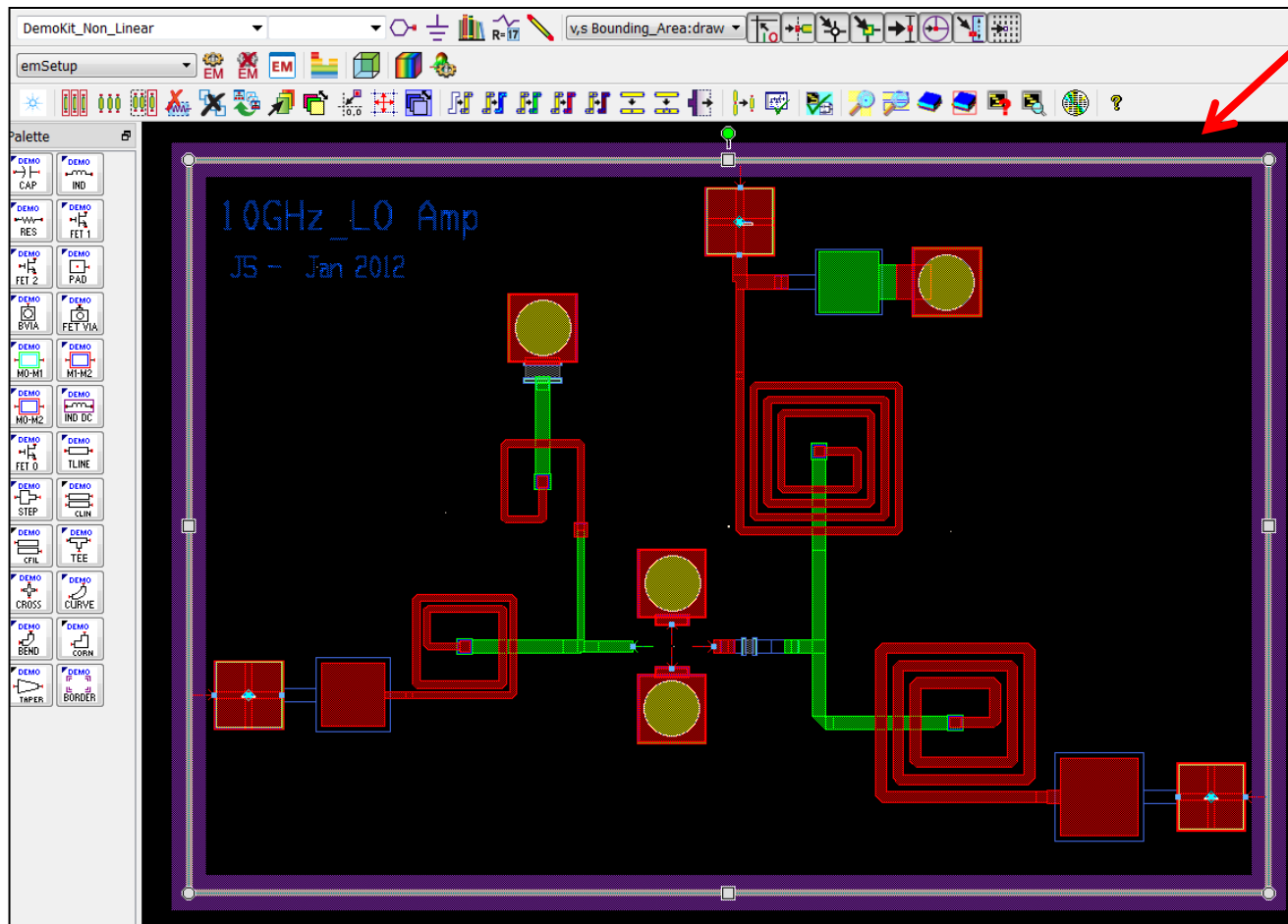
# A Word on Bounding the IC using "Boundary Area Layer"

- Layout has no Bounding Area
- 3D view shows the MMIC substrate extending out through the bond wires  
(Results in inaccurate FEM simulation results)



# Multi Technology Module Setup with Bounding the IC

- Bounding Area layer box has been added in the Layout as shown.
- 3D view (next page) shows the bounding of the MMIC for FEM simulation



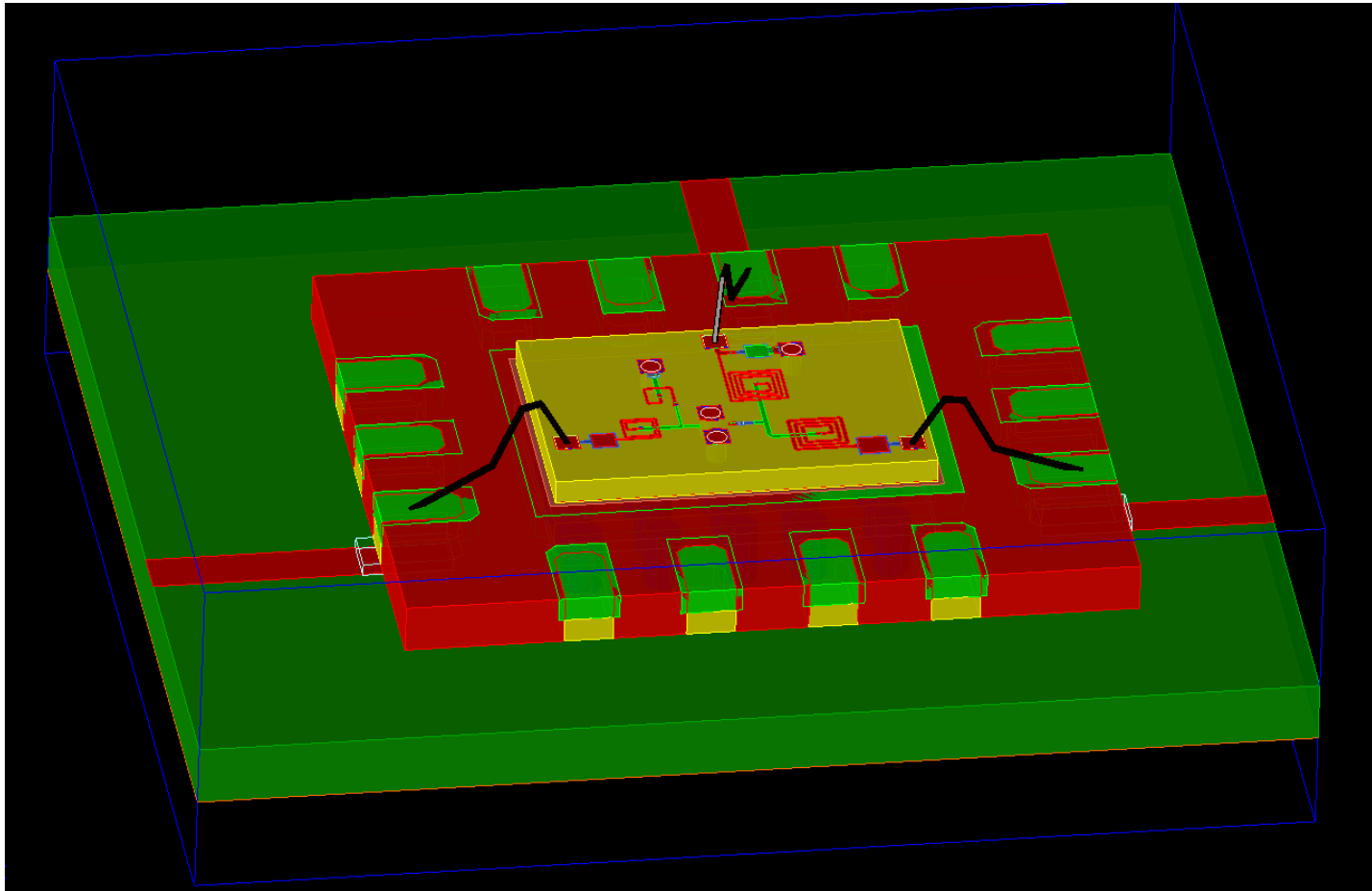
Entire Substrate

Bounding area layer: Bounding\_Area (39)

Select a substrate item to see more information about that item.

# Multi Technology Module Setup with Bounded IC

- 3D view shows how the use of “Bounding Area Layer” (last page) has resulted in bounding IC substrate (cookie cut) for FEM simulation

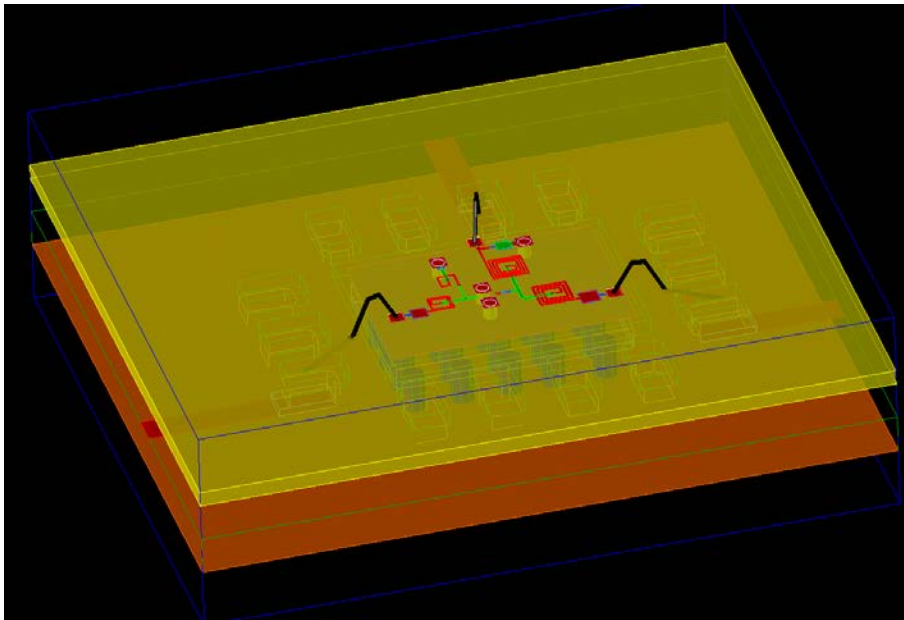




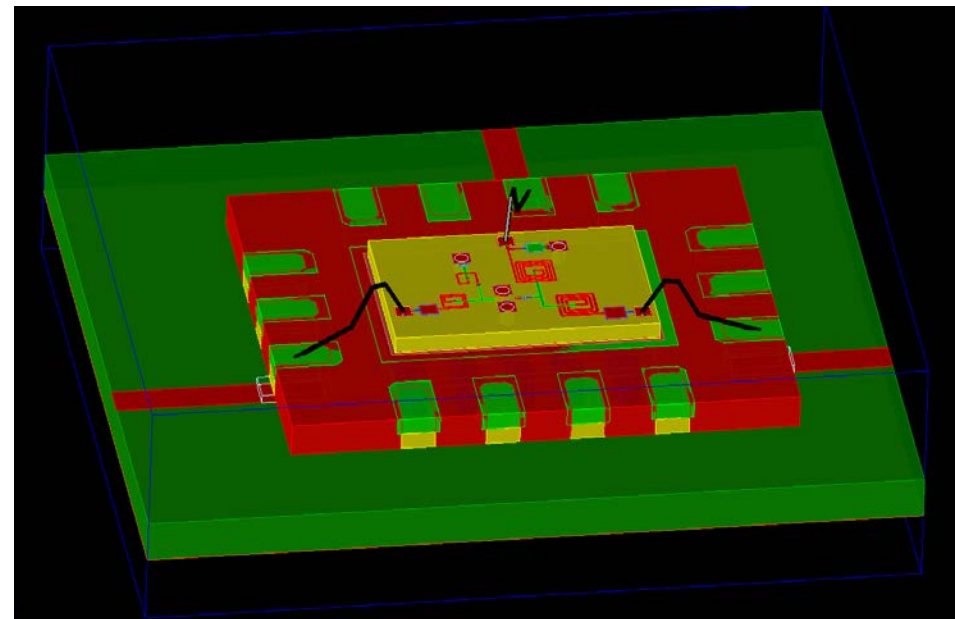
# Multi Technology Module Setup

## With and without Bounding area layer

*Before adding Bounding Layer to the IC*



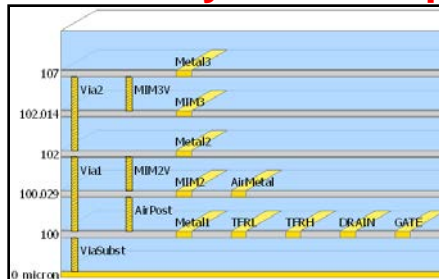
*After adding Bounding Layer to the IC*



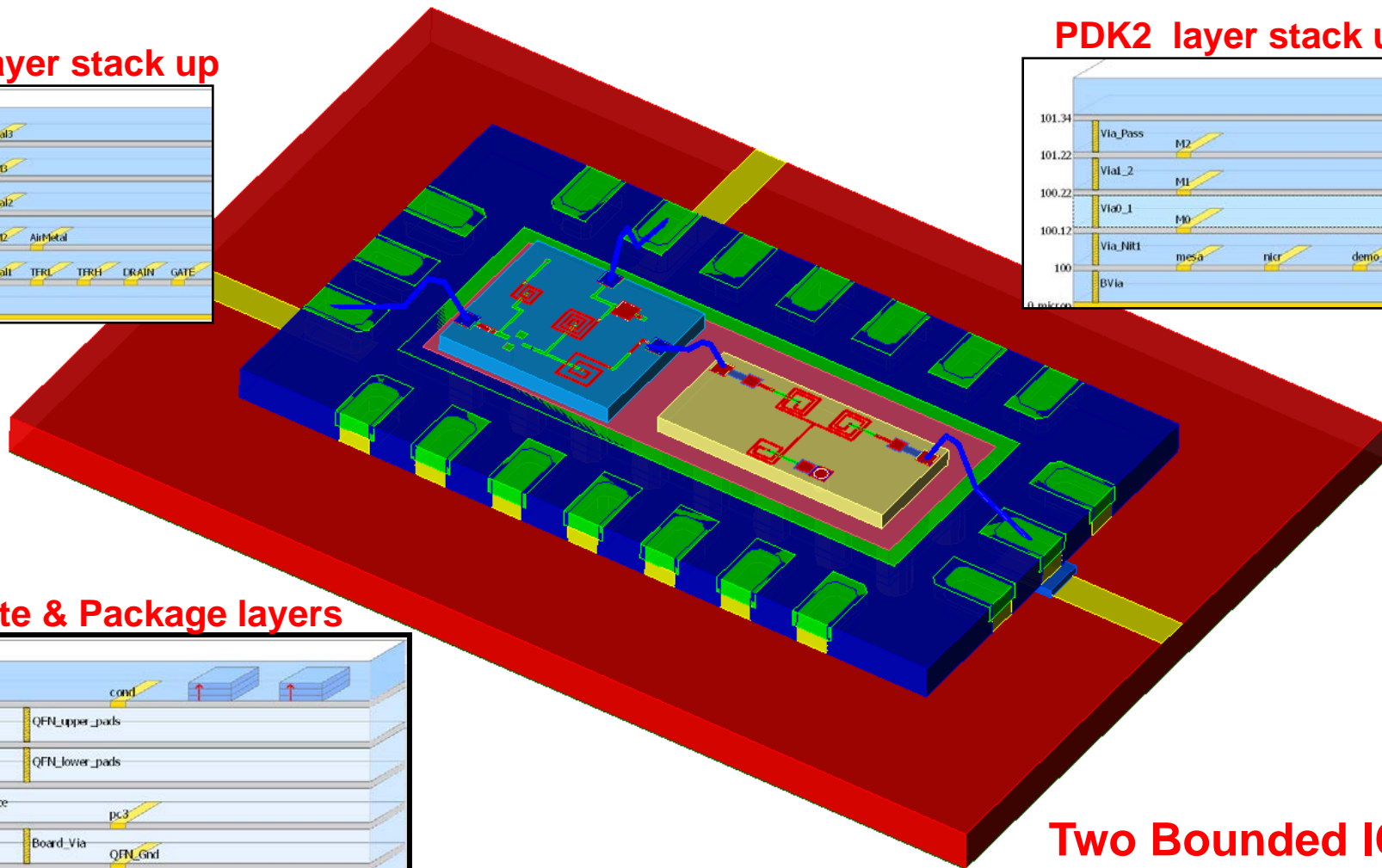
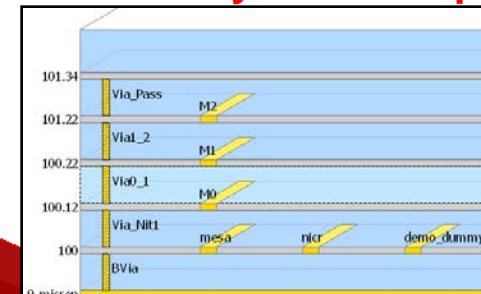
# Multi Technology FEM Simulation Set up

## Ku band LNA (PDK1) followed by Ku band Filter (PDK2)

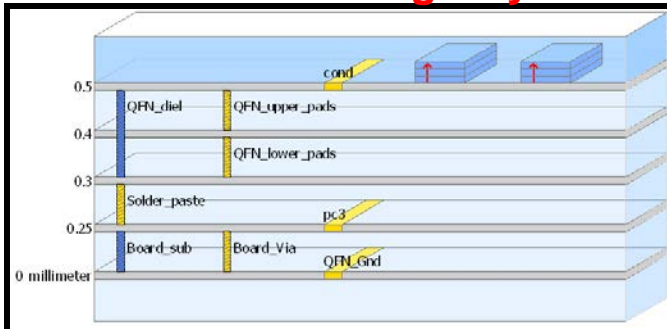
**PDK1 layer stack up**



**PDK2 layer stack up**



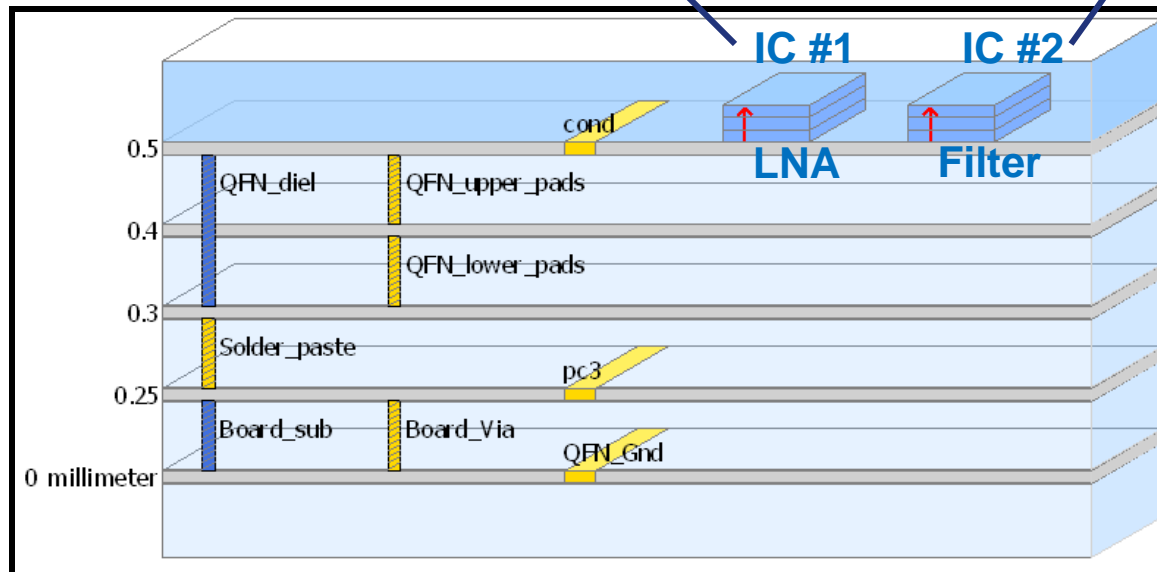
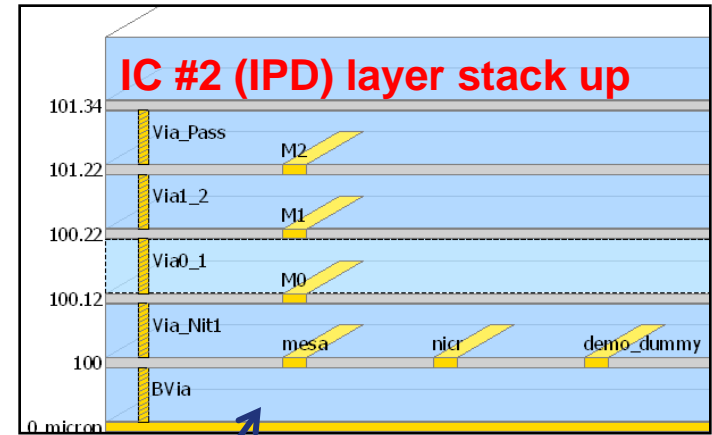
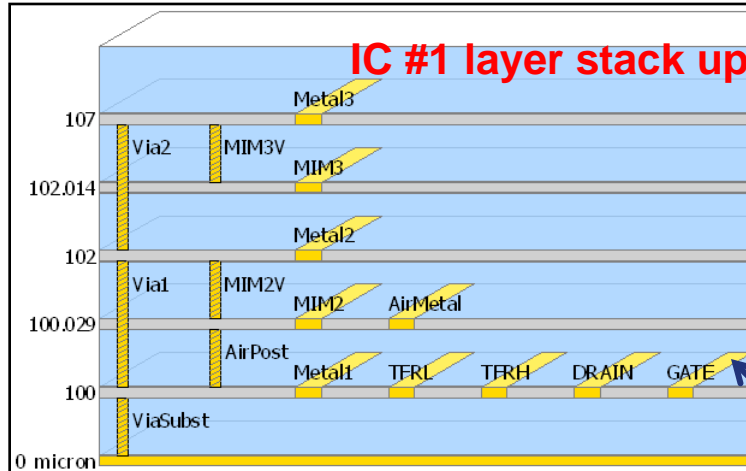
**Laminate & Package layers**



**Two Bounded IC's**

# Multi Technology Module Layers Stack up

## Nested Technology substrates



Mounted ICs

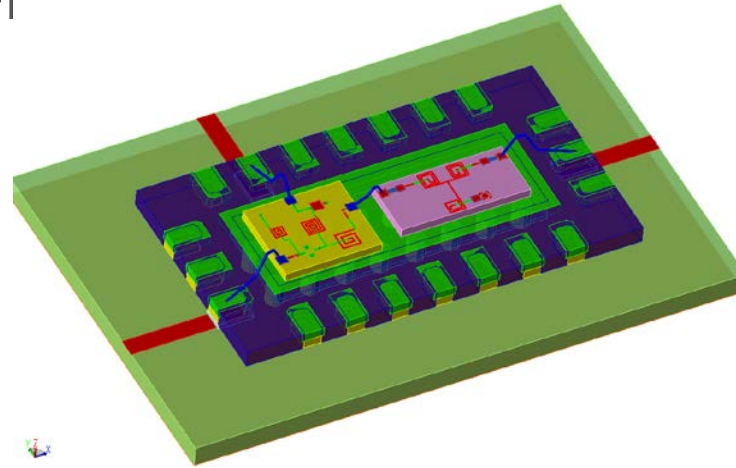
QFN Package layers

Laminate layers

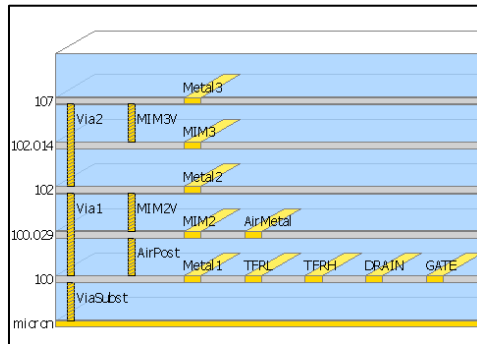
# Multi Technology 3D FEM Simulation in ADS 2012

## Substrate stackup

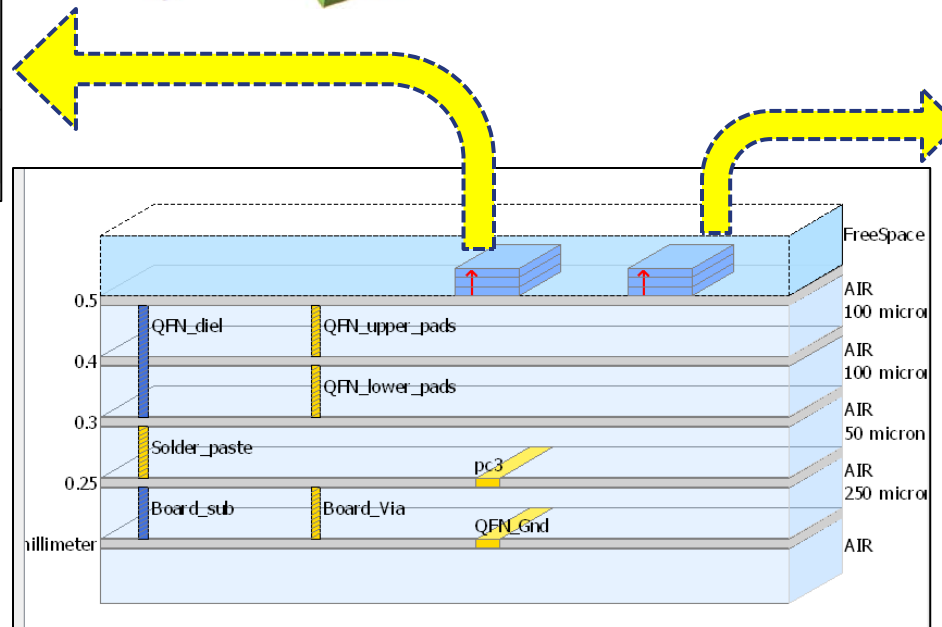
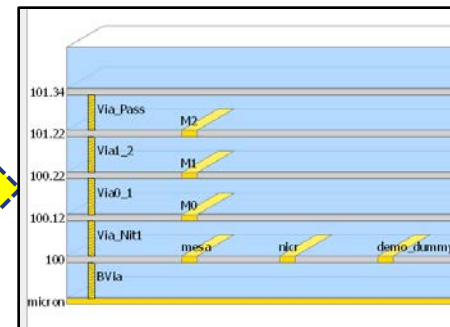
**Demo**



IC#1



IC#2



Package

Laminate

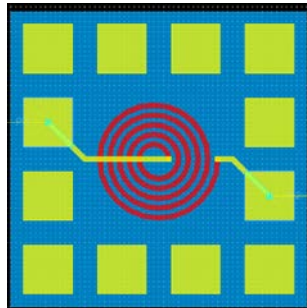
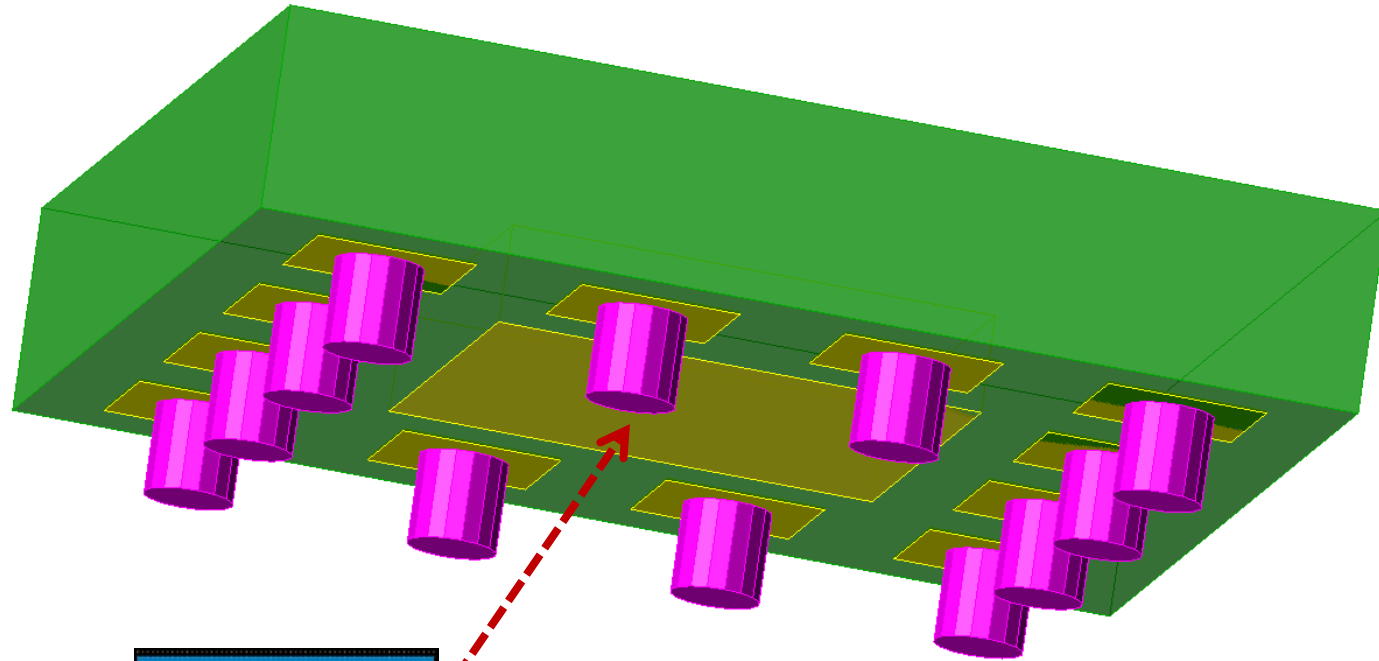
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# Flip Chip / Flip Package onto Board

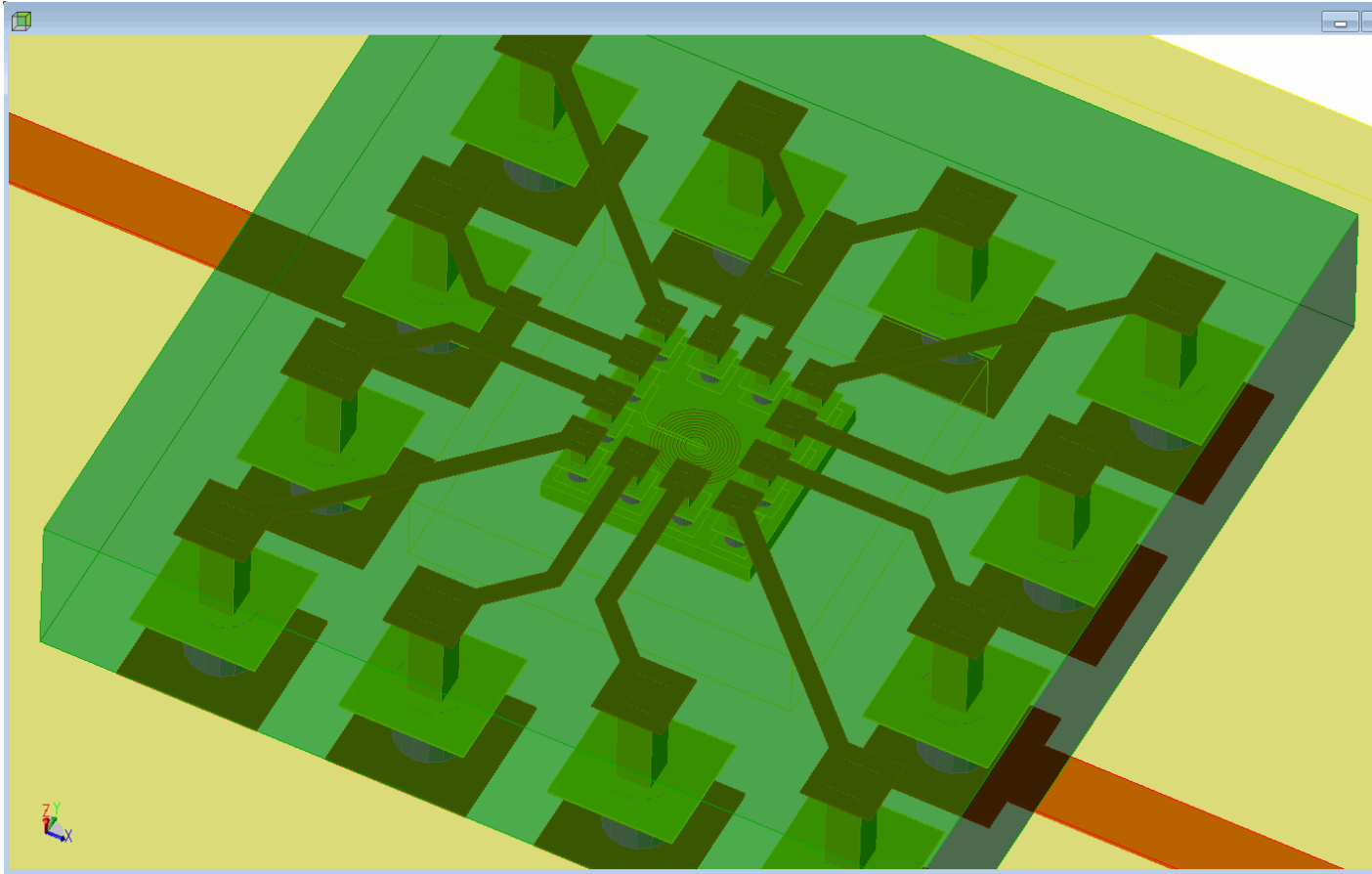
Flipped Package ready to mount onto a board



Flipped IC chip mounted inside package cavity

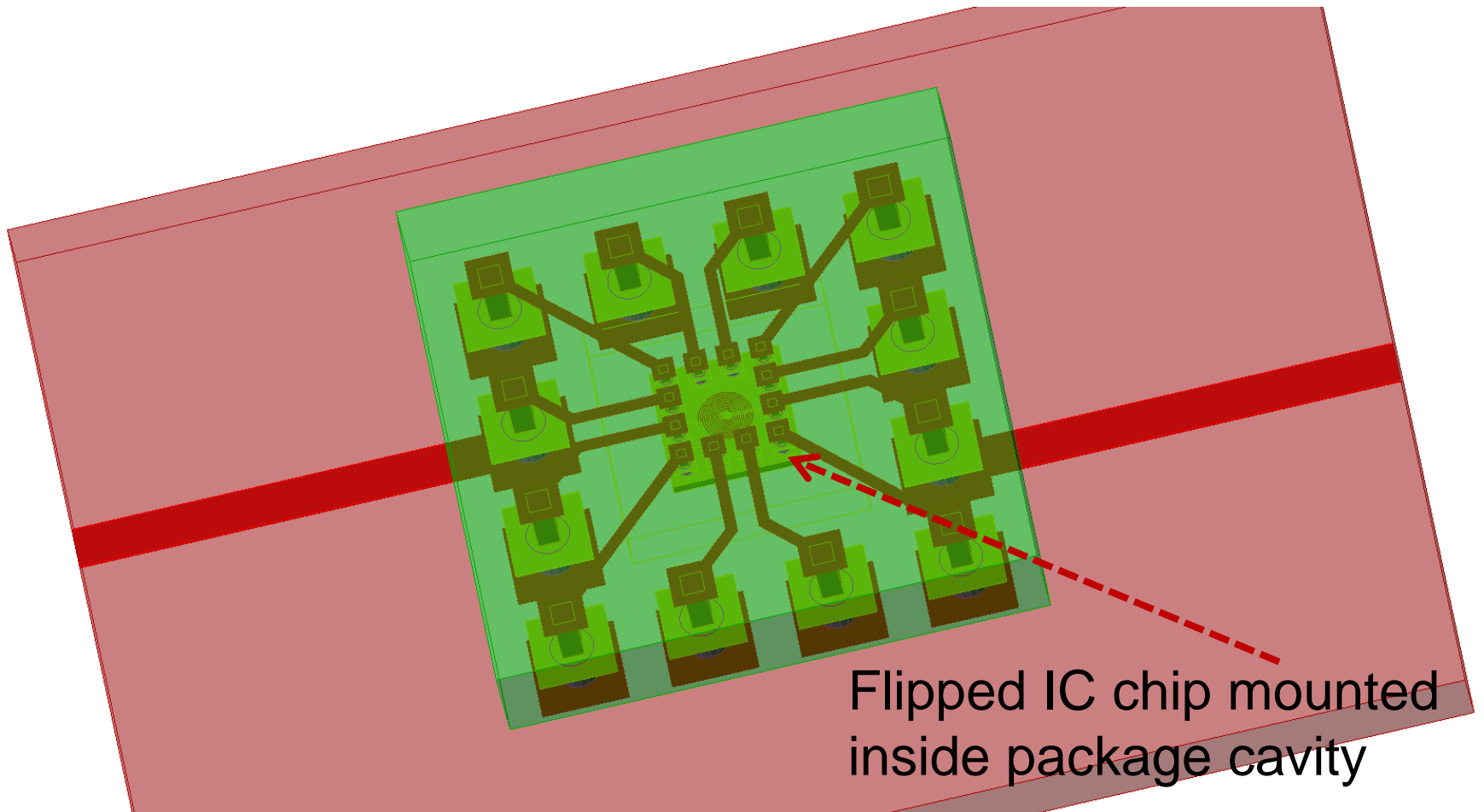
# Flip Chip / Flip Package onto Board

Flipped Package mounted onto a board



# Flip Chip / Flip Package onto Board

Flipped Package mounted onto a board

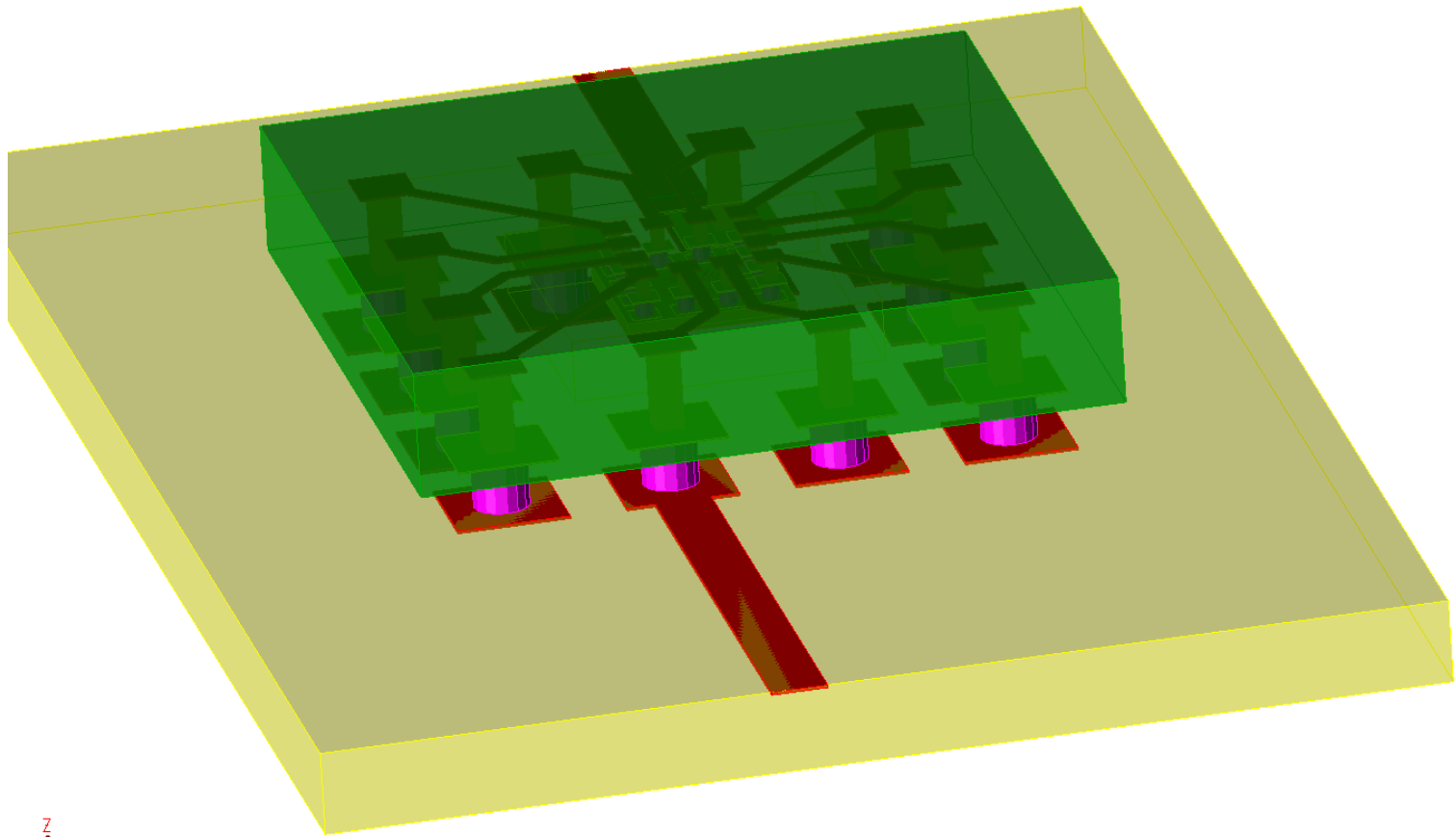


Flipped IC chip mounted  
inside package cavity

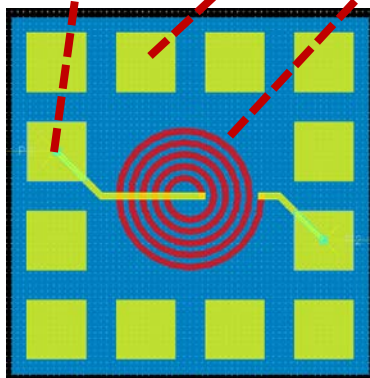
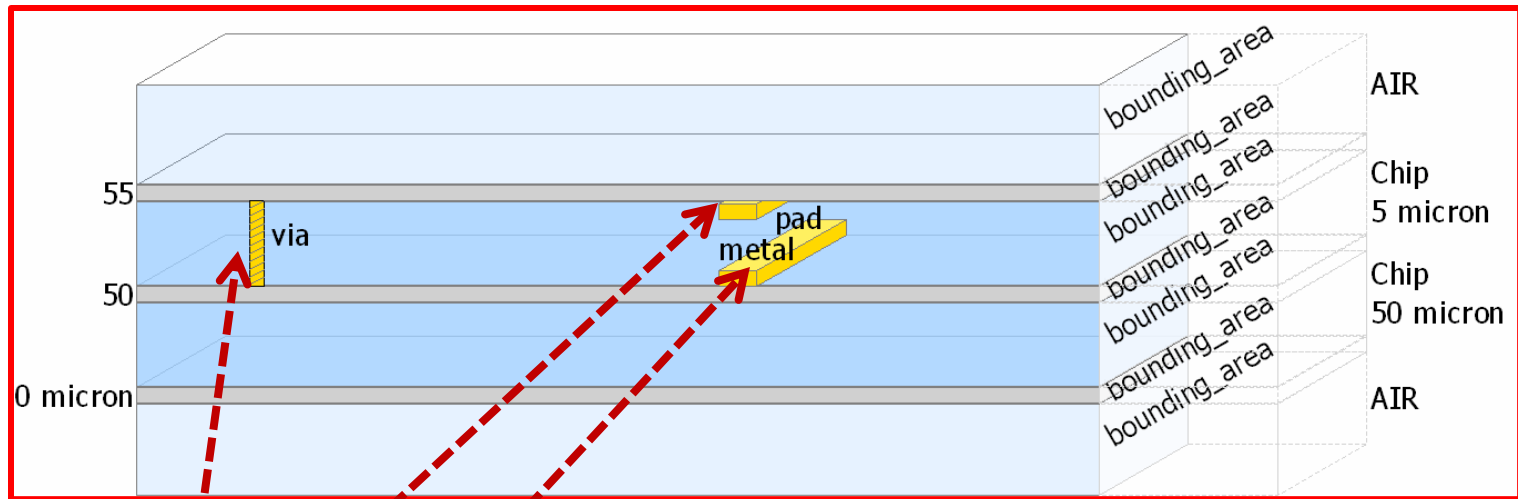


# Flip Chip / Flip Package onto Board

Flipped Package mounted onto a board – side view



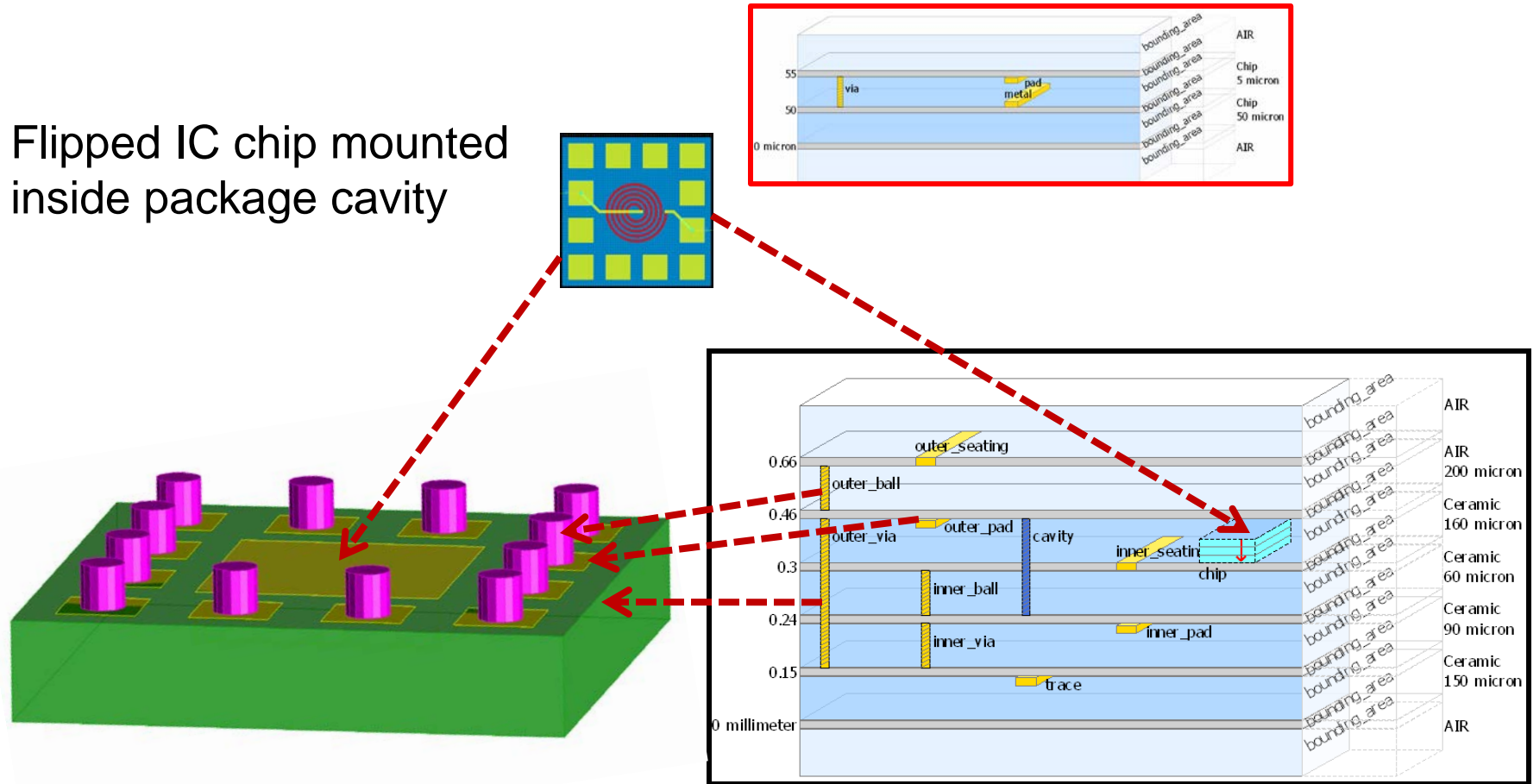
# Flip Chip / Flip Package onto Board



Flipped IC chip to be mounted inside package cavity

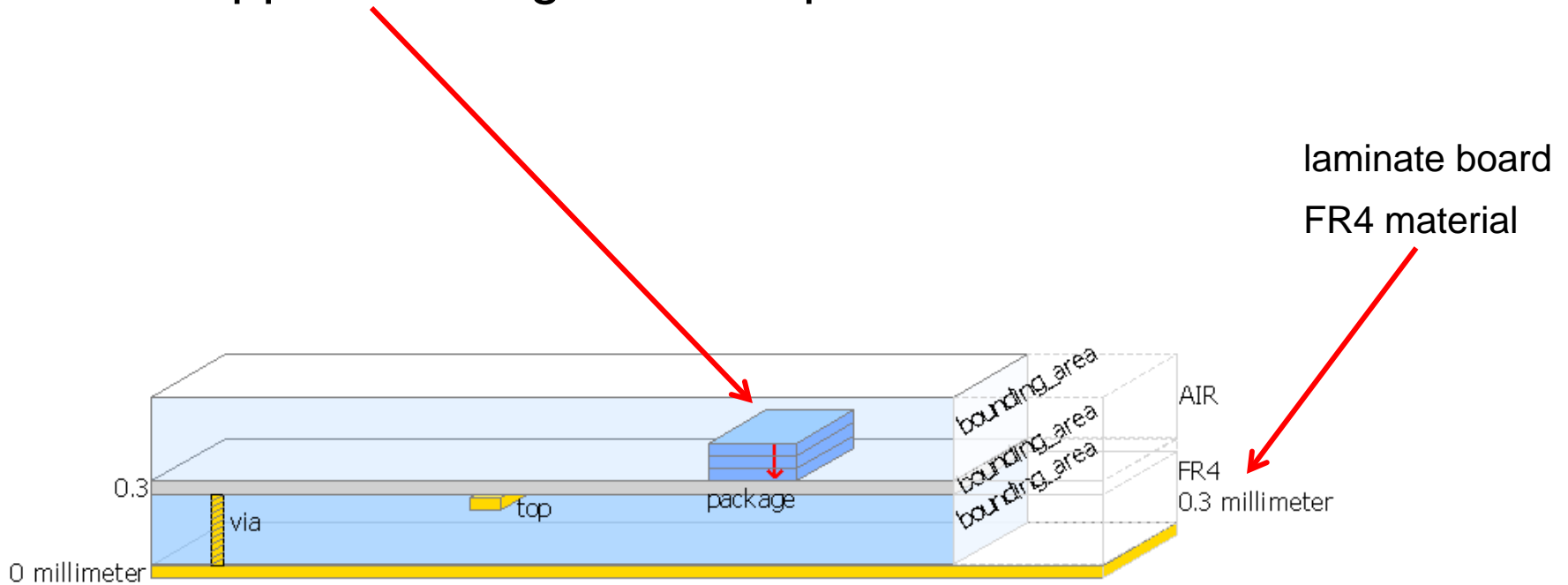
# Flip Chip / Flip Package onto Board

Flipped IC chip mounted inside package cavity



# Flip Chip / Flip Package onto Board

## Flipped Package and Chip onto a laminate board



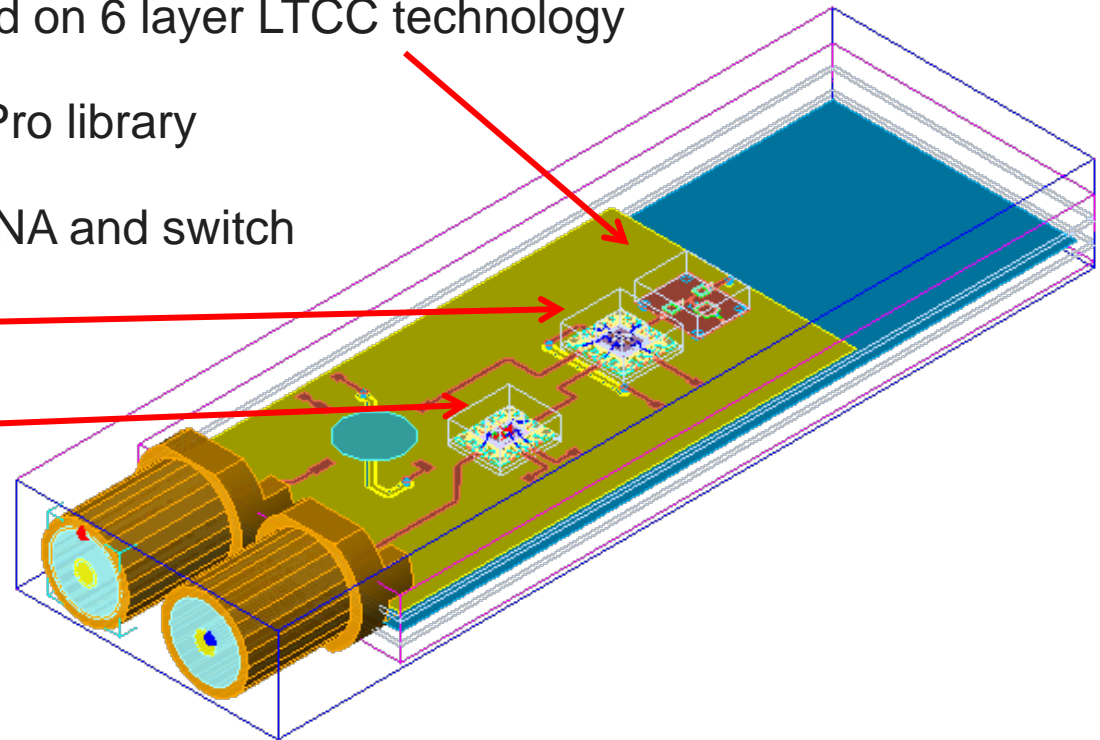
# IC, Laminate, Package Multi Technology PA Module Design

## Agenda

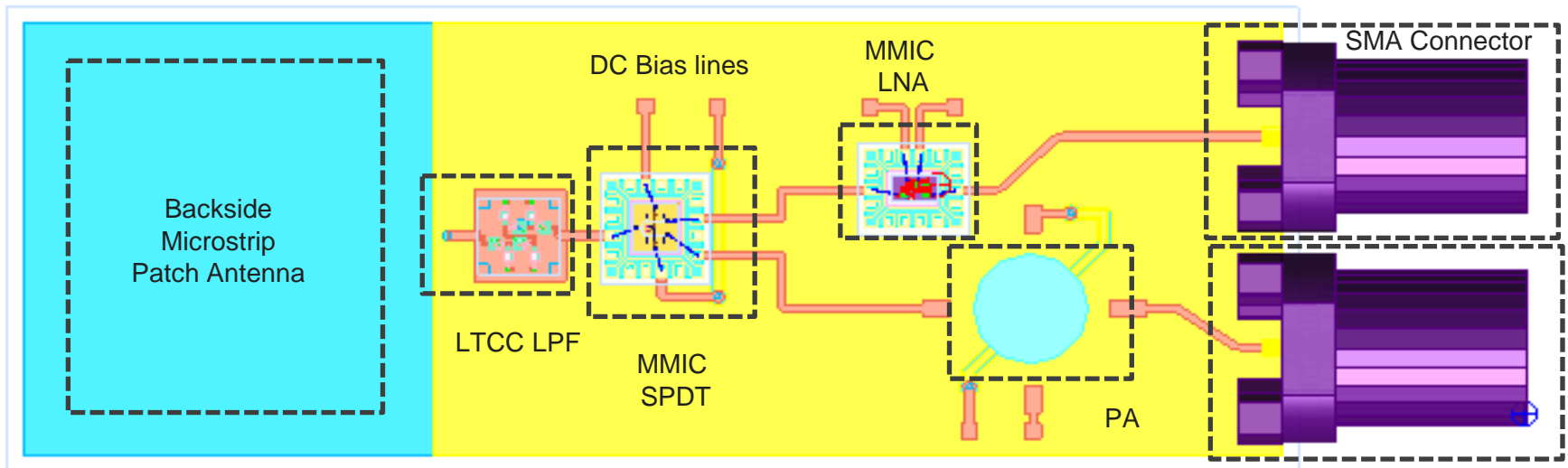
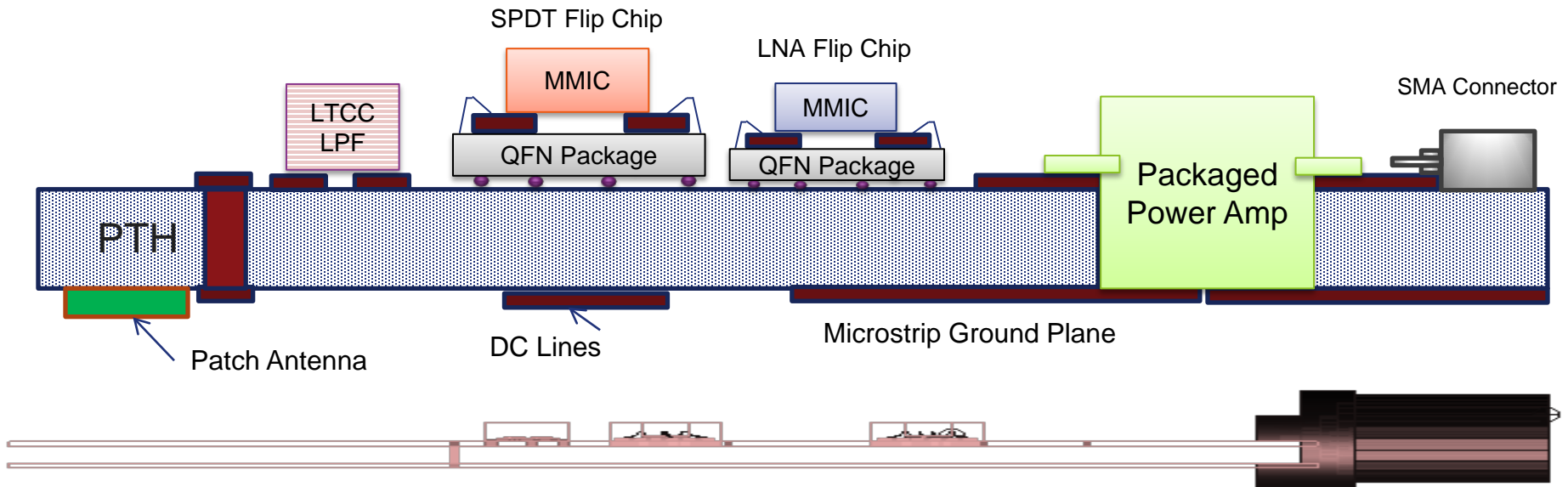
1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
  - Single chip module
  - Multi chip module
  - Flip chip /solder bumps module
  - Transceiver module
  - Electro thermal simulation
5. Conclusion

# Example: Transceiver using Multi Technology

- Transceiver consists of mainly seven major technologies:
  1. Antenna: single layer C-band microstrip patch antenna
  2. Power Amplifier - X-parameter file of MMIC power amplifier
  3. LTCC BPF : 3 pole filter based on 6 layer LTCC technology
  4. 3D SMA Connector from EMPro library
  5. Standard QFN Package for LNA and switch
  6. MMIC SPDT switch
  7. MMIC LNA

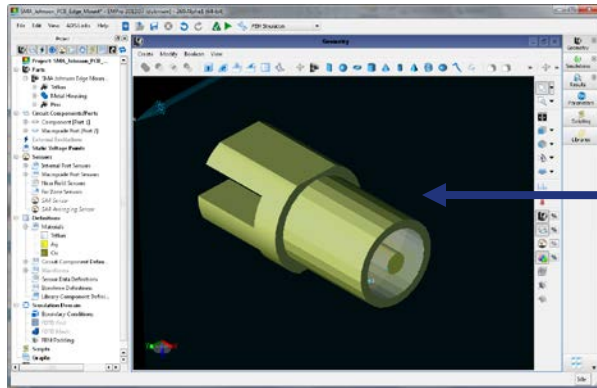


# Transceiver Cross Section View

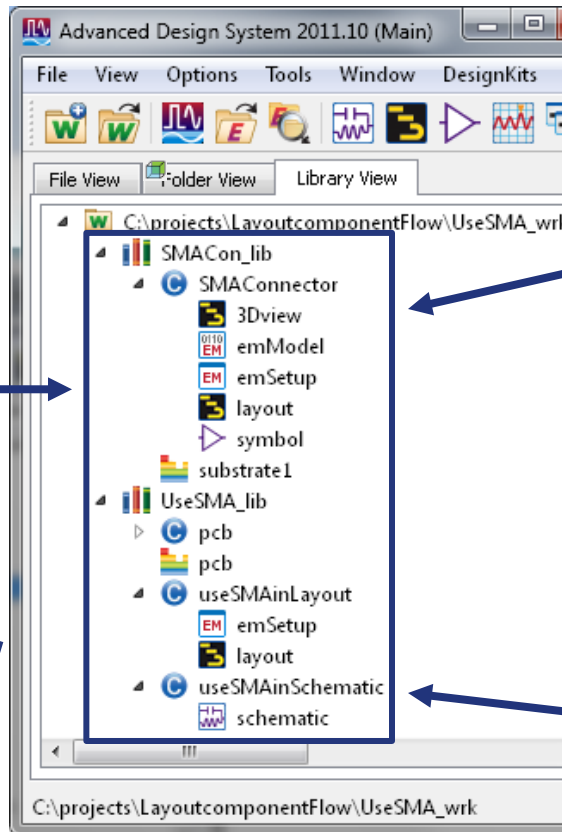


# EMPro 2012 3D EM Components Improved ADS Integration

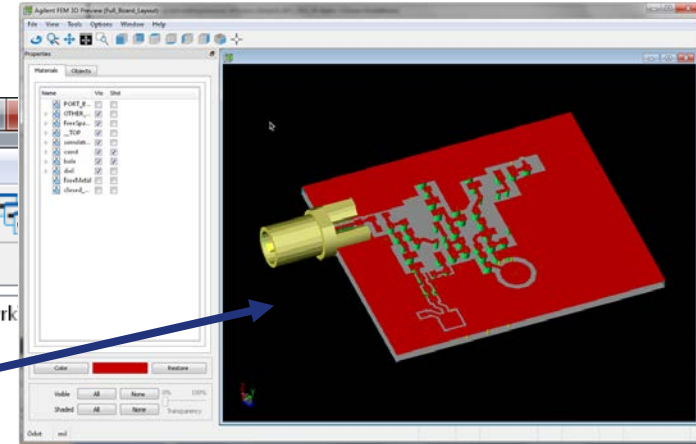
## EMPro 3D Design



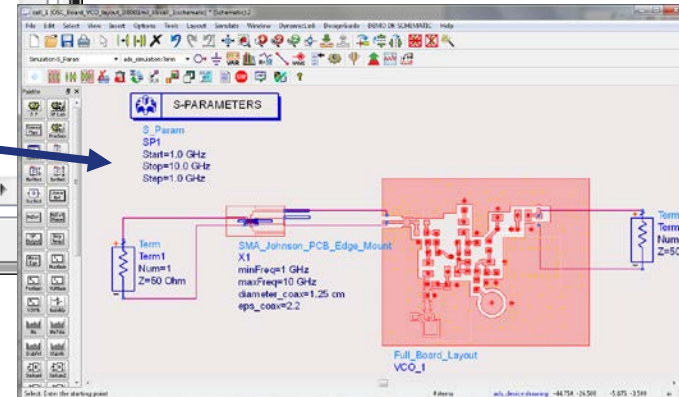
## ADS



## ADS Layout (3D View)



## ADS Schematic

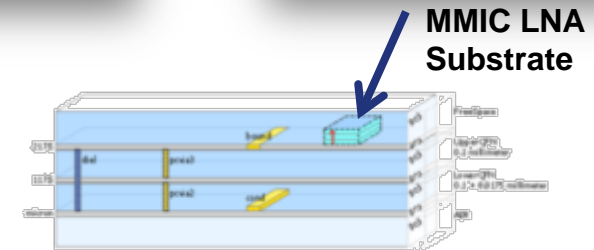
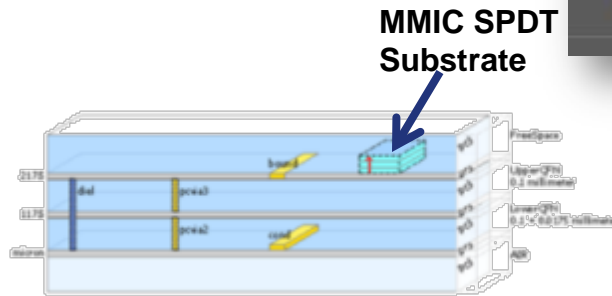
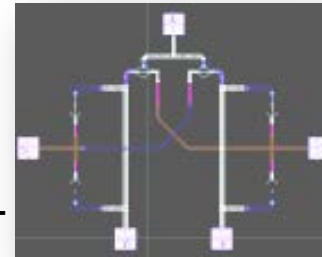
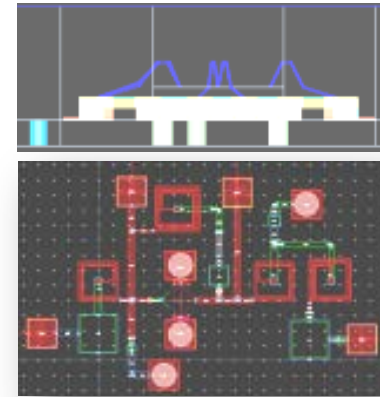
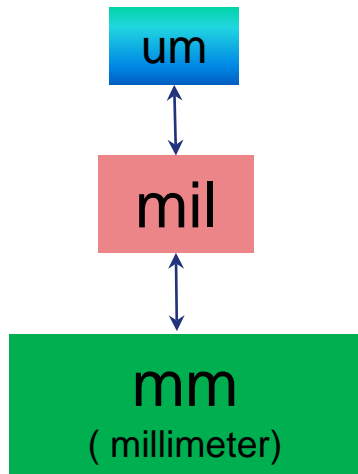


**Common  
Database**



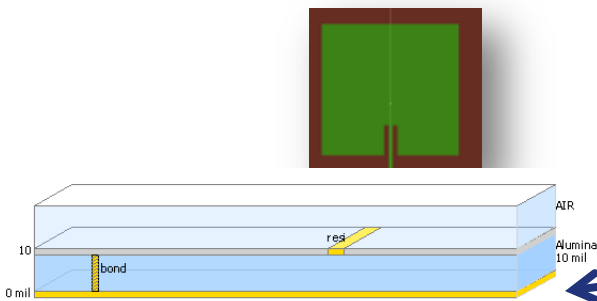
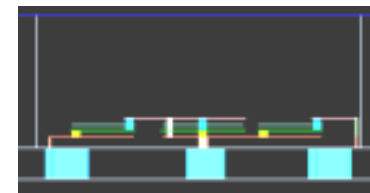
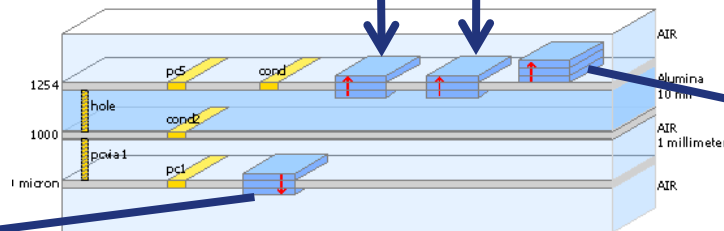
# Transceiver Parts and Technologies

- Total 12 equivalent layer board
- 7 different technologies
- 2 stack up + 4 side by side technologies
- EMPro design as lib component
- 3 different layout units



**SPDT + Package Substrate**

**LNA + Package Substrate**



**LTCC LPF**



# IC, Laminate, Package Multi Technology PA Module Design

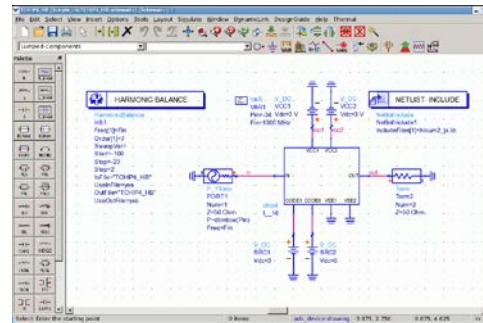
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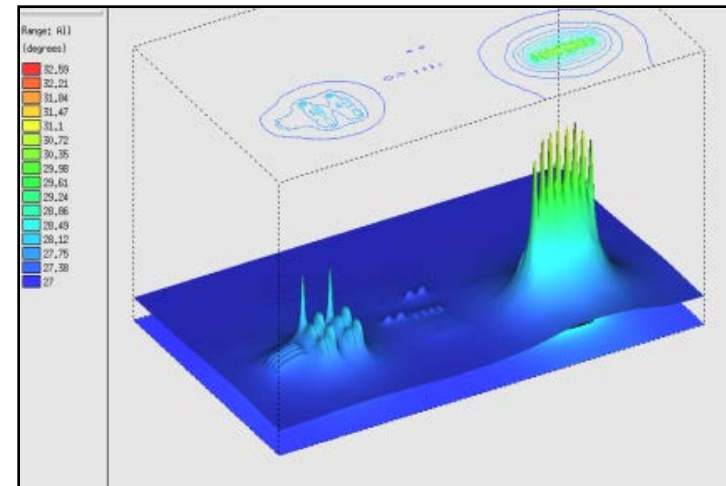
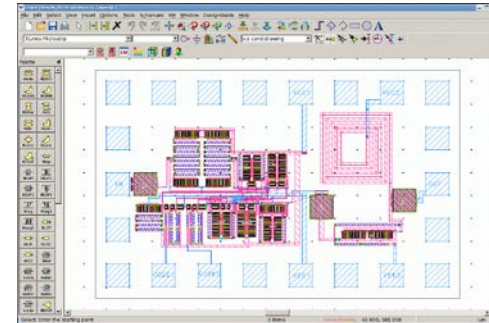
# New Electrothermal Solution in ADS2012

- Improves high power MMIC / RFIC designs
- Delivers 'thermally aware' circuit simulation results
- Includes effects of package and PCB
- Easy to set up and use from within ADS
- Works with all simulation types: DC, AC, SP, HB, Transient, Envelope

**ADS Schematic**

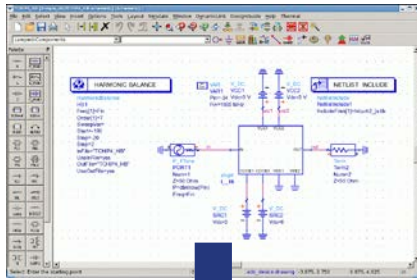


**ADS Layout**

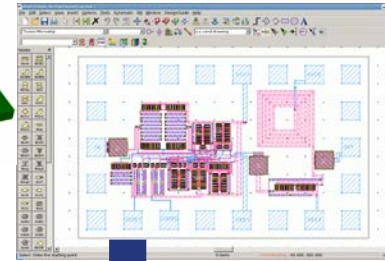
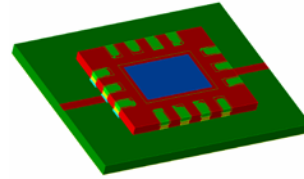


**Integrated Thermal Solver**

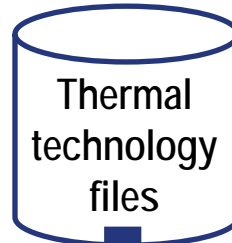
# New Electrothermal Solution in ADS2012



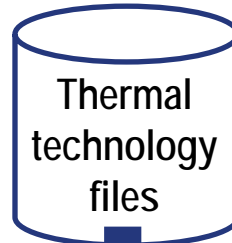
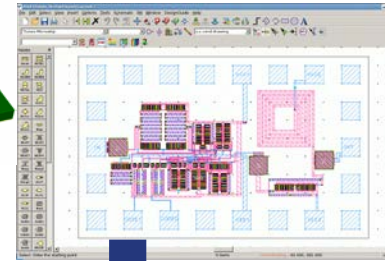
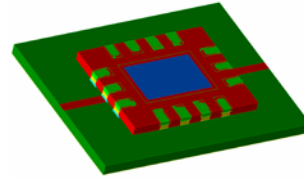
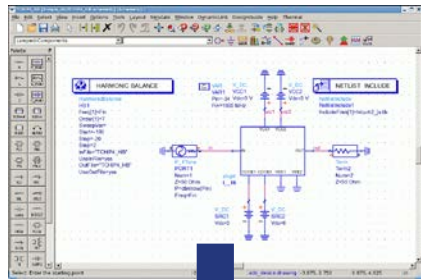
**Circuit Simulator**



**Thermal Simulator**



# New Electrothermal Solution in ADS2012

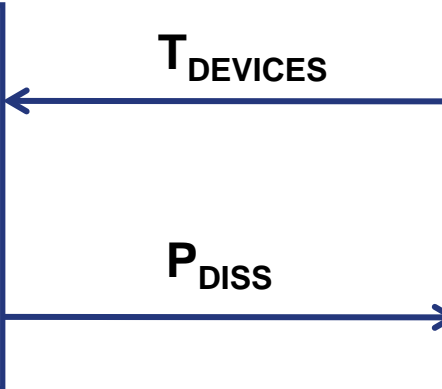


**Circuit Simulator**

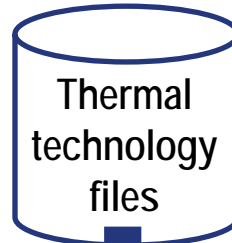
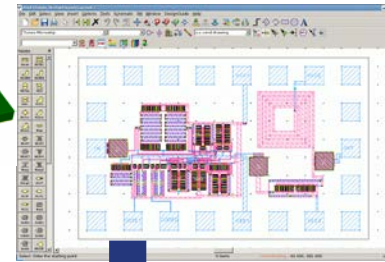
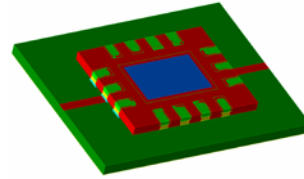
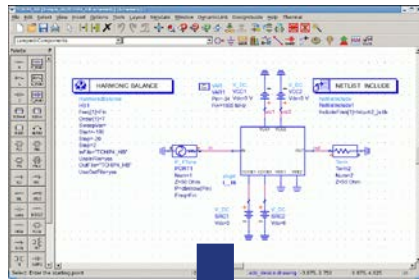
simulate to convergence  
write power dissipation

**Thermal Simulator**

read power dissipation  
create heat sources  
solve thermal equation  
write temperatures

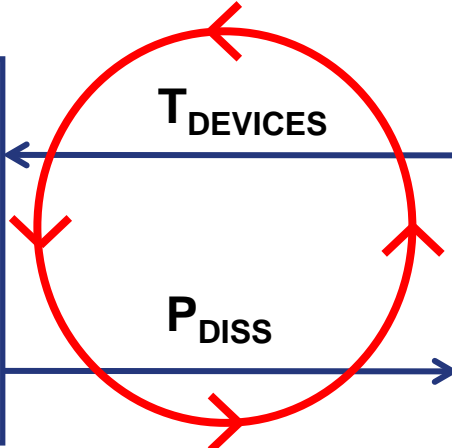


# New Electrothermal Solution in ADS2012



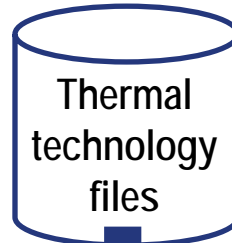
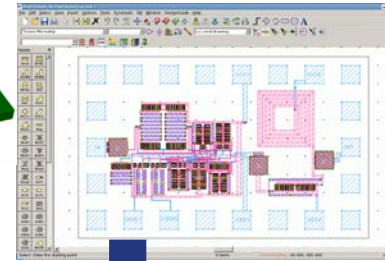
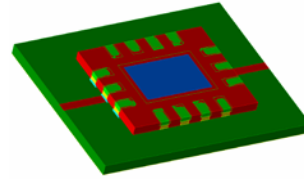
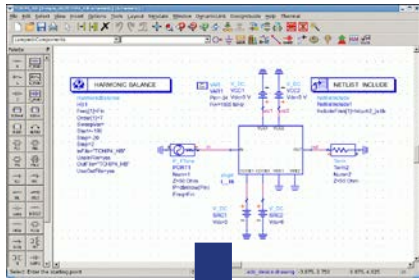
**Circuit Simulator**  
read temperatures  
use previous solution  
simulate to convergence  
write power dissipation

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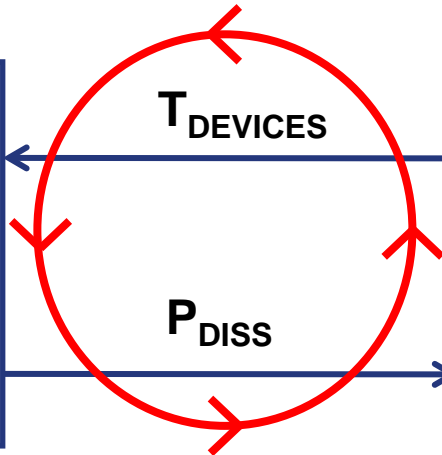
*Iteration loop is done automatically until powers and temperatures are self-consistent*

# New Electrothermal Solution in ADS2012



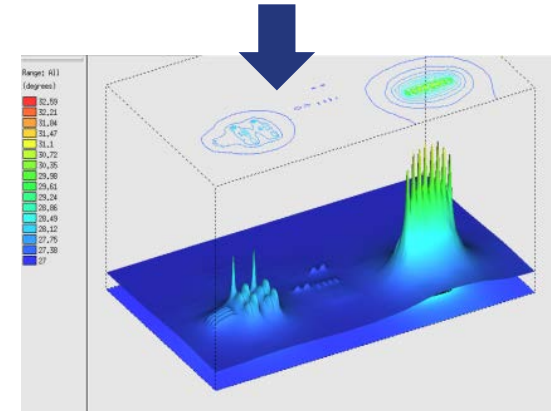
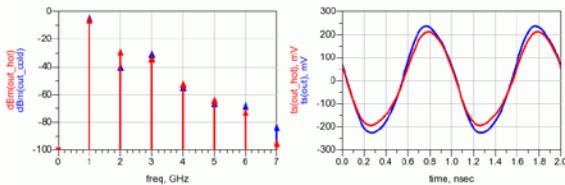
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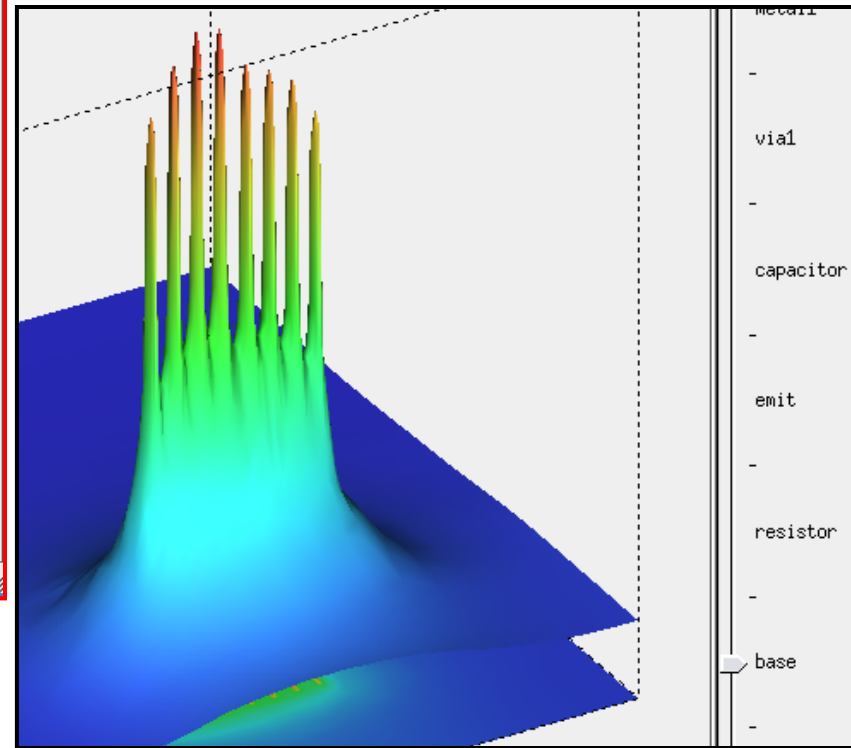
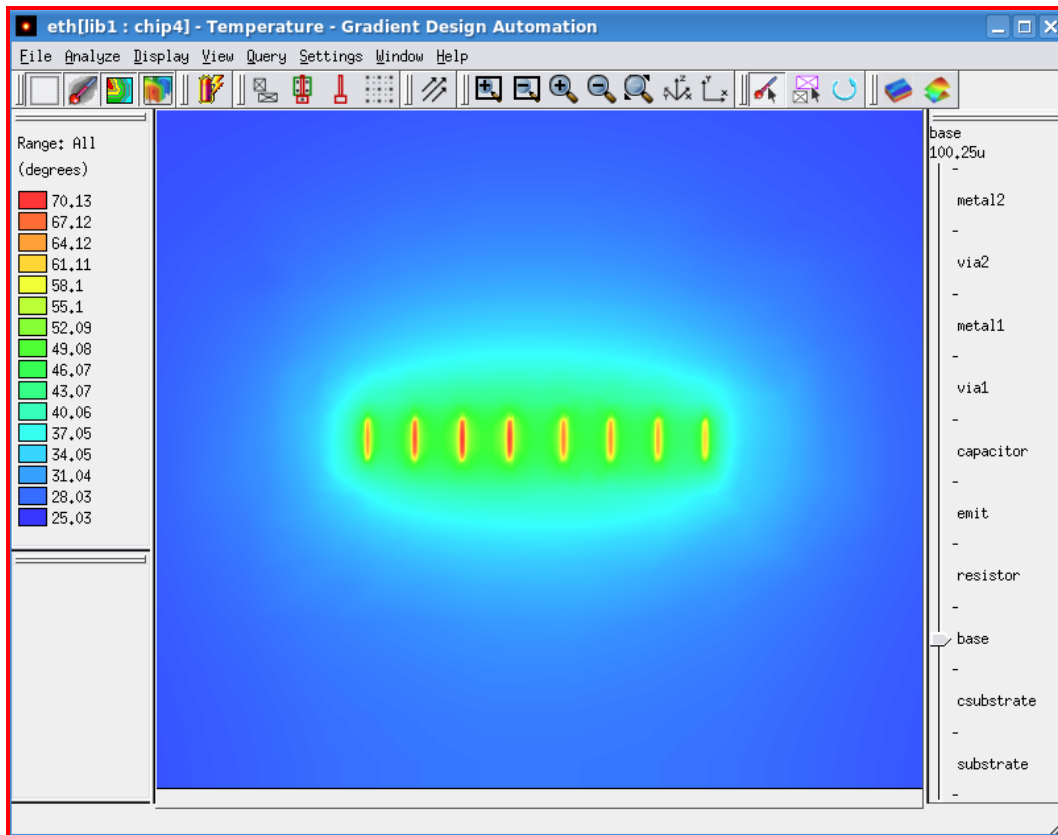


*Iteration loop is done automatically until powers and temperatures are self-consistent*

freq	dBm(out_cold)	dBm(out_hot)	delta	Pdc_cold	Pdc_hot
0.000 Hz	<invalid>	<invalid>	<invalid>	476.0 m	478.3 m
1.00 GHz	-2.63	-3.80	-1.17		
2.00 GHz	-38.13	-27.51	10.62		
3.00 GHz	-39.88	-32.94	-6.94		
4.00 GHz	-52.98	-50.57	-2.41		
5.00 GHz	-64.64	-52.14	-12.50		
6.00 GHz	-66.37	-70.67	4.30		
7.00 GHz	-81.89	-63.34	-18.55		

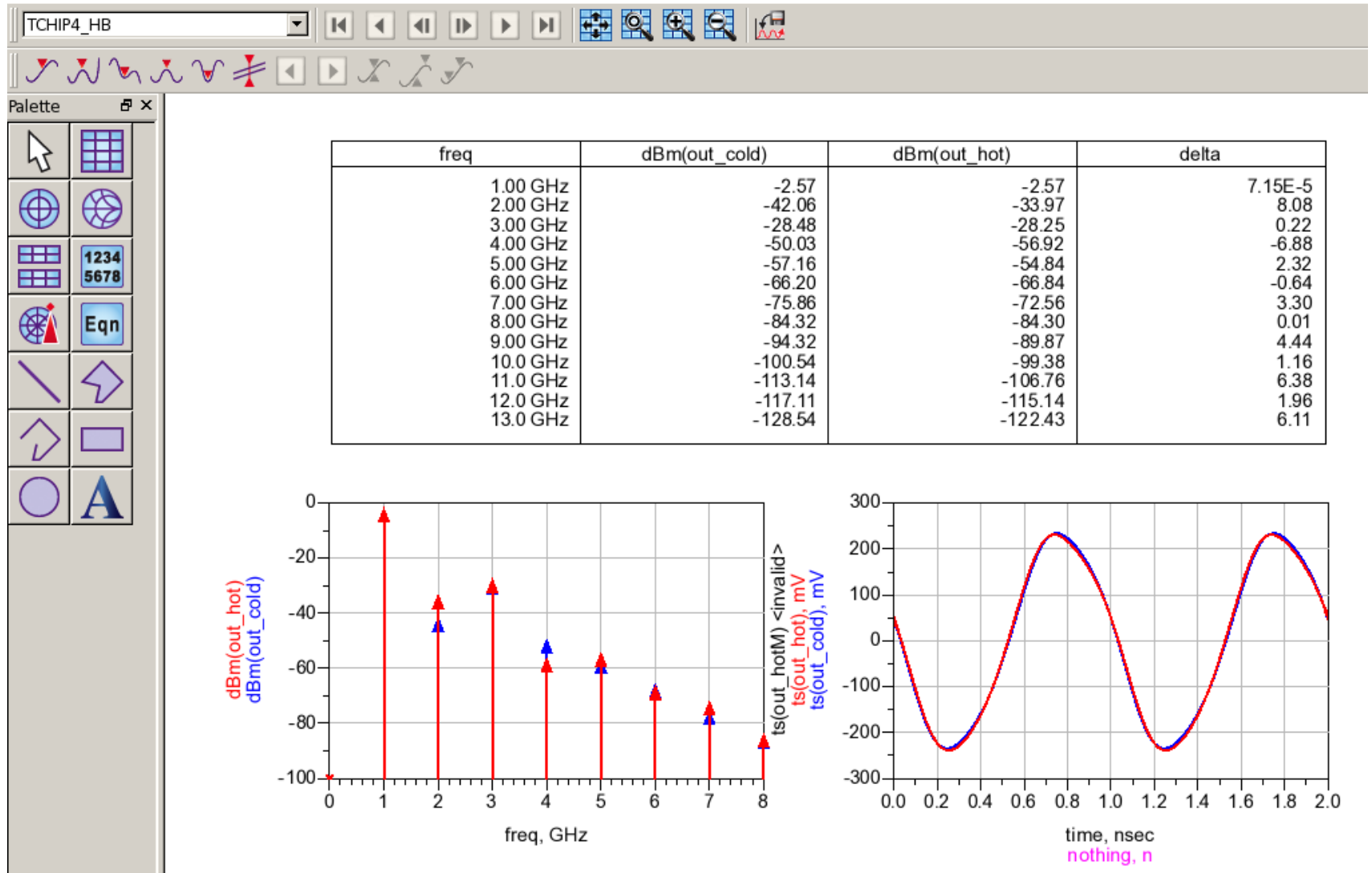


# Temperature Profile – Active Base Region

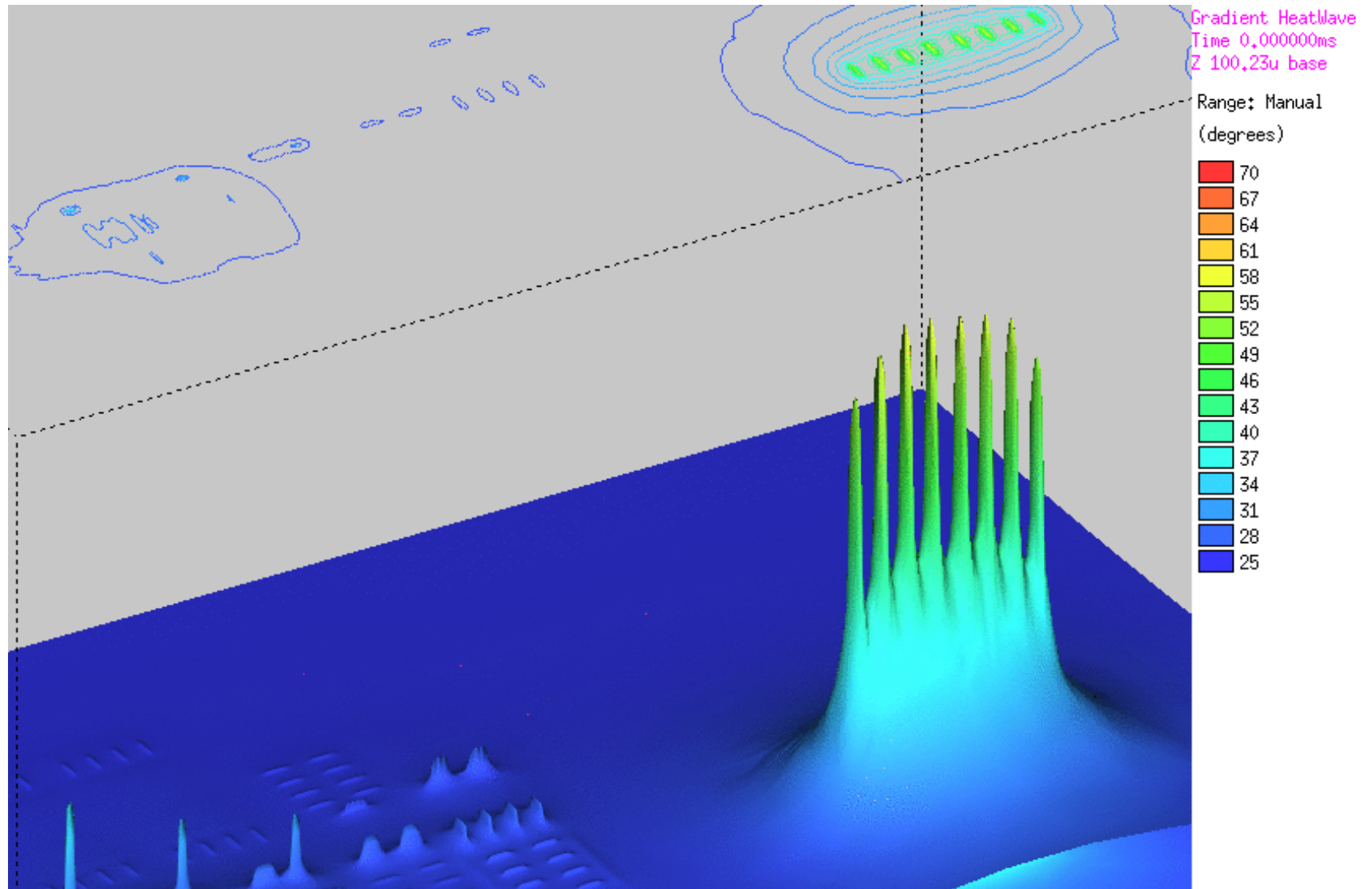




# Output Results



# Time-Domain Results

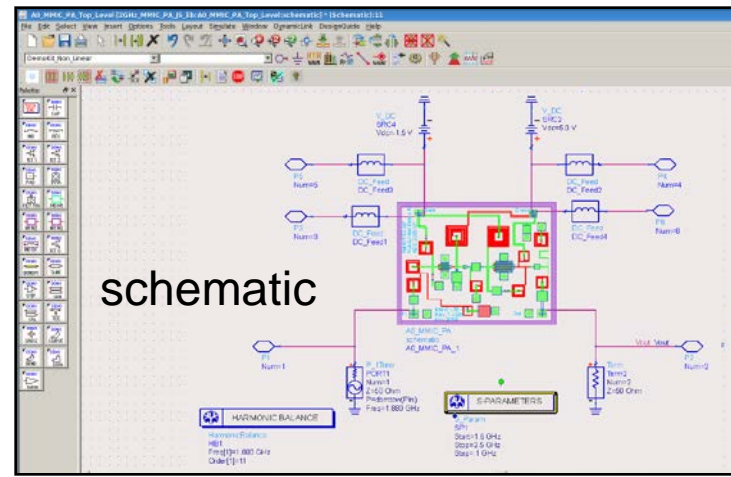


# Electro Thermal Simulation

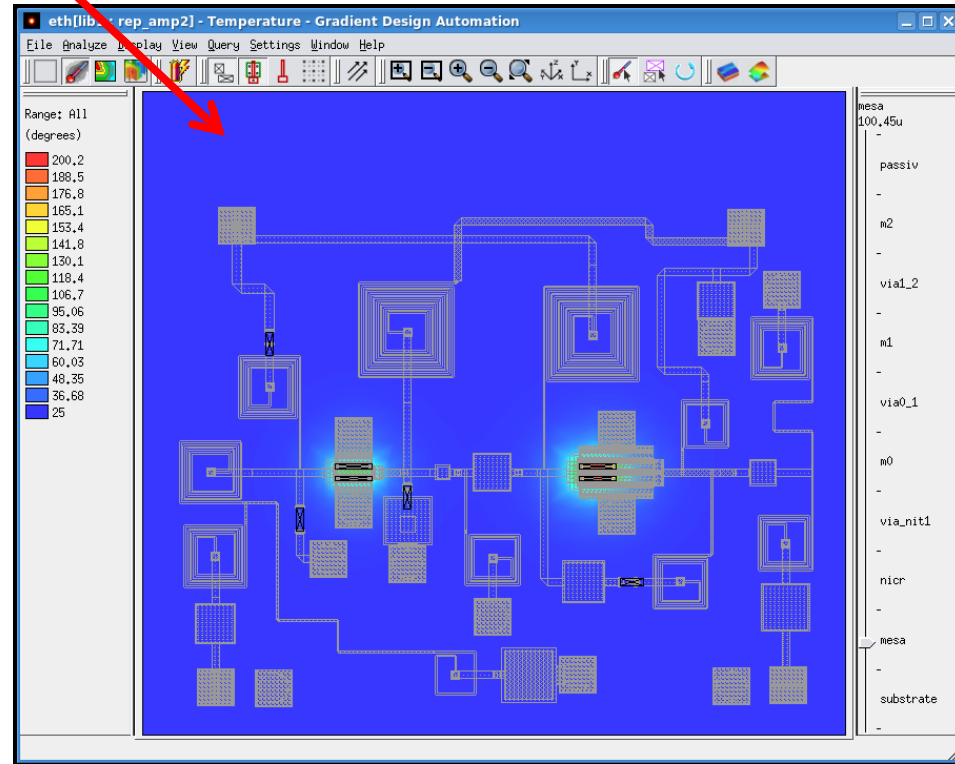
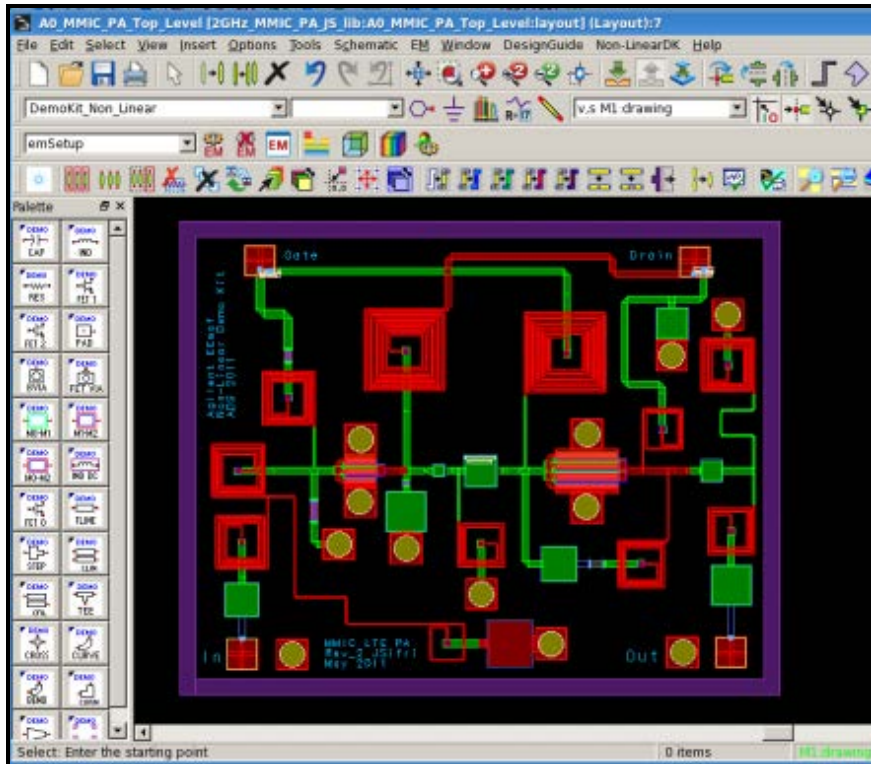
## 2-Stage GaAs LTE PA

Layout with heat sources

Layout

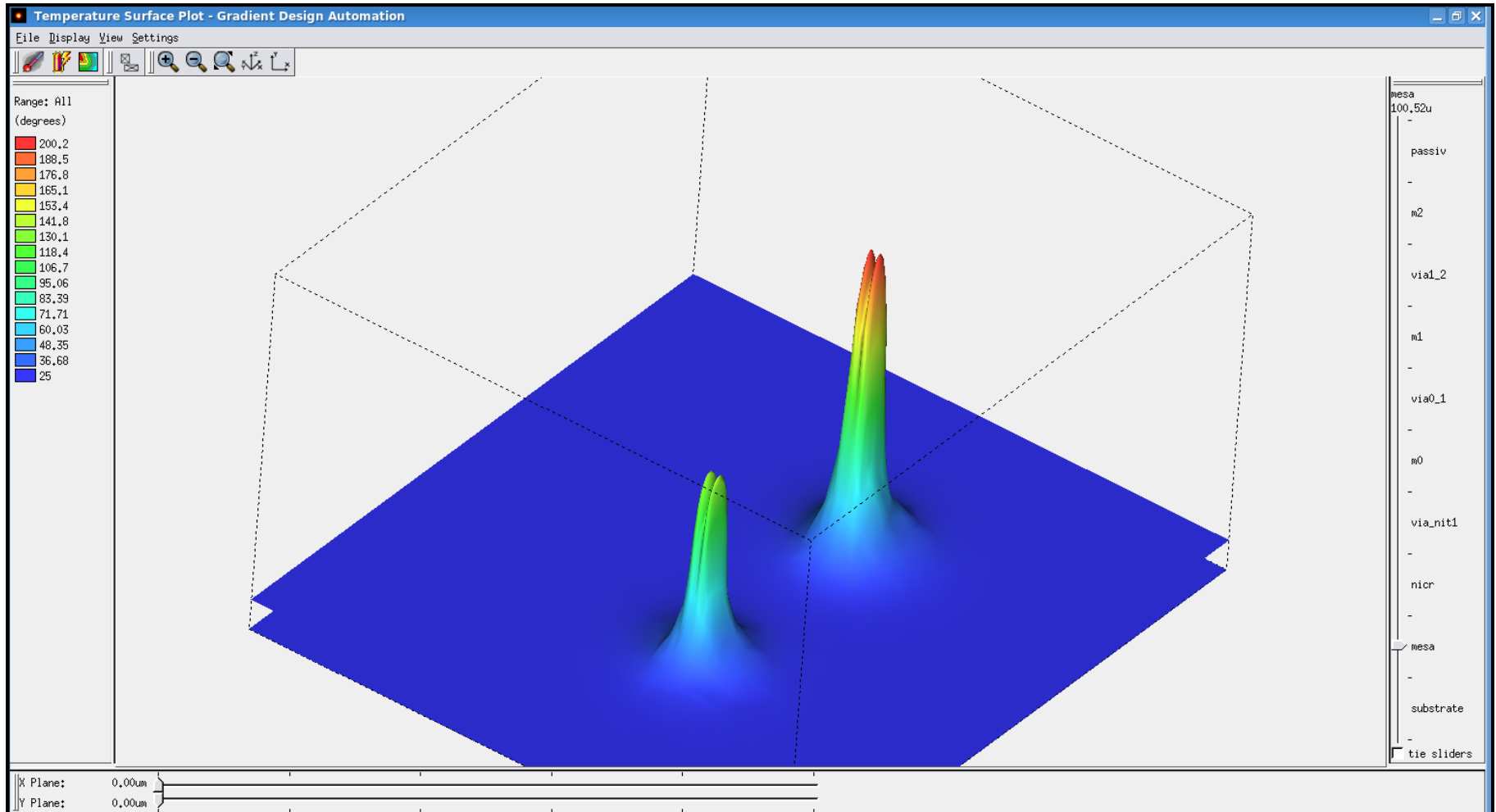


schematic



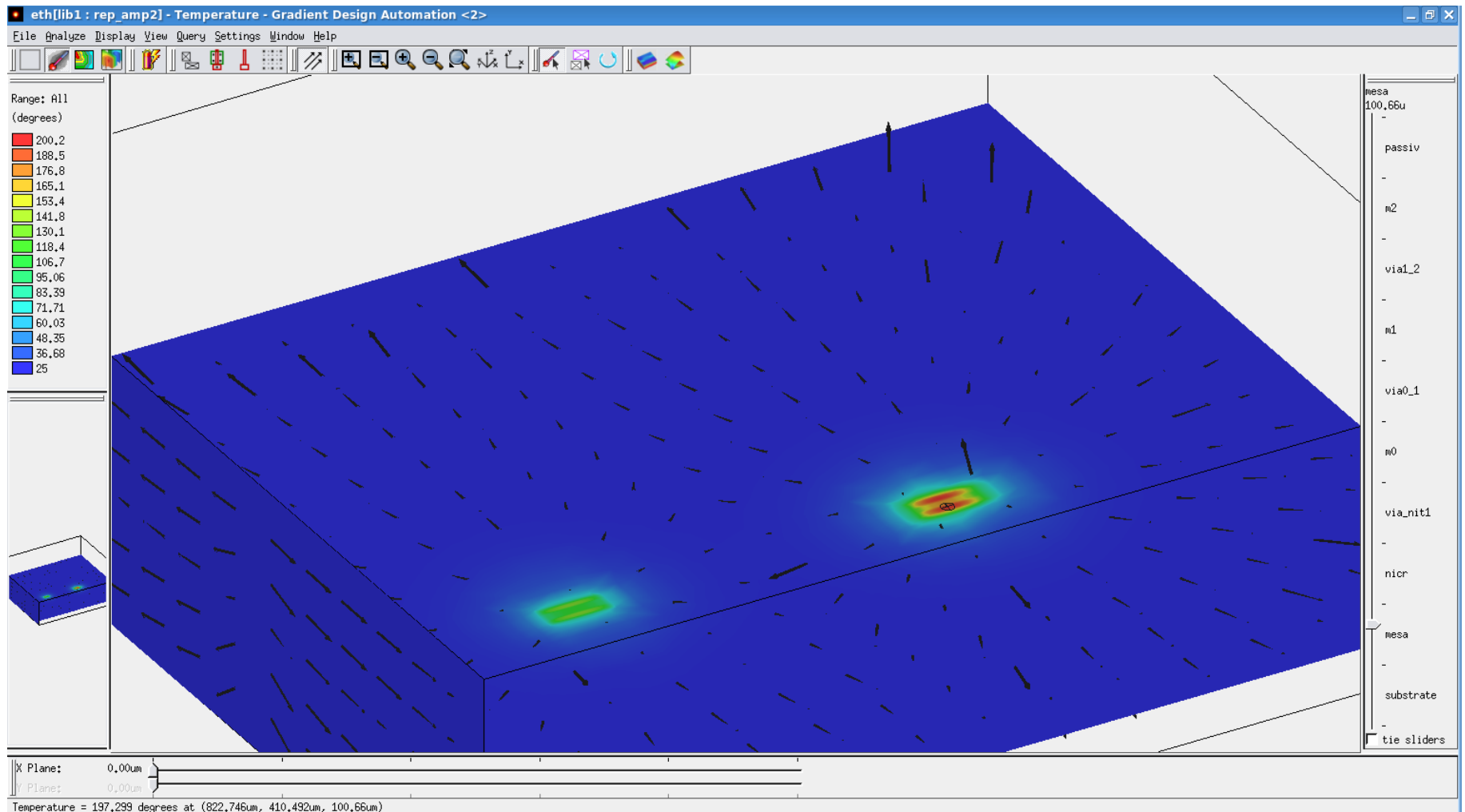
# Electro Thermal Simulation

## 2-Stage GaAs LTE PA



# Electro Thermal Simulation – Heat Flux

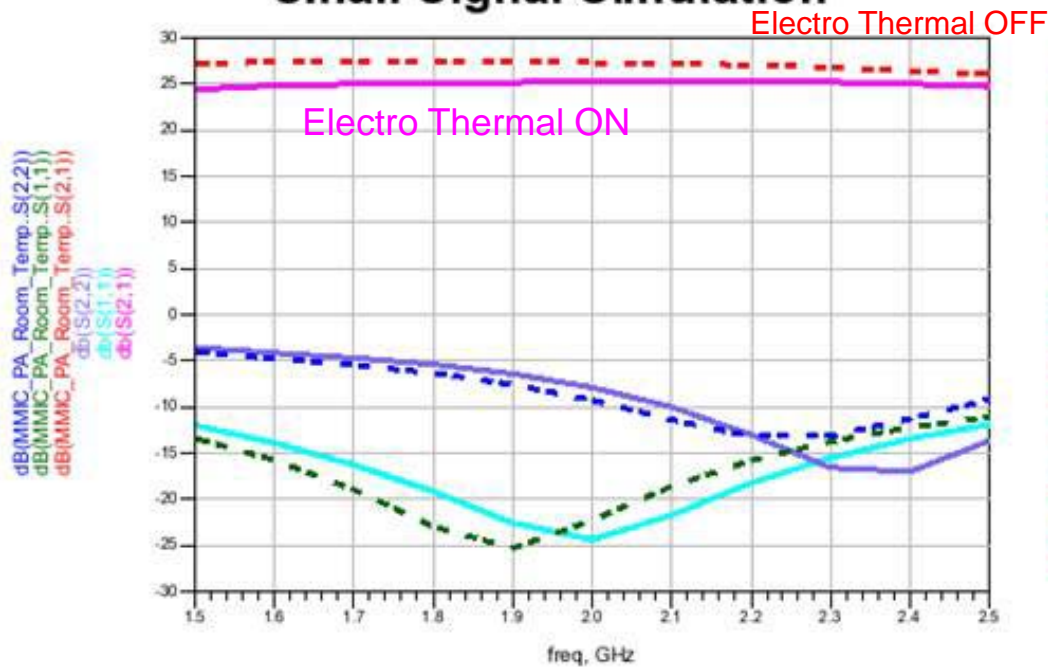
## 2-Stage GaAs LTE PA



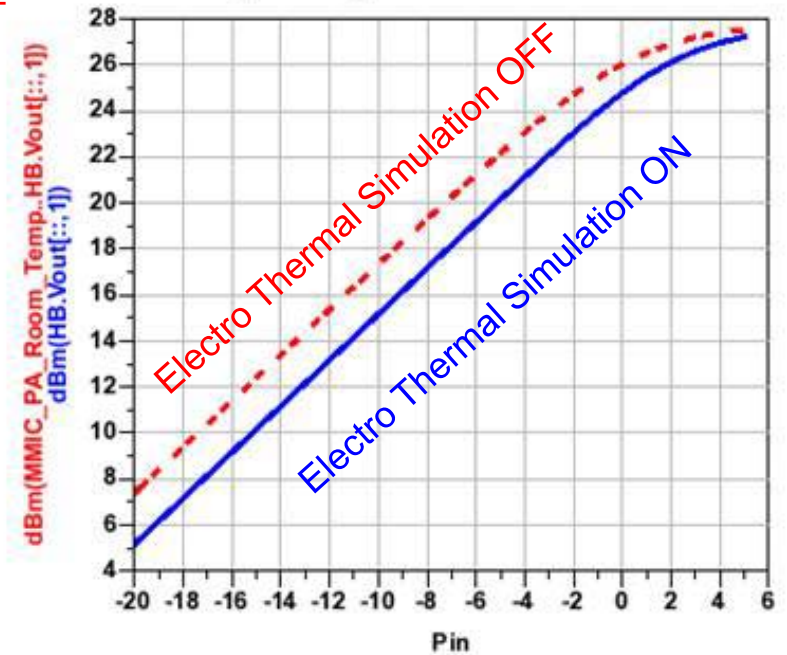
# Electro Thermal Simulation Results

## 2-Stage GaAs LTE PA

### Small Signal Simulation



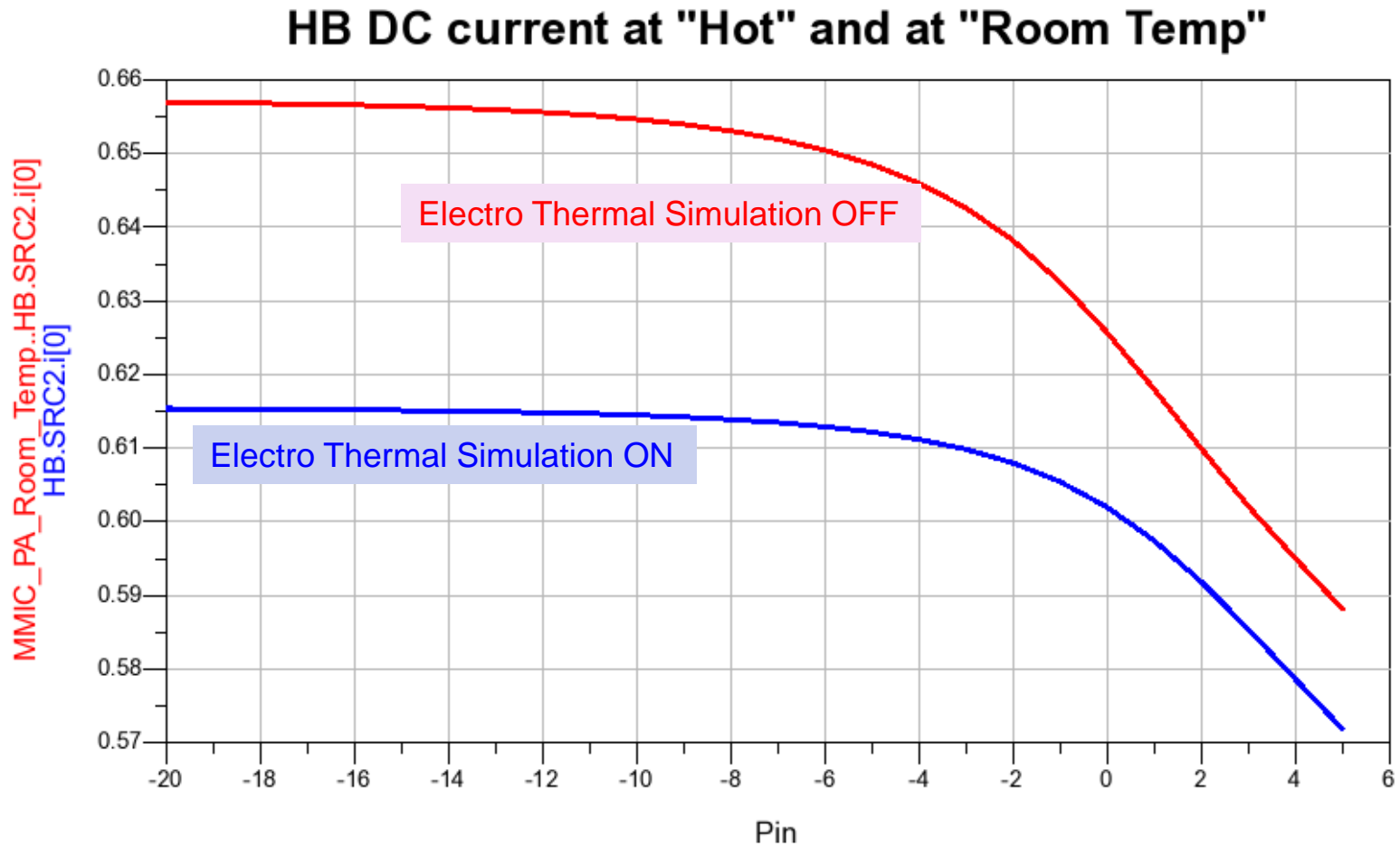
### Large Signal Simulation



Solid Lines: Electro Thermal Simulation ON  
Dashed Lines: Electro Thermal Simulation OFF

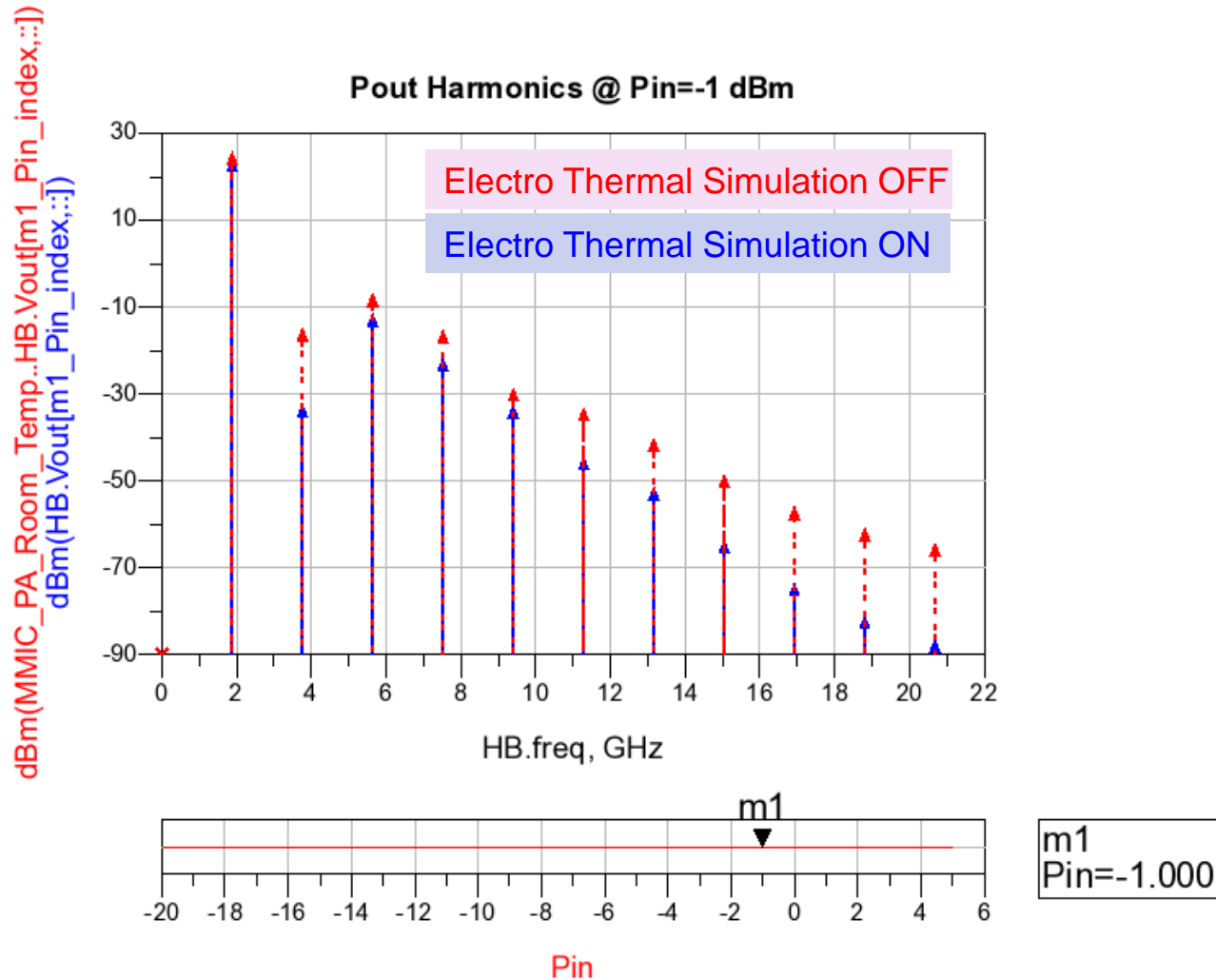
# Electro Thermal Simulation Results

## HB DC current at Hot Vs Room Temp



# Electro Thermal Simulation Results

## Harmonics at Hot Vs Room Temp





# IC, Laminate, Package Multi Technology PA Module Design

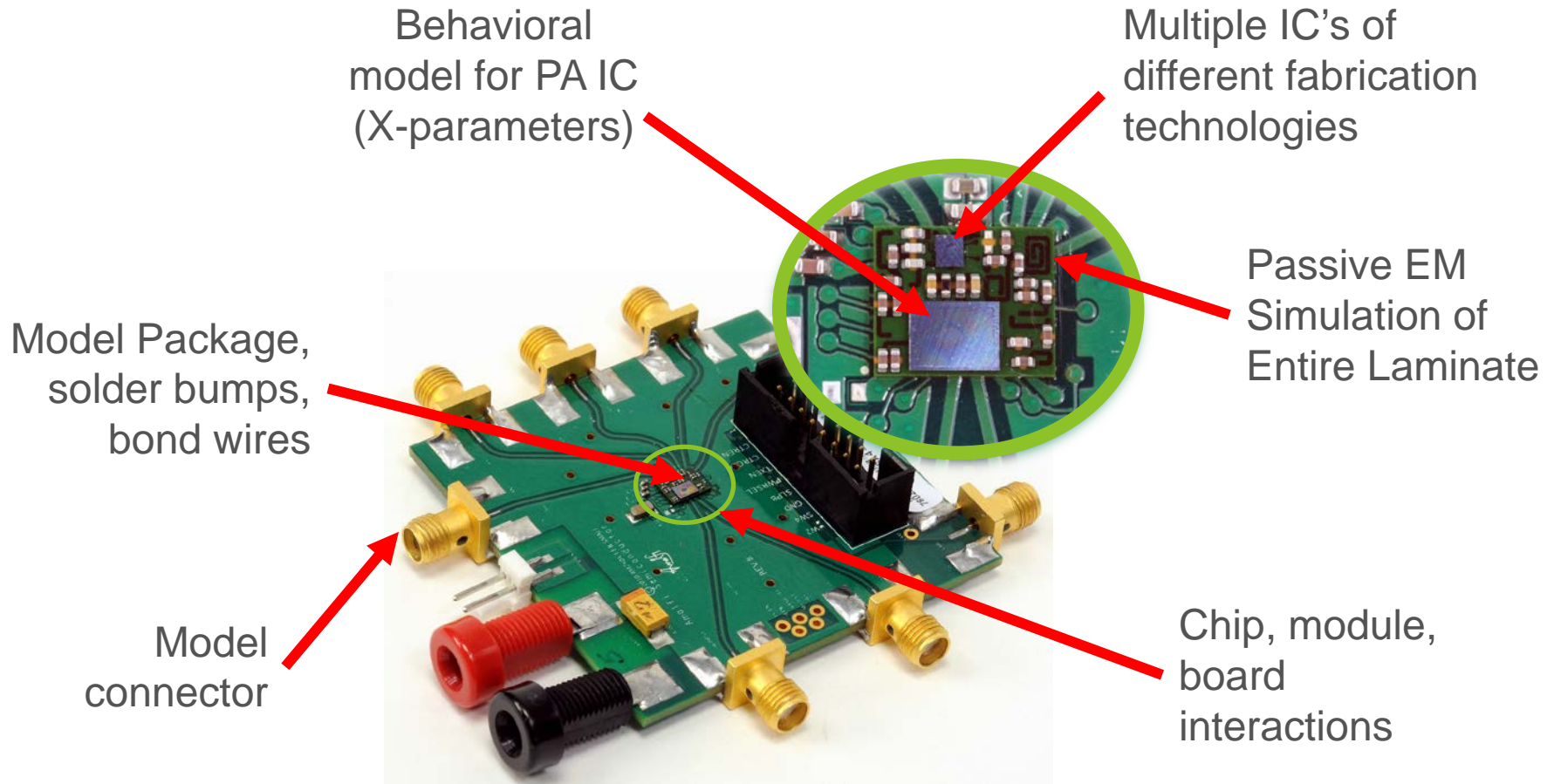
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# Integration Challenges with Multi-Technologies

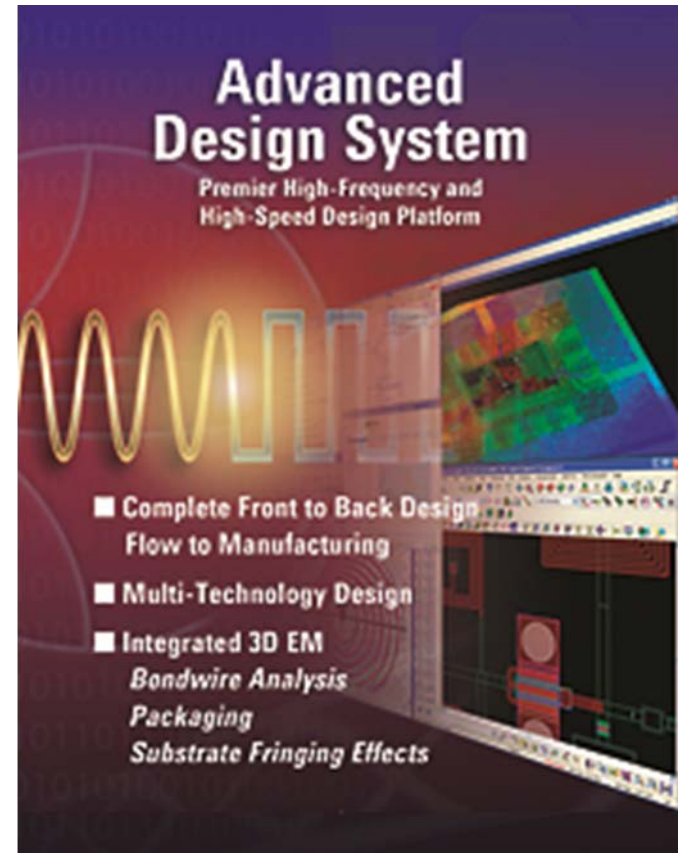
## The Ultimate "Device" Characterization Challenge



**Amalfi AM7802**  
PA Front End Module

# Summary

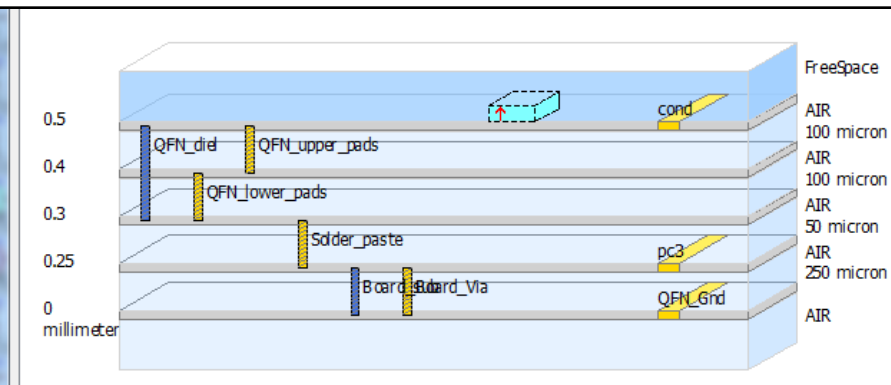
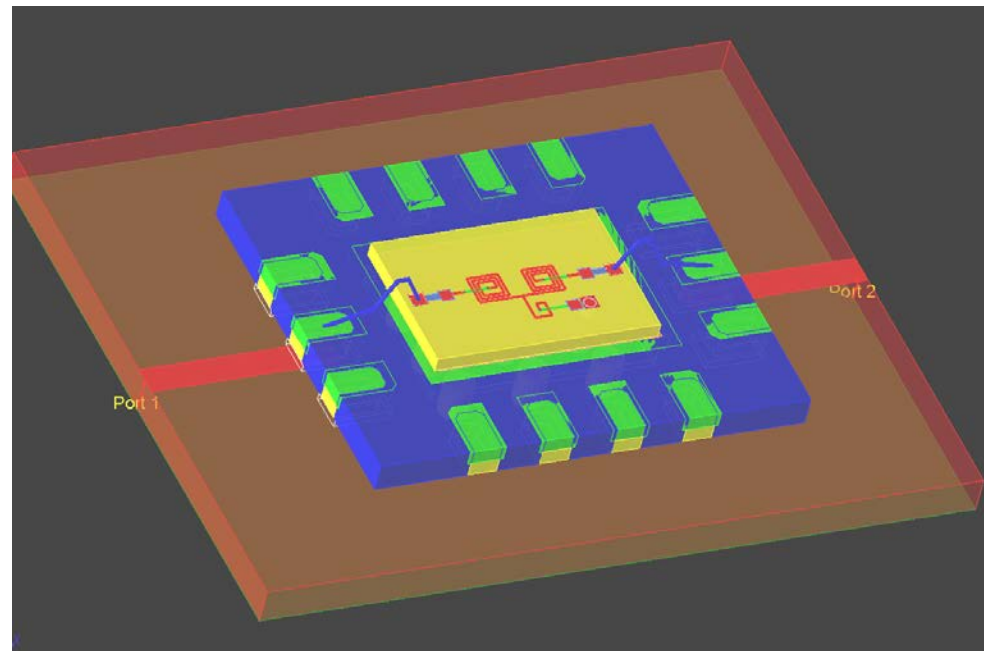
- RF design has moved to complex ICs in multi-chip RF modules
- Today's design flows are not able to address multiple technology design
- The IC, laminate, package, and PCB need to be designed together
- Electro-magnetic interactions between substrates need to be modeled
- ADS 2012 EDA software is able to address these multi-technology design challenges



Keysight EEsof EDA  
*“Innovative Solutions,  
Breakthrough Results”*

# Hands-on Workshop Available

- A Hands-on Workshop is available for training



# Workshop Outline

Section 1	Starting a New Workspace “Module”	Page 5
Section 2	Adding Libraries to our Module Workspace	Page 12
Section 3	Creating a new Cell for Module FEM simulation	Page 21
Section 4	Nested Technology / View Specific Configuration	Page 28
Section 5	Nested Technology Setup	Page 31
Section 6	Building the Module Assembly	Page 41
Section 7	Placing and Configuring the Bond Wires	Page 46
Section 8	Creating the Module Layer Stack-up Substrate	Page 52
Section 9	Defining the IC Bounding Area for FEM Simulation	Page 63
Section 10	FEM Simulation Set-up and Results	Page 76

# You Are Invited



Innovations in EDA Webcast Series

## Power Amplifier Design with X-Parameter Power Transistor Models

September 6 · 10 AM (Pacific Time)

Free 1-hour Webcast



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Dr. Larry Dunleavy, President & CEO Modelithics Inc.