Keysight N2114A & N2115A DDR4 BGA Interposer for Oscilloscope

User Guide

KEYSIGHT TECHNOLOGIES

Notices

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About This Guide

This guide provides installation information for the following Keysight products:

- N2114A x4/x8 DDR4 BGA interposer
- N2115A x16 DDR4 BGA interposer

Contents

1 N2114A and N2115A DDR4 BGA Interposer Description

The DDR4 BGA Interposers provide signal access points to clock, strobe, data, address, and command signals from a DDR4 DRAM package. These interposers let you make electrical, timing and eye diagram measurements with an Infiniium oscilloscope. The DDR4 BGA interposers are soldered in between the DRAM and PC board where the DRAM would normally be soldered.

The adapters are designed with the PCB footprint on the bottom side and the DRAM footprint on the top side. The signals from the memory controller chip and DRAM are then passed to the top side of the BGA interposer where they can be accessed with oscilloscope probes.

The probe adapters are designed to work with Keysight InfiniiMax II/III solder-in probes. There is an optional companion DDR4 riser that allows the user to elevate the interposer above surrounding passive components to avoid physical interference.

The N2114A x4/x8 BGA interposer provides support for the x4 and x8 DDR4 DRAM package footprints. The N2115A x16 BGA interposer provides support for the x16 DDR4 DRAM package footprint. Each interposer is shipped with a riser.

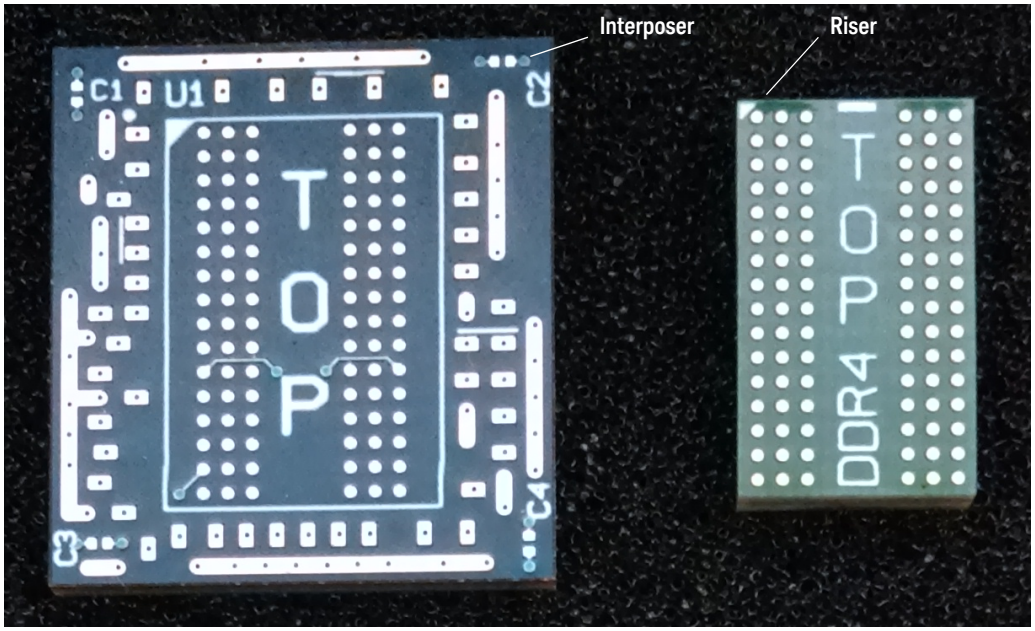


Figure 1 N2115A Interposer and DDR4 Riser

Recommended Configuration

Recommended Oscilloscopes

Data Range	Minimum Bandwidth	Minimum Channels	Compatible Oscilloscopes
Up to 3.2GT/s	13 GHz	3	Infiniium 90000 and Z series

The following is a list of the InfiniiMax oscilloscope probe amplifiers and probe heads recommended for use with the DDR4 BGA interposers.

InfiniiMax Probe Amplifiers

Model Number	Description
1169A	12-GHz InfiniiMax II probe amplifier
N2803A	30 GHz InfiniiMax III probe amplifier
N2802A	25 GHz InfiniiMax III probe amplifier
N2801A	20 GHz InfiniiMax III probe amplifier
N2800A	16 GHz InfiniiMax III probe amplifier
N2831A	8 GHz InfiniiMax III+ probe amplifier
N2832A	12 GHz InfiniiMax III+ probe amplifier

InfiniiMax Probe Heads

Model Number	Description
N5381A	InfiniiMax II 12-GHz differential solder-in probe head and accessories
N5382A	InfiniiMax II 12-GHz differential browser
E2677A	InfiniiMax II 12-GHz differential solder-in probe head and accessories
N5425A	InfiniiMax II 12-GHz ZIF probe head
N5426A	InfiniiMax II ZIF tips (x10)

Note: InfiniiMax I/II probe heads and accessories (compatible with 9000 and 90000 Series, use N5442A precision BNC adapter with 90000X/Q Series).

InfiniiMax III Probe Heads and Accessories

Model Number	Description
N5451A	Long Wire tips (x10)
N5439A	ZIF probe head
N5445A	Browser (hand held) probe head
N5441A	Solder-in probe head
N2838A	450Ω PCB ZIF tips (set of 5)
N5447A	250Ω ceramic ZIF tips (set of 5)
N2848A	InfiniiMax III QuickTip head
N2849A	InfiniiMax III QuickTip tips (4 per kit)

To learn more about Infiniium oscilloscope probes and accessories, check out the Infiniium Oscilloscope Probes and Accessories data sheet with the Keysight literature number 5968-7141EN.
For more information about Keysight's InfiniiMax III probing system, check out the InfiniiMax III data sheet with the Keysight literature number 5990-5653EN.

2 DDR4 BGA Interposers Operation

Installing the DDR4 BGA Interposer

The DDR4 BGA Interposer is installed by soldering it onto the BGA footprint of a PC board where the DRAM would normally be soldered. The DDR4 DRAM is then soldered to the top side of the BGA interposer. This attachment may occur in any order. (The BGA interposer can be soldered first to the PCB, then the DDR4 DRAM can be soldered to the BGA interposer, or the DDR4 DRAM can be soldered first to the BGA interposer, then the BGA interposer assembly can be soldered to the PCB.)

The interposer is designed to tolerate lead-free soldering temperature profiles. However, it is always recommended that the minimum temperature required for soldering be applied and that the minimum number of heating and cooling cycles be applied to reduce risk of any damage to the probe. The BGA Interposer is supplied with lead free solder balls attached.

Some general guidelines are:

- When soldering the DRAM onto the interposer, the temperature may need to rise to the point where the solder balls under the interposer soften. Some method of holding the interposer in place when soldering the DRAM may be necessary.
- Normal surface cleaning and preparation procedures for BGA soldering are recommended.

If you do not have the in-house expertise to attach the BGA interposer and DRAM, contract manufacturers with this expertise may be willing to perform the attachment for a fee. More information on BGA soldering and rework techniques that may be useful in attaching the probe can be found at:

- http://www.circuitrework.com/guides/9-1-1.shtml
- http://www.keysight.com/find/ddr4bga-scope

Installing a Riser, Interposer and DRAM

1. Attach the Riser to the DIMM (or motherboard).
2. Place glue dots (similar to what is used during two sided board manufacturing to hold passive components on the bottom-side of a board when placing parts on the top-side). These can be easily placed at the mid-point of the north and south ends of the Riser, where there are no BGA balls.
3. Attach the Interposer to the top of the Riser.
4. Place two small glue dots at the mid-point of the north and south ends of the Riser/Interposer.
5. Attach the DRAM to the top of the interposer.

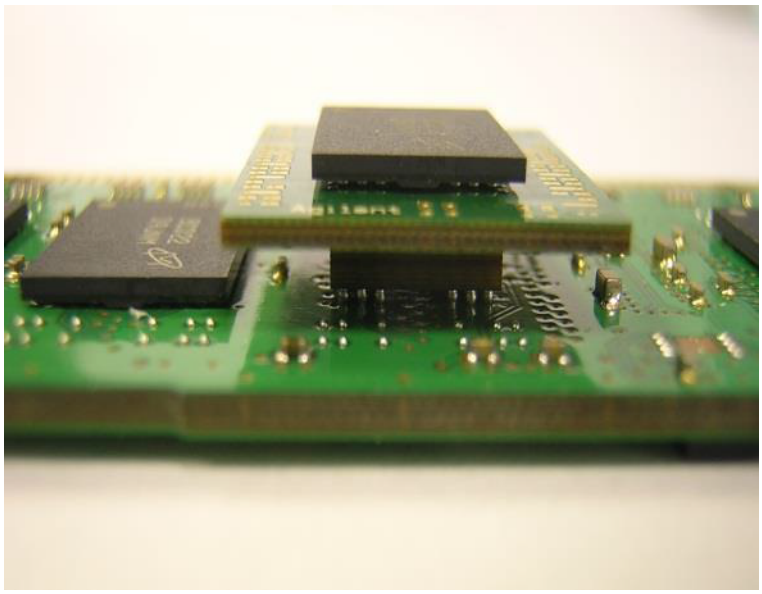


Figure 2 Final Installation of the Interposer, Riser and DRAM

Block Diagram

A high-level block diagram of the DDR4 Interposer is shown in Figure 3. The tip resistors provide isolation to minimize the impact of connecting the test equipment to the operating DDR4 memory device in the system. These tip resistors are nominally 100Ω.

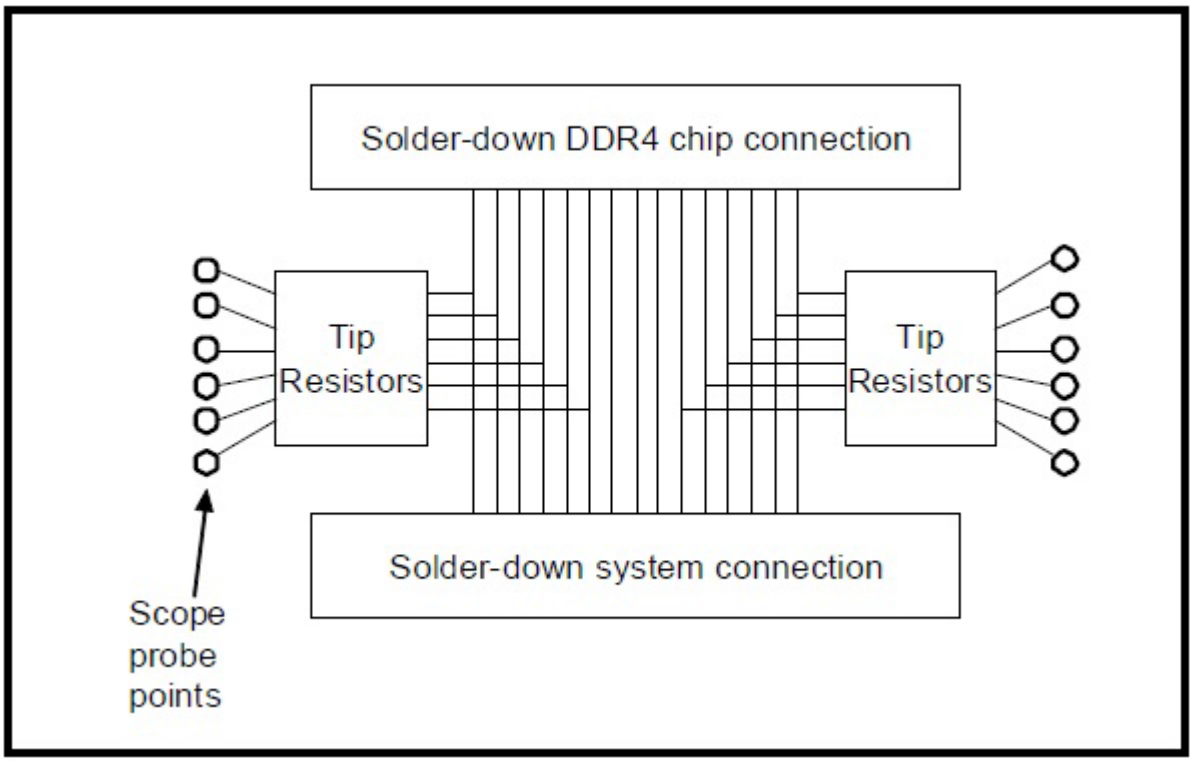


Figure 3 Solder Down Interposer Block Diagram

3 DDR4 BGA Interposers Dimensions, Pad Numbering and Location

N2114A Dimensions, Pad Numbering and Location

DDR4 x8 Footprint and Signals Probe with N2114A

The following table shows the DDR4 x4/x8 chip pin out that is supported by the N2114A interposer. Table 1 shows the signals that the N2114A interposer provides access to at the oscilloscope test points around the edge.

Table 1 DDR4 x8 Probed Signals (Probed signals are highlighted in red colored font)

1	2	3	7	8	9
VDD	GND	TDQS_c	A	DM_n/DBI/TDQS_t	GND	GND
VPP	VDDQ	DQS_c	B	DQ1	VDDQ	ZQ
VDDQ	DQ0	DQS_t	C	VDD	GND	VDDQ
GND	DQ4	DQ2	D	DQ3	DQ5	GND
GND	VDDQ	DQ6	E	DQ7	VDDQ	GND
VDD	C2/ODT1	ODT	F	CK_t	CK_c	VDD
GND	C0/CKE1	CKE	G	CS_n	C1/CS1_n	RFU
VDD	WE_n/A14	ACT_n	H	CAS_n/A15	RAS_n/A16	GND
VrefCA	BG0	A10/AP	J	A12/BC_n	BG1	VDD
GND	BA0	A4	K	A3	BA1	GND
RESET_n	A6	A0	L	A1	A5	ALERT_n/VMON
VDD	A8	A2	M	A9	A7	VPP
GND	A11	PARITY	N	A17	A13	VDD

The Interposer contains two internal planes: one for power and one for ground. All VDD and VDDQ pins are connected to the common power plane. There are sets of pads on the top of the Interposer at the corners. These 0201 pads allow the user to attach power filtering capacitors at the time they apply the DDR4 chip to the top of the Interposer, if required. The internal planes are adjacent in the stack-up and will provide high frequency noise filtering without the external capacitors present; however, use of external capacitance is recommended for applications in a potentially noisy power environment (or when the optional Riser is used).

N2114A DDR4 x4/x8 BGA Interposer Test Point Map and Dimensions

DDR4 N2114A x4/x8 DDR4 Interposer Dimensions:

- Width: 16.0 mm +/- 1 mm
- Height: 18.0 mm +/- 1 mm
- Thickness: 1.0 mm +/- 0.2 mm

Note that there are pads for attachment of power filter capacitors at the corners of the probe. These connect directly to the internal power and ground planes in the probe.

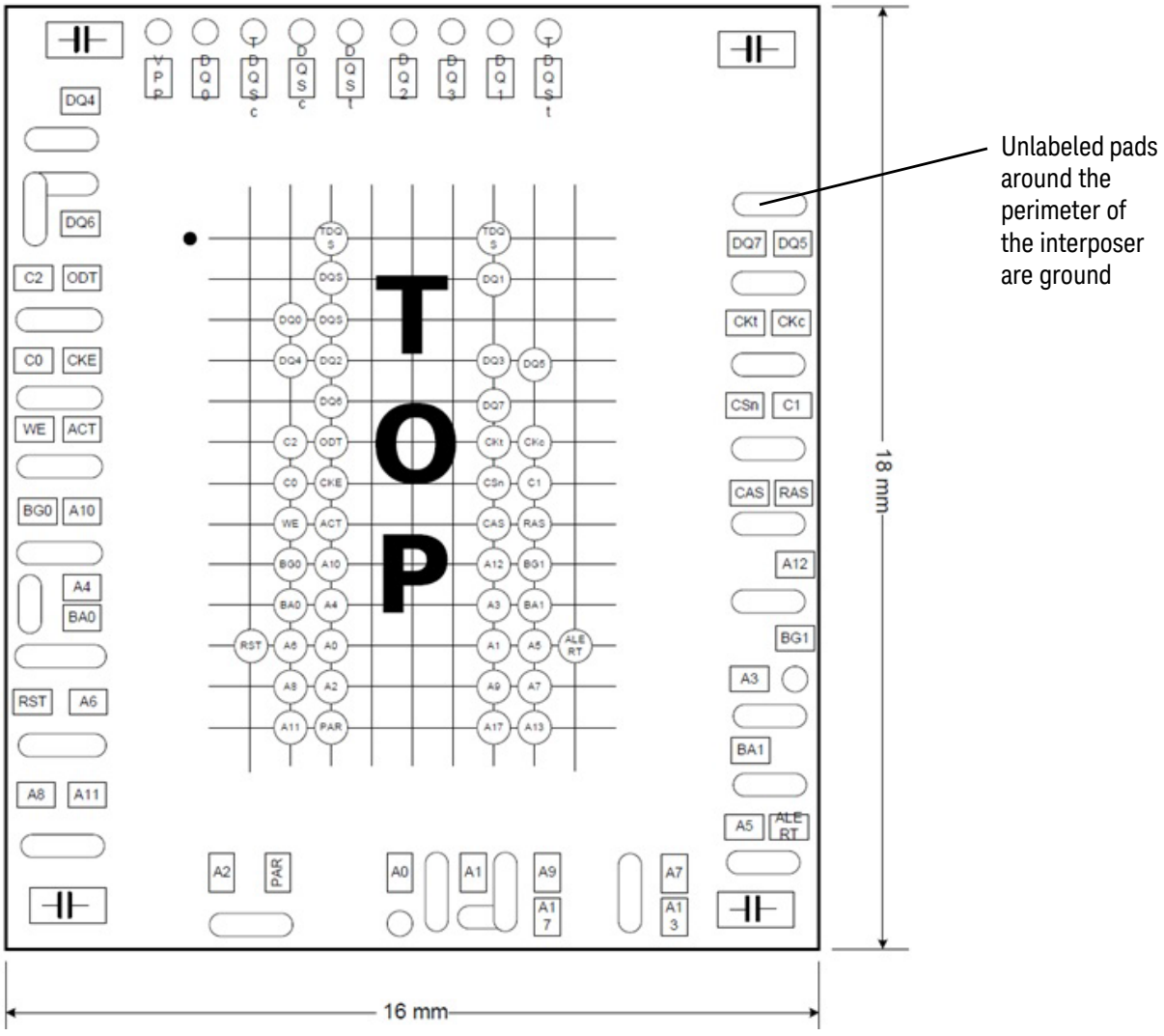


Figure 4 N2114A x4/x8 DDR4 BGA Interposer Pin Out

DDR4 x4/x8 Riser Dimensions

For applications where there are components mounted close to the chip to be probed, a DDR4 Riser is available. This Riser elevates the DDR4 Interposer to lift it above adjacent parts.

N2114A Riser Dimensions:

- Width: 7.5 mm +/- 0.5 mm
- Height: 10.5 mm +/- 0.5 mm
- Thickness: 1.5 mm minimum

The DDR4 Riser is a via-in-pad design with internal power and ground planes. All VDD and VDDQ power pads are connected to the internal power plane. All GND (VSS and VSSQ) pads are connected to the internal ground plane.

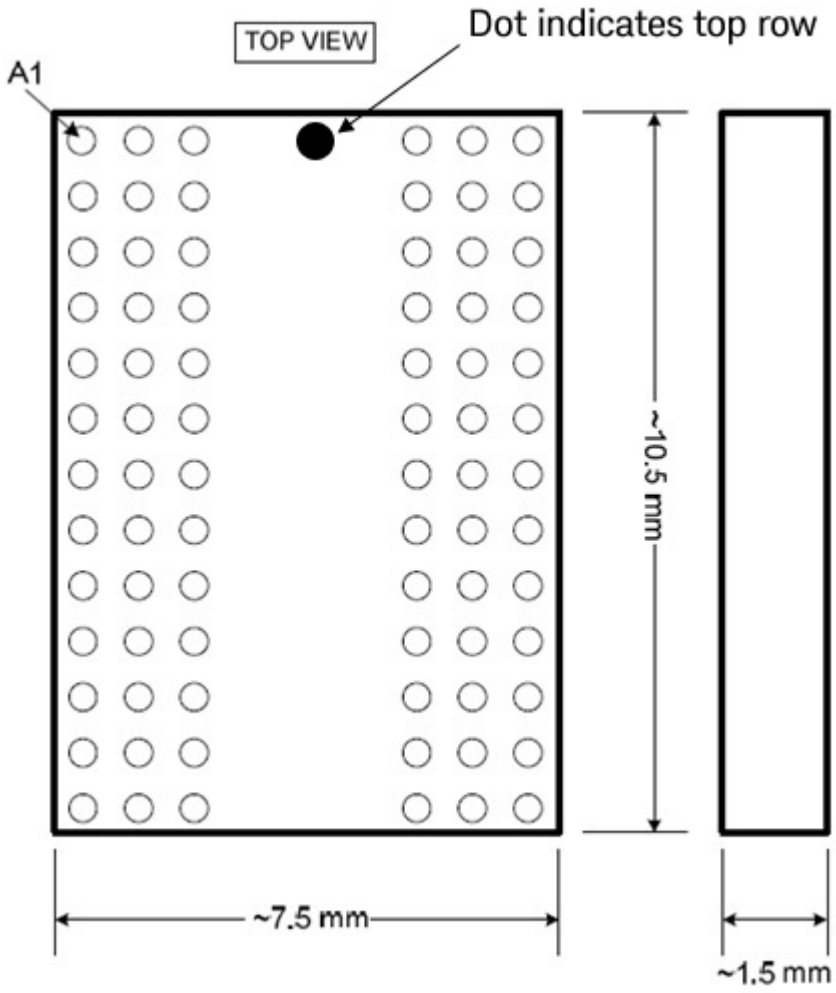


Figure 5 DDR4 x4/x8 Riser

N2115A Dimensions, Pad Numbering and Location

DDR4 x16 Footprint and Signals Probe with N2115A

The following table shows the DDR4 16 chip pin out that is supported by the N2115A interposer. Table 2 shows the signals that the N2115A interposer provides access to at the oscilloscope test points around the edge.

Table 2 DDR4 x16 Probe Signals (Probed signals are highlighted in Grey color)

1	2	3	4-6	7	8	9
VDDQ	GND	DQU0	A	DQSU_c	GND	VDDQ
VPP	GND	VDD	B	DQSU_t	DQU1	VDD
VDDQ	DQU4	DQU2	C	DQU3	DQU5	GND
VDD	GND	DQU6	D	DQU7	GND	VDDQ
GND	DMU_n/ DBIU_n	GND	E	DML_n/ DBI_n	GND	GND
GND	VDDQ	DQSL_c	F	DQL1	VDDQ	ZQ
VDDQ	DQL0	DQSL_t	G	VDD	GND	VDDQ
GND	DQL4	DQL2	H	DQL3	DQL5	GND
VDD	VDDQ	DQL6	J	DQL7	VDDQ	VDD
GND	CKE	ODT	K	CK_t	CK_c	GND
VDD	WE_n/ A14	ACT_n	L	CS_n	RAS_n/ A16	VDD
VrefCA	BG0	A10/AP	M	A12/ BC_n	CAS_u/ A15	GND
GND	BA0	A4	N	A3	BA1	TEN
RESET_n	A6	A0	P	A1	A5	ALERT_n
VDD	A8	A2	R	A9	A7	VPP
GND	A11	PARITY	T	NC	A13	VDD

N2115A DDR4 x16 BGA Interposer Test Point Map and Dimensions

DDR4 N2115A x16 DDR4 Interposer Dimensions:

- Width: 16.5 mm +/- 1 mm
- Height: 18.0 mm +/- 1 mm
- Thickness: 1.0 mm +/- 0.2 mm

Note that there are pads for attachment of power filter capacitors at the corners of the probe. These connect directly to the internal power and ground planes in the probe.

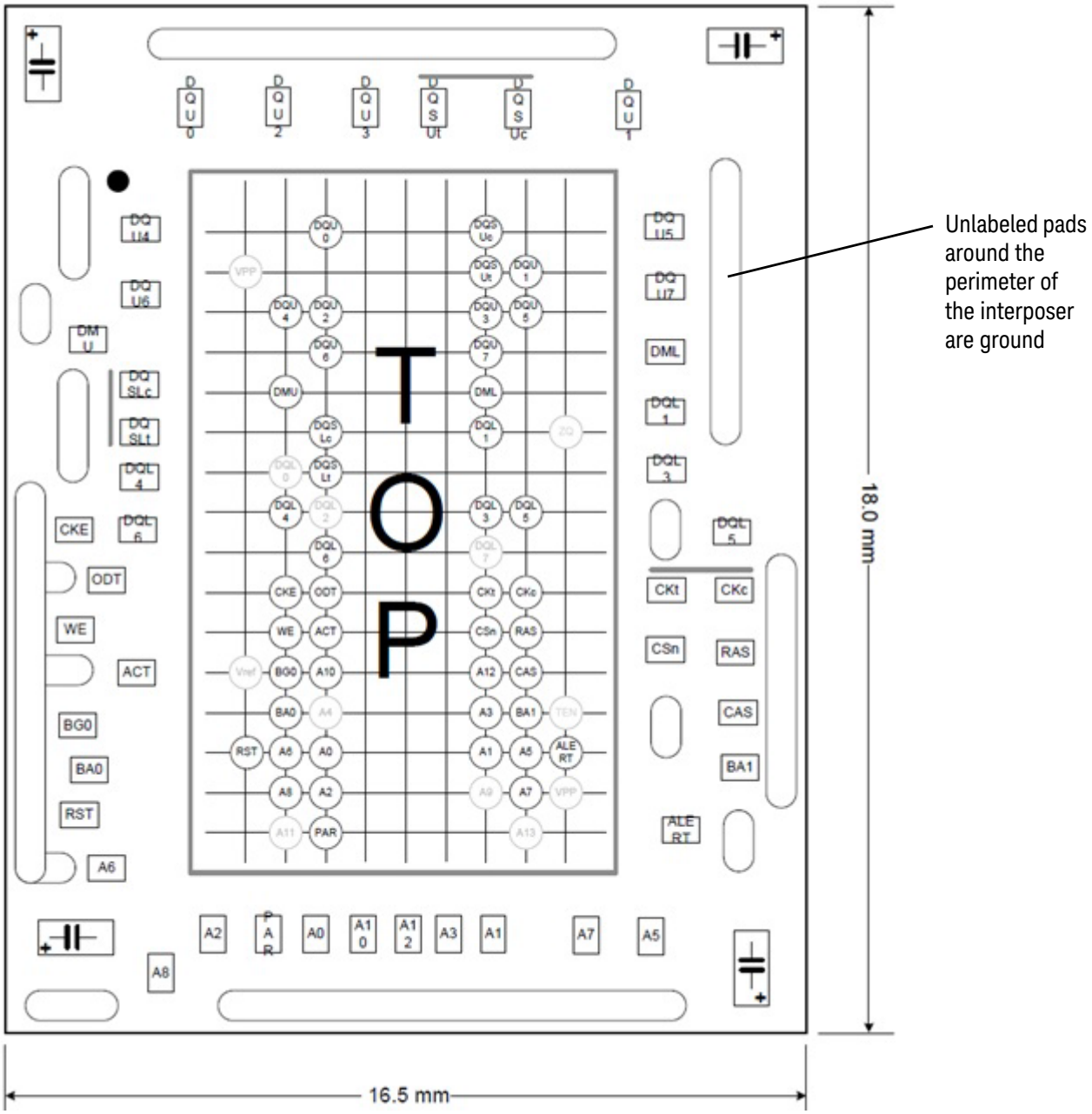


Figure 6 N2115A x16 DDR4 BGA Interposer Pin Out

DDR4 x16 Riser Dimensions

For applications where there are components mounted close to the chip to be probed, a DDR4 Riser is available. This Riser elevates the DDR4 Interposer to lift it above adjacent parts.

N2115A Riser Dimensions:

- Width: 7.6 mm +/- 0.5 mm
- Height: 13.1 mm +/- 0.5 mm
- Thickness: 1.5 mm minimum

The DDR4 Riser is a via-in-pad design with internal power and ground planes. All VDD and VDDQ power pads are connected to the internal power plane. All GND (VSS and VSSQ) pads are connected to the internal ground plane.

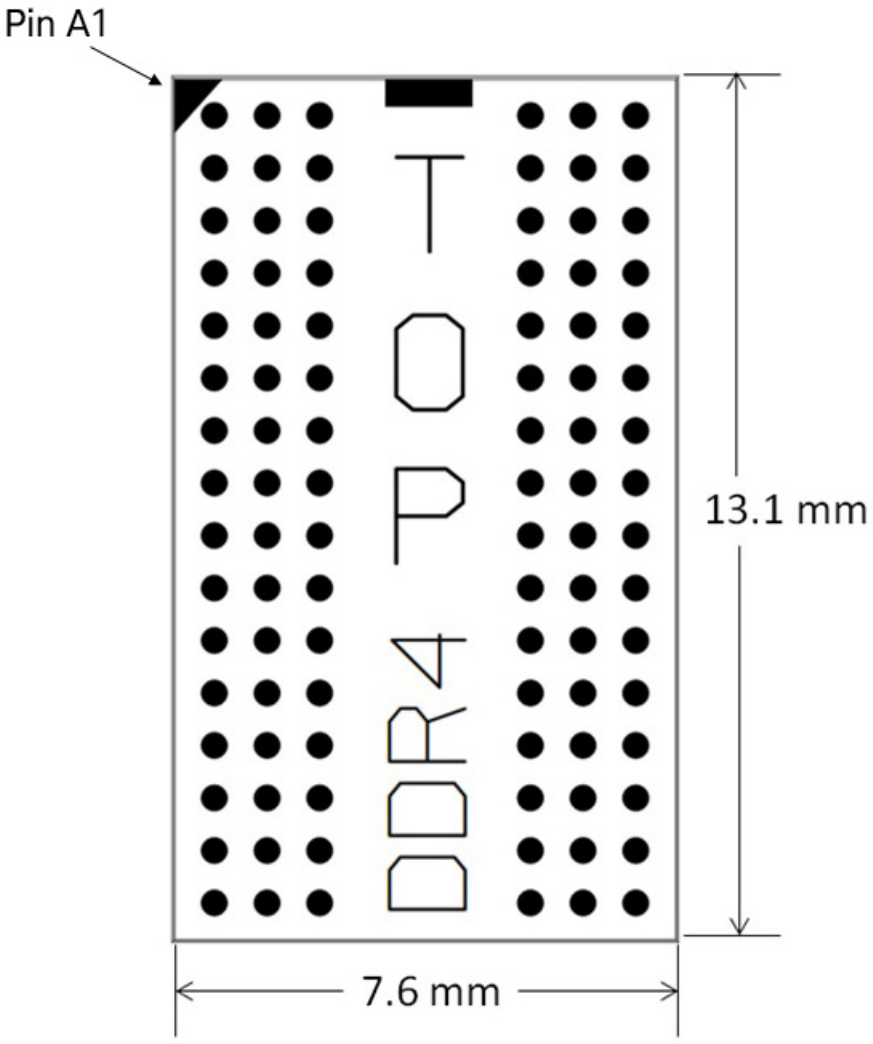


Figure 7 DDR4 x16 Riser

N2115A x16 DDR4 interposer for Large DRAM Package Use Model

Solution for large DRAM package application: Riser (or DRAM socket) elevates the large DRAM package to allow for soldering of probe tips to test points.

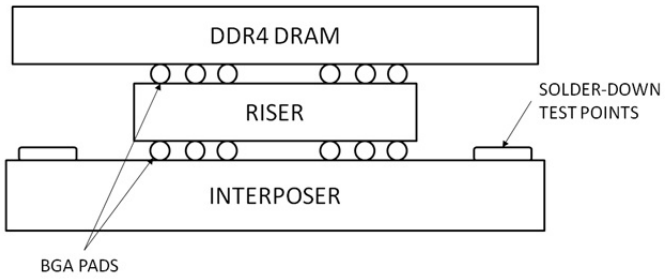


Figure 8 Large DRAM Package Use Model

3 DDR4 BGA Interposers Dimensions, Pad Numbering and Location

4 Simulation Model for Use with InfiniiSim Transformation Toolset

Simulation models of the N2114A and N2115A DDR4 BGA interposers are available at www.keysight.com/find/ddr4bga-scopes.

Single Ended Measurements

This section shows how to directly create the transfer function to convert the probed measurement on the interposer pads to a simulated measurement at the via between the DRAM and the PC board for single ended measurements. The result is a .tf2 file which the Infiniium oscilloscope family converts to an FIR filter to perform real time convolution to display the transformed acquisition.

Selecting the Probe

1 At the Infiniium oscilloscope screen, select Channel 1 (or your target channel). The **Channel Setup** dialog is displayed as shown in Figure 9.

Figure 9 Channel Setup Dialog - 2 Port Channel 1

2 Select **2 Port** in the InfiniiSim section at the bottom and before clicking **Setup**, click **Probe...**.

The **Probe Configuration Setup** screen is displayed.

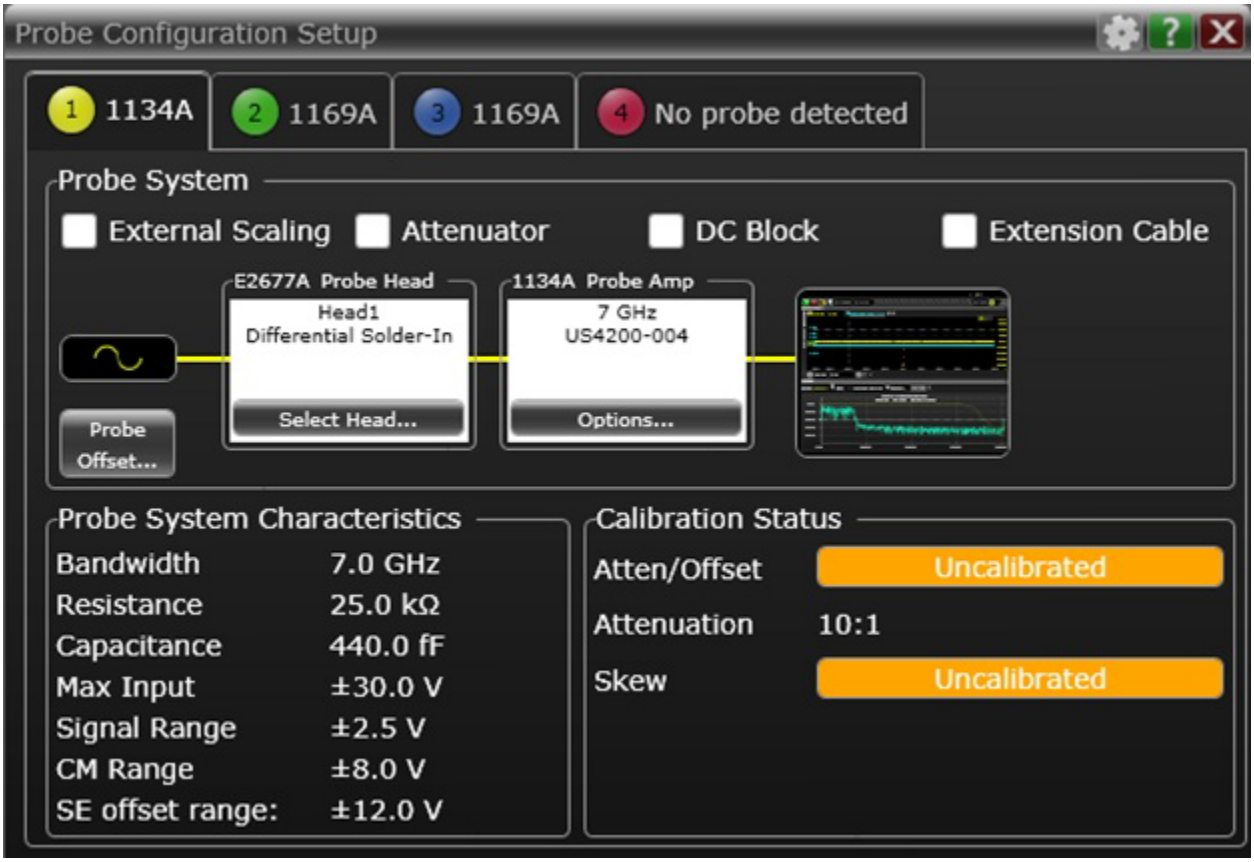


Figure 10 Probe Configuration Setup Screen- 2 Port Channel 1

3 On the **Probe Configuration Setup** screen, enter the probe and connection type (single ended). In the above example (Figure 10), the E2677A solder-in probe in single ended mode has been selected.

4 After selection, close the **Probe Configuration Setup** screen and go back to **Channel Setup** screen (Figure 9) and click **Setup** under InfiniiSim pane.

5 On the **InfiniiSim Setup** dialog that appears, click the **Create Transfer Function from Model** button to initiate a transfer function (see Figure 11).

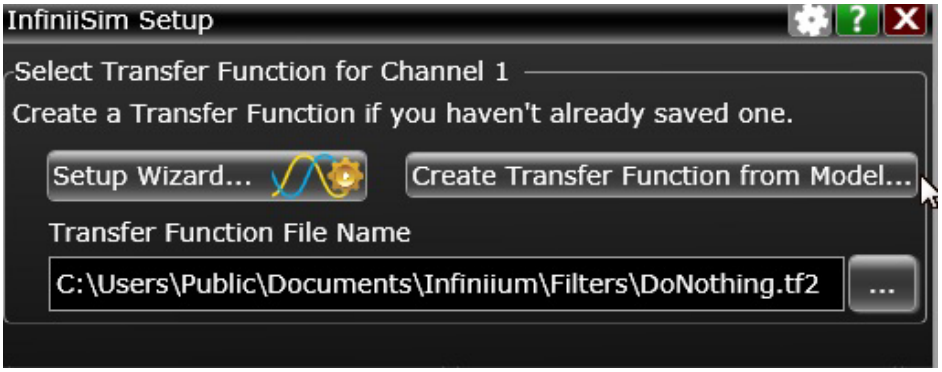


Figure 11 InfiniiSim Setup Dialog - 2 Port Channel 1

Describing the Circuit in InfiniiSim

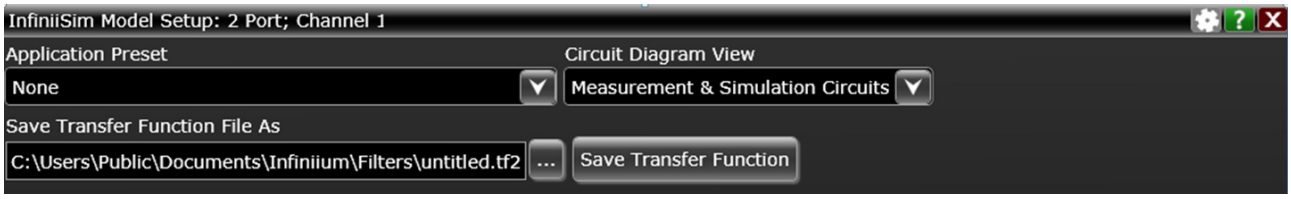


Figure 12 InfiniiSim Model Setup screen- 2 Port Channel 1

6 On the **InfiniiSim Model Setup** screen, select the default configurations for your circuit description.

7 Select **General purpose 9 blocks** from the **Application Preset** drop-down menu (see Figure 12) and enter the name of the transfer function you are going to create. To add the file name, either you can click to browse or enter the entire path and name of the file. For additional details about the model, see "**About the General Purpose 9 Block Model**" on page 27.

8 Create a Simulation Node as indicated in the diagram in Figure 13 below.

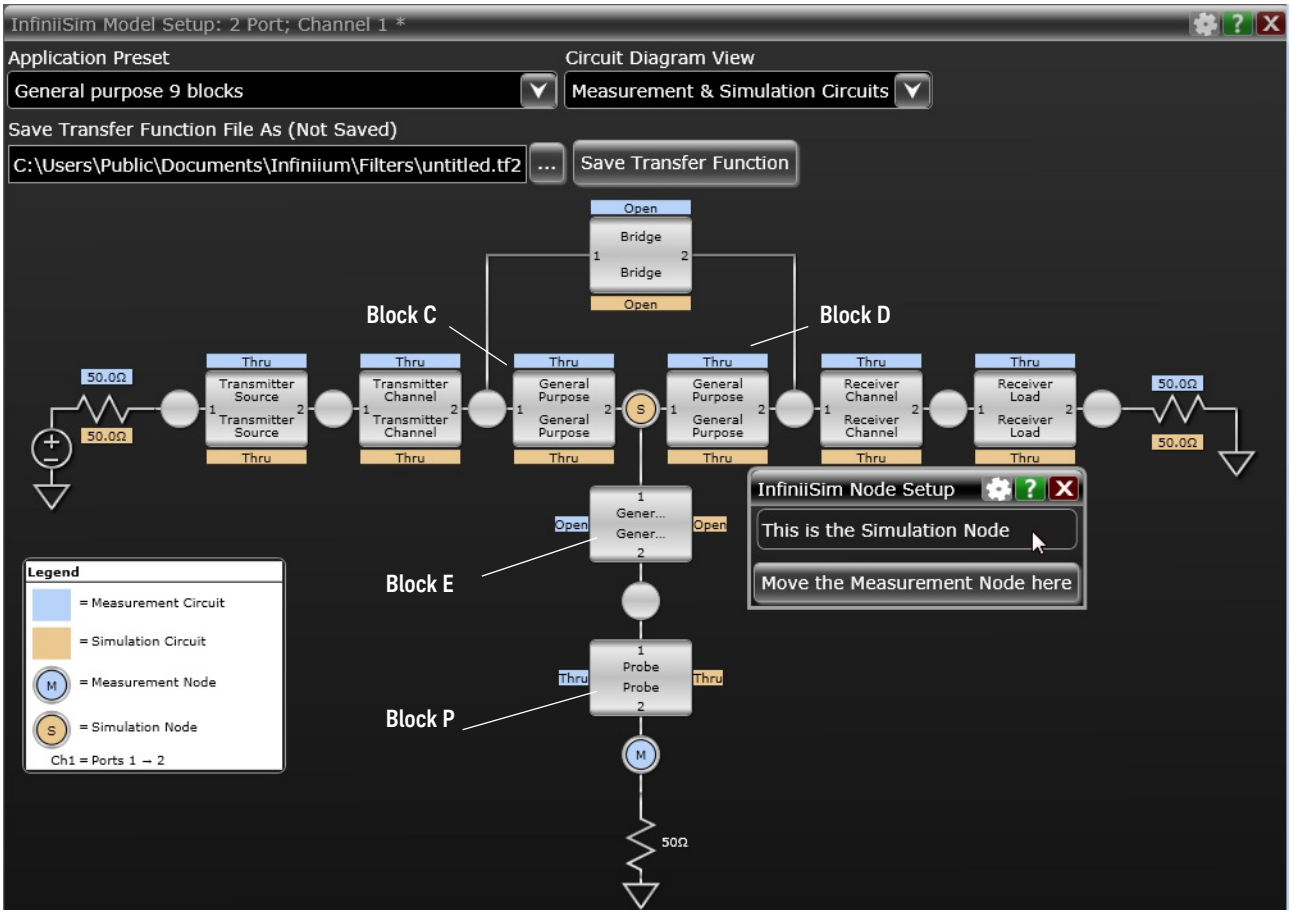


Figure 13 Simulation Node - 2 Port Channel 1

About the General Purpose 9 Block Model

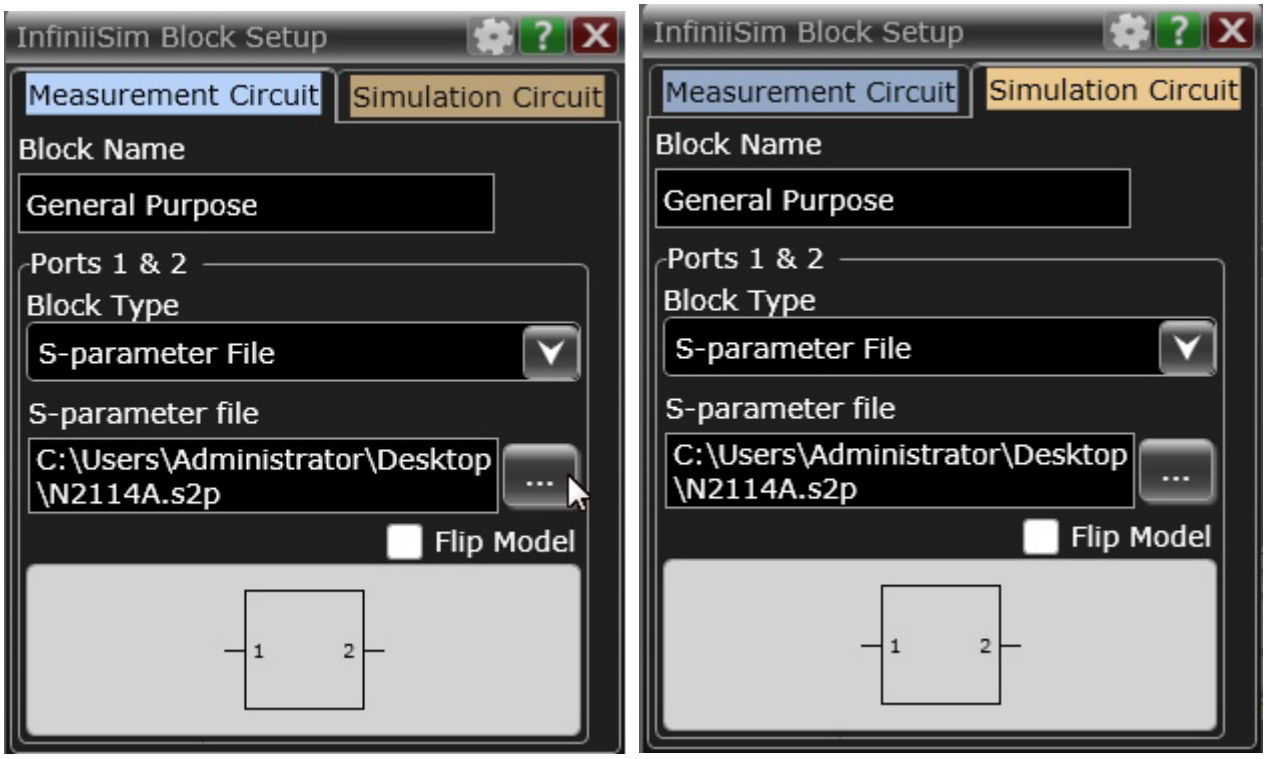
Almost any circuit can be defined in this model as it is the most extensive preset offered in InfiniiSim. Each block can be defined to be 3 separate blocks allowing up to 27 'blocks' to be described. A block is a shorthand description of circuit function or model for BOTH circuits described. The highlighted blue terms above each block describes the function in the Measurement Circuit while the descriptions in brown describe the function in the Simulation Circuit.The description can be as simple as an R, L, or C or as complex as an S-parameter file description. The blocks can be examined for their descriptions by clicking on them. In the above screen, not many of the blocks have been used. So their descriptions as thru's describes these as zero length, zero loss shorts, and therefore not influential in the analysis. You now need to make this diagram reflect the measurement and simulation circuits described earlier. The first step to perform is to move the simulation node to the via point by right clicking the node between blocks C and D and selecting <Simulation>.

Block E

This block has the S-parameter file for both measurement and simulation circuits. If you mouse hover 'Block E' you can see its default description as **opens**.

1 Double click on **Block E** to describe it.

2 The measurement description of **Block E** is displayed. Select **S-parameter File** and browse to the parameter file and repeat the process for the simulation circuit using the same file because you are simulating with the interposer in place (it is in both circuits).



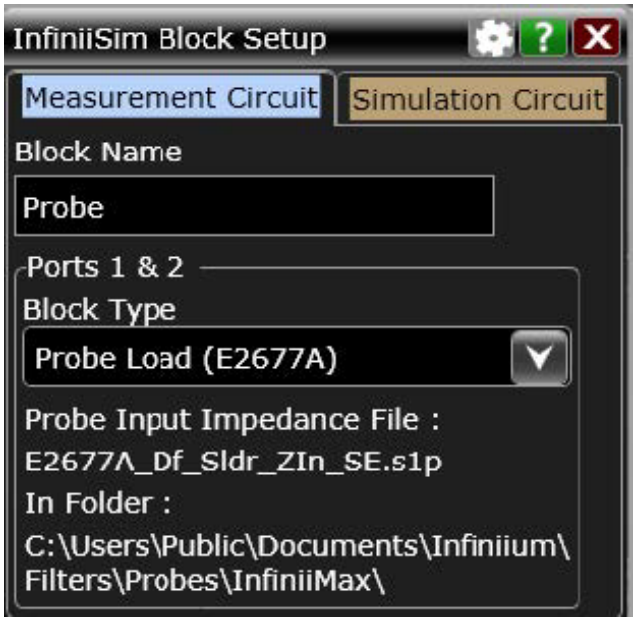
Measurement Circuit **Simulation Circuit**

Figure 14 Block E - 2 Port Channel 1- Measurement and Simulation Circuits

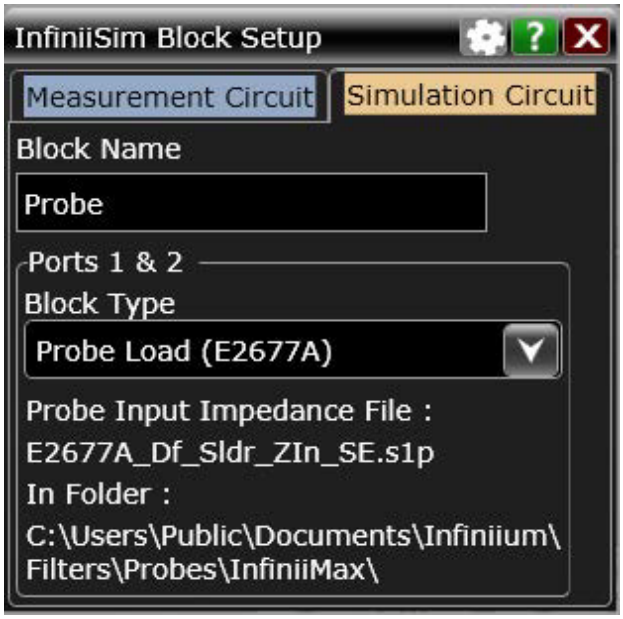
Block P

Block P describes the loading by presence of the probe used. You have selected the E2677A solder-in probe so you find that the software already provides you with the required model. Again, this probe model will be entered in both Simulation and Measurement circuits.

Now open **Block P** by double-clicking it. Note that the E2677A probe is already populated and you just need to select the Probe Load (E2677A) under the **Block Type**. Repeat for simulation circuit.



Measurement Circuit



Simulation Circuit

Figure 15 Block P- 2 Port Channel 1- Measurement and Simulation Circuits

Creating the Transfer Function

When you have completed the circuit descriptions, click the **Save Transfer Function** to calculate the transfer function. Common user errors in this step result from incompletely defined blocks (for example defined as a file with no file path given), or a block defined as an **Open** when between the measurement point and the source, or the simulation point and the source.

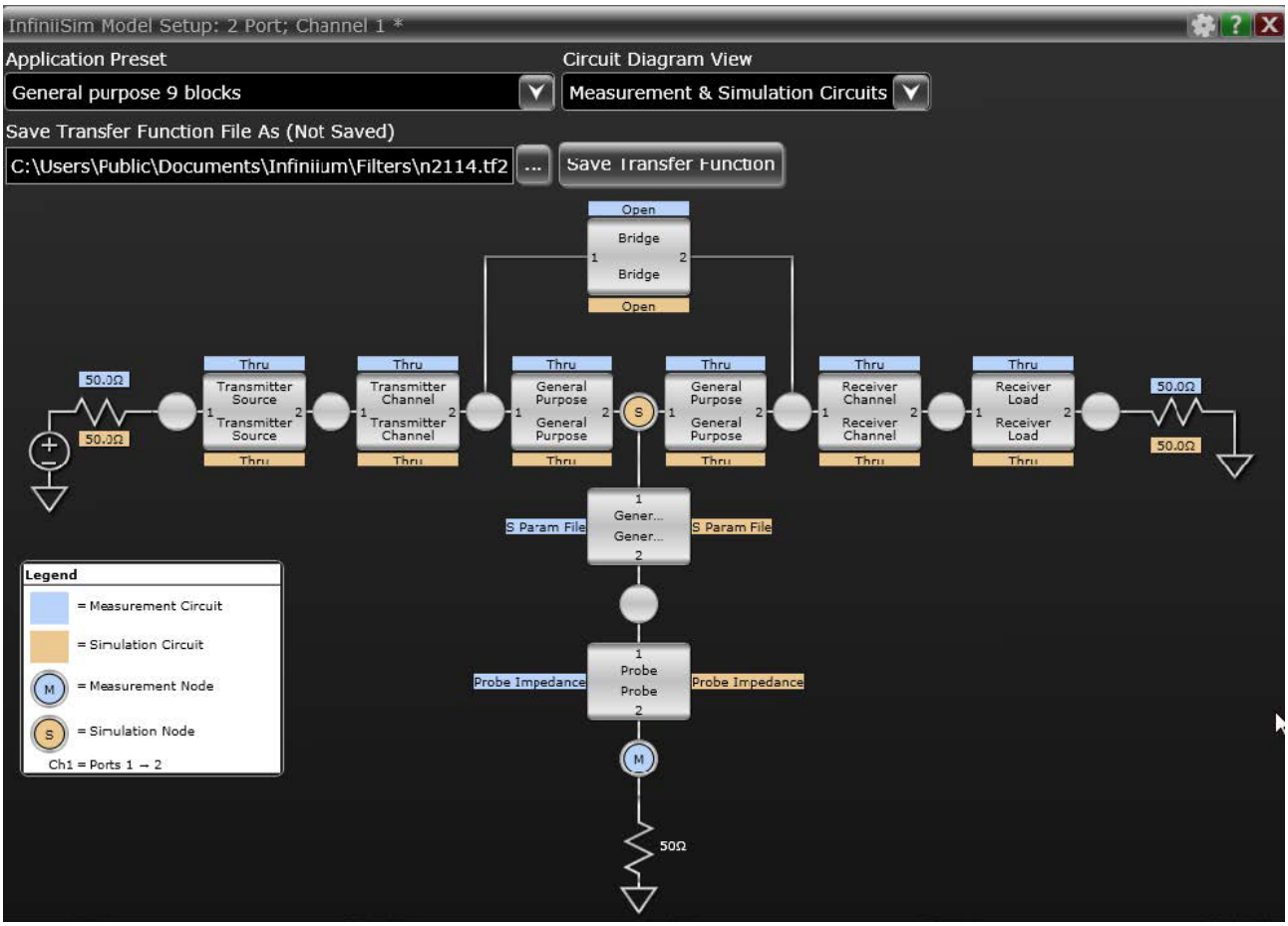


Figure 16 InfiniiSim Model Setup - 2 Port Channel 1- Save Transfer Function

Observe the transfer function

On successful completion of generating the transfer function it will be immediately applied to all subsequent acquisitions on the oscilloscope and you can look at its frequency and time responses. Before you do that, go back to **InfiniiSim Setup** screen and edit the Bandwidth Limit for the InfiniiSim transfer function. For the DDR4 interposer select 8 GHz. You might want to use full bandwidth (to the scope limit), but without having the required bandwidth may just decrease the signal to noise ratio.

Differential Measurements

This section describes how to create the transfer function to convert the probed measurement on the interposer pads to a simulated measurement at the via between the DRAM and the PC board for differential measurements such as for Clock (CK+ and CK-) or Data Strobe (Dqs+ and Dqs-). The result is a .tf4 file which the Infiniium oscilloscope family converts to an FIR filter to perform real time convolution to display the transformed acquisition.

Selecting the Probe

1 At the Infiniium oscilloscope screen, select **Channel 1** (or your target channel). The **Channel Setup** dialog is displayed as shown in Figure 17.

Figure 17 Channel Setup Dialog - 4 Port Channel 1

2 Select **4 Port (Channel 1)** in the InfiniiSim section at the bottom and before clicking **Setup**, click **Probe...**.button to set up the probe system appropriately.

Figure 18 Channel Setup - 4 Port (Channel 1)

NOTE The first 4 port selection would be the preferred choice if we were to have two single ended signals applied to the scope as we will use a differential probe we chose the latter.

3 On the **Probe Configuration Setup** screen, enter the probe and connection type (differential) In this example, the E2677A solder-in probe in differential mode has been selected.

4 After selection, close the **Probe Configuration Setup** screen and go back to **Channel Setup** screen (Figure 17) and click **Setup** under InfiniiSim pane.

5 On the **InfiniiSim Setup** dialog that appears, click the **Create Transfer Function from Model** button to initiate a transfer function.

NOTE The default transfer function file for 4 port analysis is .tf4 file.

Describing the Circuit in InfiniiSim

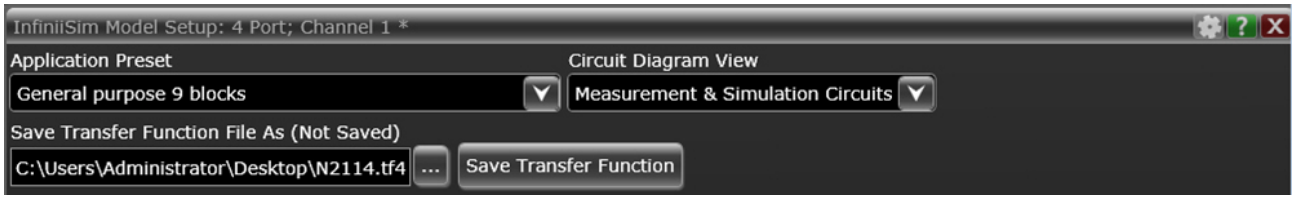


Figure 19 InfiniiSim Model Setup - 4 Port Channel 1- Save Transfer Function

6 On the **InfiniiSim Model Setup** screen, select the default configurations for your circuit description from the **Application Preset** drop-down menu (see Figure 19.)

7 Select **General purpose 9 blocks** from the drop-down menu and enter the name of the transfer function you are going to create. Relocate the simulation point by right clicking the node between blocks C and D and selecting <Simulation> as displayed in Figure 20 below. The previous comments made about the blocks and the rendering of Measurement Circuits and the Simulation Circuits applies. Note that the blocks are portrayed as 4 ports now.

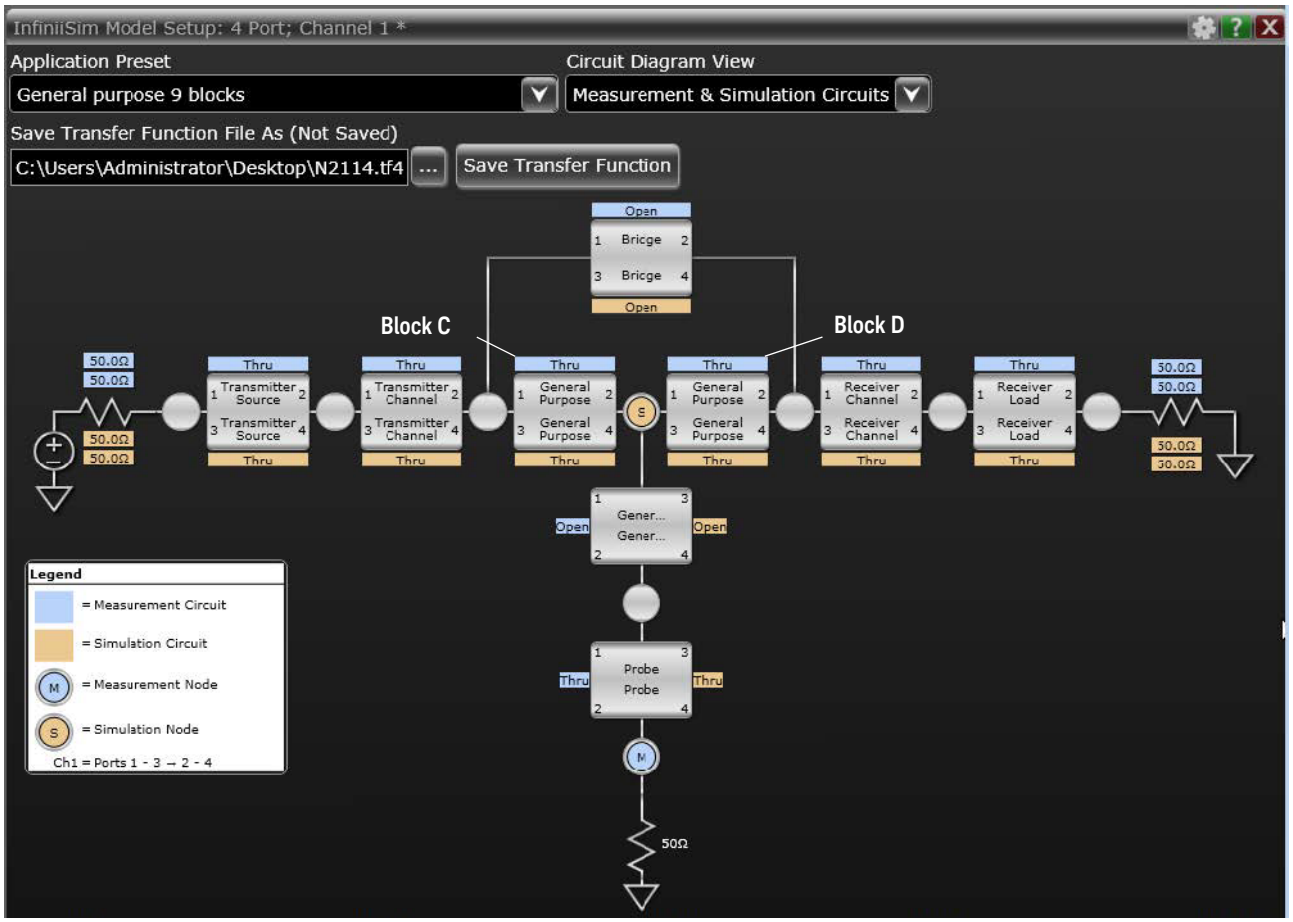


Figure 20 Simulation Node for 4 Port - Channel 1

In this example, the interposer **S-parameter** file in Block E and a probe model for Block P have been entered. Referring to circuits used in the example the nominal termination values for neither the memory controller, nor the DRAM were identified. These nominal resistances are described with the default 50Ω, however, if you know the actual nominal termination then you can enter the values by clicking on the labels. It may also be that you have a sophisticated package model as well for both the Memory controller and the DRAM; these would be entered in blocks T and R respectively. Each of these would be entered twice (once for the Measurement Circuit and then for the Simulation Circuit). The process to describe such blocks will now be shown by addressing blocks E and P.

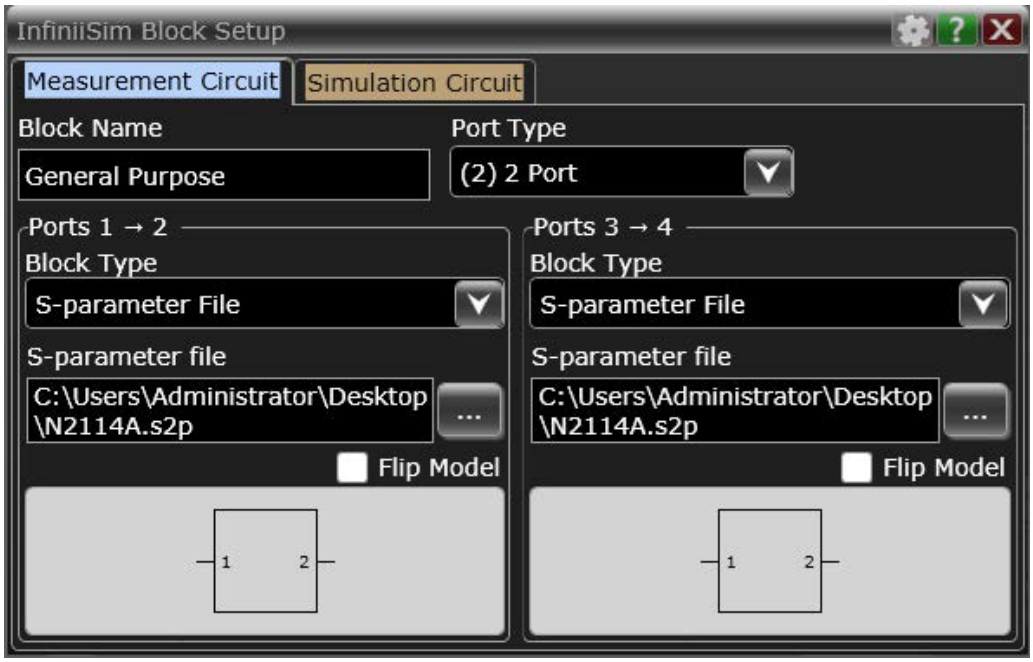
Block E

This block has the S-parameter file for both measurement and simulation circuits. If you select **Block E** you can see its default description as **thrus**.

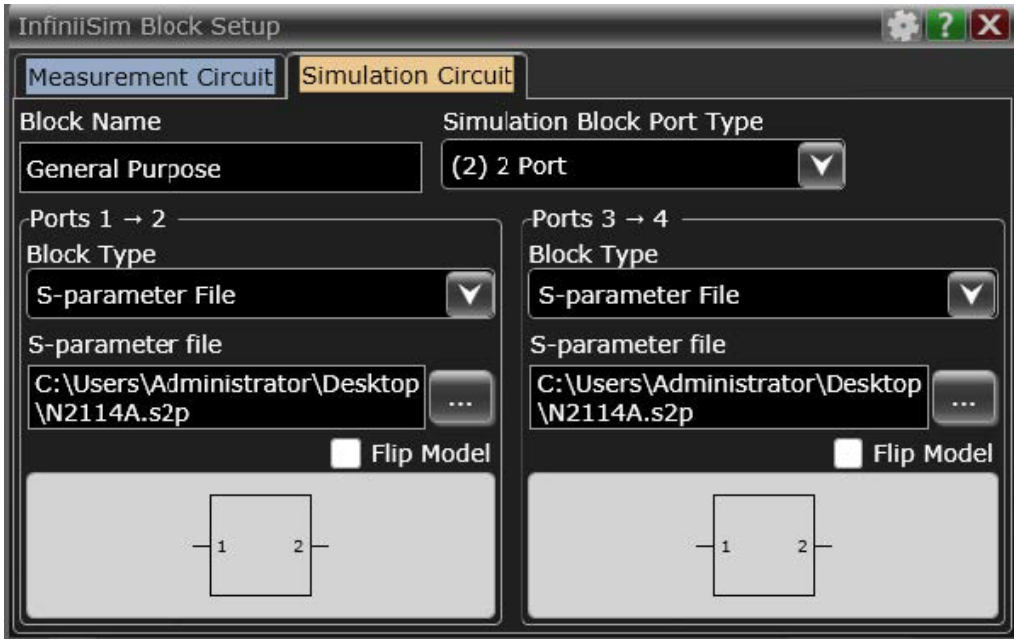
1 Double click on **Block E** to describe it.

2 In this case, the assumption is that the S-parameter file model we had of the interposer is valid for both paths AND that these paths are uncoupled.

3 From the **Port Type** drop-down menu, select **(2) 2 Port** which allows you to define a 4-port with two 2-ports, see Figure 21 in which 2-ports for the Measurement and Simulation circuits are defined.



Measurement Circuit



Simulation Circuit

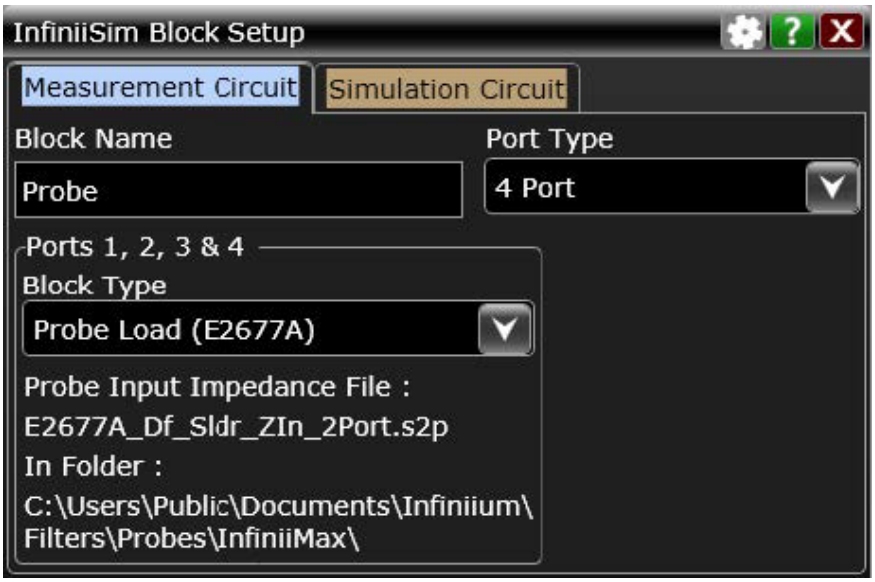
Figure 21 Block E - Simulation and Measurement Circuit- 4 Port Channel 1

When defining Block E as two 2 ports, the dialog box splits into two and allows definition of two separate paths. These reflect two separate paths from DDR pins to the differential probe connection. Because the design of the interposer layout emphasized that these have identical path lengths, it is reasonable to assume that the 2 port S parameter model define each path well. If different S-parameters were to define the two paths, you would put one S-parameter file on the Port 1->2 side and the other S parameter file on the Port 3->4 side for both Simulation and Measurement Circuit descriptions. Also, if there was a known skew (one path is longer than the other) between these paths, one S-parameter file could be used for both sides but one side could make use the 'Combination of Sub-Circuits' feature where one circuit element would be the S-parameter file, and a second circuit element could be a transmission line of the appropriate electrical length. If these paths were coupled, then 2 two port S-parameter modeling as we have done here, would not be appropriate and we should have a full 4 port measurement between the vias where the differential lines connect from the DRAM to the vias where the differential probe is connected. When finished with the measurement and simulation circuit descriptions, close the block setup and mouse hover the Block E in the ‘General Purpose 9 block’ model. The descriptions you have entered are shown.

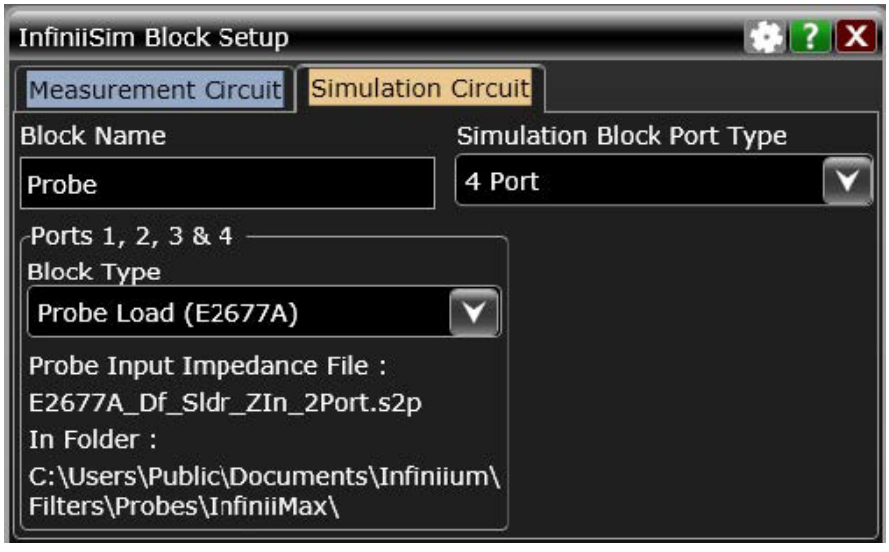
Block P

Block P describes the loading by presence of the probe used. You have selected the E2677A solder-in probe so you find that the software already provides you with the required model. Again, this probe model will be entered in both Simulation and Measurement circuits.

Now open **Block P** by double clicking it. Note that the E2677A probe is already populated and you just need to select the Probe Load (E2677A) under **Block Type**. Repeat for simulation circuit.



Measurement Circuit



Simulation Circuit

Figure 22 Block P- Simulation and Measurement Circuit - 4 Port Channel 1

Here you can see that both circuits are totally defined according to the circuit descriptions you developed in the beginning. As a point of interest for more advanced modeling, if actual circuit models were known for the source package and semiconductor models, PC board transmission line, and DRAM input, Block E's simulation model could be defined to be 'Open' to render true de-embedding of the interposer (the loading effects of the interposer would be removed).

Creating the Transfer Function

When you have completed the circuit descriptions, click the **Save Transfer Function** to calculate the transfer function. Common user errors in this step result from incompletely defined blocks (for example defined as a file with no file path given), or a block defined as an **Open** when between the measurement point and the source, or the simulation point and the source.

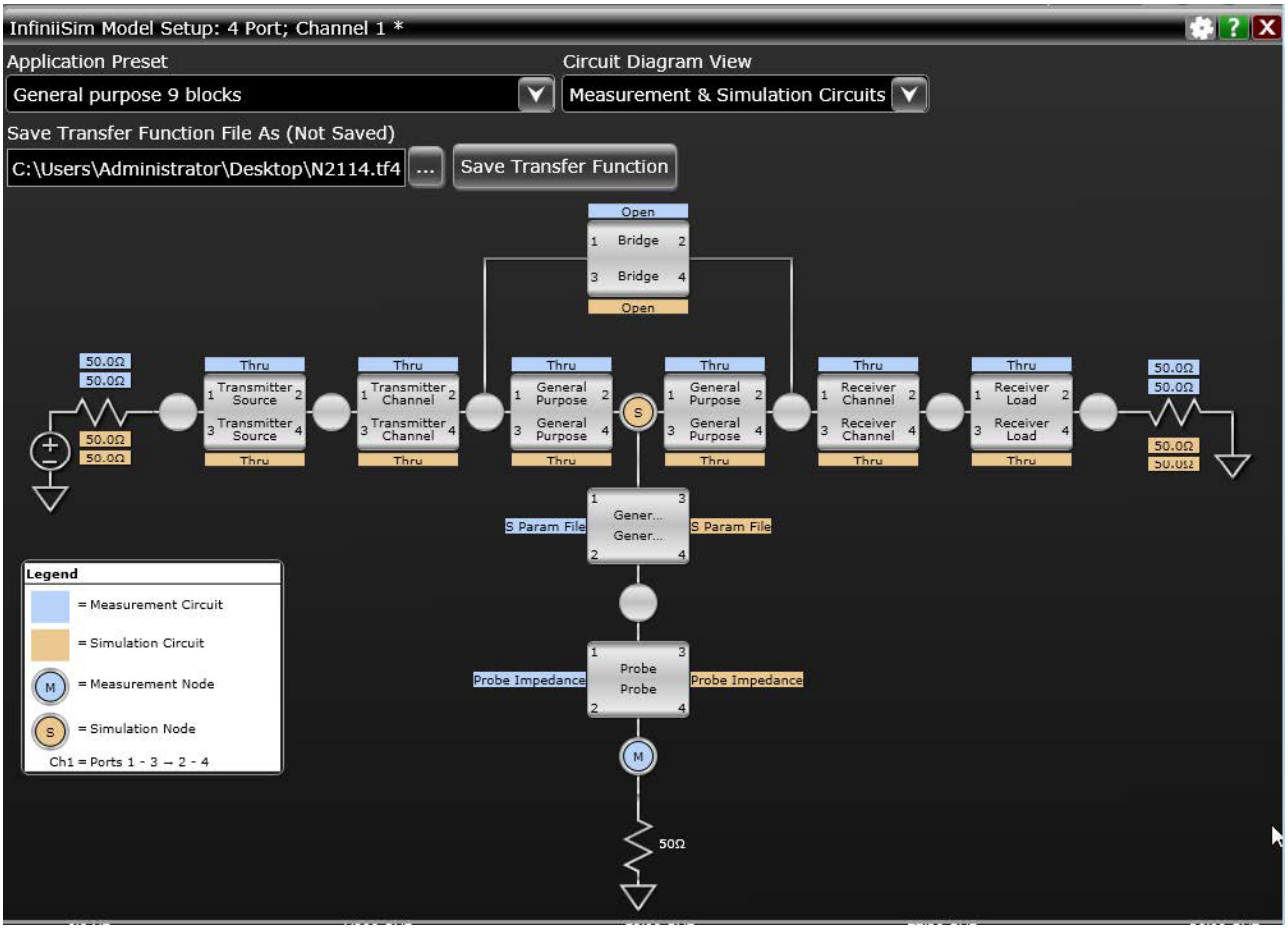


Figure 23 InfiniiSim Model Setup - 4 Port Channel 1- Save Transfer Function

Observe the transfer function

On successful completion of generating the transfer function it will be immediately applied to all subsequent acquisitions on the oscilloscope and you can look at its frequency and time responses. Before you do that, go back to **InfiniiSim Setup** screen and edit the Bandwidth Limit for the InfiniiSim transfer function. For the DDR4 interposer we select 8 GHz as we did before.

5 DDR4 BGA Interposer Load Model

N2114A Schematic and SPICE Deck

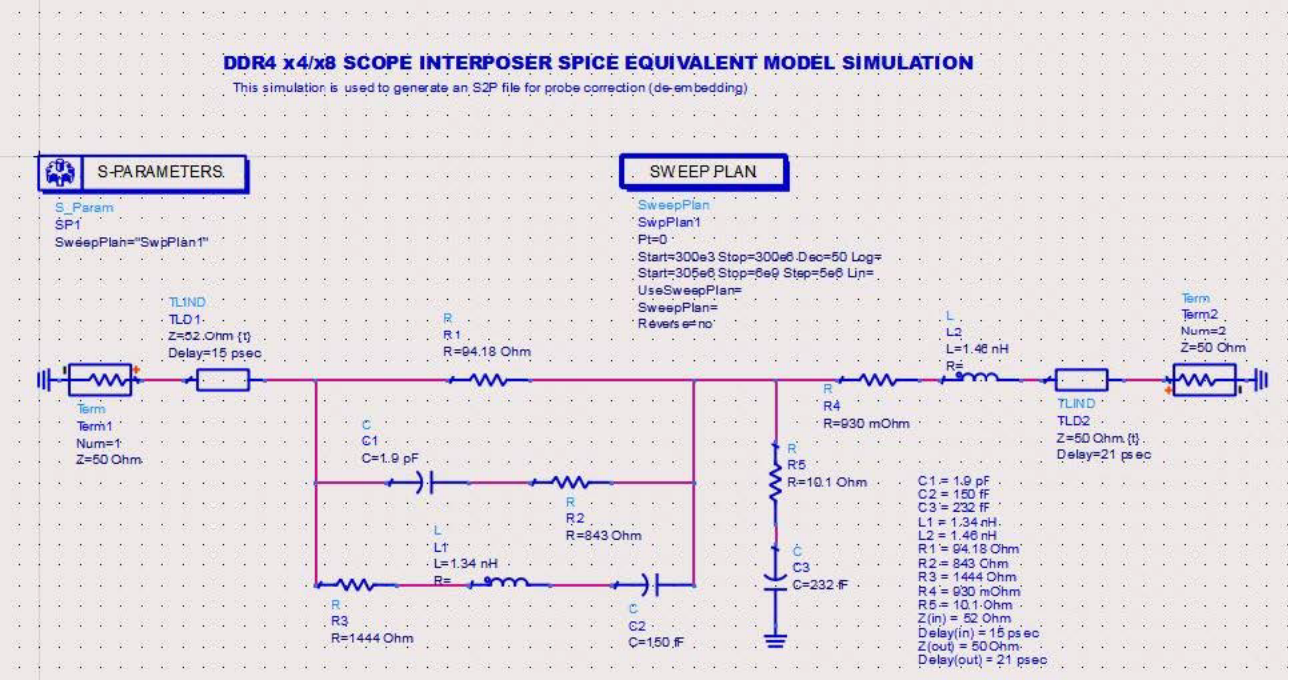


Figure 24 N2114A Schematic Diagram

N2114A SPICE Deck of Load Model

```
R1 %30 %32 94.18

C1 %30 %31 1.9e-12

R2 %31 %32 843

R3 %30 %33 1444

L1 %33 %34 1.34e-9

C2 %32 %34 150e-15

R5 %32 %37 10.1

C3 %37 %0 232e-15

R4 %32 %38 930e-3

L2 %38 %39 1.46e-9
```

```
T1 %vi %0 %30 %0 Zo=52 TD=15e-12

T2 %39 %0 %vo %0 Zo=50 TD=21e-12

    * DDR4 x4/x8 netlist
    * %vi is interposer input (BGA pad)
    * %vo is interposer output to solder-down probe tip
```

NOTE Loading depends on the solder down probe tip that is used. You need to cascade the SPICE model with the appropriate probe tip model to get the correct load model.

N2115A Schematic and SPICE Deck

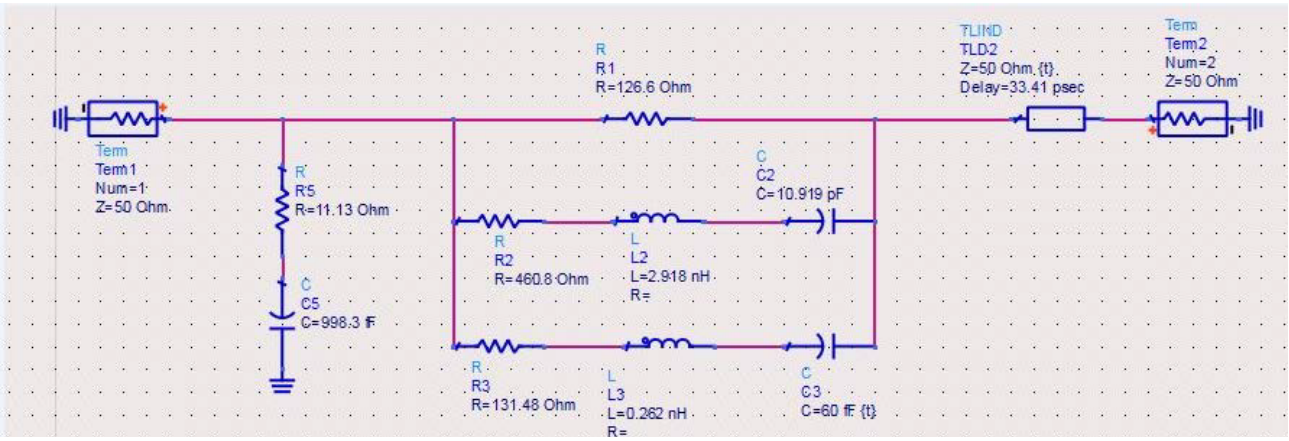


Figure 25 N2115A Schematic Diagram

```
R5 %vi %30 11.13

C5 %30 %0 998.3e-15

R1 %vi %31 126.6

R2 %vi %32 460.8

L2 %32 %33 2.918e-9

C2 %33 %31 10.919e-12

R3 %vi %34 131.48

L3 %34 %35 0.262e-9

C3 %35 %31 60e-15

T1 %31 %0 %vo %0 Zo=50 TD=33.41e-12
```

* DDR4 x16 netlist
* %vi is interposer input (BGA pad)
* %vo is interposer output to solder-down probe tip

6 Operating and Mechanical Characteristics

Operating Environment

The DDR4 Interposer is designed to operate in a temperature range of 0 to 70°C, non-condensing.

Mechanical Characteristics

Characteristic	Description
Flatness	0.2 mm
Shape and Dimension of the Signal Pad	Rectangular, 0.5 x 0.75 mm
Shape and Dimension of the Ground Pad	Circular, 0.5 mm diameter
All signal and ground solder-down test points around the perimeter of the Interposer have a via-in-pad of 0.28 mm diameter (+0.08/-0.28 mm) to assist in locating and maintaining a hand-held probe on the test point.	

Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

Use only the recommended power supply.

If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.

If it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.

Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do not install substitute parts or perform any unauthorized modification to the instrument.

Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

Do not use the instrument in a manner not specified by the manufacturer.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis

Regulatory Information