Keysight D9050PCIC PCIe Gen5 Compliance Application

KEYSIGHT TECHNOLOGIES

Programmer's Reference

Notices

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In This Book

This book is your guide to programming the Keysight Technologies D9050PCIC PCIe Gen5 Compliance Application.

- Chapter 1, “Introduction to Programming,” starting on page 7, describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 21, and Chapter 4, “Instruments,” starting on page 45 provide information specific to programming the D9050PCIC PCIe Gen5 Compliance Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, and 4 for changes.

Contents

1 Introduction to Programming

Remote Programming Toolkit / 8

This chapter introduces the basics for remote programming a compliance/test application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance/test app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance/test applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The D9050PCIC PCIe Gen5 Compliance Application uses Remote Interface Revision 6.30. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

2 Configuration Variables and Values

The following table contains a description of each of the D9050PCIC PCIe Gen5 Compliance Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Configure	Compliance Signal Check	EnableSignalCheck_16G	1.0, 0.0	When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Configure	Compliance Signal Check	EnableSignalCheck_2P5G	1.0, 0.0	When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Configure	Compliance Signal Check	EnableSignalCheck_32G	1.0, 0.0	When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Configure	Compliance Signal Check	EnableSignalCheck_5G	1.0, 0.0	When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Compliance Signal Check	EnableSignalCheck_8G	1.0, 0.0	When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Configure	Force New Waveform Acquisition	ForceNewWfmAcq	1.0, 0.0	When force new waveform acquisition is enabled, it will keep on re-acquire new waveform regardless of required waveform existed or not.
Configure	Gen 2 Ref Clock Transfer Function (Common Clock)	Gen2CommonRefClkTF	H1: 5MHz, 1.0dB peaking | H2: 16MHz, 3.0dB peaking, H1: 8MHz, 3.0dB peaking | H2: 16MHz, 3.0dB peaking	Select the transfer function for Gen 2 reference clock signal.
Configure	Noise Reduction BW, Hz	EBW_16G	(Accepts user-defined text), 50.0E+9, 25.0E+9, 20.0E+9, 16.0E+9	Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 16.0GHz to 63.0Hz.
Configure	Noise Reduction BW, Hz	EBW_2P5G	(Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9	Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 2.5GHz to 63.0Hz.
Configure	Noise Reduction BW, Hz	EBW_32G	(Accepts user-defined text), 50.0E+9, 33.0E+9	Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 32.0GHz to 63.0Hz.
Configure	Noise Reduction BW, Hz	EBW_5G	(Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9	Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 5.0GHz to 63.0Hz.
Configure	Noise Reduction BW, Hz	EBW_8G	(Accepts user-defined text), 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9	Specify the noise reduction bandwidth to use for all tests. The acceptable range of bandwidth is from 8.0GHz to 63.0Hz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Number of UI	NumUI_16G	(Accepts user-defined text), 8.0E+6, 2.0E+6, 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Number of UI	NumUI_2P5G	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Number of UI	NumUI_32G	(Accepts user-defined text), 8.0E+6, 2.0E+6, 1.6E+6	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Number of UI	NumUI_5G	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Number of UI	NumUI_8G	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Number of UI	NumUI_RefClk	(Accepts user-defined text), 200.0E+3, 100.0E+3, 50.0E+3, 25.0E+3	This is the minimum number of unit intervals used in reference clock tests.
Configure	RefClk Noise Reduction BW	ClockEBW	0.0, 8.0E+9, 7.0E+9, 6.0E+9, 5.0E+9, 4.5E+9, 4.0E+9, 3.5E+9, 3.0E+9, 2.5E+9, 2.0E+9, 1.5E+9, 1.0E+9	Select the bandwidth to acquire reference clock signal.
Configure	Sample Rate, GSa/s	SRate_16G	160.0E+9, 80.0E+9, 256.0E+9, 128.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Sample Rate, GSa/s	SRate_2P5G	160.0E+9, 80.0E+9, 40.0E+9, 20.0E+9, 128.0E+9, 64.0E+9, 32.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Configure	Sample Rate, GSa/s	SRate_32G	160.0E+9, 80.0E+9, 256.0E+9, 128.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Configure	Sample Rate, GSa/s	SRate_5G	160.0E+9, 80.0E+9, 40.0E+9, 128.0E+9, 64.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Configure	Sample Rate, GSa/s	SRate_8G	160.0E+9, 80.0E+9, 40.0E+9, 256.0E+9, 128.0E+9, 64.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Configure	Show Jitter Filter Plot	ShowJitterFilterPlot	0, 2, 3, 4, 5	Select the clock jitter plot to display. Generating plots will increase test runtime.
Configure	SigTest Version	Base_SigTestVer16GT	(Accepts user-defined text), 4.0.46, 4.0.51	Specify the version of the SigTest for 16.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	SigTest Version	Base_SigTestVer2P5GT	(Accepts user-defined text), 4.0.46, 4.0.51	Specify the version of the SigTest for 2.5 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	SigTest Version	Base_SigTestVer32GT	(Accepts user-defined text), 4.0.46, 4.0.51	Specify the version of the SigTest for 32.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	SigTest Version	Base_SigTestVer5GT	(Accepts user-defined text), 4.0.46, 4.0.51	Specify the version of the SigTest for 5.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	SigTest Version	Base_SigTestVer8GT	(Accepts user-defined text), 4.0.46, 4.0.51	Specify the version of the SigTest for 8.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	SigTest Version	Preset_SigTestVer16GT	(Accepts user-defined text), 4.0.46, 4.0.51	Specify the version of the SigTest for 16.0 GT/s Base Transmitter Tests (Equalization Preset Test). Setting is defined according to Data Rate.
Configure	SigTest Version	Preset_SigTestVer32GT	(Accepts user-defined text), 4.0.46, 4.0.51	Specify the version of the SigTest for 32.0 GT/s Base Transmitter Tests (Equalization Preset Test). Setting is defined according to Data Rate.
Configure	SigTest Version	Preset_SigTestVer8GT	(Accepts user-defined text), 4.0.46, 4.0.51	Specify the version of the SigTest for 8.0 GT/s Base Transmitter Tests (Equalization Preset Test). Setting is defined according to Data Rate.
Configure	Sine(x)/x Interpolation	SineXInterpolation	ON, OFF, INT1, INT2, INT4	Sine(x)/x Interpolation. If "Use Real Edge Connection" is enabled, interpolation will be set to OFF since Real-Edge connection already uses a high sample rate of 160Gsa/s.
Configure	Use Real Edge Connection	UseRealEdgeConnection	Enabled, Disabled	Use the Real Edge Channels when performing tests for 32GT/s data rate. By default Real-Edge Connection will be disabled.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 99	Specify N using the 'Minimum required margin %' control.
Set Up	All CTLE Embedding	CTLEAlldB	0.0, 1.0	Enable/disable All CTLE Embedding.
Set Up	CTLE 10dB Embedding	CTLE10dB	0.0, 1.0	Enable CTLE 10dB Embedding.
Set Up	CTLE 11dB Embedding	CTLE11dB	0.0, 1.0	Enable CTLE 11dB Embedding.
Set Up	CTLE 12dB Embedding	CTLE12dB	0.0, 1.0	Enable CTLE 12dB Embedding.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	CTLE 13dB Embedding	CTLE13dB	0.0, 1.0	Enable CTLE 13dB Embedding.
Set Up	CTLE 14dB Embedding	CTLE14dB	0.0, 1.0	Enable CTLE 14dB Embedding.
Set Up	CTLE 15dB Embedding	CTLE15dB	0.0, 1.0	Enable CTLE 15dB Embedding.
Set Up	CTLE 5dB Embedding	CTLE5dB	0.0, 1.0	Enable CTLE 5dB Embedding.
Set Up	CTLE 6dB Embedding	CTLE6dB	0.0, 1.0	Enable CTLE 6dB Embedding.
Set Up	CTLE 7dB Embedding	CTLE7dB	0.0, 1.0	Enable CTLE 7dB Embedding.
Set Up	CTLE 8dB Embedding	CTLE8dB	0.0, 1.0	Enable CTLE 8dB Embedding.
Set Up	CTLE 9dB Embedding	CTLE9dB	0.0, 1.0	Enable CTLE 9dB Embedding.
Set Up	Connection Type	OptConnectionType	Single-Ended	Select Connection Type.
Set Up	Device Directory	OfflineDeviceDirectoryName	New Device1	Available directories to run Analyze Captured Waveforms operation.
Set Up	Device Name	DeviceName	(Accepts user-defined text)	Name for the DUT in testing.
Set Up	DevicePCIERev	DevicePCIERev	PCIE 4.0, PCIE 5.0	Select the PCI Express device specification to use.
Set Up	Enable Collective Data Acquisition	PresetWfmCollectiveAcqConfigVar	0.0, 1.0	Enable Collective Data Acquisition.
Set Up	Enable DUT Automation	DUT Automation	0.0, 1.0	Enable DUT Automation.
Set Up	Enable Workshop Compliance Mode	Workshop Compliance Mode	0.0, 1.0	Enable Workshop Compliance Mode.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Perform Done operation to apply all setting changes.	DoneConnectionSetupConfigVar	1	This button is required to click/set in order to apply on all the settings have been set in this Connection Setup window. Perform Done operation to apply all setting changes.
Set Up	Perform Done operation to apply all setting changes.	DoneDeviceDefConfigVar	1	This button is required to click/set in order to apply on all the settings have been set in this Device Definition window. Perform Done operation to apply all setting changes.
Set Up	Saved Files Directory	SavedFilesDirectory	(Accepts user-defined text)	Directory to save output files from Workshop Mode Test.
Set Up	Select 16.0 GT/s related tests	16.0 GT/s	0.0, 1.0	Select 16.0 GT/s related tests.
Set Up	Select 2.5 GT/s related tests	2.5 GT/s	0.0, 1.0	Select 2.5 GT/s related tests.
Set Up	Select 32.0 GT/s related tests	32.0 GT/s	0.0, 1.0	Select 32.0 GT/s related tests.
Set Up	Select 5.0 GT/s related tests	5.0 GT/s	0.0, 1.0	Select 5.0 GT/s related tests.
Set Up	Select 8.0 GT/s related tests	8.0 GT/s	0.0, 1.0	Select 8.0 GT/s related tests.
Set Up	Select De-Emphasis -3.5dB for data speed 5GT/s	DeEmphasis3P5dBConfigVar	0.0, 1.0	Select De-Emphasis -3.5dB for data speed 5GT/s Select De-Emphasis -3.5dB for data speed 5GT/s
Set Up	Select De-Emphasis -6.0dB for data speed 5GT/s	DeEmphasis6P0dBConfigVar	0.0, 1.0	Select De-Emphasis -6.0dB for data speed 5GT/s Select De-Emphasis -6.0dB for data speed 5GT/s
Set Up	Select Lane 0	Lane0	0.0, 1.0	Select Lane 0 Select Lane 0
Set Up	Select Lane 1	Lane1	0.0, 1.0	Select Lane 1 Select Lane 1
Set Up	Select Lane 10	Lane10	0.0, 1.0	Select Lane 10 Select Lane 10
Set Up	Select Lane 11	Lane11	0.0, 1.0	Select Lane 11 Select Lane 11
Set Up	Select Lane 12	Lane12	0.0, 1.0	Select Lane 12 Select Lane 12

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Select Lane 13	Lane13	0.0, 1.0	Select Lane 13 Select Lane 13
Set Up	Select Lane 14	Lane14	0.0, 1.0	Select Lane 14 Select Lane 14
Set Up	Select Lane 15	Lane15	0.0, 1.0	Select Lane 15 Select Lane 15
Set Up	Select Lane 2	Lane2	0.0, 1.0	Select Lane 2 Select Lane 2
Set Up	Select Lane 3	Lane3	0.0, 1.0	Select Lane 3 Select Lane 3
Set Up	Select Lane 4	Lane4	0.0, 1.0	Select Lane 4 Select Lane 4
Set Up	Select Lane 5	Lane5	0.0, 1.0	Select Lane 5 Select Lane 5
Set Up	Select Lane 6	Lane6	0.0, 1.0	Select Lane 6 Select Lane 6
Set Up	Select Lane 7	Lane7	0.0, 1.0	Select Lane 7 Select Lane 7
Set Up	Select Lane 8	Lane8	0.0, 1.0	Select Lane 8 Select Lane 8
Set Up	Select Lane 9	Lane9	0.0, 1.0	Select Lane 9 Select Lane 9
Set Up	Select Switch Matrix.	optSwitchMatrix	No Switch Matrix, BitifEye BIT 2100, Keysight U3020A S26	Select SwitchMatrix.
Set Up	Select clock channel +	SingleEndedClockChannelPConfigVar	Channel-1, Channel-2, Channel-3, Channel-4	Select clock channel +.
Set Up	Select clock channel -	SingleEndedClockChannelNConfigVar	Channel-1, Channel-2, Channel-3, Channel-4	Select clock channel -.
Set Up	Select data channel +	SingleEndedDataChannelPConfigVar	Channel-1, Channel-2, Channel-3, Channel-4	Select data channel +.
Set Up	Select data channel -	SingleEndedDataChannelNConfigVar	Channel-1, Channel-2, Channel-3, Channel-4	Select data channel -.
Set Up	Select preset for 16.0 GT/s related tests	Preset16GConfigVar	(Accepts user-defined text), P00, P01, P02, P03, P04, P05, P06, P07, P08, P09, P10	Select preset for 16.0 GT/s related tests.
Set Up	Select preset for 32.0 GT/s related tests	Preset32GConfigVar	(Accepts user-defined text), P00, P01, P02, P03, P04, P05, P06, P07, P08, P09, P10	Select preset for 32.0 GT/s related tests.
Set Up	Select preset for 8.0 GT/s related tests	Preset8GConfigVar	(Accepts user-defined text), P00, P01, P02, P03, P04, P05, P06, P07, P08, P09, P10	Select preset for 8.0 GT/s related tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Select switching modules in BIT2100 Frame.	BIT2100Modules	2xSP4T, 2xSP6T, 2xSP8T	Select switching modules in BIT2100 Frame.
Set Up	Select the Power Level.	PowerLevelConfigVar	Full, Half	Select the Power Level.
Set Up	Select the Reference Clock Type.	RefClkConfigVar	Clean Clock, SSC	Select the Reference Clock Type.
Set Up	Select the SRIS type.	SRISEnabledConfigVar	None, Enabled	Select the SRIS type.
Set Up	Test Mode	OptTestMode	Analyze Captured Waveforms, Capture and Analyze Stored Waveforms	Select the test mode to be tested.
Set Up	Test Point	TestPoint	Base - Transmitter Tests, Base - Reference Clock Tests	Select the PCIExpress device test point to be tested.
Set Up	Test Point Preset Test	TestPointPresetTest	0.0, 1.0	Select to run Equalization Preset Tests.
Set Up	User Comment	UserComments	(Accepts user-defined text)	Additional comments for the DUT in testing. Additional comments for the DUT in testing.
*Limited availability: Availability of this setting depends upon the oscilloscope model and installed license options.				

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application. Listed at the end, you may also find:

- Deprecated IDs and their replacements.
- Macro IDs which may be used to select multiple related tests at the same time.

NOTE The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
Base Reference Clock Test (Workshop) (16.0 GT/s)	4049001	
Base Reference Clock Test (Workshop) (16.0 GT/s)	5049001	
Base Reference Clock Test (Workshop) (2.5 GT/s)	4019001	
Base Reference Clock Test (Workshop) (2.5 GT/s)	5019001	
Base Reference Clock Test (Workshop) (32.0 GT/s)	5059001	
Base Reference Clock Test (Workshop) (5.0 GT/s)	4029001	
Base Reference Clock Test (Workshop) (5.0 GT/s)	5029001	
Base Reference Clock Test (Workshop) (8.0 GT/s)	4039001	
Base Reference Clock Test (Workshop) (8.0 GT/s)	5039001	
Base Tx Test - Workshop Mode Test (16.0 GT/s)	4049000	
Base Tx Test - Workshop Mode Test (16.0 GT/s)	5049000	
Base Tx Test - Workshop Mode Test (2.5 GT/s)	4019000	
Base Tx Test - Workshop Mode Test (2.5 GT/s)	5019000	
Base Tx Test - Workshop Mode Test (32.0 GT/s)	5059000	

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Base Tx Test - Workshop Mode Test (5.0 GT/s)	4029000	
Base Tx Test - Workshop Mode Test (5.0 GT/s)	5029000	
Base Tx Test - Workshop Mode Test (8.0 GT/s)	4039000	
Base Tx Test - Workshop Mode Test (8.0 GT/s)	5039000	
Reference Clock, Absolute Crossing Point Voltage	4014008	This test verifies that the absolute crossing point voltage of the reference clock single-ended waveforms is within the allowed range.
Reference Clock, Absolute Crossing Point Voltage	5014008	This test verifies that the absolute crossing point voltage of the reference clock single-ended waveforms is within the allowed range.
Reference Clock, Absolute Max Input Voltage	4014014	This test verifies that the absolute maximum input voltage of the reference clock is within the allowed range.
Reference Clock, Absolute Max Input Voltage	5014014	This test verifies that the absolute maximum input voltage of the reference clock is within the allowed range.
Reference Clock, Absolute Min Input Voltage	4014016	This test verifies that the absolute minimum input voltage of the reference clock is within the allowed range.
Reference Clock, Absolute Min Input Voltage	5014016	This test verifies that the absolute minimum input voltage of the reference clock is within the allowed range.
Reference Clock, Average Clock Period	4014004	This test verifies that the average clock period accuracy of the differential waveform is within the allowed range.
Reference Clock, Average Clock Period	5014004	This test verifies that the average clock period accuracy of the differential waveform is within the allowed range.
Reference Clock, Average Clock Period (32.0GT/s)	5054004	This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. This test is applicable for devices that support 32.0GT/s data speed.
Reference Clock, Average Clock Period (32.0GT/s, SRIS)	5054005	This test verifies that the average clock period accuracy of the differential waveform is within the allowed range. This test is applicable for devices that support 32.0GT/s speed with SRIS mode.
Reference Clock, Clock Frequency (Common Clk) (16.0 GT/s)	4044024	This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range.
Reference Clock, Clock Frequency (Common Clk) (8.0 GT/s)	4034024	This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range.
Reference Clock, Differential Input High Voltage	4014006	This test verifies that the high voltage of the reference clock differential waveform is greater than the minimum allowed value.
Reference Clock, Differential Input High Voltage	5014006	This test verifies that the high voltage of the reference clock differential waveform is greater than the minimum allowed value.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Reference Clock, Differential Input Low Voltage	4014007	This test verifies that the low voltage of the reference clock differential waveform is greater than the maximum allowed value.
Reference Clock, Differential Input Low Voltage	5014007	This test verifies that the low voltage of the reference clock differential waveform is greater than the maximum allowed value.
Reference Clock, Duty Cycle	4014005	This test verifies that the duty cycle of the reference clock differential waveform is within the allowed range.
Reference Clock, Duty Cycle	5014005	This test verifies that the duty cycle of the reference clock differential waveform is within the allowed range.
Reference Clock, Falling Edge Rate	4014003	This test verifies that the falling edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.
Reference Clock, Falling Edge Rate	5014003	This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.
Reference Clock, Max SSC df/dt	5014021	This test verifies that the reference clock maximum SSC df/dt is within the allowed range.
Reference Clock, Peak to Peak Jitter (Common Clk) (2.5 GT/s)	5014011	This test verifies that the measured Peak to Peak jitter, TREFCLK-PP, is less than the maximum allowed value.
Reference Clock, Peak to Peak Jitter (Common Clk) (PCIE4 2.5 GT/s)	4014011	This test verifies that the measured Peak to Peak jitter, TREFCLK-PP, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (16.0 GT/s)	4044011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (16.0 GT/s)	5044011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (32.0 GT/s)	5054011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (5.0 GT/s)	4024011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (5.0 GT/s)	5024011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)	4034011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)	5034011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, Rise-Fall Matching	4014018	This test verifies that the rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Reference Clock, Rise-Fall Matching	5014018	This test verifies that the rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching is within the allowed range.
Reference Clock, Rising Edge Rate	4014002	This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.
Reference Clock, Rising Edge Rate	5014002	This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.
Reference Clock, SSC deviation	5014020	This test verifies that the reference clock SSC deviation is within the allowed range.
Reference Clock, SSC deviation (Common Clk) (16.0 GT/s)	4044020	This test verifies that the reference clock SSC deviation is within the allowed range.
Reference Clock, SSC deviation (Common Clk) (5.0 GT/s)	4024020	This test verifies that the reference clock SSC deviation is within the allowed range.
Reference Clock, SSC deviation (Common Clk) (8.0 GT/s)	4034020	This test verifies that the reference clock SSC deviation is within the allowed range.
Reference Clock, SSC frequency range	5014019	This test verifies that the reference clock SSC frequency is within the allowed range.
Reference Clock, SSC frequency range (Common Clk) (16.0 GT/s)	4044019	This test verifies that the reference clock SSC frequency is within the allowed range.
Reference Clock, SSC frequency range (Common Clk) (5.0 GT/s)	4024019	This test verifies that the reference clock SSC frequency is within the allowed range.
Reference Clock, SSC frequency range (Common Clk) (8.0 GT/s)	4034019	This test verifies that the reference clock SSC frequency is within the allowed range.
Reference Clock, Variation of VCross	4014010	This test verifies that the variation of VCross over all rising clock edges is within the allowed range.
Reference Clock, Variation of VCross	5014010	This test verifies that the variation of VCross over all rising clock edges is within the allowed range.
Tx, AC common mode voltage - 1.25GHz (LPF) (2.5 GT/s)	5011026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 16GHz (LPF) (32.0 GT/s)	5051026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 2.5GHz (LPF) (5.0 GT/s)	4021026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, AC common mode voltage - 2.5GHz (LPF) (5.0 GT/s)	5021026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (16.0 GT/s)	4041027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (16.0 GT/s)	5041027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (32.0 GT/s)	5051027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (5.0 GT/s)	4021027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (5.0 GT/s)	5021027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (8.0 GT/s)	4031027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (8.0 GT/s)	5031027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 4GHz (LPF) (8.0 GT/s)	5031026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 4GHz (LPF) (8.0 GT/s)	4031026	This test verify the AC common mode, VTX-CM-AC-PP (4GHz LPF) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 8GHz (LPF) (16.0 GT/s)	4041026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, AC common mode voltage - 8GHz (LPF) (16.0 GT/s)	5041026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, Absolute delta of DC common mode voltage between D+ and D- (16.0 GT/s)	4041028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (16.0 GT/s)	5041028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (2.5 GT/s)	5011028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (32.0 GT/s)	5051028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (5.0 GT/s)	5021028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (8.0 GT/s)	4031028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (8.0 GT/s)	5031028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (16.0 GT/s)	4041029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Absolute delta of DC common mode voltage during L0 and Idle (16.0 GT/s)	5041029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (2.5 GT/s)	5011029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (32.0 GT/s)	5051029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (5.0 GT/s)	4021029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (5.0 GT/s)	5021029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (8.0 GT/s)	4031029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (8.0 GT/s)	5031029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Avg DC Common Mode Output Voltage (2.5 GT/s)	4011025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, Avg DC common mode voltage (5.0 GT/s)	4021025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, DC Common Mode Line Delta (2.5 GT/s)	4011028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, DC Common Mode Line Delta (5.0 GT/s)	4021028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, DC common mode voltage (16.0 GT/s)	4041025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (16.0 GT/s)	5041025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (2.5 GT/s)	5011025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (32.0 GT/s)	5051025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (5.0 GT/s)	5021025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (8.0 GT/s)	4031025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (8.0 GT/s)	5031025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, Data dependent jitter (16.0 GT/s)	4041016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (16.0 GT/s)	5041016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (2.5 GT/s)	4011016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (2.5 GT/s)	5011016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (32.0 GT/s)	5051016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (5.0 GT/s)	4021016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (5.0 GT/s)	5021016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Data dependent jitter (8.0 GT/s)	4031016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (8.0 GT/s)	5031016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, De-emphasis Preset #0 (16.0 GT/s)	4041100	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #0 (16.0 GT/s)	5041100	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #0 (32.0 GT/s)	5051100	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #0 (8.0 GT/s)	4031100	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #0 (8.0 GT/s)	5031100	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (16.0 GT/s)	4041101	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (16.0 GT/s)	5041101	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (32.0 GT/s)	5051101	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (8.0 GT/s)	4031101	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (8.0 GT/s)	5031101	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #10 (16.0 GT/s)	4041111	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #10 (16.0 GT/s)	5041111	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, De-emphasis Preset #10 (32.0 GT/s)	5051111	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #10 (8.0 GT/s)	4031111	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #10 (8.0 GT/s)	5031111	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #2 (16.0 GT/s)	4041102	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #2 (16.0 GT/s)	5041102	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #2 (32.0 GT/s)	5051102	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #2 (8.0 GT/s)	4031102	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #2 (8.0 GT/s)	5031102	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #3 (16.0 GT/s)	4041103	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #3 (16.0 GT/s)	5041103	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #3 (32.0 GT/s)	5051103	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #3 (8.0 GT/s)	4031103	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #3 (8.0 GT/s)	5031103	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, De-emphasis Preset #7 (16.0 GT/s)	4041107	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (16.0 GT/s)	5041107	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (32.0 GT/s)	5051107	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (8.0 GT/s)	4031107	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (8.0 GT/s)	5031107	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (16.0 GT/s)	4041109	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (16.0 GT/s)	5041109	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (32.0 GT/s)	5051109	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (8.0 GT/s)	4031109	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (8.0 GT/s)	5031109	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Deemphasized Voltage Ratio (2.5 GT/s)	4011001	The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB.
Tx, Deemphasized Voltage Ratio (2.5 GT/s)	5011001	The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)	4021001	The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB.
Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)	5021001	The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -3.5dB.
Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)	4021002	The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -6dB.
Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)	5021002	The de-emphasis level is measured as the ratio of the non-transition voltage to transition voltage, VTX-DE-RATIO = -20log10 (VTX-DIFF-PP/VTX-DE-EMPH-PP). This measurement is for de-emphasis level settings of -6dB.
Tx, Deterministic DjDD uncorrelated PWJ (16.0 GT/s)	4041015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (16.0 GT/s)	5041015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (2.5 GT/s)	4011015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (32.0 GT/s)	5051015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (5.0 GT/s)	4021015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (5.0 GT/s)	5021015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s)	4031015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s)	5031015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Eye-Width (2.5 GT/s)	4011006	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (5.0 GT/s)	4021006	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Eye-Width (Low Power) (2.5 GT/s)	4011009	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Full swing Tx voltage with no TxEQ (16.0 GT/s)	4041010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (16.0 GT/s)	5041010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (32.0 GT/s)	5051010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (8.0 GT/s)	4031010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (8.0 GT/s)	5031010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Median to Max Jitter (2.5 GT/s)	4011005	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (Low Power) (2.5 GT/s)	4011008	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Min swing during EIEOS for full swing (16.0 GT/s)	4041019	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for full swing (16.0 GT/s)	5041019	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for full swing (32.0 GT/s)	5051019	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for full swing (8.0 GT/s)	4031019	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for full swing (8.0 GT/s)	5031019	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (16.0 GT/s, Low Power)	4041020	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (16.0 GT/s, Low Power)	5041020	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (32.0 GT/s, Low Power)	5051020	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (8.0 GT/s, Low Power)	4031020	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (8.0 GT/s, Low Power)	5031020	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s)	4011035	This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range.
Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s)	5011035	This test verifies that the Peak Differential Output Voltage (Non-Transition) is within the allowed range.
Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s, Low Power)	4011036	This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range.
Tx, Peak Differential Output Voltage (Non-Transition)(2.5 GT/s, Low Power)	5011036	This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range.
Tx, Peak Differential Output Voltage (Non-Transition)(5.0 GT/s, Low Power)	4021036	This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range.
Tx, Peak Differential Output Voltage (Non-Transition)(5.0 GT/s, Low Power)	5021036	This test verifies that the Peak Differential Output Voltage (Non-Transition) (Low Power) is within the allowed range.
Tx, Peak Differential Output Voltage (Transition) (5.0 GT/s, Low Power)	4021011	This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range.
Tx, Peak Differential Output Voltage (Transition) (5.0 GT/s, Low Power)	5021011	This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s)	4011010	This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s)	5011010	This test verifies that the Peak Differential Output Voltage (Transition) is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s, Low Power)	4011011	This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s, Low Power)	5011011	This test verifies that the Peak Differential Output Voltage (Transition) (Low Power) is within the allowed range.
Tx, Peak Differential Output Voltage -3.5dB (Non-Transition)(5.0 GT/s)	4021035	This test verifies that the Peak Differential Output Voltage -3.5dB (Non-Transition) is within the allowed range.
Tx, Peak Differential Output Voltage -3.5dB (Non-Transition)(5.0 GT/s)	5021035	This test verifies that the Peak Differential Output Voltage -3.5dB (Non-Transition) is within the allowed range.
Tx, Peak Differential Output Voltage -3.5dB (Transition) (5.0 GT/s)	4021010	This test verifies that the Peak Differential Output Voltage -3.5dB (Transition) is within the allowed range.
Tx, Peak Differential Output Voltage -3.5dB (Transition)(5.0 GT/s)	5021010	This test verifies that the Peak Differential Output Voltage -3.5dB (Transition) is within the allowed range.
Tx, Peak Differential Output Voltage -6.0dB (Non-Transition)(5.0 GT/s)	4021038	This test verifies that the Peak Differential Output Voltage -6.0dB (Non-Transition) is within the allowed range.
Tx, Peak Differential Output Voltage -6.0dB (Non-Transition)(5.0 GT/s)	5021038	This test verifies that the Peak Differential Output Voltage -6.0dB (Non-Transition) is within the allowed range.
Tx, Peak Differential Output Voltage -6.0dB (Transition) (5.0 GT/s)	4021037	This test verifies that the Peak Differential Output Voltage -6.0dB (Transition) is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Peak Differential Output Voltage -6.0dB (Transition)(5.0 GT/s)	5021037	This test verifies that the Peak Differential Output Voltage -6.0dB (Transition) is within the allowed range.
Tx, Preshoot Preset #5 (16.0 GT/s)	4041104	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #5 (16.0 GT/s)	5041104	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #5 (32.0 GT/s)	5051104	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #5 (8.0 GT/s)	4031104	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #5 (8.0 GT/s)	5031104	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #6 (16.0 GT/s)	4041105	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #6 (16.0 GT/s)	5041105	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #6 (32.0 GT/s)	5051105	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #6 (8.0 GT/s)	4031105	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #6 (8.0 GT/s)	5031105	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #7 (16.0 GT/s)	4041106	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #7 (16.0 GT/s)	5041106	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Preshoot Preset #7 (32.0 GT/s)	5051106	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #7 (8.0 GT/s)	4031106	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #7 (8.0 GT/s)	5031106	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #8 (16.0 GT/s)	4041108	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #8 (16.0 GT/s)	5041108	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #8 (32.0 GT/s)	5051108	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #8 (8.0 GT/s)	4031108	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #8 (8.0 GT/s)	5031108	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #9 (16.0 GT/s)	4041110	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #9 (16.0 GT/s)	5041110	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #9 (32.0 GT/s)	5051110	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #9 (8.0 GT/s)	4031110	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #9 (8.0 GT/s)	5031110	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Pseudo package loss, Non-Root Device (32.0 GT/s)	5051018	This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.
Tx, Pseudo package loss, Non-Root Device (8.0 GT/s)	4031018	This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.
Tx, Pseudo package loss, Non-Root Device (8.0 GT/s)	5031018	This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.
Tx, Pseudo package loss, Non-Root Device, Captive Channel (16.0 GT/s)	4041018	This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.
Tx, Pseudo package loss, Non-Root Device, Captive Channel (16.0 GT/s)	5041018	This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.
Tx, Pseudo package loss, Non-Root Device, No Captive Channel (16.0 GT/s)	4041031	This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.
Tx, Pseudo package loss, Non-Root Device, No Captive Channel (16.0 GT/s)	5041031	This test verifies that the maximum pseudo package loss for all devices without root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.
Tx, Pseudo package loss, Root Device (16.0 GT/s)	4041030	This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range.
Tx, Pseudo package loss, Root Device (16.0 GT/s)	5041030	This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Pseudo package loss, Root Device (32.0 GT/s)	5051030	This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.
Tx, Pseudo package loss, Root Device (8.0 GT/s)	5031030	This test verifies that the maximum pseudo package loss for all devices with root ports, ps21TX is within the allowed range. Pseudo package loss is calculated as ratio of voltage swing of a 1010 pattern against a 64-zeroes/64-ones pattern as described in Section 8.3.3.11.
Tx, Pseudo package loss, Root Device (8.0 GT/s)	4031030	This test verifies that the maximum pseudo package loss of all devices with root ports, ps21TX is within the allowed range.
Tx, RMS AC Peak Common Mode Output Voltage (2.5 GT/s)	4011033	The maximum allowable RMS AC (>30Khz) common mode voltage is 20mV (Vtx-cm-acp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, Random jitter (16.0 GT/s)	4041017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (16.0 GT/s)	5041017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (2.5 GT/s)	4011017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (32.0 GT/s)	5051017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (5.0 GT/s)	4021017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (5.0 GT/s)	5021017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (8.0 GT/s)	4031017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (8.0 GT/s)	5031017	This test verifies that the random jitter, it is informative only.
Tx, Reduced swing Tx voltage with no TxEQ (16.0 GT/s, Low Power)	4041011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (16.0 GT/s, Low Power)	5041011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (32.0 GT/s, Low Power)	5051011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (8.0 GT/s, Low Power)	4031011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (8.0 GT/s, Low Power)	5031011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 4.0 16.0GT/s)	4041024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 4.0 8.0GT/s)	4031024	This test verifies that the SSC maximum slew rate is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, SSC Df/Dt (Max)(PCIE 5.0 16.0GT/s)	5041024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 5.0 2.5GT/s)	5011024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 5.0 32.0GT/s)	5051024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 5.0 5.0GT/s)	5021024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 5.0 8.0GT/s)	5031024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Modulation Frequency (PCIE 4.0 16.0GT/s)	4041021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 4.0 8.0GT/s)	4031021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 5.0 16.0GT/s)	5041021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 5.0 2.5GT/s)	5011021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 5.0 32.0GT/s)	5051021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 5.0 5.0GT/s)	5021021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 5.0 8.0GT/s)	5031021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Peak Deviation (Max) (PCIE 4.0 16.0GT/s)	4041022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 4.0 8.0GT/s)	4031022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 5.0 16.0GT/s)	5041022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 5.0 2.5GT/s)	5011022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 5.0 32.0GT/s)	5051022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 5.0 5.0GT/s)	5021022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 5.0 8.0GT/s)	5031022	This test verifies that the SSC maximum deviation within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, SSC Peak Deviation (Min) (PCIE 4.0 16.0GT/s)	4041023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 4.0 8.0GT/s)	4031023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 16.0GT/s)	5041023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 2.5GT/s)	5011023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 32.0GT/s)	5051023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 5.0GT/s)	5021023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 8.0GT/s)	5031023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, Template Tests (2.5 GT/s)	4011004	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (Low Power) (2.5 GT/s)	4011007	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (Low Power) (5.0 GT/s)	4021007	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests -3.5dB (5.0 GT/s)	4021004	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests -6.0dB (5.0 GT/s)	4021032	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Total uncorrelated PWJ (16.0 GT/s)	4041014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (16.0 GT/s)	5041014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (2.5 GT/s)	4011014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (32.0 GT/s)	5051014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (5.0 GT/s)	4021014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (5.0 GT/s)	5021014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (8.0 GT/s)	4031014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Total uncorrelated PWJ (8.0 GT/s)	5031014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Uncorrelated deterministic jitter (16.0 GT/s)	4041013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (16.0 GT/s)	5041013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (2.5 GT/s)	4011013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (2.5 GT/s)	5011013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (32.0 GT/s)	5051013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (5.0 GT/s)	4021013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (5.0 GT/s)	5021013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (8.0 GT/s)	4031013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (8.0 GT/s)	5031013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated total jitter (16.0 GT/s)	4041012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (16.0 GT/s)	5041012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (2.5 GT/s)	4011012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (2.5 GT/s)	5011012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (32.0 GT/s)	5051012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (5.0 GT/s)	4021012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (5.0 GT/s)	5021012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (8.0 GT/s)	4031012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (8.0 GT/s)	5031012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Unit interval (16.0 GT/s)	4041000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification.
Tx, Unit interval (16.0 GT/s)	5041000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification.
Tx, Unit interval (2.5 GT/s)	4011000	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here.
Tx, Unit interval (2.5 GT/s)	5011000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification.
Tx, Unit interval (32.0 GT/s)	5051000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification.
Tx, Unit interval (5.0 GT/s)	4021000	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The mean recovered TX UI is reported here.
Tx, Unit interval (5.0 GT/s)	5021000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification.
Tx, Unit interval (8.0 GT/s)	4031000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 4-19 of the PCI Express Base Specification.
Tx, Unit interval (8.0 GT/s)	5031000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 6 Instrument Names

Instrument Name	Description
Infiniium	The primary oscilloscope

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