Keysight Technologies

Early Design Review of Boundary Scan in Enhancing Testability and Optimization of Test Strategy

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KEYSIGHT TECHNOLOGIES

Unlocking Measurement Insights

Early Design Review of Boundary Scan in Enhancing Testability and Optimization of Test Strategy

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How good is my product?

Is there a guiding principle to influence a good test?

YES

'Design For Test' in short... **DFT**

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What is 'Design For Test' or 'DFT'?

It is a concept that influences the design of a component or a system to facilitate in maximizing tests to diagnose maximum defects.

- Involves additional test circuitry added to designs
- Based on Boundary Scan Standard - IEEE 1149.1
- Test tools and methodologies maximizing defect detection

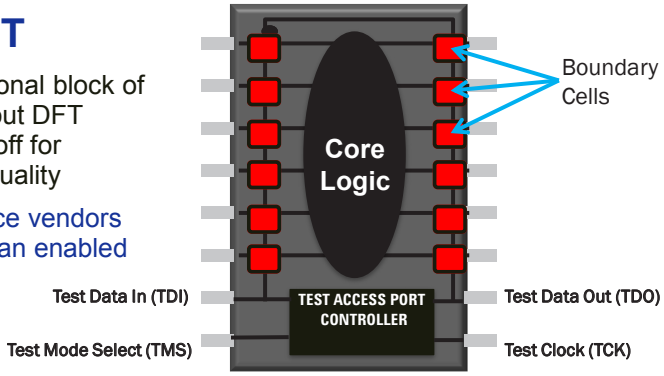
Where all can this concept of DFT span?

- Device level all the way to Systems

Device Level DFT

Device being the foundational block of a system, a well thought out DFT architecture always pays off for enabling determinism of quality

- Rising number of device vendors provided Boundary Scan enabled chip



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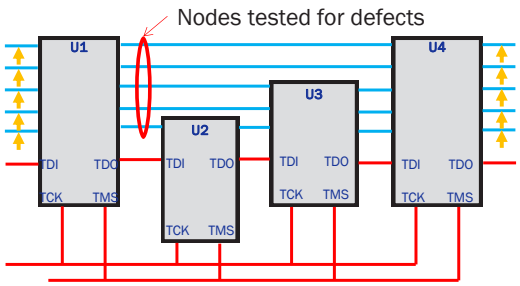
Device Level DFT – Defect Detection Between Devices Enabled with IEEE 1149.1

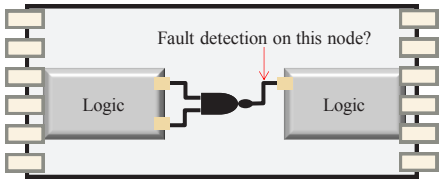
With basic implementation of IEEE 1149.1 enabled devices structural defects on boards arising on digital nodes interfacing with other devices can be detected

- Limits the defect detection to IOs on the devices
- Restricted to type of node interconnects on it



Device level DFT for defect detection inside the device?

- Basic implementation provides structural defect detection to IO interconnects on the devices
- What about defect detection inside the chip?



Basic Boundary Scan cells can be leveraged to enable fault detection on nodes inside the chips

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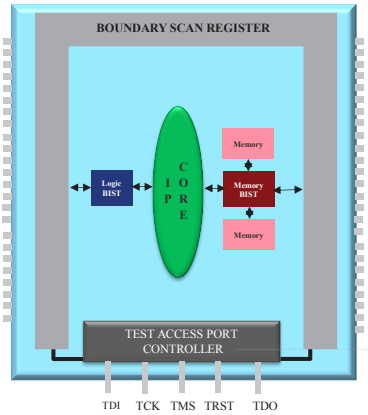
Device level DFT for defect detection inside the device - BIST

- Pattern based and scan based test architectures for

Device level DFT for defect detection inside the device - BIST



- Increase of System-On-Chip and System-In-Package designs necessitates an architecture for a flexible test methodology to be leveraged in multiple phases of the life cycle, ranging from chip test to system
- Provides flexibility to test at different phases and IPs can be re-used easily into different SOCs.
- Enabling DFT at a device will help in ensuring that the chips are defect free.
- New standards - IEEE 1687 and IEEE 1149.1-2013 standard cater to increasing the test logic within the chips.

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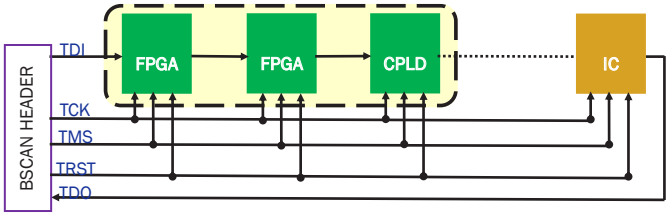
What are the elements needed to ensure a good Board Level DFT?

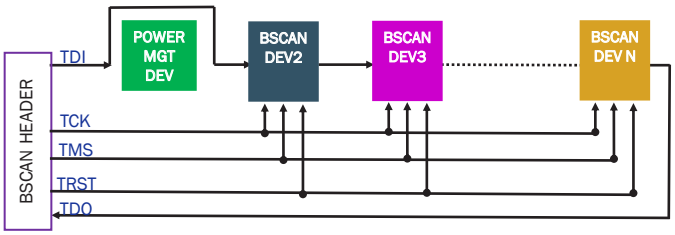
- First step is to choose IEEE 1149.X enabled device for the required functionality, if available.
- Design teams must qualify JTAG enabled parts to supplement into their functional requirements and specifications.
- Qualifying new devices compliant to IEEE 1149.1 standard by Procurement team facilitates an effective process for good DFT.
- Chain the devices with similar logic voltage together

Board Level DFT – Some Basic Good Practices

Devices of similar logic are chained together



Better to keep Power management ICs, out of the chain as it may affect stability of the board during the test.



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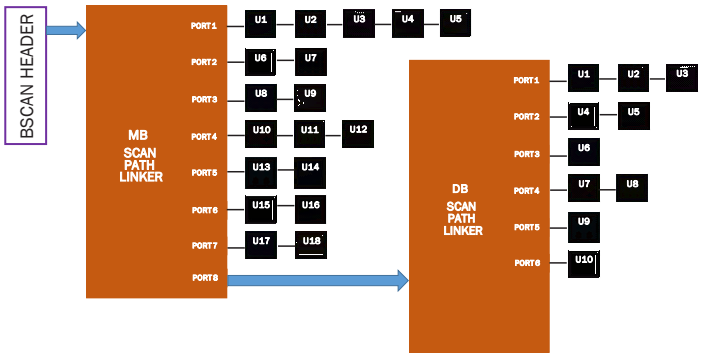
Board Level DFT – Good Practices

- On complex designs using a CPLD as a scan path linker, provides better management and flexibility of boundary scan chain in test.
- A scan path for each circuit (CPU block, Data Processing block, IO management, Memories, etc.) would help control the TAP signals independently.



Board Level DFT – Good Practices

- Dynamic configuration of system constituting multiple boards enables the boundary scan chain to be tested as a system once all the boards are stacked.
- Detects any defects resulting from Board-to-Board connector issues