

Keysight Technologies

Frequently Asked Questions

B4656A FPGA Dynamic Probe for Altera

Data Sheet

This document addresses common questions whose answers are not found in the B4656A

FAQ

The Keysight Technologies, Inc. FPGA dynamic probe provides greater real-time measurement productivity for logic analysis based validation of FPGAs and the surrounding system. The tool features:

- Increased visibility – Traditional logic analyzer probes limit engineers to measuring signals at the periphery of the FPGA. With Keysight's FPGA dynamic probe, engineers are able to measure up to 256 internal FPGA signals for each external FPGA pin dedicated to debug.
- Faster probing changes – Keysight's FPGA dynamic probe enables your design team to move probe points internal to the FPGA with a mouse click – without any design changes and without any changes to the timing of your design.
- Automatic setup of the logic analyzer – The FPGA dynamic probe maps internal signal names from your FPGA design tool to your logic analyzer. The signal-naming capability of the Keysight FPGA probe eliminates mistakes and saves you the time it would take to manually set up signal and bus names and logic analyzer connections, providing a significant advantage over logic analyzers without this capability.

The FPGA dynamic probe data sheet is available at www.keysight.com/find/FPGA.

Q1 What Altera Software is required to use Keysight's FPGA Dynamic Probe?

In addition to the B4656A FPGA dynamic probe option for your Keysight logic analyzer, you will need Altera's Quartus II FPGA Design Software, version 6.0 or higher. Quartus II includes Altera's Logic Analyzer Interface (LAI) that provides the MUX core and insertion mechanisms to enable FPGA dynamic probe. You will also need to install Altera's Quartus II Programmer Software on your Keysight logic analyzer to provide the necessary drivers for control of the Altera JTAG cable.

Q2 I already put my own MUXes in my FPGA design to better utilize debug pins. How is this solution better?

FPGA dynamic probe was designed to have minimal intrusion in both the design flow and the design itself. Here are the top areas where the FPGA dynamic probe solution will save you work and time, even if you already use your own MUXes.

1. FPGA dynamic probe does not require you to modify your HDL code. Altera's LAI Interface Editor lets you specify details of the MUX and automatically includes it in your FPGA. Teams not using FPGA dynamic probe must modify HDL code to include MUXes.
2. Control of which signals are presented for measurement is done from the logic analyzer in about a second (only 2 mouse clicks). Teams not using FPGA dynamic probe must design in special capability (such as changing register values) to change which signals are presented to IO pins.
3. With FPGA dynamic probe, signal names are imported from the FPGA Design Tools and automatically updated in the logic analyzer each time the user selects a new signal bank to measure. This saves considerable time and reduces errors over a manual process for making sure the MUX outputs are correctly reflected in the logic analyzer.

Q3 When would I want to use an LAI state core (synchronous) versus a timing (asynchronous) core?

State cores:

- Provide most-accurate measurements for functional debug in one time domain
- Register outputs to synchronize sampling data with your system's clock.

Timing cores:

- Are best for measurements across multiple time domains
- Run at fastest-possible speed of device, no registering of MUX inputs or outputs
- Have minimal impact on design timing

Q4 Can I use FPGA dynamic probe with multiple logic analyzers?

With option 010, the perpetual node locked license, the FPGA dynamic probe is licensed to the logic analyzer (1680 Series, 1690 Series, 16800 Series or 16900 Series). Multiple instances of the FPGA dynamic probe are supported so you can use a single license for all logic analysis modules in the system.

With option 020, the perpetual floating license, you have one instance of the FPGA dynamic probe that can be used by any 1680 Series, 1690 Series, 16800 Series or 16900 Series logic analyzer that has access to the license server.

Q5 Who do I contact if I'm having problems?

Altera provides the LAI Editor and core, including expertise on inserting the core into your design. Keysight's expertise is on the FPGA dynamic probe application. Keysight and Altera work together on issues that cross company boundaries.

Q6 What if I didn't assign all of the signals of interest early when I created the LAI core?

Altera supports incremental compilation in Quartus II with the Logic Analyzer Interface. This feature allows you to preserve the synthesis and fitting of your original design and add the LAI to your design without recompiling your original source code.

Q7 Can I use the FPGA dynamic probe application to download configuration bits into my Altera FPGA?

Yes.

Q8 What Altera JTAG cables work with FPGA dynamic probe?

Altera ByteBlaster, USB Blaster and MasterBlaster cables. The cable makes a connection between the parallel or USB port on the logic analyzer and the JTAG pins on the FPGA being measured.

Q9 Can I use a different clock on each bank or do I need a clock with each bank?

Timing cores do not have a clock, because information is sampled using the logic analyzer's internal clock. For state cores, the LAI core has a master clock that is used for all banks. Multiple LAI cores can be used for multiple clock domains. This requires a separate logic analyzer card or machine for each domain.

Q10 Can I put multiple LAI cores in a single device?

Yes. The FPGA dynamic probe application has been architected to support multiple cores in a single FPGA device. If the cores are state cores, each will need a clock from the design it is measuring.

Q11 Can I map two cores onto a single physical probe?

Yes. For example the first LAI core with 16 output pins could be mapped to the outside of a mictor connector with its corresponding clock. A second core with five output pins could be mapped to the even side of the same mictor connector. A separate logic analysis module is required to collect acquisition data for each core.

Q12 Which Altera FPGAs are supported?

The FPGA dynamic probe support all families that the Altera LAI core supports including: Stratix IV GX (where SOF* support is available), Stratix IV, Stratix III, Stratix II, and Stratix; Cyclone IV (where SOF* support is available), Cyclone III, Cyclone II, and Cyclone; Arria II and Arria *SOF is the SRAM Object File (.sof) that is generated in Quartus for a specific device.

Q13 What triggering resources are available with the FPGA dynamic probe?

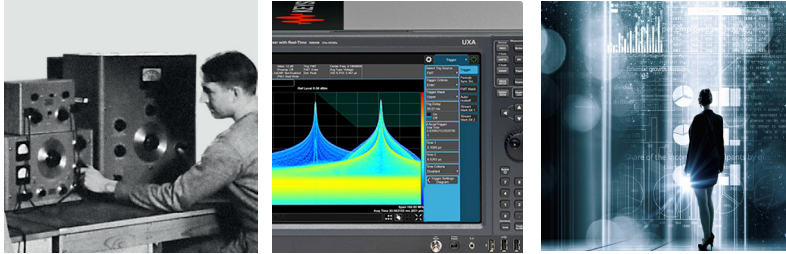
The full trigger resources of the Keysight logic analyzer being used are available.

Q14 What special pinouts are required by FPGA dynamic probe?

No special pinouts are required. The FPGA dynamic probe includes a graphical feature called pin mapping. This feature lets you visually tell the tool how the FPGA physical pins that carry the MUX output are connected to the logic analyzer. If you are using a traditional probing connection, such as a Mictor or Samtec connector, or a soft touch probe, the graphic lets you specify the location of each LAI output and which logic analysis cable is connected to this probe.

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