

Dynamic On-Resistance Measurement Technique for GaN Power Transistors

By Takamasa Arai – Keysight Solution Application Engineer, Ryo Takeda - Keysight Solution Architect, Bernhard Holzinger - Keysight Technical Architect, Michael Zimmerman - Keysight R&D Engineer, and Mike Hawes - Keysight Power Solution Consultant

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“Current collapse” behavior of GaN Power Transistors

While GaN power transistors are becoming popular in power electronics applications because of their low energy loss and high power density capability, design engineers still have some concerns about their reliability. One of the key concerns about GaN power transistors is their dynamic on-state resistance ($R_{DS(ON)}$) increase during switching operation, the phenomenon known as “current collapse”. Current collapse is the result of trapped electrons in the transistor structure when a high drain off-voltage is applied. It takes time to clear out the trapped electrons during a switch on event, which is characterized by the dynamic $R_{DS(ON)}$ measurement. Increased dynamic $R_{DS(ON)}$ degrades conduction loss of the GaN power transistors and leads to higher temperature, which affects reliability of the GaN power transistor and the system overall. Although many manufacturers provide “collapse-free” GaN power transistors, engineers are still concerned about the effect of the current collapse. Therefore, not only device manufacturers, but also power converter design engineers need to evaluate dynamic $R_{DS(ON)}$ of GaN power transistors accurately.

Challenges for dynamic ON-state resistance measurement

Many engineers are struggling to evaluate dynamic $R_{DS(ON)}$ accurately. There are two main reasons: 1) overdriving, and 2) the limitation in the oscilloscopes’ dynamic range.

When we measure dynamic $R_{DS(ON)}$, we would like to set the oscilloscope range just enough to monitor only on-state drain voltage ($V_{DS(ON)}$) such as 1V/div, giving us the best resolution from the oscilloscope. Unfortunately, the transistor is switching from high drain off-voltage ($V_{DS(OFF)}$) such as 400 V. The amplifiers in the oscilloscope distort the waveform if the measurement range is not wide enough to cover both $V_{DS(OFF)}$ and $V_{DS(ON)}$. This phenomenon is called “overdriving” of the oscilloscope [1] and results in saturated oscilloscope amplifiers and erroneous $V_{DS(ON)}$ measurements.

Therefore, we must set the oscilloscope range wide enough to capture both $V_{DS(OFF)}$ and $V_{DS(ON)}$ to avoid overdriving the input. However, the issue we come across this time is the limitation in the dynamic range of oscilloscopes. Even the high-end oscilloscopes, which have the highest vertical resolution in the market only have around nine effective number of bits (ENOB) at 20 MHz bandwidth (NOTE: In most cases, ENOB is the more useful parameter to use than the raw number of bits of the ADC in the oscilloscope. Often a few of the raw bits are below the noise floor of the amplifier, making them unusable). Therefore, the oscilloscope can only identify $1/2^9 = 1/512$ of full scale. If $V_{DS(OFF)}$ is 400 V, the minimum resolution will be $400/512 = 0.78$ V, which is completely unacceptable resolution for dynamic $R_{DS(ON)}$ measurements.

Keysight’s approach to measure dynamic $R_{DS(ON)}$

To overcome this and other challenges in testing GaN power transistors, Keysight developed a customized GaN test board to use with the PD1500A Dynamic Power Device Analyzer and Double Pulse Tester. To specifically overcome the limitation of the oscilloscope dynamic range, we developed a clamp circuit. Figure 1 shows our customized GaN test board. The newly developed clamp circuit is placed near the interface of the device under test (DUT). As we discussed in previous articles, the board also has Keysight’s solderless DUT interface, low insertion inductance current sensor, and replaceable gate resistors that we call Repeatable & Reliable GaN Characterization (R^2GC) Technologies.

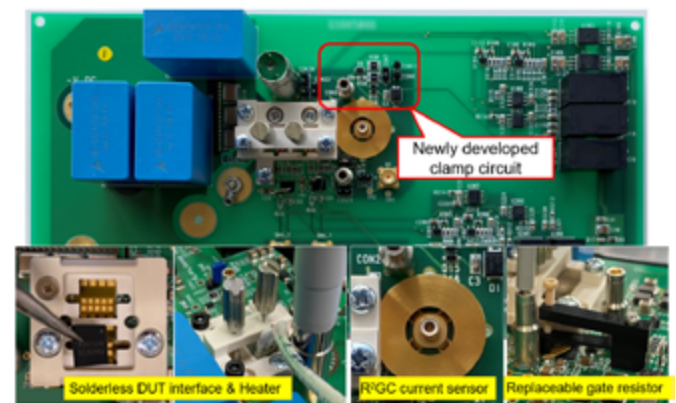


Figure 1: Keysight’s customized GaN test board with R^2GC technology.

Figure 2 shows a simplified concept of the clamp circuit. This circuit is placed in parallel to the output of the DUT. For example, assume the voltage threshold (V_{TH}) of Q1 is 2 V. If the Clamp Voltage is set to 8 V, then this circuit accurately measures the voltage V_{CLAMP} up to 6 V when the V_{DS} of the DUT is below 6 V. However, when V_{DS} is

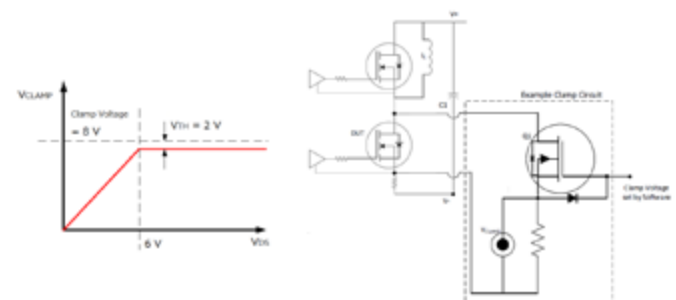


Figure 2: Simplified example of the clamp circuit.

above 6 V, then the system measures no more than 6 V. This means the oscilloscope can be set at a low-voltage range such as 1 V/div, which gives enough vertical resolution for dynamic $R_{DS(ON)}$ measurements. This test method using a clamp circuit is also suggested in JEDEC's publication JEP173 [2].



Figure 3: Turn-on switching waveform of a 650 V rating GaN E-HEMT obtained by the newly developed GaN test board with a clamped circuit.

We evaluated the performance of our customized GaN test board with a commercially available 650 V rating GaN E-HEMT (Enhancement mode High Electron Mobility Transistor). Figure 3 shows the turn-on waveforms of the GaN E-HEMT switching at $V_{DS(OFF)} = 400$ V, $I_{DS(ON)} = 30$ A. The yellow waveform shows clamped drain voltage

(V_{CLAMP}) and the brown line shows $R_{DS(ON)}$ calculated by V_{CLAMP}/I_{DS} using a 20 MHz low pass filter setting on the oscilloscope. The yellow waveform shows that the measured V_{DS} is clamped at around 4.5 V and that $V_{DS(ON)}$ around 2 V is clearly measured. Peak-to-peak noise of $R_{DS(ON)}$ waveform was around 1 m Ω (30 mV in terms of $V_{DS(ON)}$), which is much more precise than the original V_{DS} resolution of 0.78 V we discussed above and sufficient to evaluate dynamic $R_{DS(ON)}$ for most GaN power transistors.

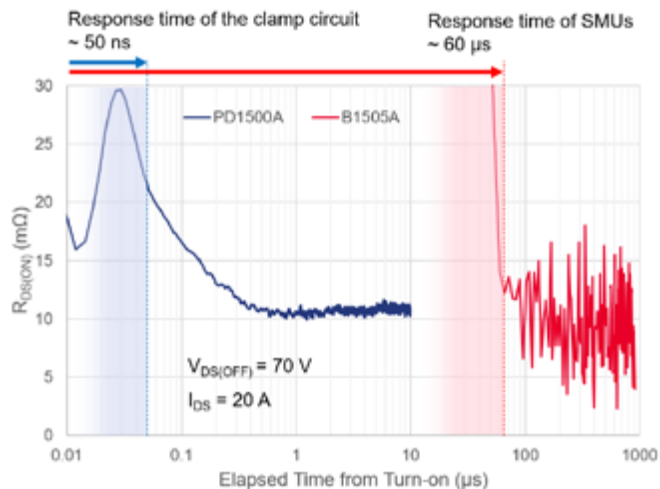


Figure 4: Measurement result of 100 V/10 m Ω GaN E-HEMT dynamic $R_{DS(ON)}$ obtained by both PD1500A (with the newly developed clamp circuit) and B1505A.

Another important characteristic for the clamp circuit is response time of the circuit. In typical power electronics applications like DC-DC converters, the switching frequency of the GaN power transistors is getting faster and faster and has become more than 1 MHz. That means the response time of the clamp circuit should be less than a few hundreds of nanoseconds to measure the dynamic $R_{DS(ON)}$ under practical operating conditions. The components of the clamp circuit like transistors and diodes intrinsically have a certain amount of junction capacitance and recovery characteristics that degrade the response time of the circuit. Therefore, getting fast response of the clamp circuit is another challenge.

Getting back to Figure 3, the clamped V_{DS} waveform (yellow) shows a negative dip for about 50 ns just after the turn on transition starts. This negative dip is attributed to the effect of parasitics of the clamp circuit. After this dip, the clamped V_{DS} shows correct $V_{DS(ON)}$ waveform. The response time of the clamp circuit in our double pulse test system proved to be less than 100 ns, which is fast enough for most applications.

We also compared our new dynamic $R_{DS(ON)}$ test method with our previous system (B1505A with N1267A HVSMU/HCSMU fast switch). Figure 4 shows the measurement result of 100 V/10 m Ω GaN E-HEMT obtained by both systems. Since B1505A is based on source measure unit (SMU) technology, it takes the measurement tens of microsecond to settle. On the other hand, PD1500A's clamp circuit has approximately 1000 times faster response time and successfully detects the fast response of the current collapse behavior which occurs within 100 ns from turn-on. The result also shows that the noise floor of the measured dynamic $R_{DS(ON)}$ is roughly ten times smaller than B1505A, proving that we did a significant improvement in the dynamic $R_{DS(ON)}$ measurement.

To explore more about our dynamic $R_{DS(ON)}$ test capability, we evaluated Off pulse length and $V_{DS(OFF)}$ dependency of the dynamic $R_{DS(ON)}$ for a 650 V rating GaN E-HEMT. In general, the dynamic

$R_{DS(ON)}$ of GaN power transistors which have current collapse increases when longer and higher $V_{DS(OFF)}$ stress is applied. The effect of the current collapse can be seen by comparing $R_{DS(ON)}$ between the first pulse and the second pulse of double pulse test waveform.

Figure 5 shows the dynamic $R_{DS(ON)}$ behavior of the GaN E-HEMT during double pulse test. We extracted the deviation of $R_{DS(ON)}$ ($\Delta R_{DS(ON)}$) between 1st pulse (100 ns before V_{GS} turns off) and 2nd pulse (100 ns after V_{GS} turns on). As shown in Figure 6, $\Delta R_{DS(ON)}$ slightly increased as longer and higher $V_{DS(OFF)}$ stress was applied, confirming that our double pulse test system can evaluate the current collapse of GaN power transistors effectively.

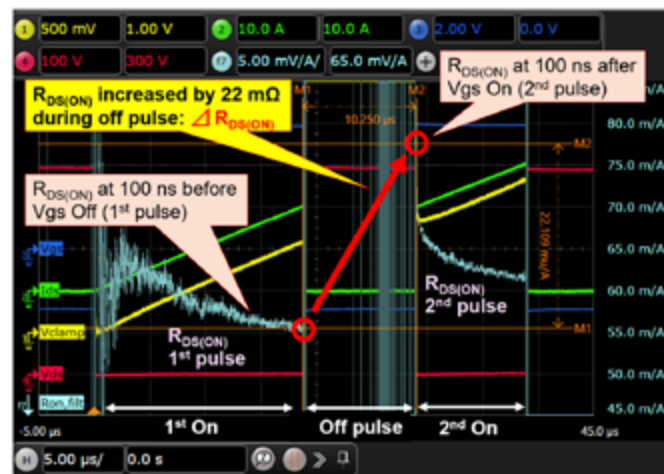


Figure 5: Dynamic $R_{DS(ON)}$ double pulse test result and $\Delta R_{DS(ON)}$ extraction of a 650 V rating GaN E-HEMT at 500 V/20 A.

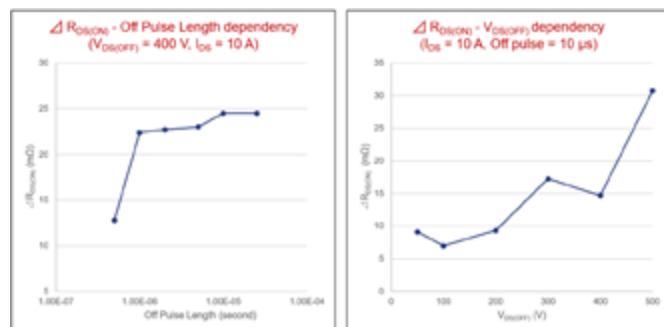


Figure 6: Off pulse length and $V_{DS(OFF)}$ dependency of $\Delta R_{DS(ON)}$ for a 650V rating GaN E-HEMT.

Summary

Current collapse is still one of the biggest concerns over GaN power transistors for many engineers, and its evaluation is very challenging due to the limitation of test instruments. As we discussed in this article, we successfully created a repeatable and reliable double pulse test system that can effectively evaluate dynamic $R_{DS(ON)}$ of GaN power transistors by employing a newly developed clamp circuit.

References

1. "Overcoming Overdrive Recovery on High-Speed Digital Storage Oscilloscopes" Application Note 5989-0068EN, Keysight Technologies
2. "Dynamic ON-Resistance Test Method Guidelines for GaN HEMT based Power Conversion Devices," Version 1.0, JEP173.

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