The Ideal Power Distribution Network

YOUR BEST POWER INTEGRITY DESIGN WILL BE YOUR NEXT ONE

Heidi Barnes

2019.08.21

SI/PI Applications Engineer / Keysight Technologies

Agenda

- **Overview of current design and test trends**
- Power delivery network complexity
- Power rail impedance finds worst case failures
- Target impedance and root cause of ringing on power rail
- Designing for flat impedance
- Power integrity workflow

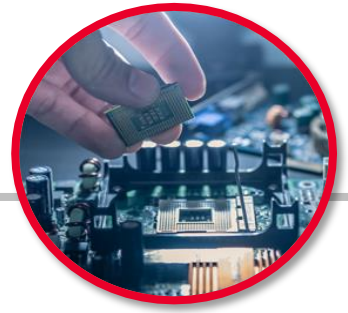
Digital High Speed Electronics Are Everywhere

Smart Cities

Every year, designers push new limits:

Faster data rates, lower power, smaller components, higher levels of integration

Smart Devices

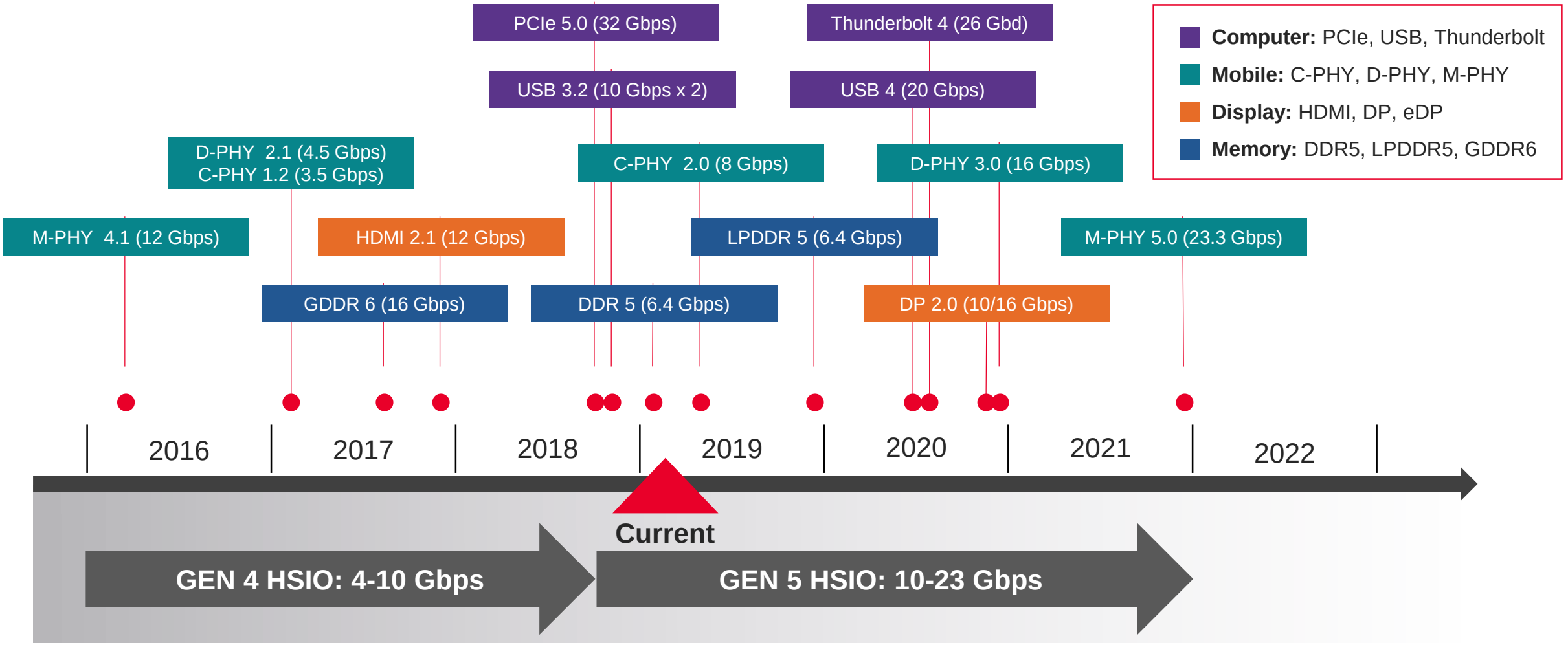


Smart Compute

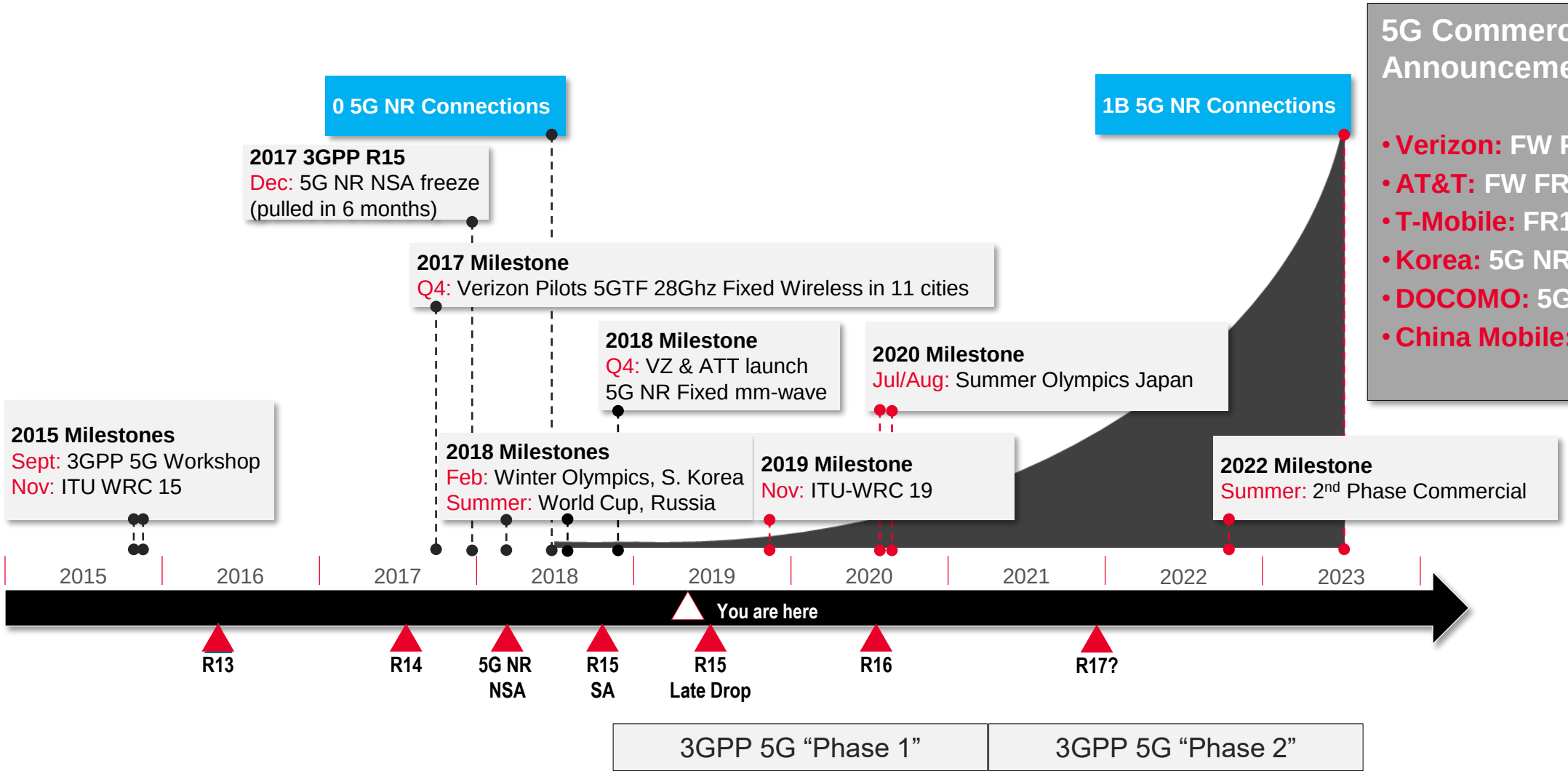
Smart Automotive

Smart Energy

Technology Waves Driving Higher Throughput



5G Networks Timeline

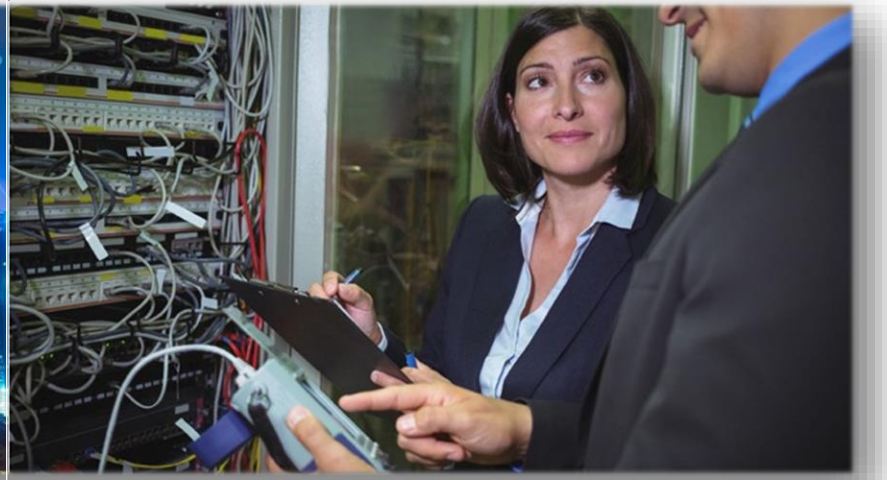


5G Commercialization Announcements

- **Verizon:** FW FR2 Oct 2018
- **AT&T:** FW FR2 Dec 2018
- **T-Mobile:** FR1 Late 2019
- **Korea:** 5G NR March 2019
- **DOCOMO:** 5G 2020 (Late 2019)
- **China Mobile:** 5G Early 2020

Design & Test Requirements are Growing Exponentially

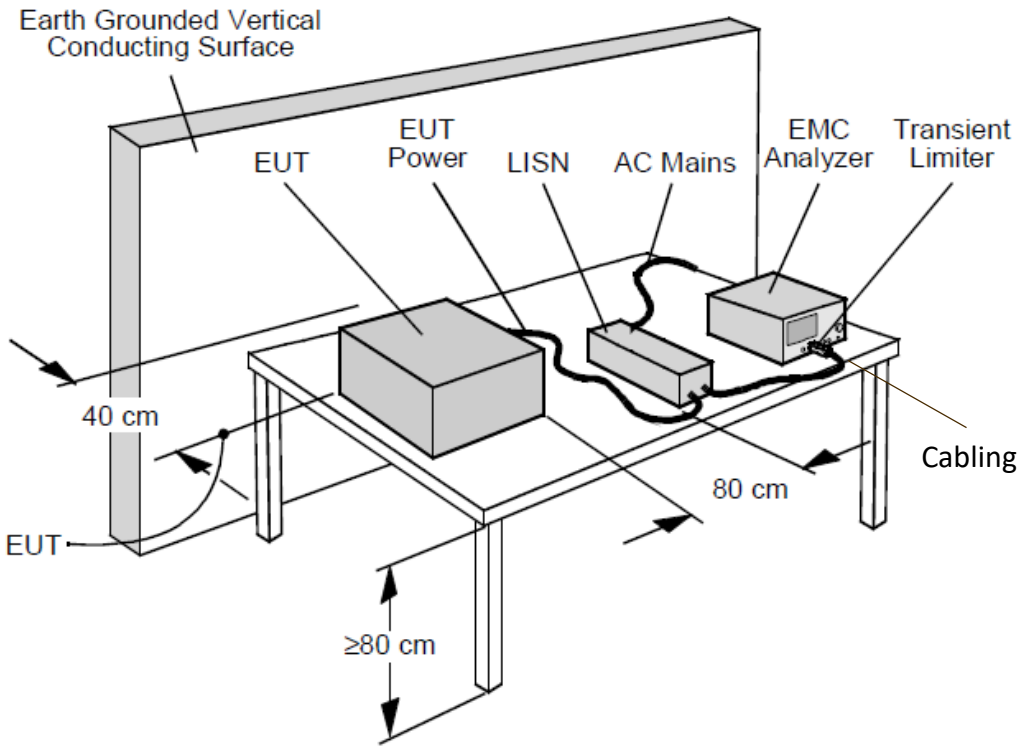
5G NR	Wireless Coexistence	EMI/EMC and Regulatory Test
20x more conformance tests than 4G	Wi-Fi, *Bluetooth*® GPS, FM Radio, 4G, 5G,NFC, RFID, Qi	20+ IEC & European (EN) Standards



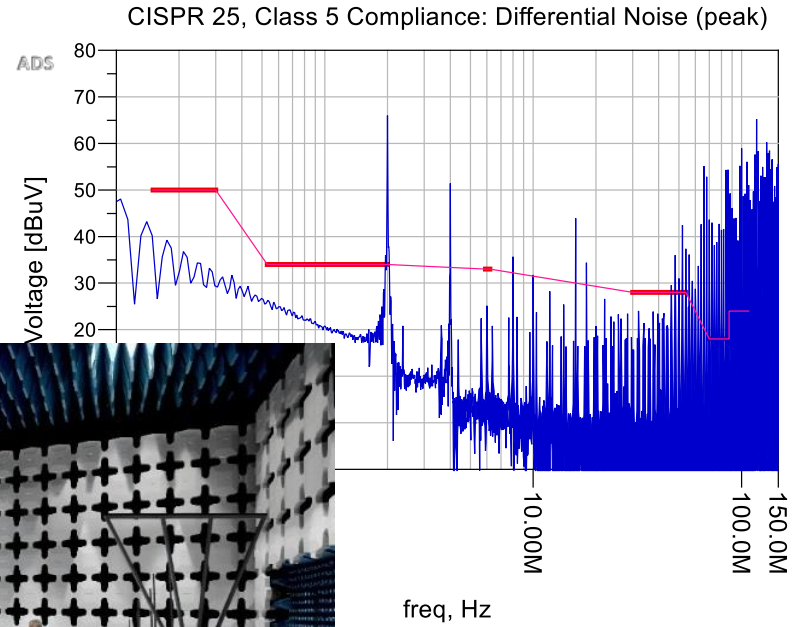
Failing EMI is Expensive

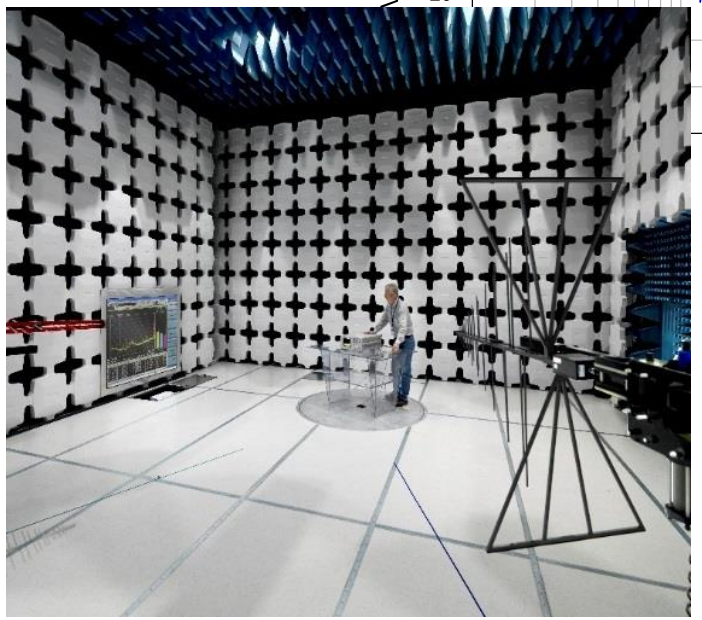
FINAL PRODUCT MUST PASS EMI/EMC REGULATIONS

Conducted Emission Testing



CISPR Compliance



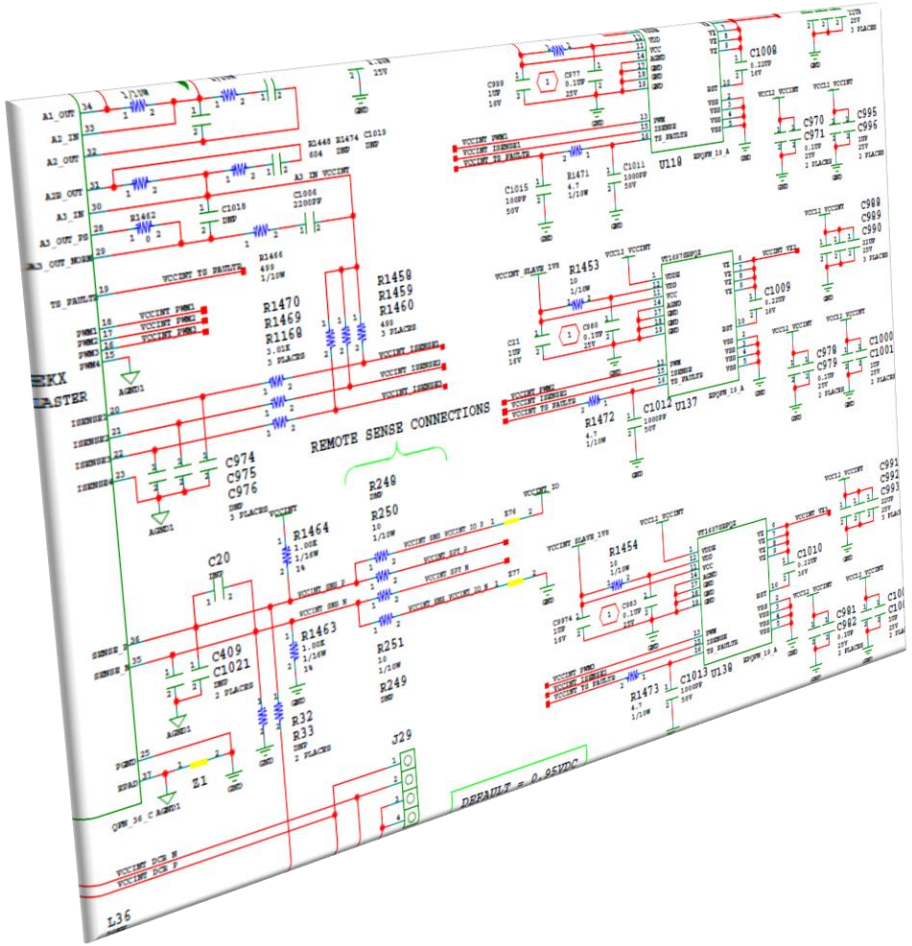


Agenda

- Overview of current design and test trends
- **Power delivery network complexity**
- Power rail impedance finds worst case failures
- Target impedance and root cause of ringing on power rail
- Designing for flat impedance
- Power integrity workflow

Electrical Schematics vs. Layout

POWER IS THE FOUNDATION THAT CONNECTS TO EVERYTHING

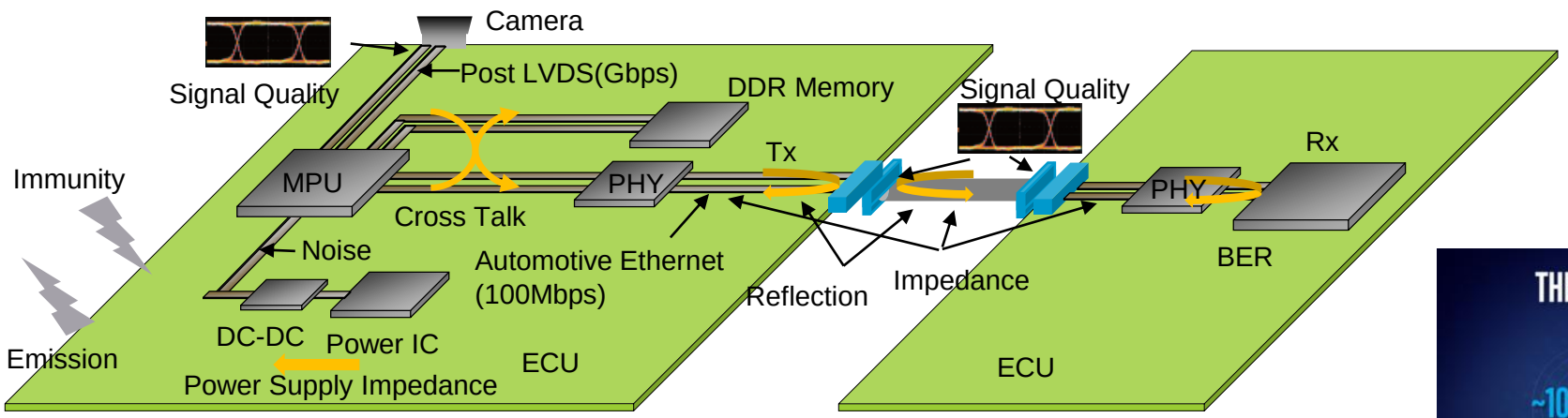


Modern High Density Electronics

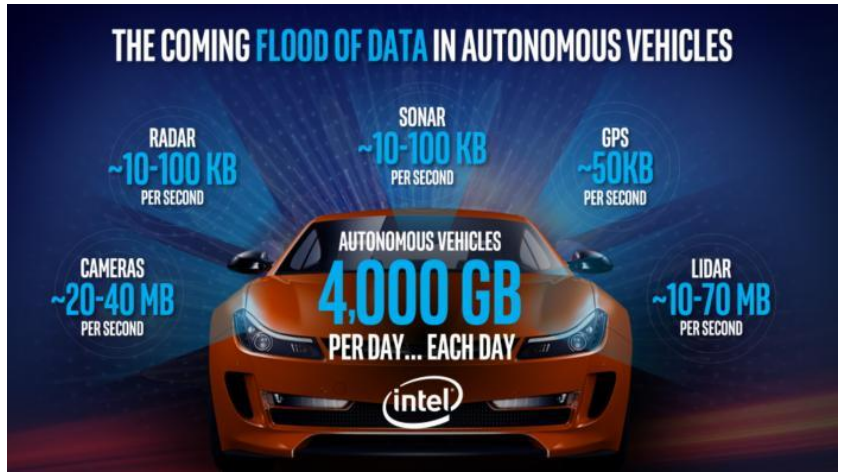
- 1000s of nets
- A web of interconnected point of load power supplies
- 1 ground net
  - Barely noticeable on a schematic
  - Typically the largest copper net in layout
  - Noise path connected to everything

Power Integrity – Not Just DC

FAST DELIVERY OF POWER AT MICROWAVE FREQUENCIES



Key Take Away:
Power Integrity Engineers need RF/uW design and measurement tools!



Power Delivery Eco-System

- Many Point-of-Load power supplies
- Low Voltage, High $\frac{dI}{dt}$ Switching Loads
- Target Z to reduce broadband $L\frac{dI}{dt}$ Voltage Noise
- Power Supply Rejection Ration (PSRR)
- DC-DC Converter Switching Noise and Stability

Note: A Point-of-Load (POL) Power Supply is typically a Switched Mode Power Supply (SMPS) with a Buck Regulator DC-DC Converter design that the Microprocessor PCB world often calls as a Voltage Regulator Module (VRM)

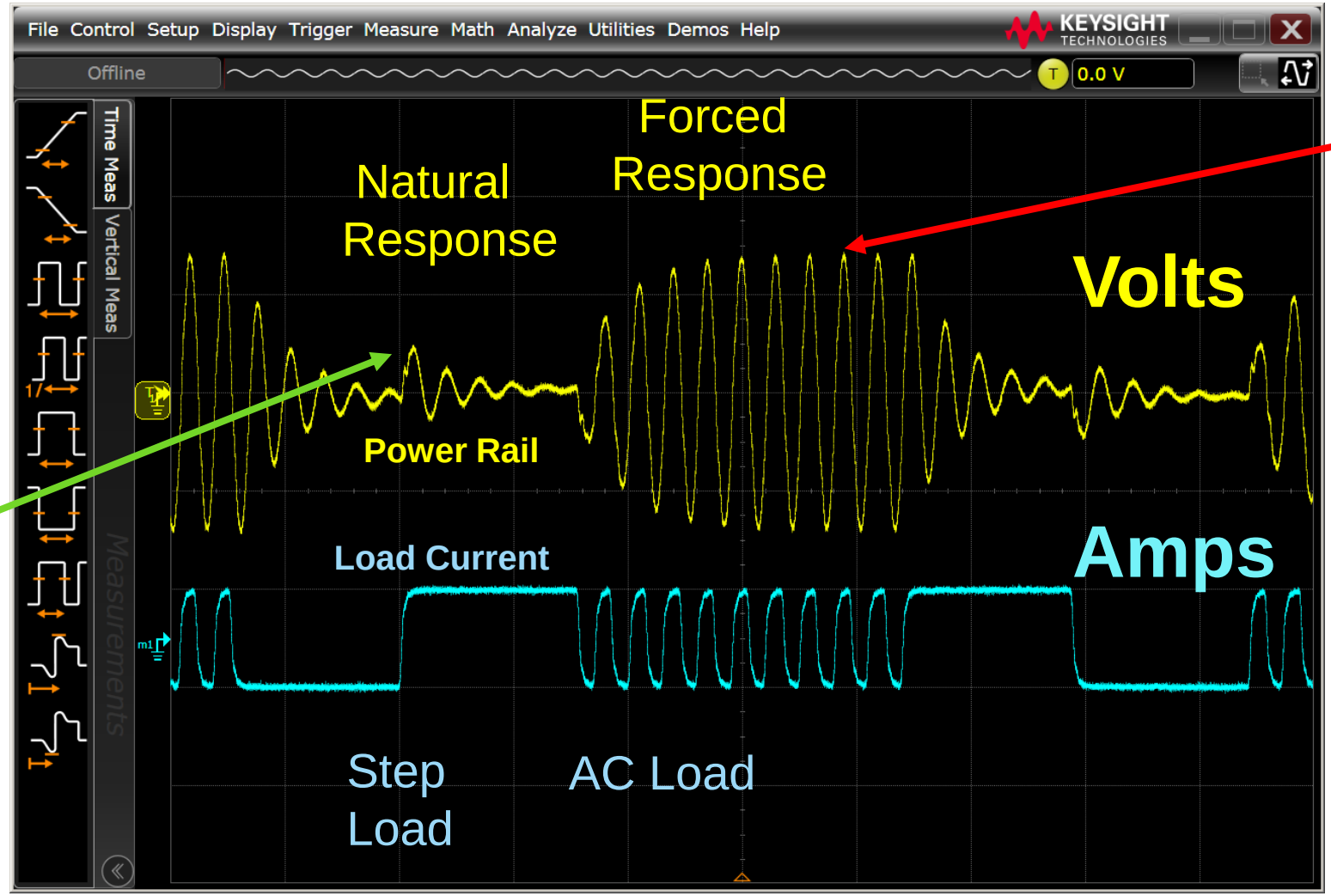
Old Methods Fail to Detect Worst Case Failures

DATA TX/RX FAILURE, OVER VOLTAGE, EMI/EMC, CROSSTALK

$$V = L\frac{dI}{dt}$$

Old Method:
Step Load
Transient Test
(False Positive)

PASS
Datasheet
Design



New Method:
Finding the
worst case Load

FAIL
Over Voltage
Tx/Rx Bit Error
EMI
Crosstalk

Key Take Away:
Forced response is worst case, not the data sheet step load.

Agenda

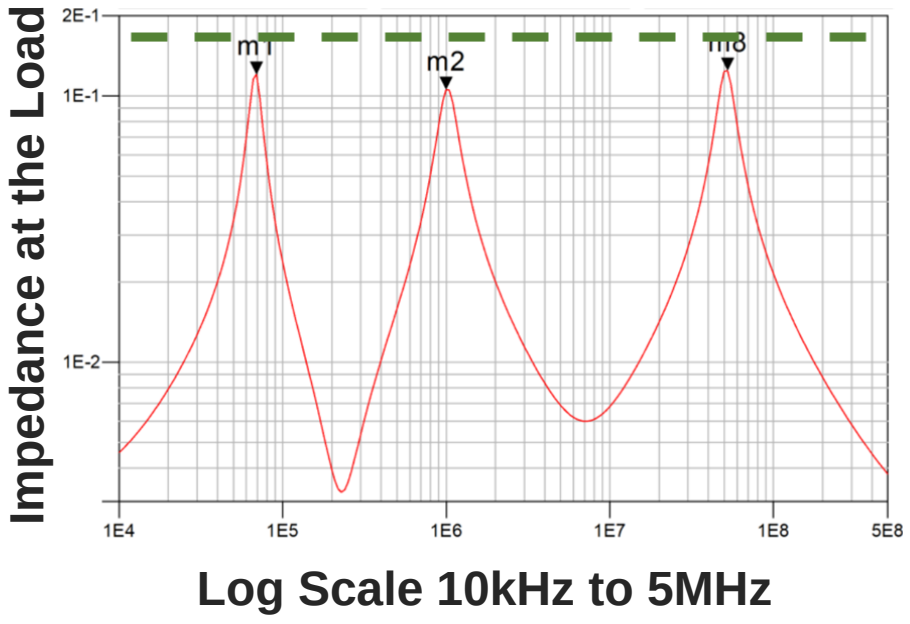
- Overview of current design and test trends
- Power delivery network complexity
- **Power rail impedance finds worst case failures**
- Target impedance and root cause of ringing on power rail
- Designing for flat impedance
- Power integrity workflow

Power Rail Impedance is the New Way!

IMPEDANCE PEAKS IN THE FREQUENCY DOMAIN CAUSE POWER RAIL RIPPLE

$$Vripple = Itransient * Zpdn$$

Impedance Peaks Help Predict Worst Case Load Transients

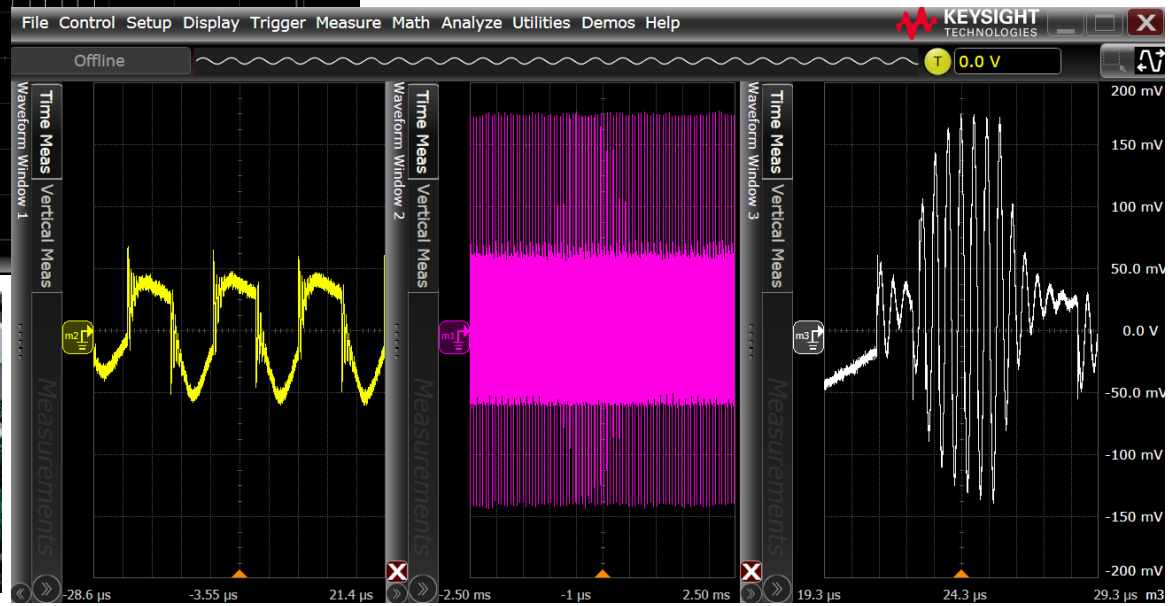


Log Scale 10kHz to 5MHz

Forced Excitation at Peak Z Frequencies

Key Take Away:
Voltage Rogue Waves are Real

Rogue Wave Captured

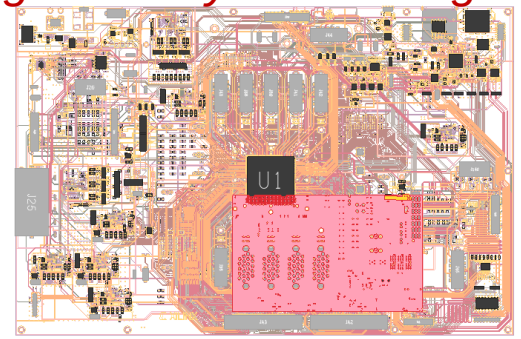


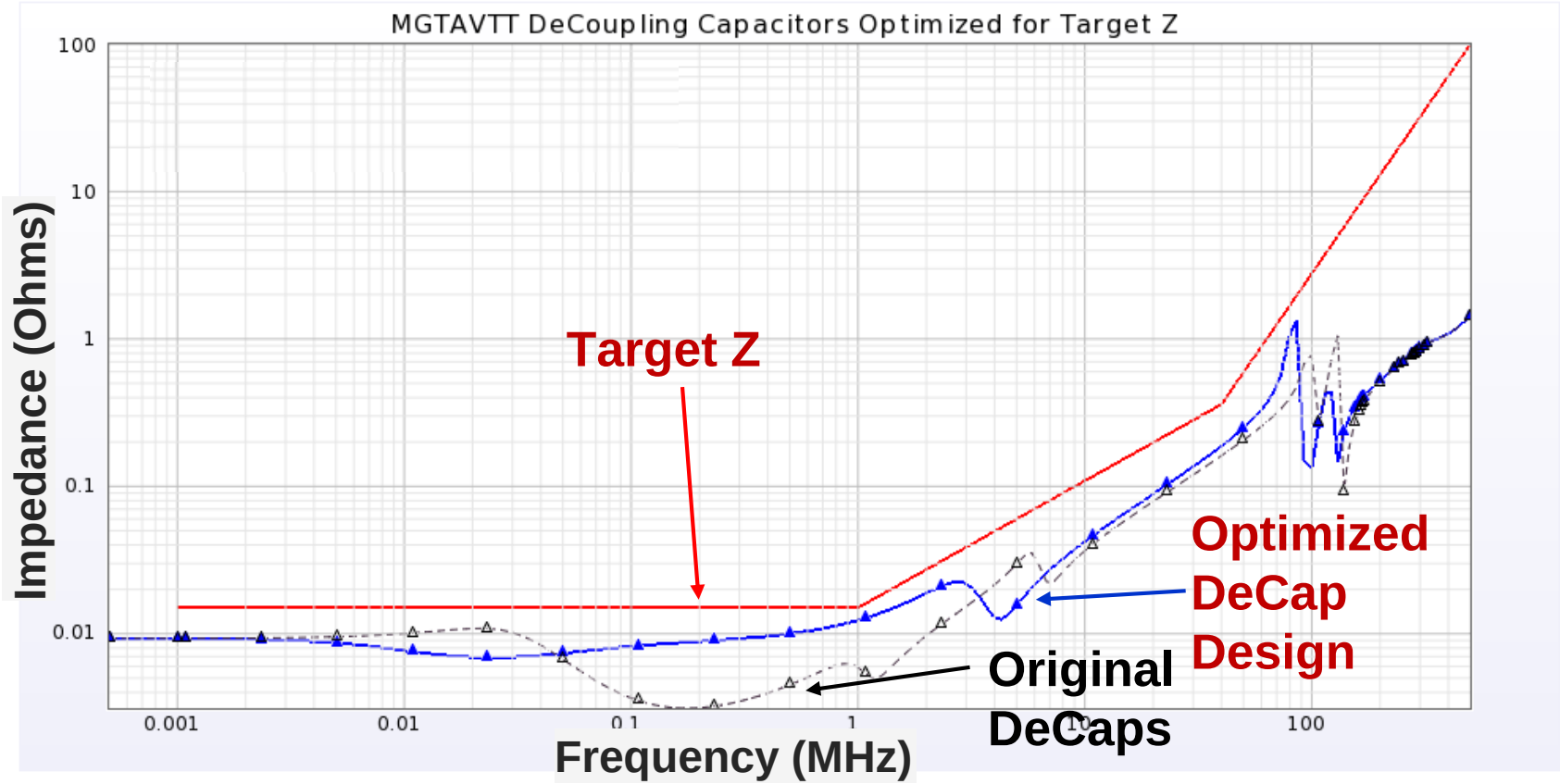
Target Z Keeps Getting Lower

FLAT Z DECOUPLING CAPACITOR OPTIMIZATION

- EM simulation and Measure Based Models Enable Low Z Designs
- Flat Z Optimization Lowers Cost, Reduces Risk of Failures, Maximizes Performance

High Density PCB Designs





Decoupling Capacitors

Yes	C190	330 uF
Yes	C215	330 uF
Yes	C216	330 uF
Yes	C218	330 uF
Yes	C303	220 nF
Yes	C305	220 nF
Yes	C750	220 nF
Yes	C753	220 nF
Yes	C757	220 nF
No	C217	100 uF
No	C225	100 uF
No	C315	4.7 uF
No	C316	4.7 uF
No	C778	4.7 uF
No	C779	4.7 uF
No	C780	4.7 uF

40% Fewer Components

Fewer solder joints higher reliability

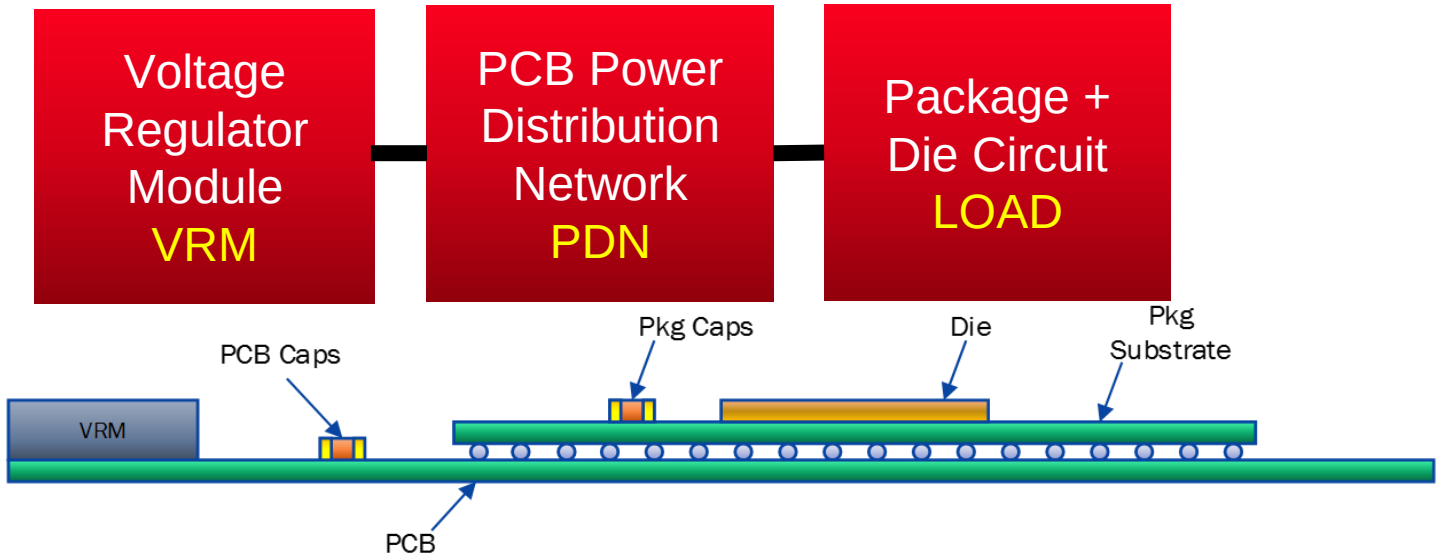
Key Take Away:
Flat Z design over a wide bandwidth gives the best performance!

Agenda

- Overview of current design and test trends
- Power delivery network complexity
- Power rail impedance finds worst case failures
- **Target impedance and root cause of ringing on power rail**
- Designing for flat impedance
- Power integrity workflow

Power Integrity Target Impedance

TARGET Z TIMES DI/DT CURRENT TRANSIENT IS THE VOLTAGE RIPPLE



Target Impedance Calculation

$$Z_{\text{Target}} = \frac{\Delta V_{\text{Max Ripple}}}{\Delta I_{\text{Max Transient Load}}}$$

Where Does the Ringing Come From?

ENERGY SWINGS BETWEEN THE L AND THE C

Energy stored in the Magnetic Field

$$V(t) = L\frac{di}{dt}$$

$$Z = j\omega L$$

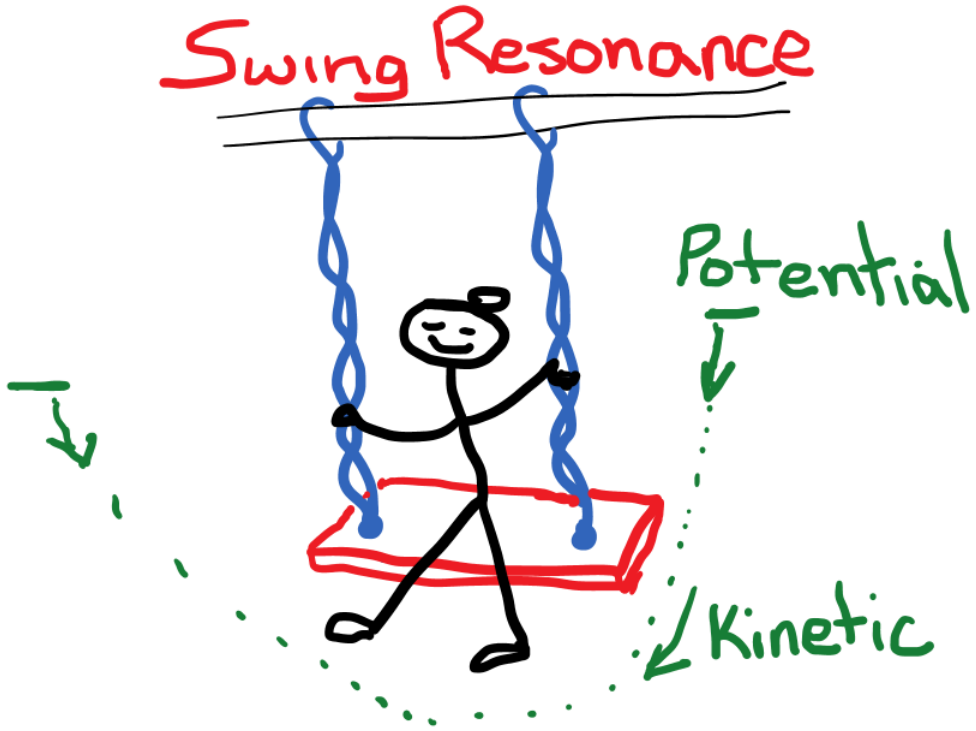
Phase V Leads I

Energy stored in the Electric Field

$$I = \int C\frac{dV}{dt}$$

$$Z = \frac{-1}{j\omega C}$$

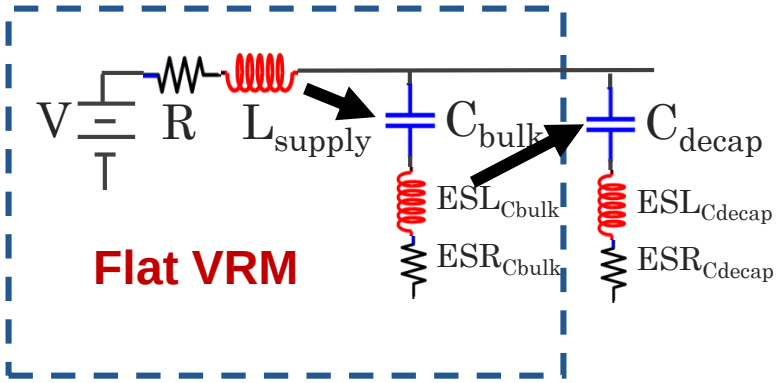
Phase V Lags I

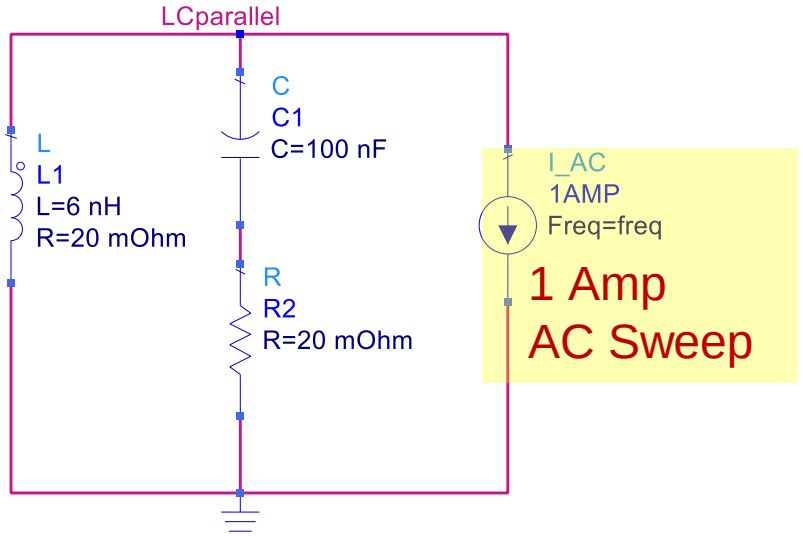


Root Cause of Ringing on the Power Rail

PARALLEL INDUCTANCE CAN RESONATE WITH THE DECOUPLING CAPACITANCE

Parallel L-C in the PDN





$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

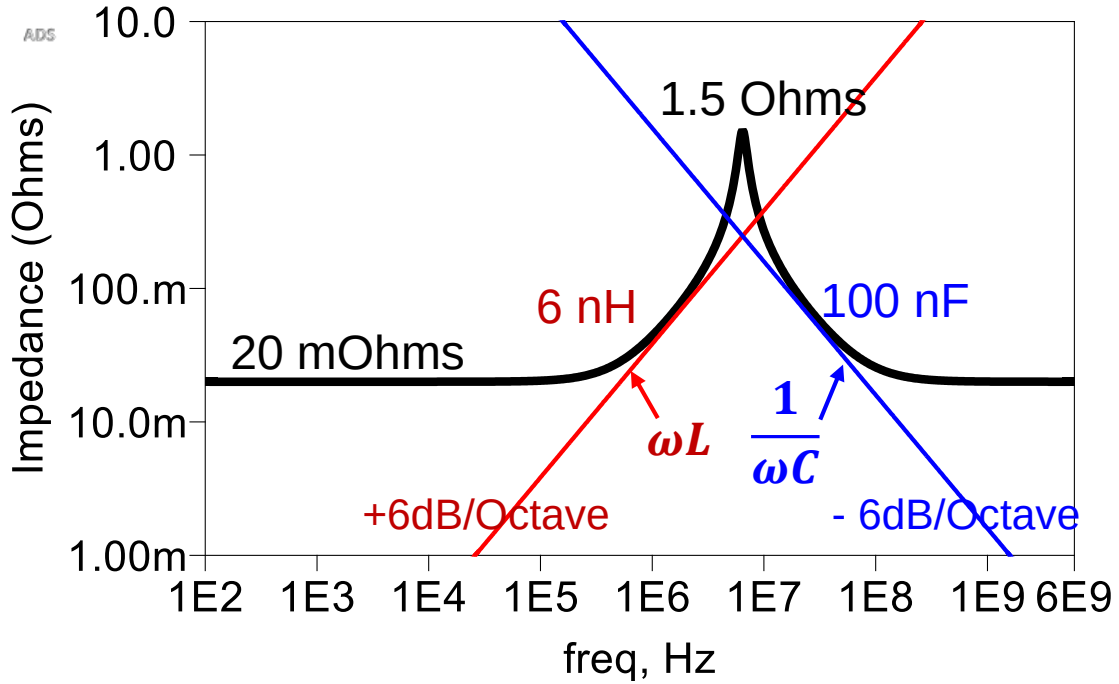
$$\Delta V = \Delta I \cdot Z_{peak}$$

$$\boldsymbol{Z_{peak} = Z_0 \cdot Q}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$Q = \frac{Z_0}{R_{total}}$$

Impedance vs. Frequency



Zpeak=1.5 Ohms

Zo=250 mOhms

Agenda

- Overview of current design and test trends
- Power delivery network complexity
- Power rail impedance finds worst case failures
- Target impedance and root cause of ringing on power rail
- **Designing for flat impedance**
- Power integrity workflow

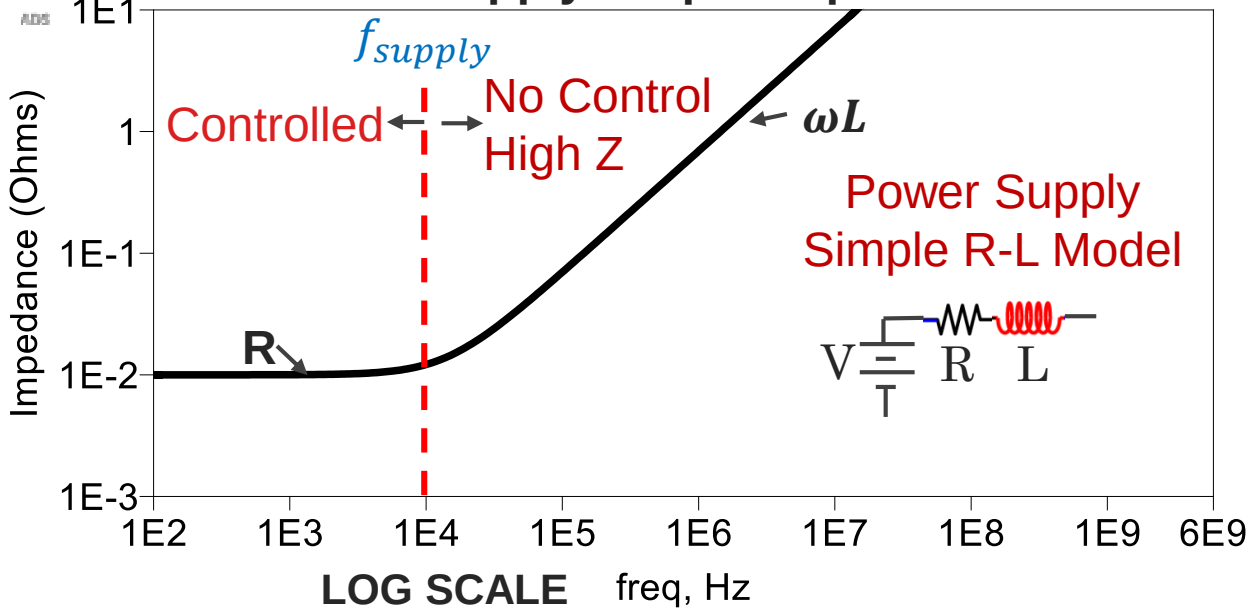
Bandwidth of the Power Supply Control Loop f_{supply}

DECOUPLING IS REQUIRED TO EXTEND THE POWER SUPPLY BANDWIDTH

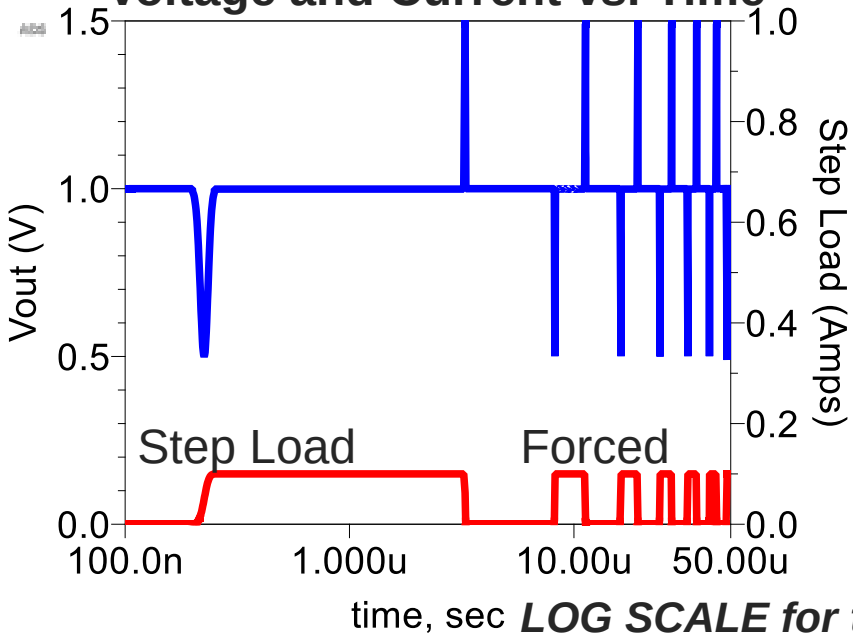
PROBLEM
The Load can make the Power Supply Control Loop go unstable

1st Order SOLUTION
Design for Flat Impedance at the output to keep V and I in phase and the feedback stable.

Frequency Domain
Power Supply Output Impedance



Time Domain
Voltage and Current vs. Time

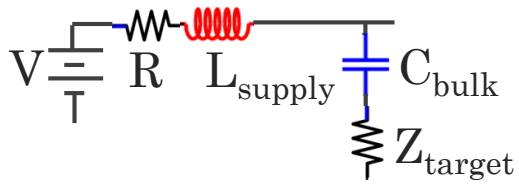


Transition from Power Supply to Bulk Capacitor

DESIGNING FOR FLAT IMPEDANCE

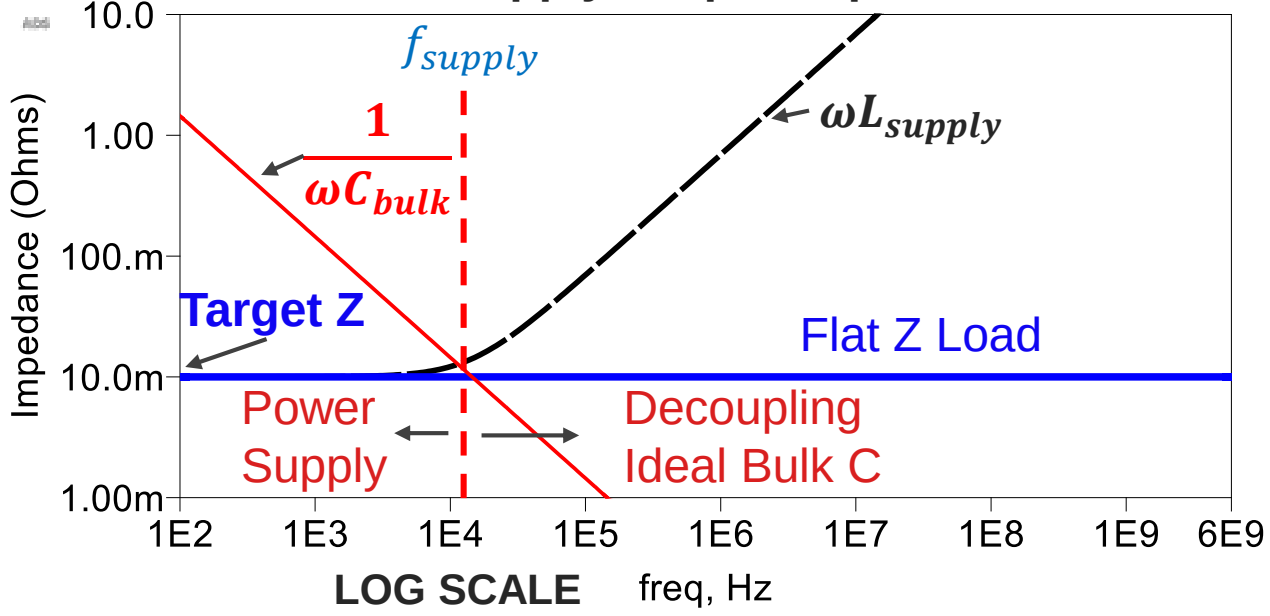
PROBLEM
Find the decoupling capacitor that will maintain a Flat Z Load for the Power Supply

1st Order SOLUTION
Add Bulk Capacitor to maintain flat impedance

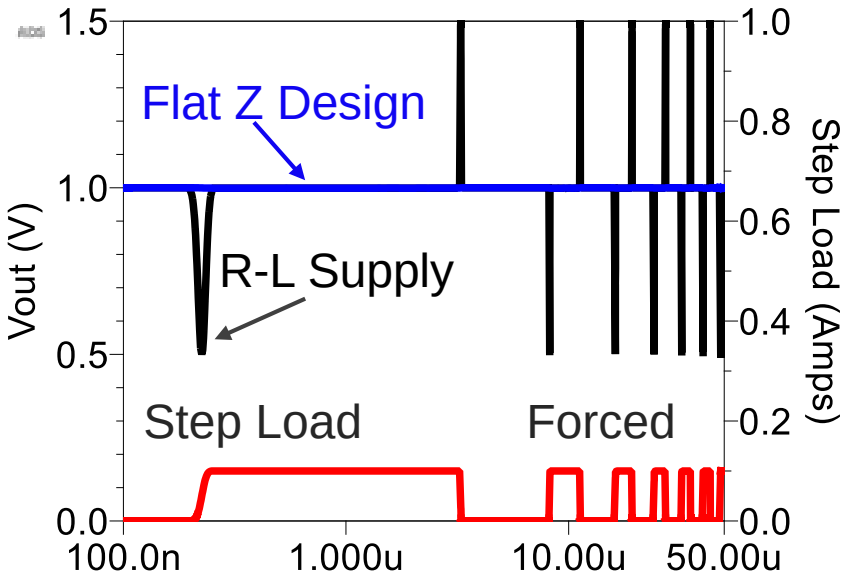


$$C_{bulk} = \frac{L_{supply}}{Z_{Target}^2}$$

Frequency Domain
Power Supply Output Impedance



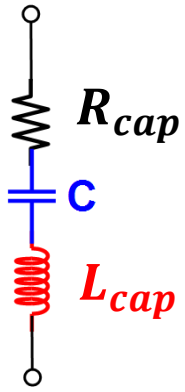
Time Domain
Voltage and Current vs. Time



Capacitors Have Series L and Series R

SELECT ESR FOR FLAT Z PDN, MINIMIZE THE ESL

Capacitor Model



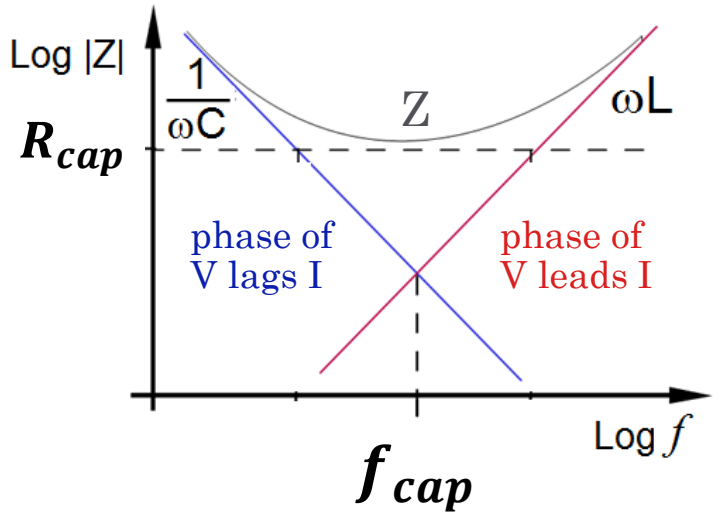
Impedance Equation

$$Z = R_{cap} + \left(j\omega L_{cap} - j\frac{1}{\omega C}\right)$$

$$f_{cap} = \frac{1}{2\pi\sqrt{L_{cap} \times C}}$$

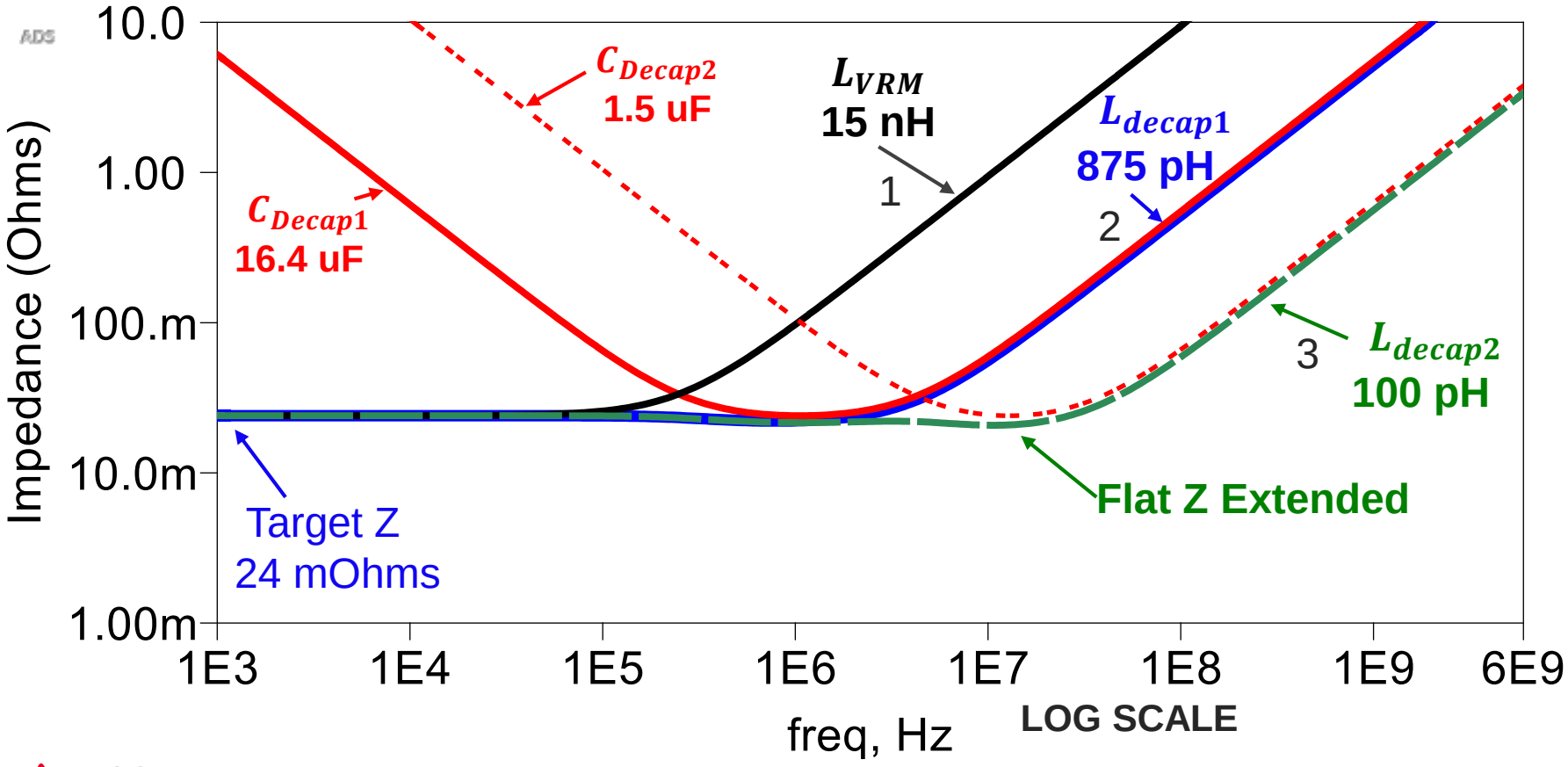
Voltage and current are in phase at f_{cap}

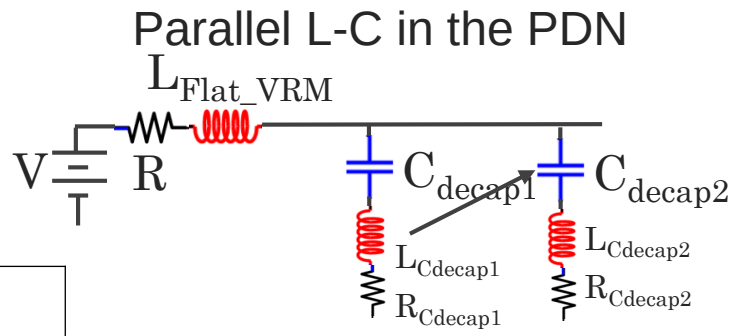
Series RLC Impedance vs. Frequency



Adding Decoupling Capacitors to Reduce L

SMALLER CAPACITORS HAVE LOWER ESL



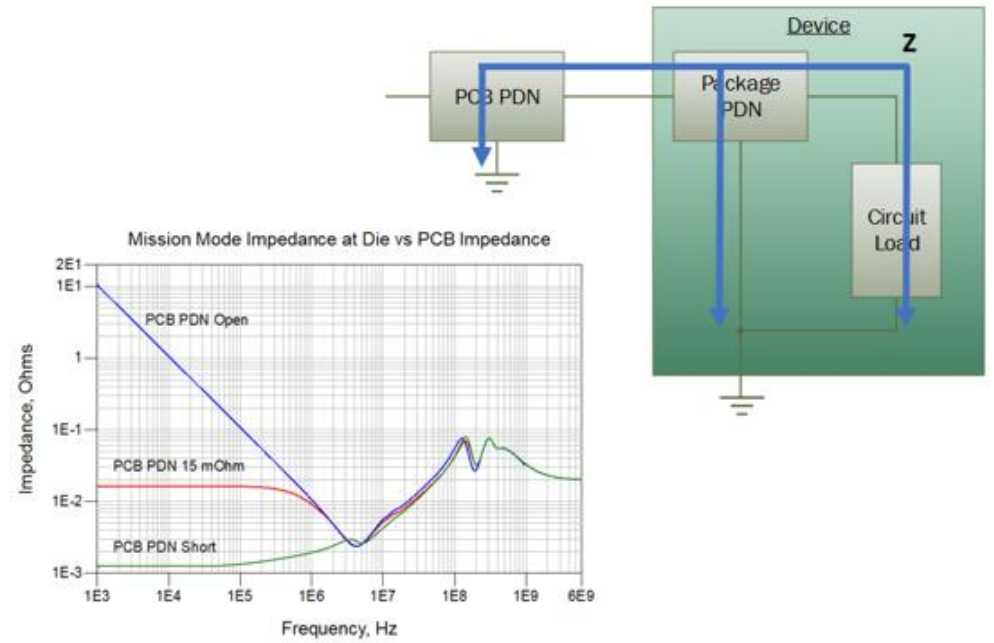


$$C_{decap2} = \frac{L_{decap1}}{Z_{Target}^2}$$

$$= \frac{875pH}{(24\ mOhm)^2}$$

$$\approx 1.5\ uF$$

It’s All About the Load and Noise Sources

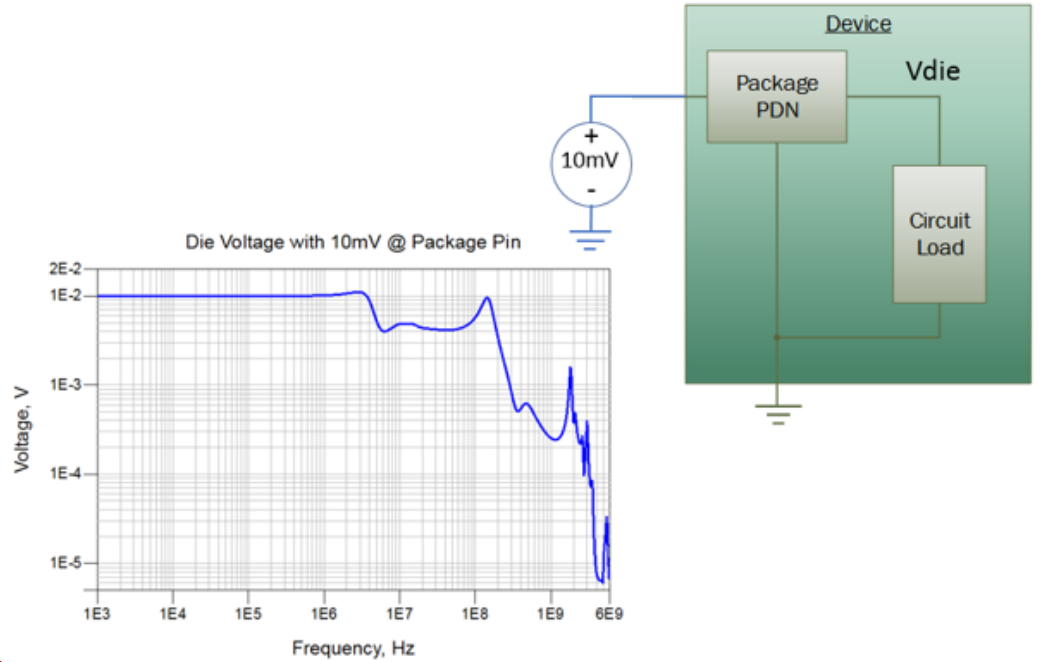


Self-induced [inflicted] noise

Power Supply Noise Limits @ Package Ball

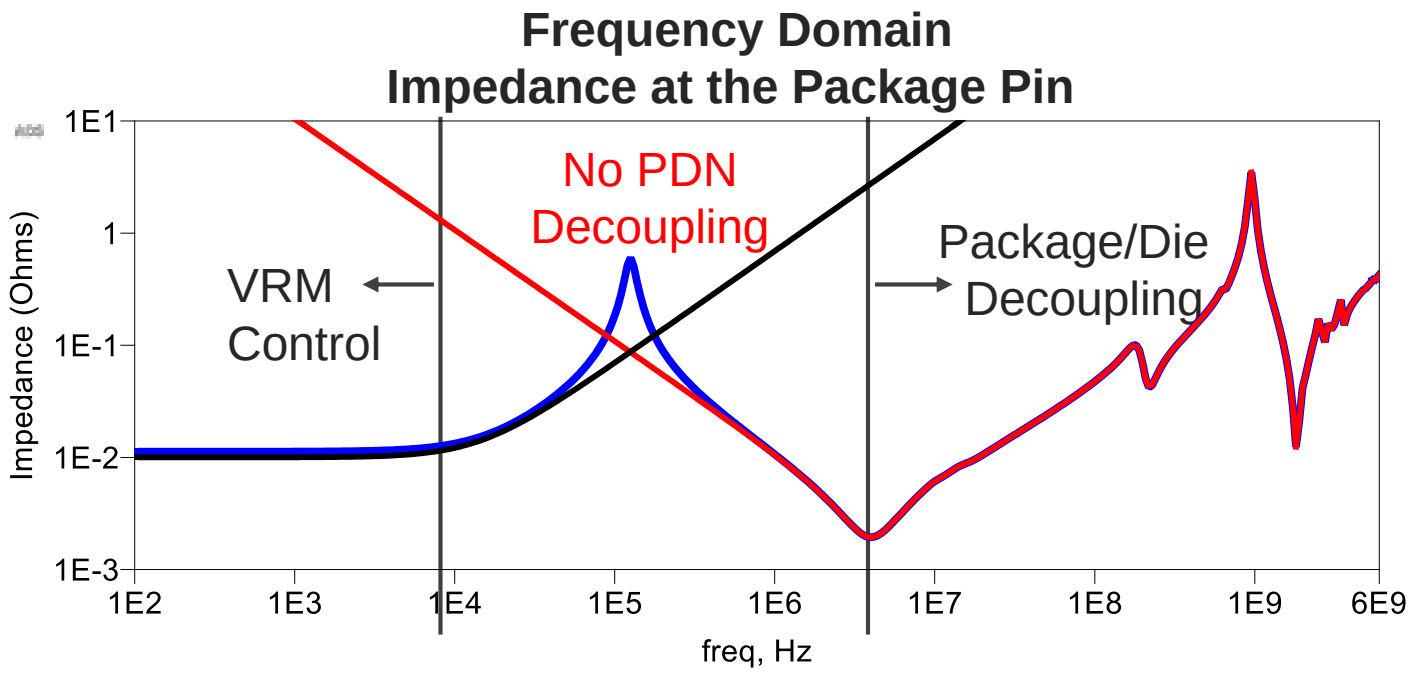
Power Supply Noise Spec: 10mV pk-pk

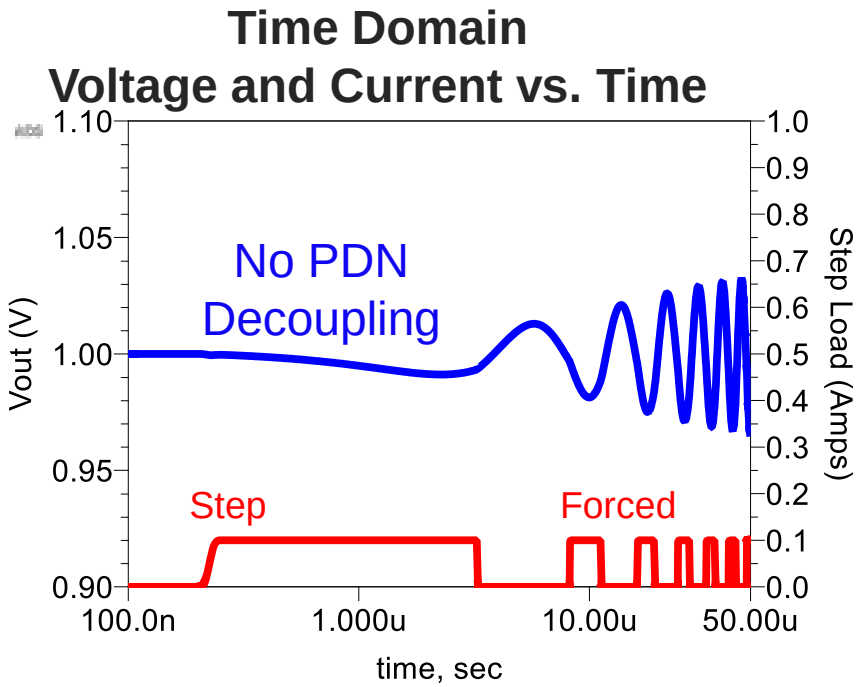
External [injected] noise



VRM + Load and No Decoupling Capacitors

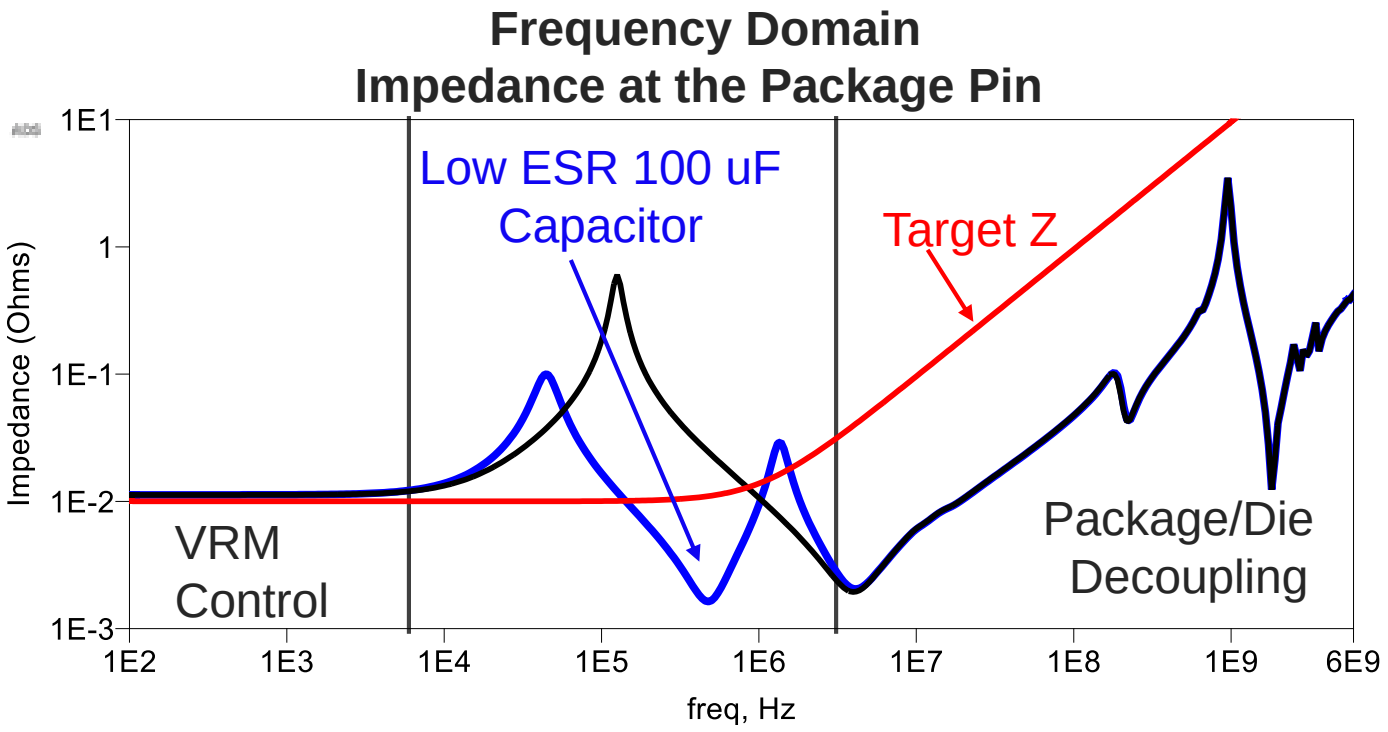
PARALLEL RESONANCE CAUSES AN IMPEDANCE PEAK

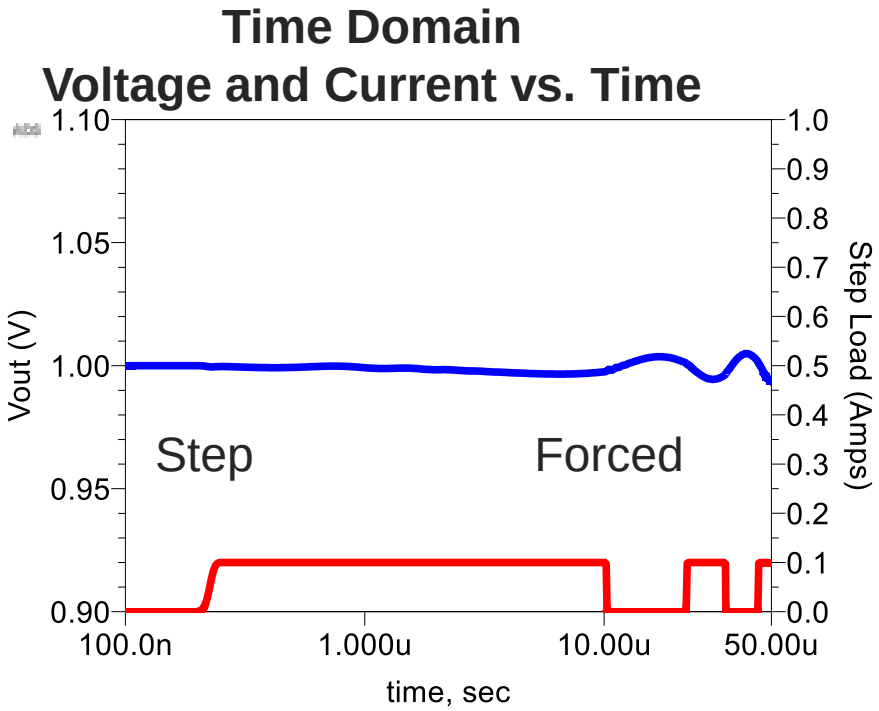




The Wrong Capacitor Can Add Parallel Resonances

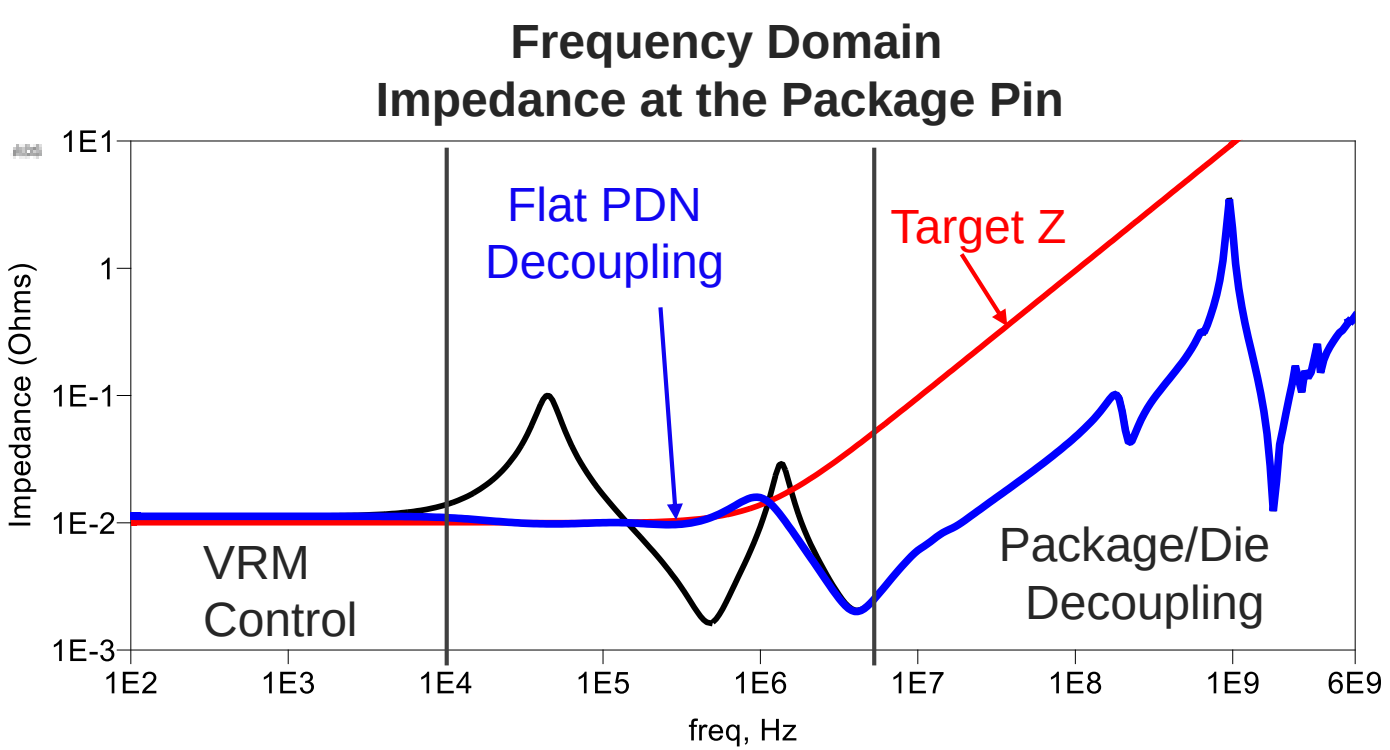
INCREASES PART COUNT TO REACH TARGET Z

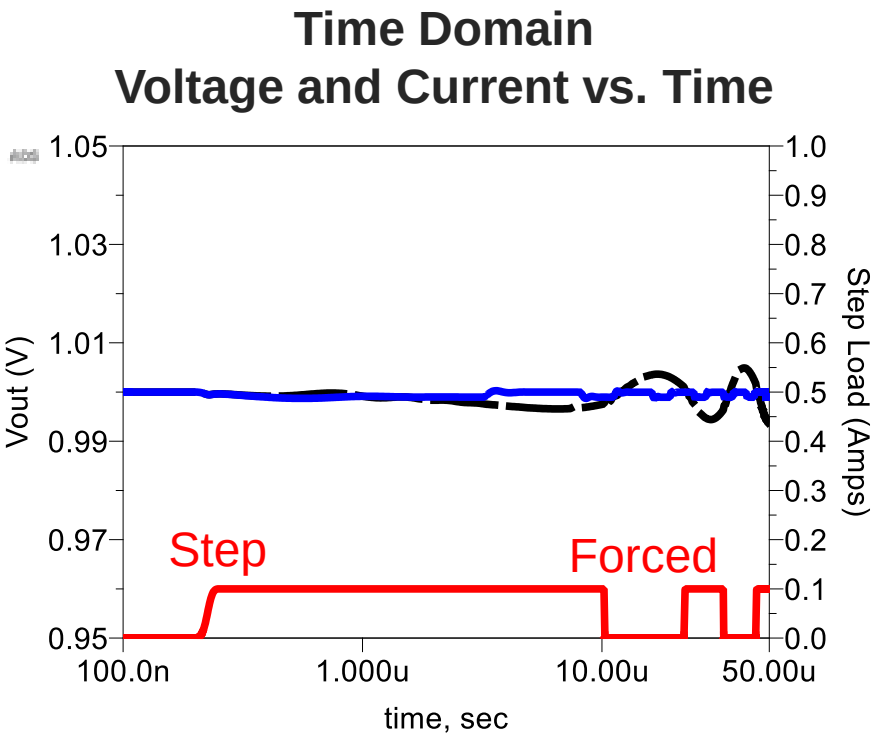




Flat Impedance PDN Design

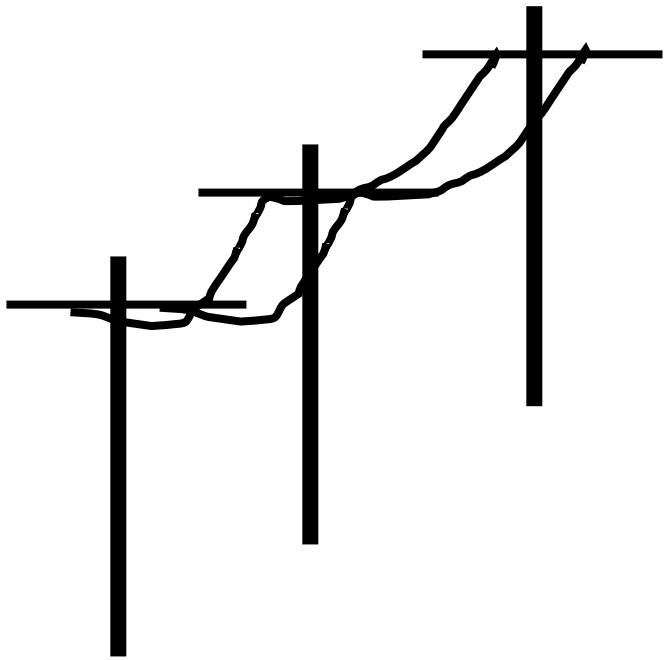
FLAT Z = MAXIMUM STABILITY AND MINIMUM RIPPLE





History Lesson – The Transatlantic Cable

ENGINEERED DESIGN VS. COSTLY DEBUG/REDESIGN



What is so hard about stringing a wire between the transmitter and the receiver?

Where was the SI Engineer in 1858?

Transatlantic telegraph cable

In 1858…signal quality declined rapidly, slowing transmission to an almost unusable speed. The cable was destroyed the following month when Wildman Whitehouse applied excessive voltage to it while trying to achieve faster operation.

Questions For Your Next Design

PI ENGINEERS REQUIRE SIMULATION AND MEASUREMENT TOOLS

1. Are your designs still leveraging decade capacitor values?
2. Are poor designs band-aided with added filters and more capacitors?
3. Where is the PI engineer?

Agenda

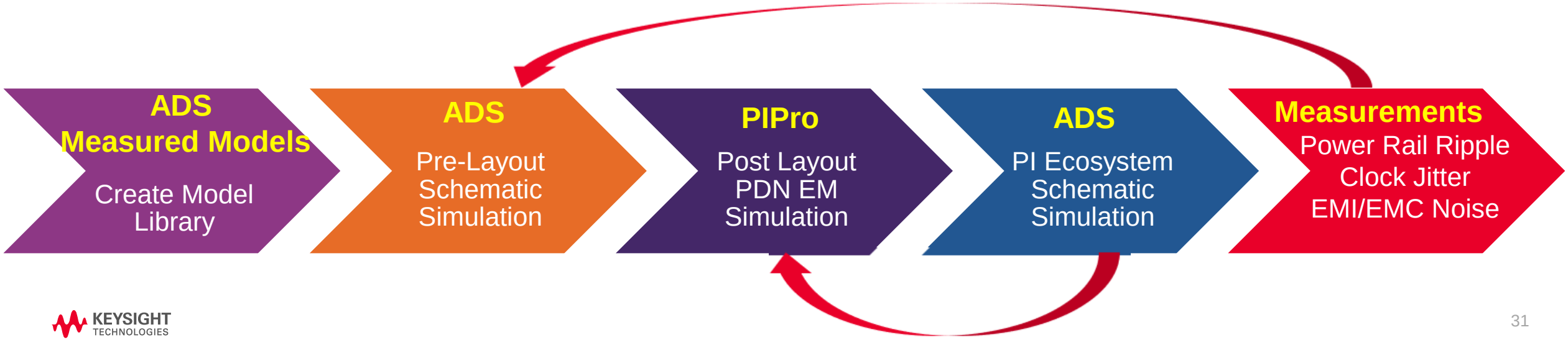
- Overview of current design and test trends
- Power delivery network complexity
- Power rail impedance finds worst case failures
- Target impedance and root cause of ringing on power rail
- Designing for flat impedance
- **Power integrity workflow**

Power Delivery Needs Simulation and Measurement

WHAT IS THE POWER INTEGRITY WORKFLOW?

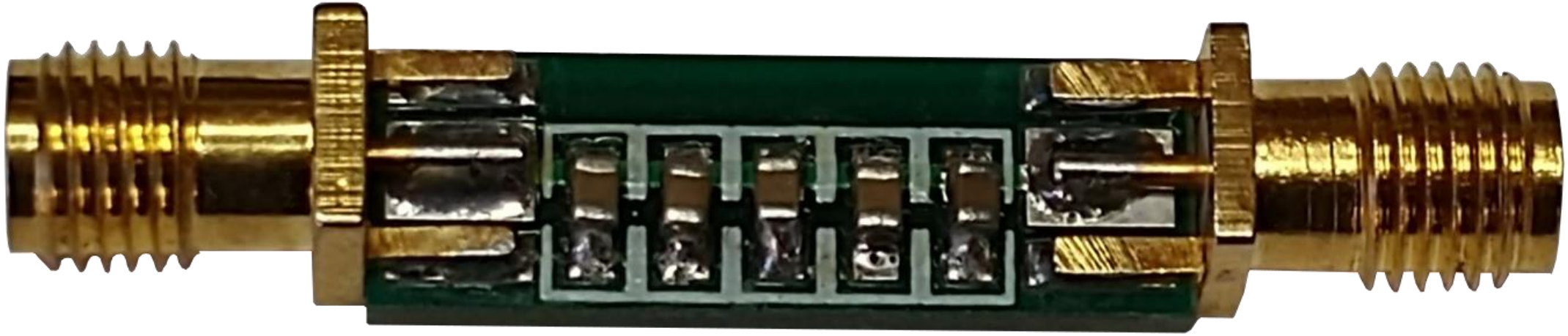
Key Take Away:
The combined simulation and measurement of the PI Ecosystem reduces EMI/EMC failures

- Designers often leverage designs and wait until **measurement** to debug
- Current industry workflow starts at **post-layout**, need to move to **pre-layout**
- Combined **power integrity** + **power electronics** covers both delivery and generation of power

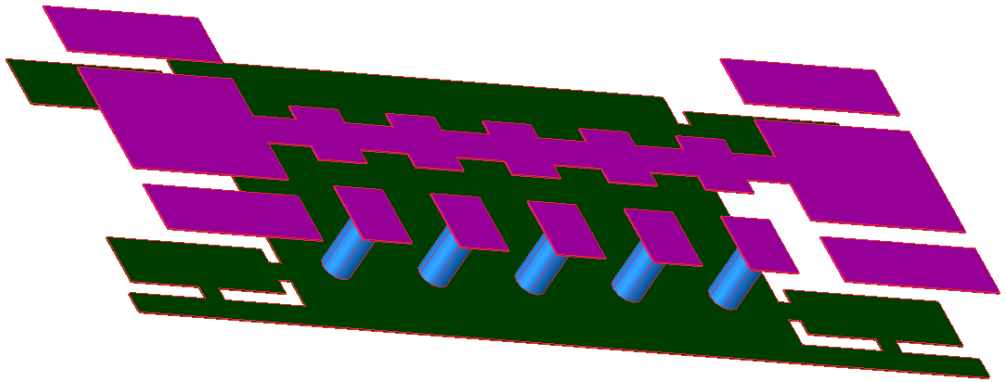


Why the PI Workflow Needs EM Modeling

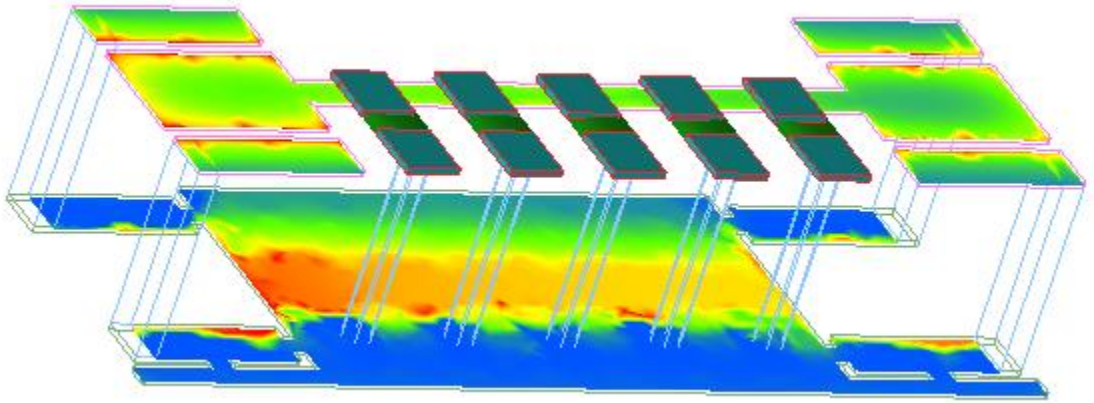
PDN EXAMPLE OF PARALLELING 5 CAPACITORS



Layout



EM Simulation with PIPro

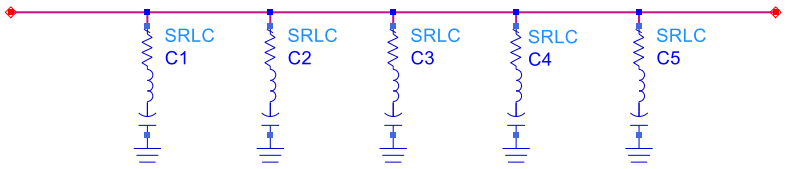


EM Models Capture Real World PCB Parasitics

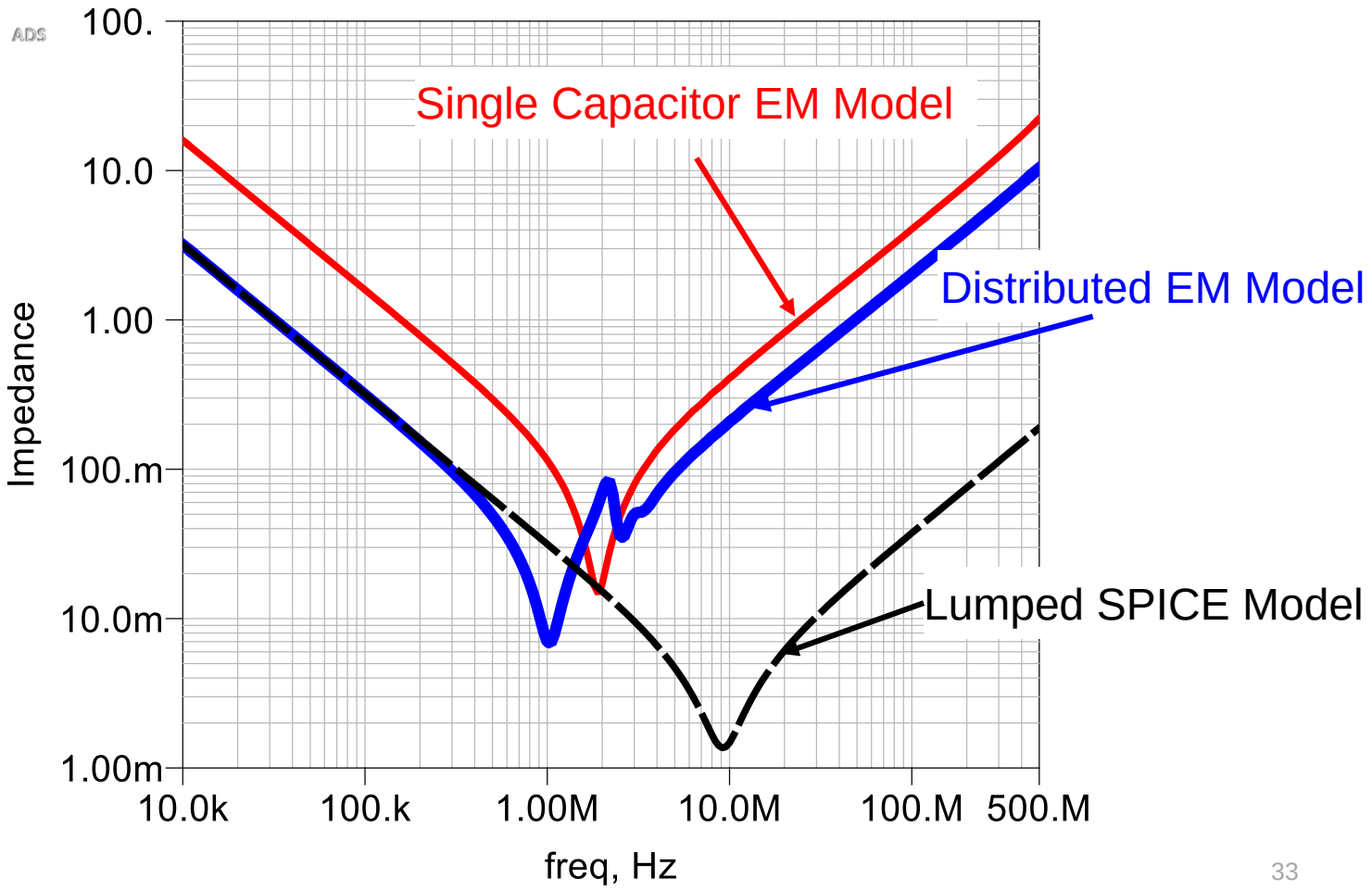
LUMPED SPICE MODEL GETS IT WRONG

Paralleling same value caps

	C	ESR	ESL
C1	1 uF	7 mΩ	300 pH



Parallel Capacitors SPICE vs PCB EM Model

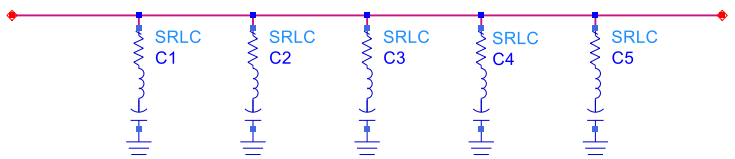


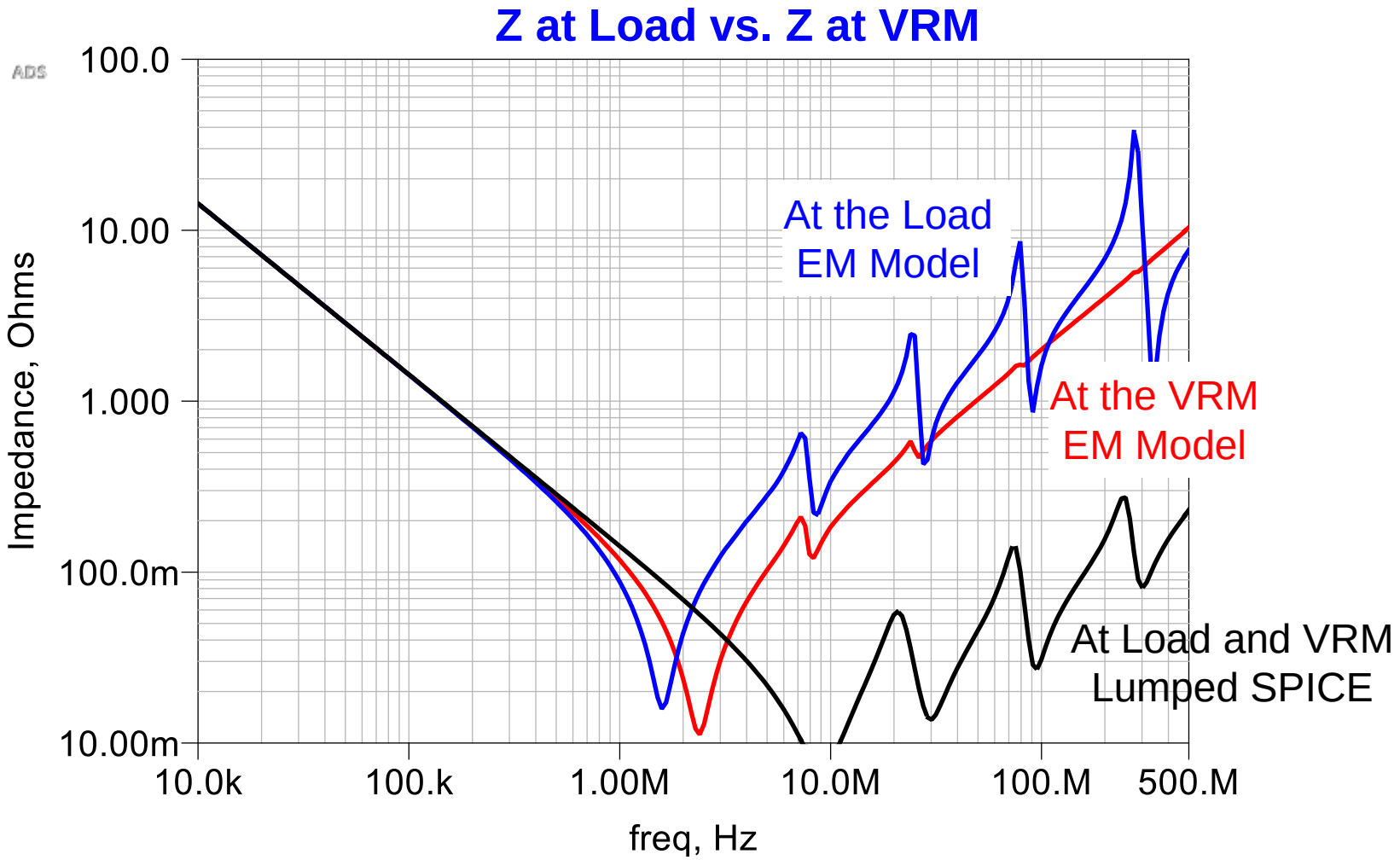
EM Models Capture Real World PCB Parasitics

Z AT THE LOAD IS NOT THE SAME AS Z AT THE VRM

Capacitor Loading by the Decade

	C	ESR	ESL
C1	1 uF	7 mΩ	300 pH
C2	0.10uF	15 mΩ	300 pH
C3	0.01uF	30 mΩ	300 pH
C4	0.001uF	100 mΩ	300 pH
C5	100pF	200 mΩ	300 pH





PathWave ADS PIPro EM Simulation of the PCB PDN

EASY SETUP FOR HIGH PORT COUNT SIMULATIONS

1) IMPORT THE PCB

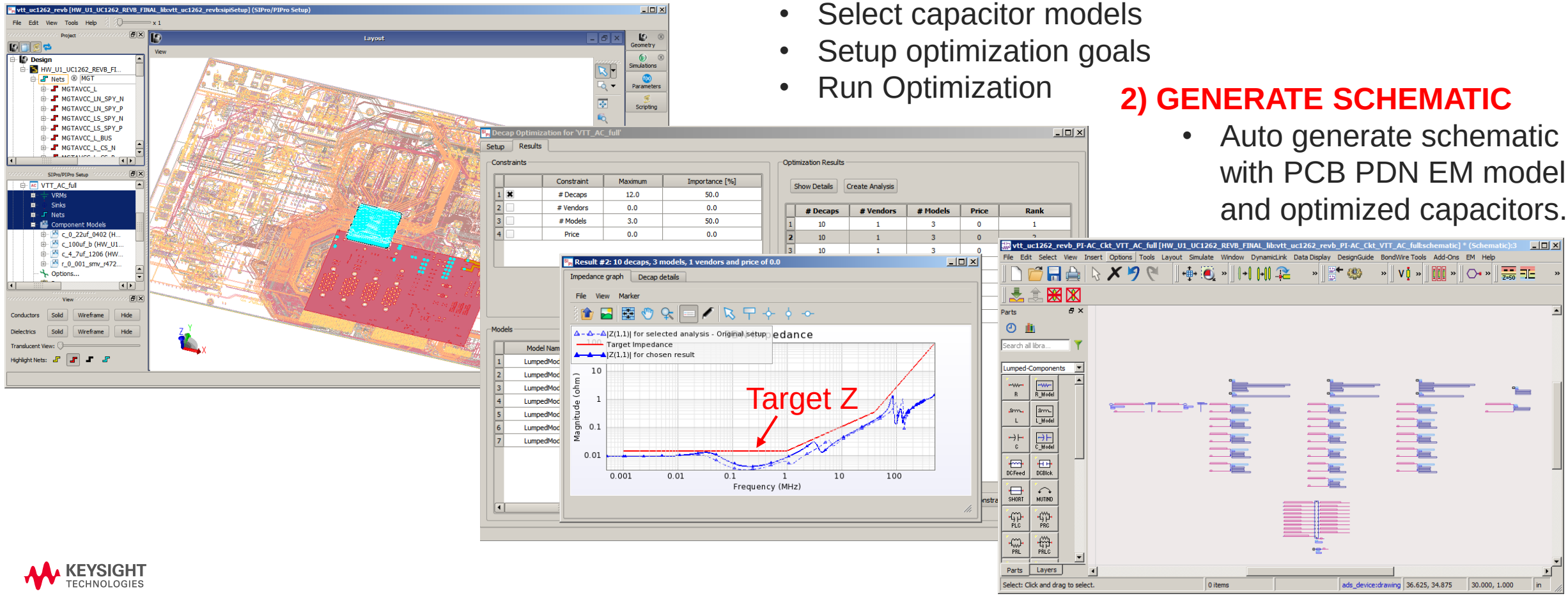
- Select VRM, Sink, Nets, Components
- Run EM AC Frequency Sweep

2) OPTIMIZE DECOUPLING

- Select capacitor models
- Setup optimization goals
- Run Optimization

2) GENERATE SCHEMATIC

- Auto generate schematic with PCB PDN EM model and optimized capacitors.



KEYSIGHT TECHNOLOGIES

Voltage Regulator State Spaced Averaged Models

KEYSIGHT YOUTUBE VIDEO WITH PICOTEST

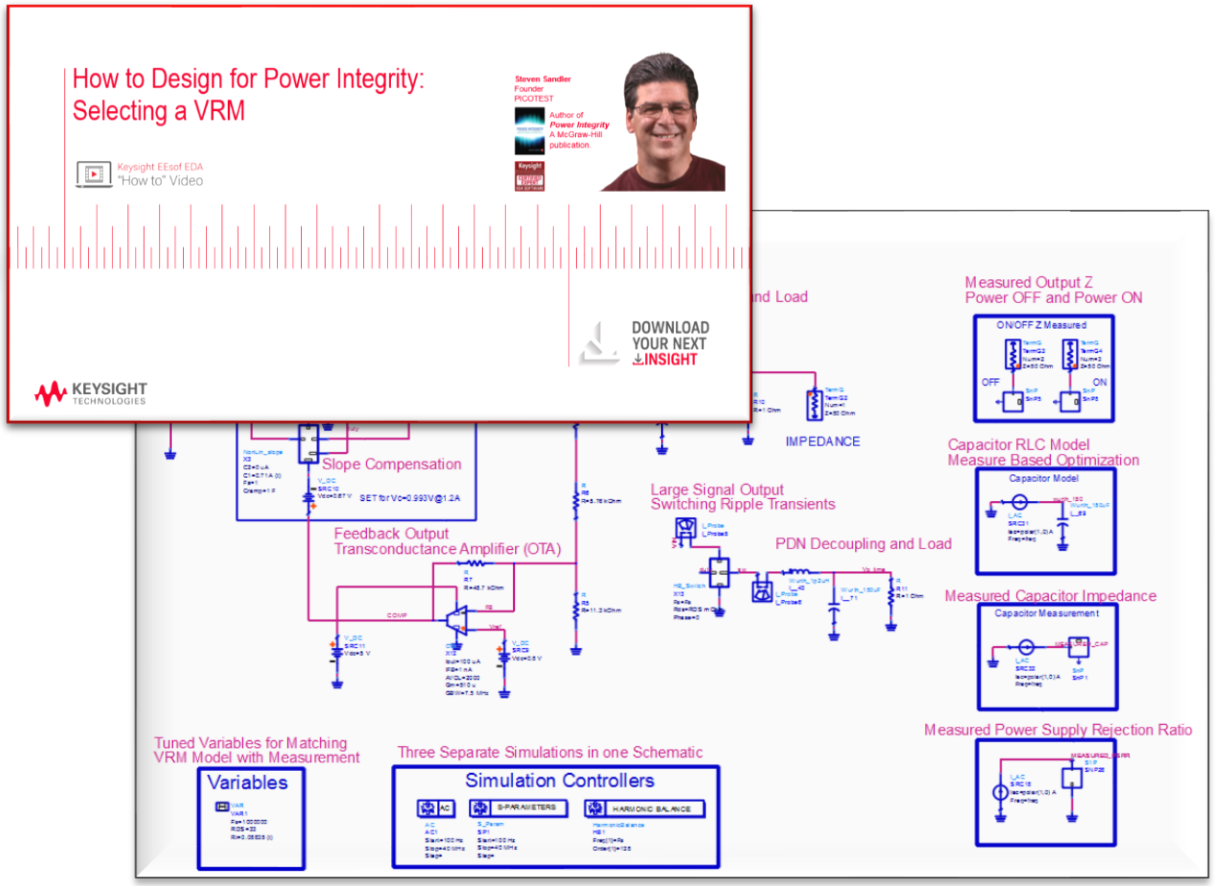
Measurement Based VRM Modeling

Steve Sandler – PICOTEST

PICOTEST

How to Video

http://tinyurl.com/vrm-video



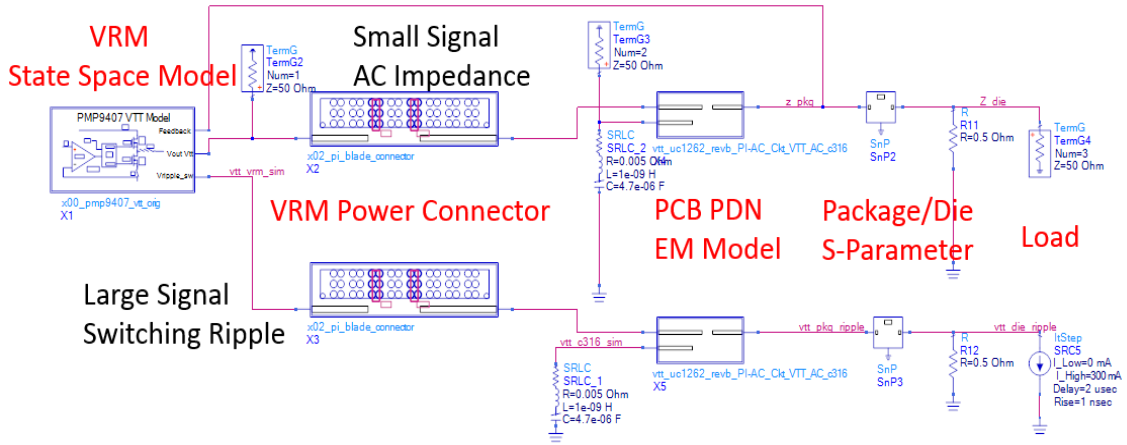
Modeling the Power Integrity Ecosystem

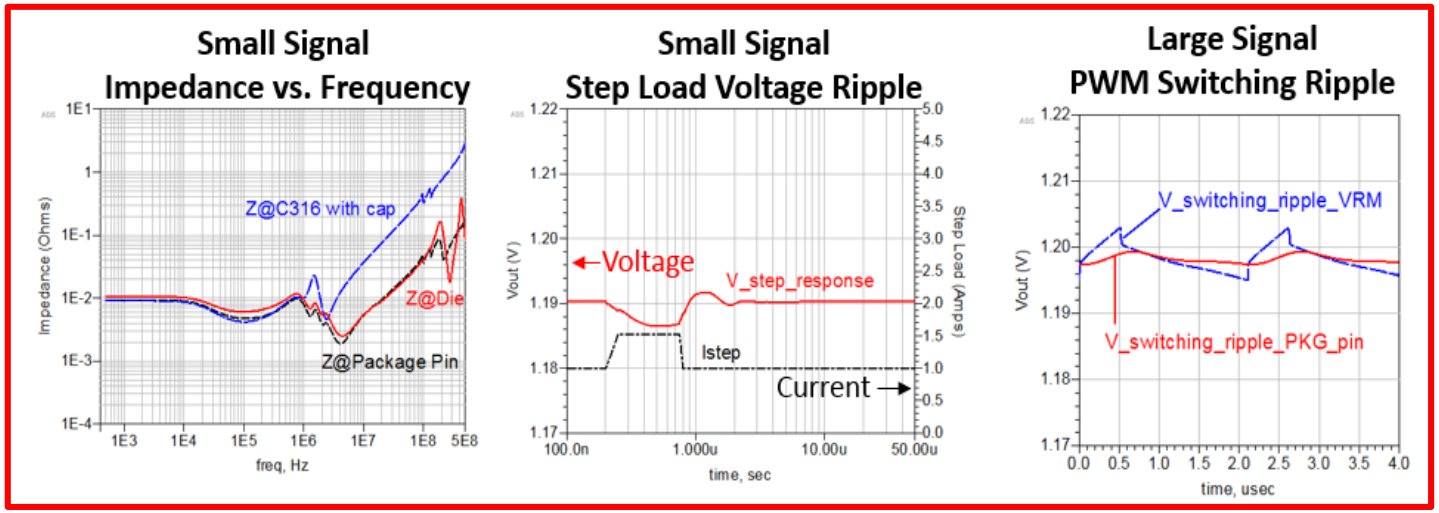
VRM + PDN + LOAD = PI ECOSYSTEM

Three Separate Simulations in one Schematic

Simulation Controllers

AC	S-PARAMETERS	HARMONIC BALANCE
AC	S_Param	HarmonicBalance
AC1	SP1	HB1
Start=100 Hz	Start=100 Hz	Freq[1]=Fs
Stop=40 MHz	Stop=40 MHz	Order[1]=256
Step=	Step=	

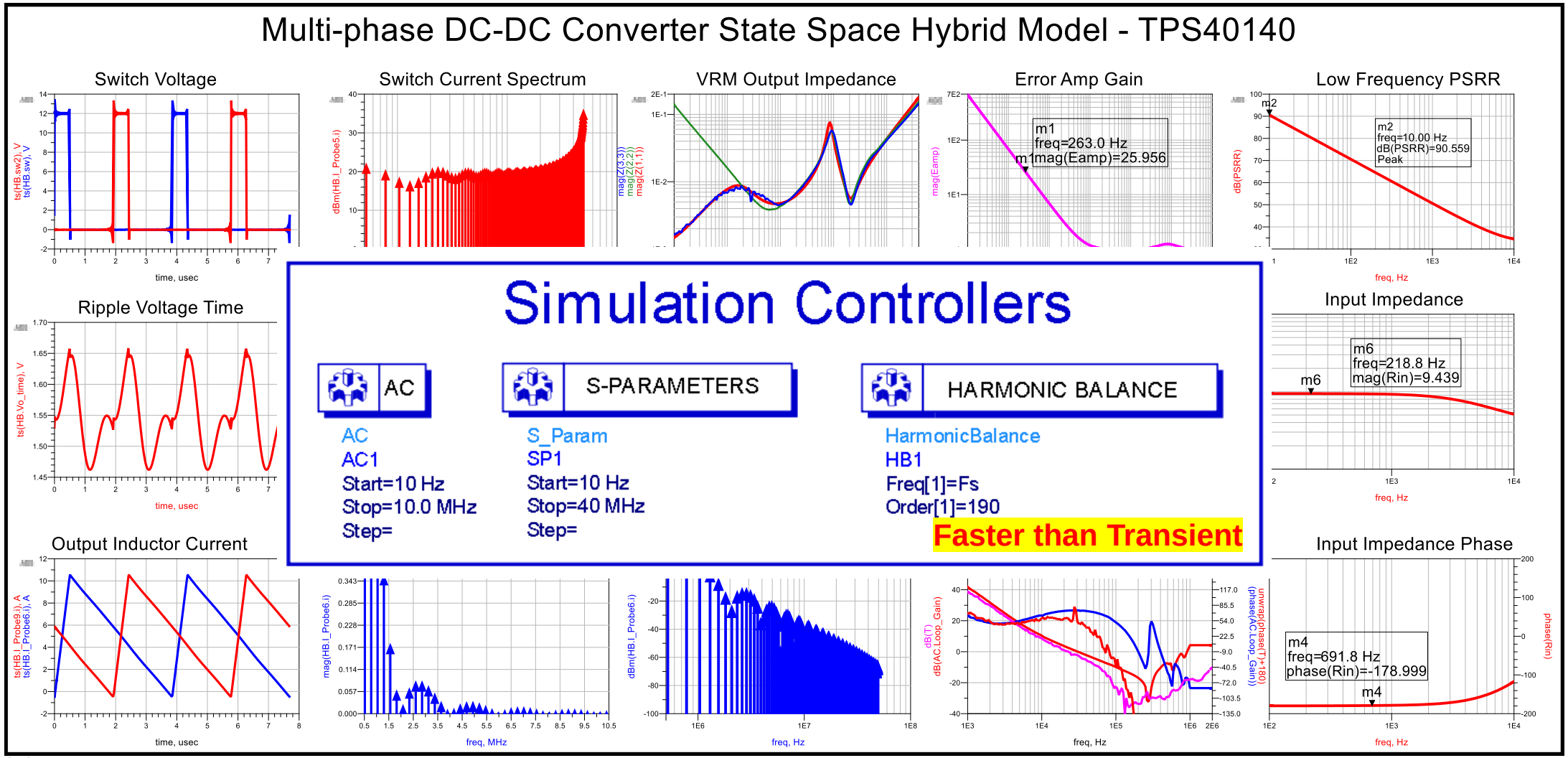




PI Simulation Demo with Harmonic Balance:

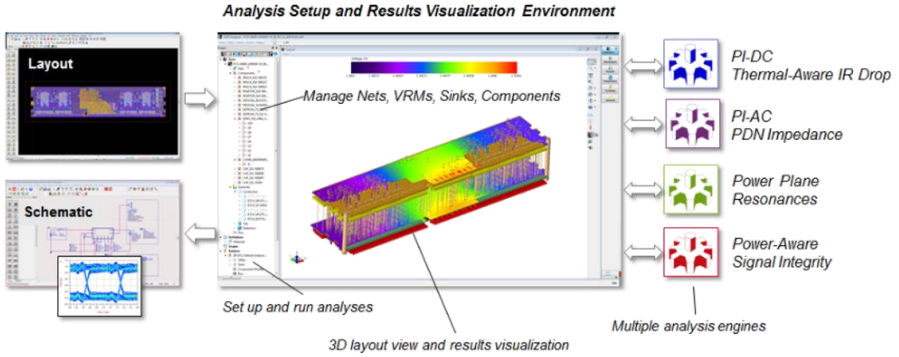
SMALL SIGNAL AC AND LARGE SIGNAL SWITCHING RIPPLE

ADS Schematic + Data Display

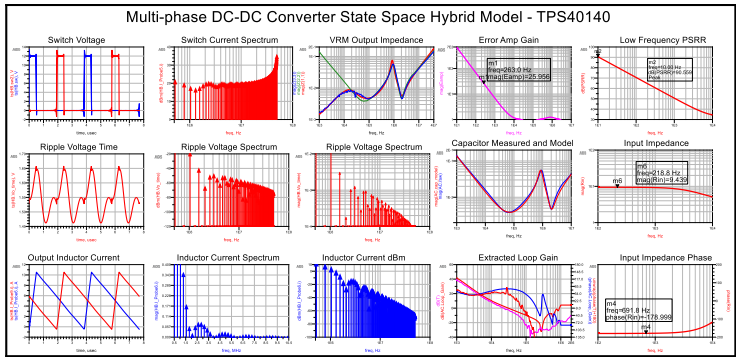


Power Integrity Simulation and Measurement Eco-System

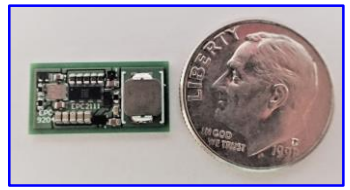
PathWave ADS PIPro
EM Models for DeCap Optimization



PathWave ADS PI Eco-System Simulations
Pre-Layout and Post Layout

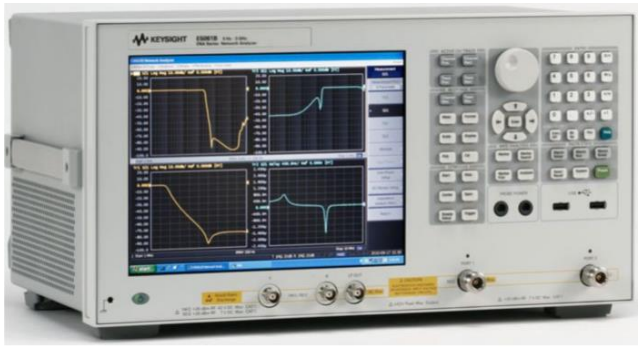


PE Next Generation GaN

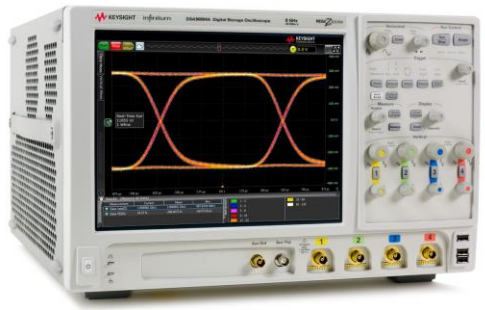


Reaching for 99% Efficiency
MHz Switching
Doubling the Power Density
> 1000 W/in³

E5061B for measuring *micro*-Ohms of Impedance



Infiniium Scope for Realtime Power Rail Diagnostics



CX33000 Current Analyzer for Load Transient Diagnostics

Picotest Accessories
PWR5061B PI Bundles

Summary

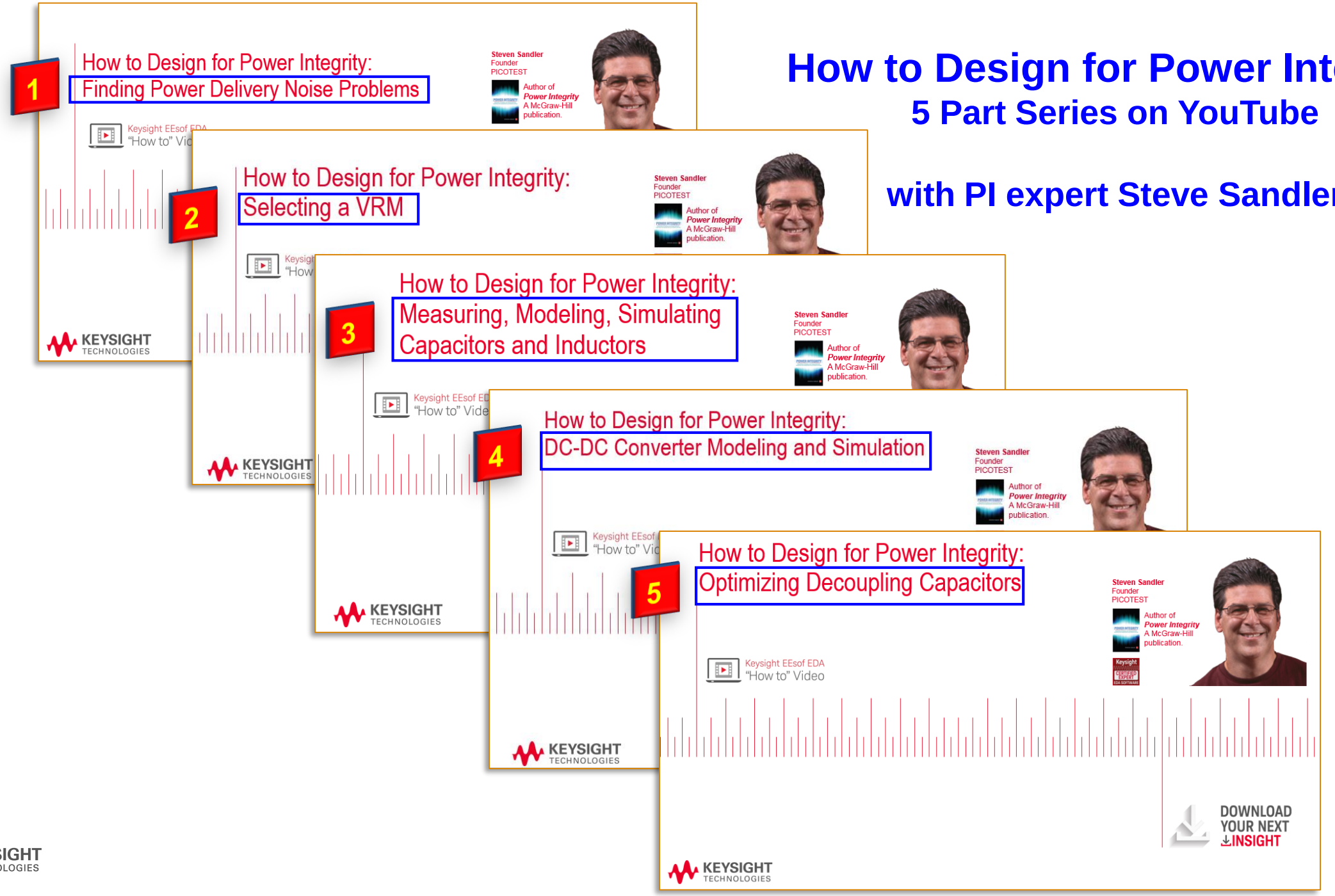
DESIGN METHODOLOGY FOR DECAP OPTIMIZATION

1. Calculate 1st order approximations

$$C_{bulk} = \frac{L_{supply}}{Z_{Target}^2} \qquad C_{decap} = \frac{ESL_{Cbulk}}{Z_{Target}^2} \qquad \text{Max } L_{PDN} = C_{pkg} * Z_{Target}^2$$

2. Decoupling capacitor optimization requires a Target Z input

3. Power Integrity Eco-System includes switching VRM models



How to Design for Power Integrity

5 Part Series on YouTube

with PI expert Steve Sandler

Hands-On Lab 1b: 190219_PI_Lab1b_Load_wrk.7zads

Basics – Instructor Led Demo

Transceiver Turn-on with ideal R-L PCB PDN

Frequency Domain Impedance and Time Domain Excitation for ripple

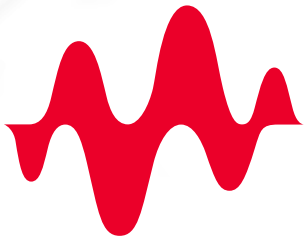
Explore –

Package Model Impedance

Impedance at Package Pin vs. Die

Advanced –

Tune C_total for a given Target Z profile



KEYSIGHT
TECHNOLOGIES