KEYSIGHT

# Validation at the Edge: Pre-Silicon

**As AI scales, data rates rise, and system complexity increases, validation must connect simulation, measurement, and manufacturing at scale across the entire engineering life cycle.**

Learn More in the Engineering at the Edge Webinar Series

Pre-Silicon | Lab | Network Traffic | Manufacturing

## Industry Advancements Driving Shifts in Pre-Silicon Validation

Data rates are doubling while signal margins collapse: DDR5 beyond 6400 MT/s, PCIe Gen7 at 128 GT/s, Ethernet to 1.6T, and optical at 448 Gbps. At 224G and beyond, power noise couples into signals and post-tape-out fixes become prohibitively expensive.

Today, validation must happen before silicon exists, using high-fidelity models that correlate with lab measurement. Here's how to evolve your workflows.

## 1 Simulate Across Domains Before Silicon Exists

Signal integrity, power integrity, and thermal effects interact in ways that can't be evaluated in isolation. Cross-domain simulation models circuit, electromagnetic, and thermal behavior simultaneously.

**The Keysight Solution**

Electronic Design Automation (EDA) Circuit Design and Simulation Software

Models circuit, EM, and thermal interactions simultaneously at sub-terahertz frequencies with Python API for workflow automation

## 2 Analyze Chiplet Signal and Link Margins Earlier

Multi-chiplet architectures with high bandwidth memory stacks require voltage transfer function analysis, forwarded clock architectures, and early link margin exploration.

**The Keysight Solution**

Chiplet PHY Designer

Provides voltage transfer function analysis and forwarded clock architecture support with signal integrity exploration tools to evaluate link margins earlier in the design cycle

## 3 Validate Against Industry Standards Early

PCIe Gen7, USB4v2, and multi-terabit Ethernet demand compliance validation before hardware exists. Standards-based simulation enables full-topology analysis for specific bus architectures.

**The Keysight Solution**

System Designer for PCIe

Supports Gen7 NRZ and PAM4 to validate compliance and signal integrity before tape-out

System Designer for USB

Validates USB4v2 PAM3 to assess link margins under power noise and channel loss

System Designer for Ethernet

Analyzes S-parameters for Ethernet channels and enables channel operating margin simulations

## 4 Automate and Correlate with Lab Measurement

Architectural simulation must connect with real-world signal validation. Correlating pre-silicon models with lab measurements closes the loop between design assumptions and actual behavior at 224G and beyond.

**The Keysight Solution**

M8199B Arbitrary Waveform Generator (AWG)

Generates link conditions at 256 GSa/s for PCIe, Ethernet, and AI interconnect validation

SX2-class DCA-M Sampling Oscilloscope

Delivers 224G/112 Gbd PAM4 measurement to validate 1.6T optical link performance

XR8-class Oscilloscope

Correlates pre-silicon simulation with lab measurements at collapsed signal margins

Find out how NTT Innovative Devices and Lumentum worked with Keysight on a high-speed signaling demonstration of 224 Gbaud / 448 Gbps at PAM4, laying the groundwork for 3.2T AI infrastructure.

Learn More