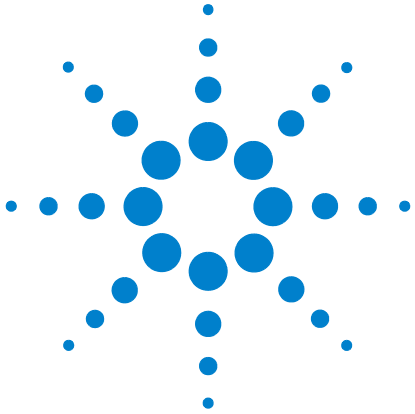

Agilent N6465A eMMC Compliance Test Application

Methods of Implementation

Agilent Technologies

Notices

Software Version

Version 01.00.0000 or greater

Edition

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eMMC Compliance Test Application — At a Glance

The Agilent N6465A eMMC Compliance Test Application is an eMMC test solution that covers the electrical timing parameters of the Joint Electronic Device Engineering Council (JEDEC) specifications (JESD84-B451). This application tests backwards compatible, single data rate, dual data rate, and HS200 clock speeds and their respective parameters.

The eMMC compliance test application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device-under-test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test.
- Provides detailed information of each test that has been run. The result of maximum 25 worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run. This report includes pass/fail limits, margin analysis, and screen shots.

The minimum number of probes required for the tests are:

- Clock tests – one probe
- CMD tests – two probes
- DAT tests – three probes

NOTE While only one probe (for clock tests) and two probes (for CMD tests) are required, for most efficient and continual testing, it is recommended to connect all three probes across three channels for all testing, so as to not have to connect between test groups.

Required Equipment and Software

In order to run the eMMC automated tests, you need the following equipment and software:

- N6465A eMMC Compliance Test Application software and license.
- The minimum version of Infiniium oscilloscope software (see the N6465A test application release notes).
- Infiniium 9000 or 90000 series oscilloscope.
- N5465A InfiniiSim Basic/Advanced software (optional).
- N2809A Precision Probe software (optional).
- Three active probes.
- Keyboard, qty = 1, (provided with the Infiniium oscilloscope).

- Mouse, qty = 1, (provided with the Infiniium oscilloscope).
- Agilent also recommends using a second monitor to view the compliance test application.

In This Book

This manual describes the tests that are performed by the eMMC compliance test application in more detail.

- Chapter 1, “Installing the eMMC Compliance Test Application” shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” shows how to start the eMMC compliance test application and gives a brief overview of how it is used.
- Chapter 3, “Bus Signal Levels Tests” shows how to run the eMMC bus signal levels tests available.
- Chapter 4, “Backwards Compatible Device Interface Timing Tests” shows how to run the eMMC backwards compatible device interface timing tests available.
- Chapter 5, “High-Speed Device Interface Timing Tests” shows how to run the eMMC high-speed device interface timing tests available.
- Chapter 6, “High-Speed Dual Rate Interface Timing Tests” shows how to run the eMMC high-speed dual rate interface timing tests available.
- Chapter 7, “HS200 Device Interface Timing Tests” shows how to run the eMMC HS200 device interface timing tests available.
- Chapter 8, “Debug Mode” shows how to use the Debug mode to make measurements on saved waveforms.
- Chapter 9, “Calibrating the Infiniium Oscilloscope and Probe” describes how to calibrate the oscilloscope in preparation for running the eMMC automated tests.
- Chapter 10, “InfiniiMax Probing” describes the probe amplifier and probe head recommendations for the eMMC compliance testing.

See Also

- The eMMC compliance test application’s online help, which describes:
  - Starting the eMMC compliance test application.
  - Creating or opening a test project.
  - Setting up the eMMC test environment.
  - Setting up InfiniiSim.
  - Setting up the precision probe/cable.
  - Setting up acquisition.
  - Selecting tests.
  - Configuring selected tests.
  - Defining compliance limits.
  - Connecting the oscilloscope to the DUT.

- Running tests.
- Automating the application.
- Viewing test results.
- Viewing/exporting/printing the HTML test report.
- Understanding the HTML report.
- Saving test projects.
- Installing/removing add-ins.
- Controlling the application via a remote PC.
- Using a second monitor for the application.

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10 InfiniiMax Probing

1 Installing the eMMC Compliance Test Application

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Installing the License Key 18

If you purchased the N6465A eMMC Compliance Test Application separate from your Infiniium oscilloscope, you need to install the software and license key.

Installing the Software

1. Make sure you have the minimum version of Infiniium oscilloscope software (see the N6465A release notes) by choosing **Help>About Infiniium...** from the main menu.
2. To obtain the eMMC Compliance Test Application, go to Agilent's website: http://www.agilent.com/find/N6465A.
3. The link for the eMMC Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application.

Installing the License Key

1. Request a license code from Agilent by following the instructions on the Entitlement Certificate.

   You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.
2. After you receive your license code from Agilent, choose **Utilities>Install Option License...**.
3. In the Install Option License dialog, enter your license code and click **Install License**.
4. Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application to complete the license installation.
5. Click **Close** to close the Install Option License dialog.
6. Choose **File>Exit**.
7. Restart the Infiniium oscilloscope application to complete the license installation.

2 Preparing to Take Measurements

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Before running the eMMC automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this application. After the oscilloscope and probe have been calibrated, you are ready to start the eMMC Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, see Chapter 9, “Calibrating the Infiniium Oscilloscope and Probe”.

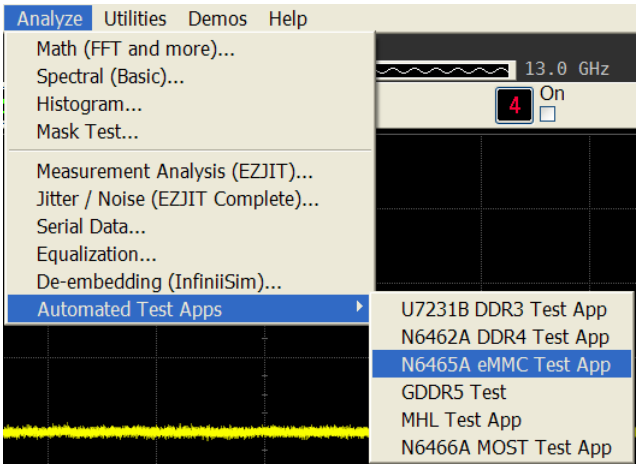
NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities>Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the eMMC Compliance Test Application

1 Ensure that the eMMC device-under-test (DUT) is performing read and write operations in the test and speed setup that you plan to test.

2 To start the eMMC Compliance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze > Automated Test Apps > N6465A eMMC Test App.**



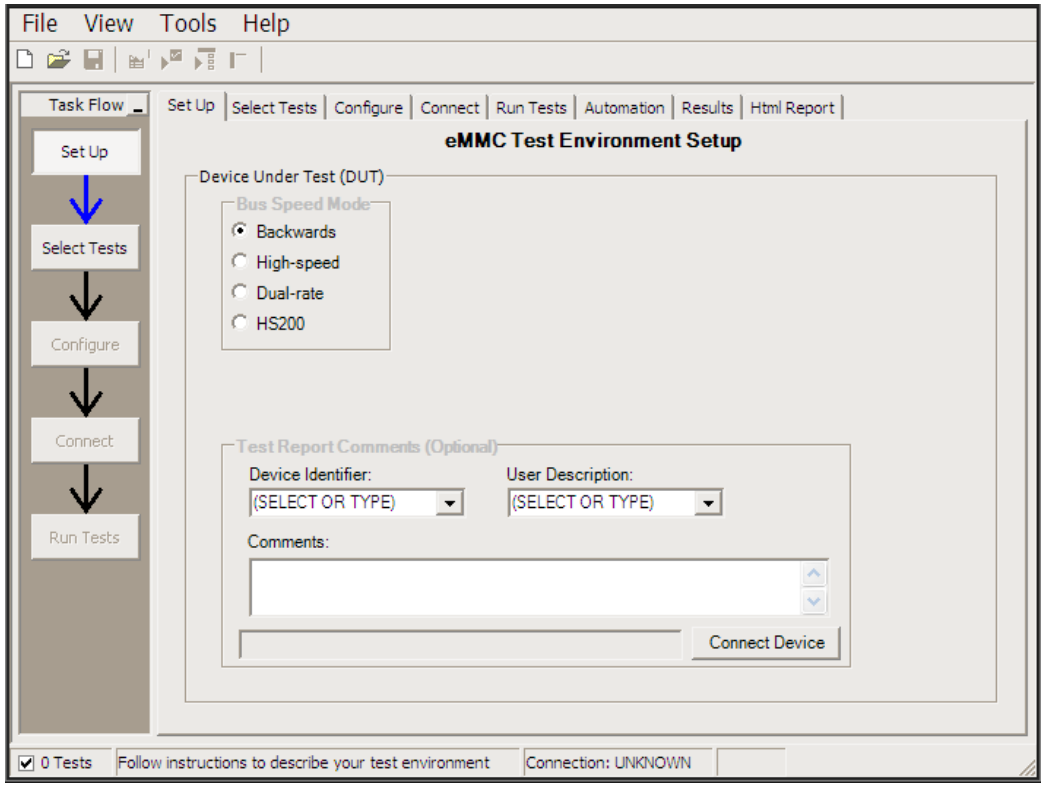


Figure 1 eMMC Compliance Test Application

NOTE If the N6465A eMMC Test App does not appear in the Automated Test Apps menu, the eMMC Compliance Test Application has not been installed (see Chapter 1, "Installing the eMMC Compliance Test Application").

Figure 1 shows the eMMC Compliance Test Application's main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device being tested. The "Device Identifier", "User Description", and "Comments" are all printed in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (i.e., channels used in the test, voltage levels).
Connect	Shows you how to connect the oscilloscope to the device-under-test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device-under-test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automation	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the eMMC Compliance Test Application, see its online help (which you can access by choosing **Help > Contents...** from the application's main menu).

The eMMC Compliance Test Application's online help describes:

- Starting the N6465A eMMC Compliance Test Application
  - To view/minimize the task flow pane
  - To view/hide the toolbar
- Creating or Opening a Test Project
  - To set load preferences
- Setting Up the Test Environment
- Setting Up InfiniiSim
- Setting Up the Precision Probe/Cable
- Setting Up Acquisition
- Selecting Tests
- Configuring Tests
- User-Defined Compliance Limits
- Connecting the Oscilloscope to the DUT
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This section provides the Methods of Implementation (MOIs) for the Bus Signal Level tests using an Agilent Infiniium oscilloscope and the N6465A eMMC Compliance Test Application.

Probing and Connection for Bus Signal Levels Tests

When performing the Bus Signal Levels tests, the eMMC Compliance Test Application will prompt you to make the proper connections. The connections for the Bus Signal Levels tests may look similar to the following diagram. Refer to the Connect tab in the eMMC Compliance Test Application for details.

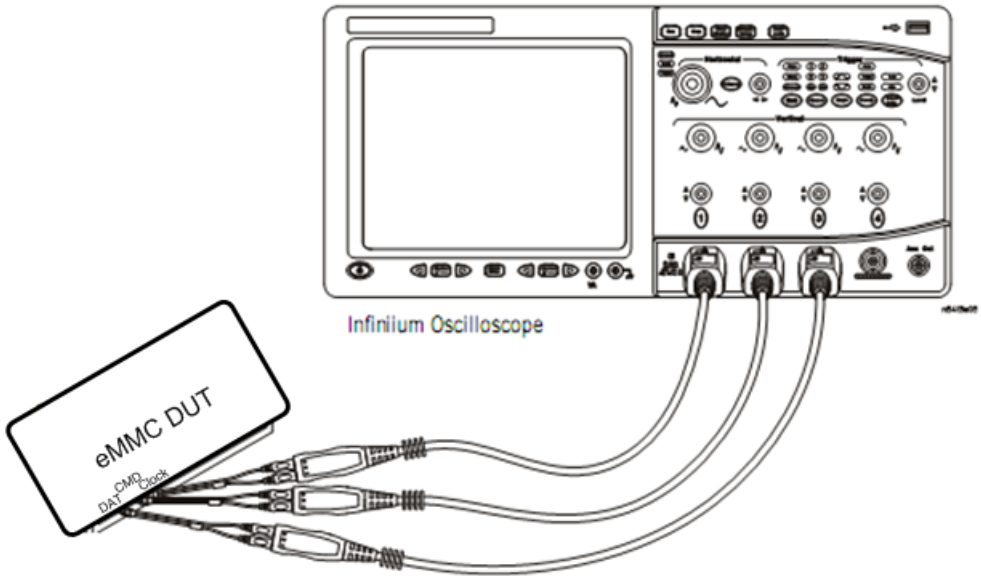

Figure 2 Probing for Bus Signal Levels Tests

You can use any of the oscilloscope channels as Pin-Under-Test (PUT) source channel. You can identify the channels used for each signal in the Configure tab of the eMMC Compliance Test Application. (The channels shown in Figure 2 are just examples.)

Test Procedure

1. Start the automated test application as described in "Starting the eMMC Compliance Test Application" on page 21.
2. Ensure that the eMMC device-under-test (DUT) is performing read and write operations in the test and speed setup that you plan to test.
3. Connect the probes to the PUTs on the eMMC DUT.
4. Connect the oscilloscope probes to the channels of the oscilloscope that you have set up in the Configure tab.
5. In the eMMC test application, click the Set Up tab.

6 Select the Bus Speed Mode that you plan to test.

NOTE The bus signal levels are the same for all Bus Speed Modes.

7 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

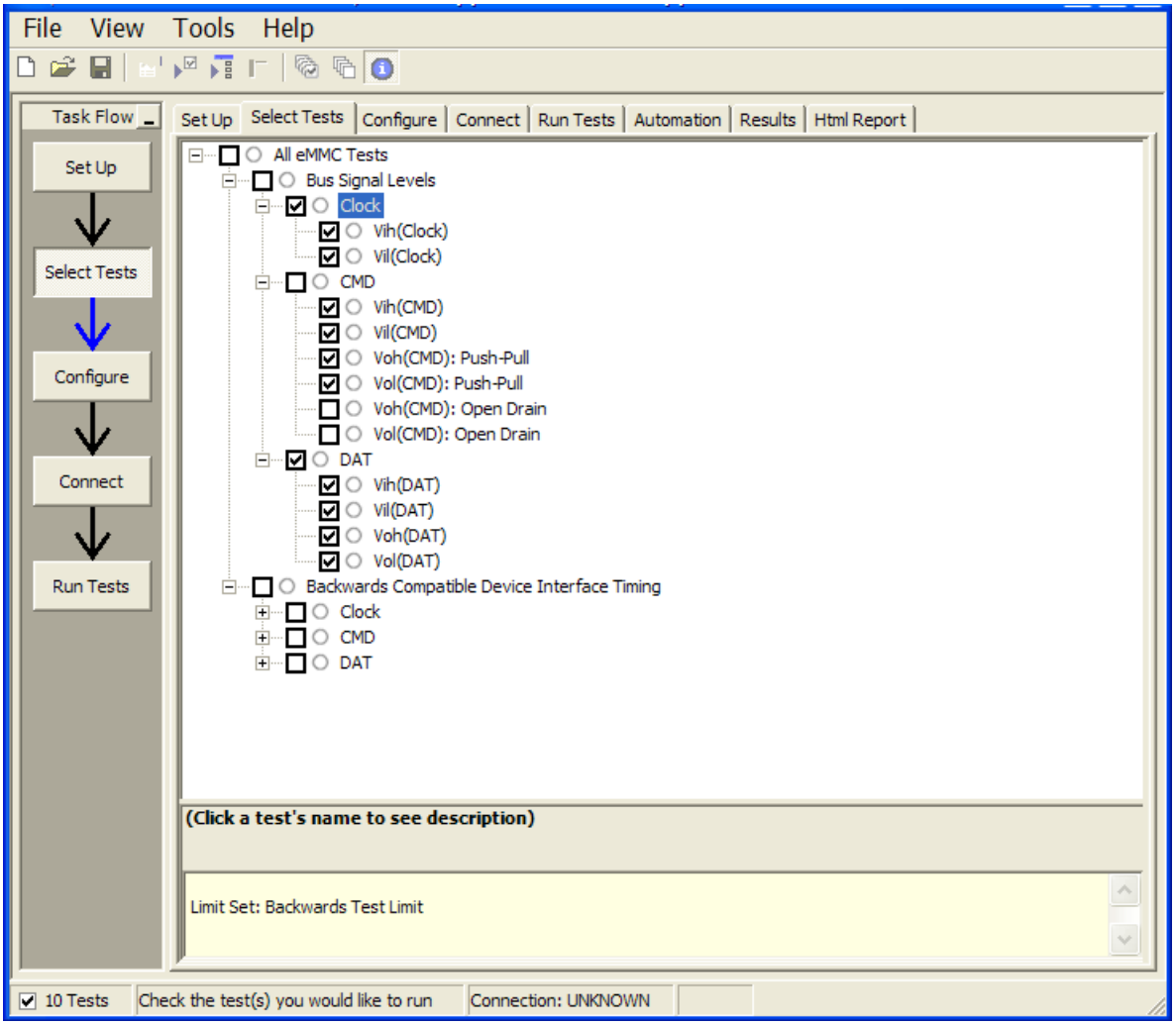

Figure 3 Selecting Bus Signal Levels Tests

Bus Signal Levels Specifications

Since there are various valid voltage supply options for the eMMC device, all input levels specifications are defined based on V_{CC} and V_{CCQ}. **It is important to set V_{cc} and V_{ccq} levels in the Configure tab to ensure the correct bus level test limits.** The following tables show the V_{IH}/V_{IL} test limits per voltage setting.

Table 1 Open-Drain Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	$V_{DD} - 0.2$		V	Note 1)*
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2 mA

* Note 1) Because V_{OH} depends on external resistance value (including outside the package), this value does not apply as device specification. The host is responsible to choose the external pull-up and open drain resistance value to meet the V_{OH} Min value. The input levels are identical with the push-pull mode bus signal levels.

Table 2 Push-Pull Signal Level — High Voltage *e*•MMC

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75 * V_{CCQ}		V	I_{OH} = –100 µA @ V_{CCQ} min
Output LOW voltage	V_{OL}		0.125 * V_{CCQ}	V	I_{OL} = 100 µA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 * V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.25 * V_{CCQ}	V	

Table 3 Push-Pull Signal Level — 1.70 –1.95 V_{CCQ} Voltage Range

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{CCQ} – 0.45 V		V	I_{OH} = –2 mA
Output LOW voltage	V_{OL}		0.45 V	V	I_{OL} = 2 mA
Input HIGH voltage	V_{IH}	0.65 * V_{CCQ}*	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.35 * V_{DD}†	V	

* 0.7 * V_{DD} for MMC4.3 and older revisions.

† 0.3 * V_{DD} for MMC4.3 and older revisions.

Table 4 Push-Pull Signal Level — 1.1 V –1.3 V V_{CCQ} Range *e*•MMC

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75 * V_{CCQ}		V	I_{OH} = –2 mA
Output LOW voltage	V_{OL}		0.25 * V_{CCQ}	V	I_{OL} = 2 mA
Input HIGH voltage	V_{IH}	0.65 * V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.35 * V_{CCQ}	V	

V_{IH} (Clock) Test Method of Implementation

The purpose of this test is to verify that the high level voltage value of the Clock Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The high level voltage value of the test signal should be greater than or equal to the min values specified in the tables under “Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency and set the memory depth to capture the number of clock edges specified in the Configure tab.
3. Perform a V_{MAX} measurement on the acquired signal.
4. Compare the V_{MAX} value to the specified value and report pass/fail and margin.

V_{IL} (Clock) Test Method of Implementation

The purpose of this test is to verify that the low level voltage value of the Clock Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The low level voltage value of the test signal should be greater than or equal to the min values specified in the tables under “Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency and set the memory depth to capture the number of clock edges specified in the Configure tab.
3. Perform a V_{MIN} measurement on the acquired signal.
4. Compare the V_{MIN} value to the specified value and report pass/fail and margin.

V_{IH} (CMD) Test Method of Implementation

The purpose of this test is to verify that the high level voltage value of the CMD Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The high level voltage value of the test signal should be greater than or equal to the min values specified in the tables under “Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Perform a V_{MAX} measurement on Function 1.
7. Compare the V_{MAX} value to the specified value and report pass/fail and margin.

V_{IL} (CMD) Test Method of Implementation

The purpose of this test is to verify that the low level voltage value of the CMD Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The low level voltage value of the test signal should be greater than or equal to the min values specified in the tables under “Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Perform a V_{MIN} measurement on Function 1.
7. Compare the V_{MIN} value to the specified value and report pass/fail and margin.

V_{OH} (CMD) Push-Pull and Open-Drain Test Method of Implementation

The purpose of this test is to verify that the output high level voltage value of the CMD Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab. Select the Push-Pull tests if CMD is set to the push-pull mode. Select the Open-Drain tests if CMD is set to the open-drain mode.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The high level voltage value of the test signal should be greater than or equal to the min values specified in the tables under "Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Perform a V_{MAX} measurement on Function 1.
7. Compare the V_{MAX} value to the specified value and report pass/fail and margin.

V_{OL} (CMD) Push-Pull and Open-Drain Test Method of Implementation

The purpose of this test is to verify that the output low level voltage value of the CMD Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab. Select the Push-Pull tests if CMD is set to the push-pull mode. Select the Open-Drain tests if CMD is set to the open-drain mode.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The low level voltage value of the test signal should be greater than or equal to the min values specified in the tables under "Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Perform a V_{MIN} measurement on Function 1.
7. Compare the V_{MIN} value to the specified value and report pass/fail and margin.

V_{IH} (DAT) Test Method of Implementation

The purpose of this test is to verify that the high level voltage value of the DAT Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The high level voltage value of the test signal should be greater than or equal to the min values specified in the tables under "Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Perform a V_{MAX} measurement on Function 1.
8. Compare the V_{MAX} value to the specified value and report pass/fail and margin.

V_{IL} (DAT) Test Method of Implementation

The purpose of this test is to verify that the low level voltage value of the DAT Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The low level voltage value of the test signal should be greater than or equal to the min values specified in the tables under "Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Perform a V_{MIN} measurement on Function 1.
8. Compare the V_{MIN} value to the specified value and report pass/fail and margin.

V_{OH} (DAT) Test Method of Implementation

The purpose of this test is to verify that the output high level voltage value of the DAT Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The high level voltage value of the test signal should be greater than or equal to the min values specified in the tables under "Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Perform a V_{MAX} measurement on Function 1.
8. Compare the V_{MAX} value to the specified value and report pass/fail and margin.

V_{OL} (DAT) Test Method of Implementation

The purpose of this test is to verify that the output low level voltage value of the DAT Test signal is within a valid voltage range. This range is defined by the V_{CC} and V_{CCQ} values set in the Configure tab.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Backwards, High-Speed, Dual-Rate, HS200

PASS Condition

The low level voltage value of the test signal should be greater than or equal to the min values specified in the tables under "Bus Signal Levels Specifications" on page 28. The signal should also be less than or equal to the max value specified in those tables.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
7. Perform a V_{MIN} measurement on Function 1.
8. Compare the V_{MIN} value to the specified value and report pass/fail and margin.

4 Backwards Compatible Device Interface Timing Tests

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This section provides the Methods of Implementation (MOIs) for the Backwards Compatible Device Interface Timing tests using an Agilent Infiniium oscilloscope and the N6465A eMMC Compliance Test Application.

Probing and Connection for Backwards Compatible Device Interface Timing Tests

When performing the Backwards Compatible Device Interface Timing tests, the eMMC Compliance Test Application will prompt you to make the proper connections. The connections for the Backwards Compatible Device Interface Timing tests may look similar to the following diagram. Refer to the Connect tab in the eMMC Compliance Test Application for details.

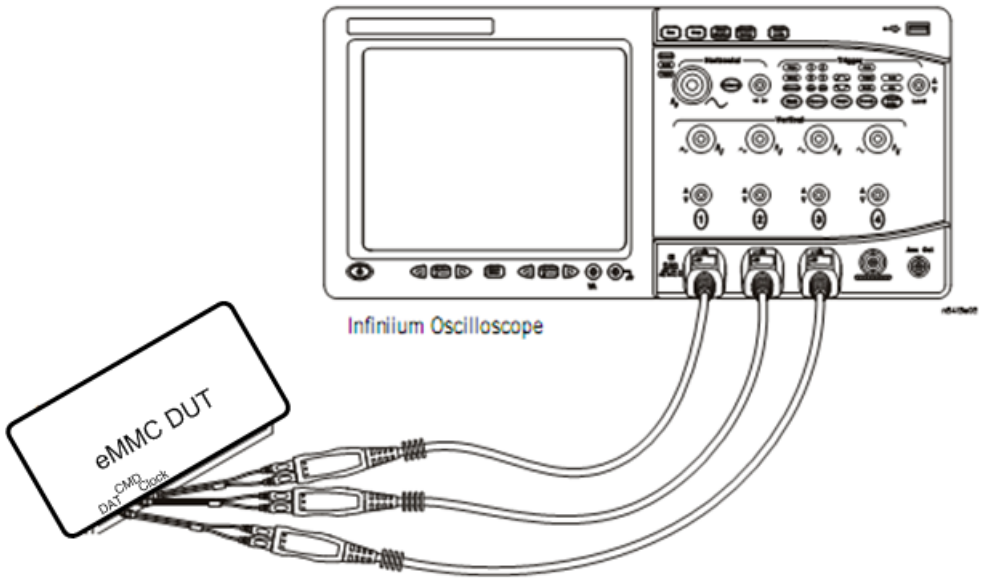

Figure 4 Probing for Backwards Compatible Device Interface Timing Tests

You can use any of the oscilloscope channels as Pin-Under-Test (PUT) source channel. You can identify the channels used for each signal in the Configure tab of the eMMC Compliance Test Application. (The channels shown in Figure 4 are just examples.)

Test Procedure

1. Start the automated test application as described in "Starting the eMMC Compliance Test Application" on page 21.
2. Ensure that the eMMC device-under-test (DUT) is performing read and write operations in the test and speed setup that you plan to test.
3. Connect the probes to the PUTs on the eMMC DUT.
4. Connect the oscilloscope probes to the channels of the oscilloscope that you have set up in the Configure tab.

5 In the eMMC test application, click the Set Up tab.

6 Select the Bus Speed Mode Backwards.

NOTE Selecting any of the other bus speed modes will still enable these tests because all devices should be backwards compatible.

7 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

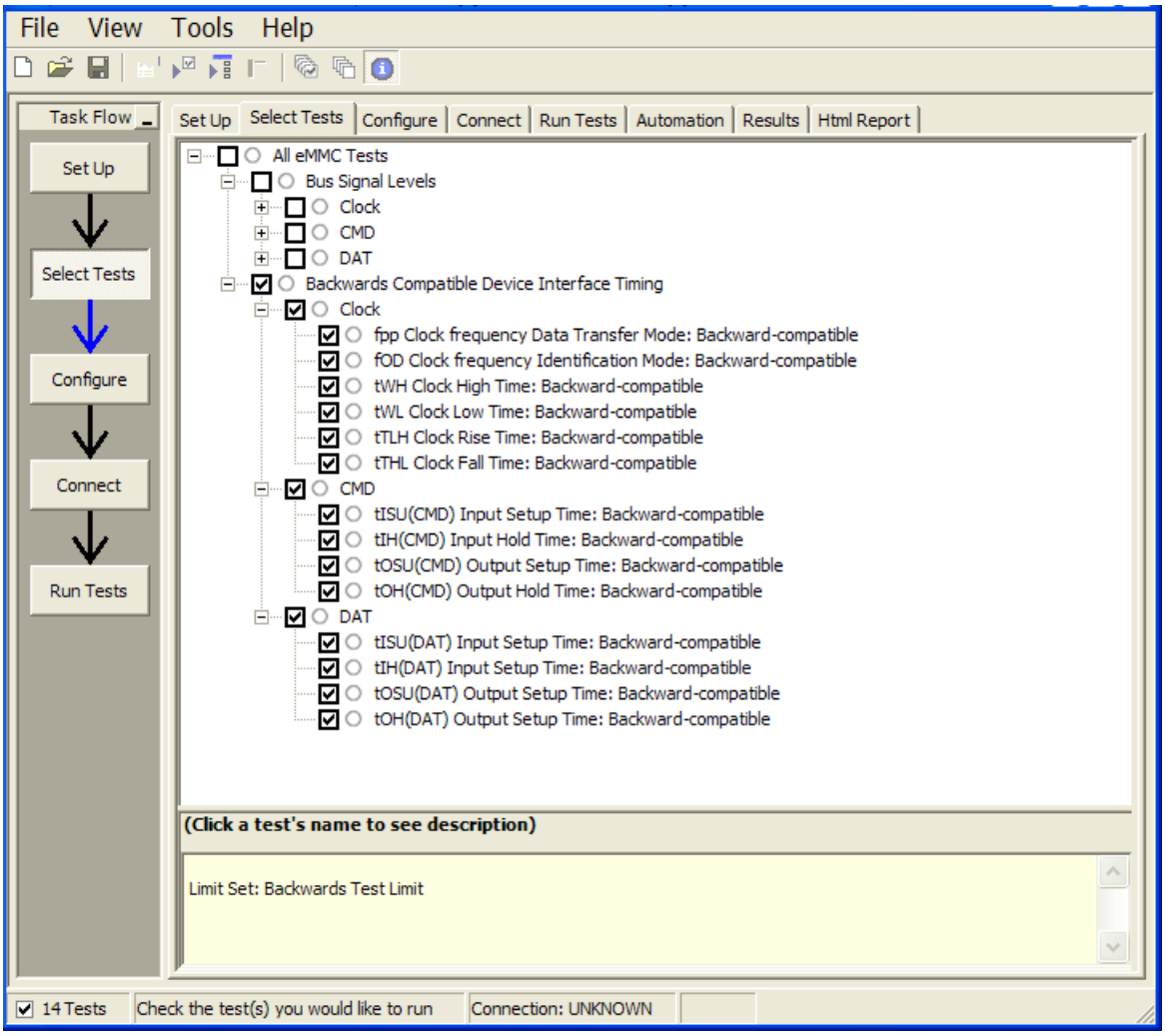

Figure 5 Selecting Backwards Compatible Device Interface Timing Tests

Backwards Compatible Device Interface Timing Specifications

Table 5 Backwards Compatible Device Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark[1]
Clock CLK[2]					
Clock frequency Data Transfer Mode (PP)[3]	f_{PP}	0	26	MHz	$C_L \leq 30$ pF
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	
Clock high time	t_{WH}	10			$C_L \leq 30$ pF
Clock low time	t_{WL}	10		ns	$C_L \leq 30$ pF
Clock rise time[4]	t_{TLH}		10	ns	$C_L \leq 30$ pF
Clock fall time	t_{THL}		10	ns	$C_L \leq 30$ pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	$C_L \leq 30$ pF
Input hold time	t_{IH}	3		ns	$C_L \leq 30$ pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time[5]	t_{OSU}	11.7		ns	$C_L \leq 30$ pF
Output hold time[5]	t_{OH}	8.3		ns	$C_L \leq 30$ pF

[1] The Device must always start with the backwards compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

[2] CLK timing is measured at 50% of V_{DD}.

[3] For compatibility with Devices that support the v4.2 standard or earlier, host should not use >26 MHz before switching to high-speed interface timing.

[4] CLK rise and fall times are measured by min (V_{IH}) and max (V_{IL}).

[5] t_{OSU} and t_{OH} are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backwards compatibility mode. Therefore, it is recommended for hosts either to set t_{WL} value as long as possible within the range which will not go over t_{CK}–t_{OH}(min) in the system or to use slow clock frequency, so that hosts could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation between t_{WL} and t_{OSU} or between t_{CK} and t_{OSU} for the device in its own datasheet as a note or its application notes.

Clock — f_{pp} Clock Frequency Data Transfer Mode Test Method of Implementation

The purpose of this test is to verify that the clock frequency remains between 0 and 26 MHz in Data Transfer Mode. Ensure that the eMMC DUT is in Data Transfer Mode.

Modes Supported

- Backwards

PASS Condition

The frequency of the clock is between 0 and 26 MHz across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a FREQuency measurement on Clock Channel at 50% on rising edges.
7. Compare the min FREQuency value to the specified value and report pass/fail and margin.

Clock — f_{OD} Clock Frequency Identification Mode Test Method of Implementation

The purpose of this test is to verify that the clock frequency remains between 0 and 400 kHz in Identification Mode. Ensure that the eMMC DUT is in Identification Mode.

Modes Supported

- Backwards

PASS Condition

The frequency of the clock is between 0 and 400 kHz across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a FREQuency measurement on Clock Channel at 50% on rising edges.
7. Compare the min FREQuency value to the specified value and report pass/fail and margin.

Clock — t_{WH} Clock High Time Test Method of Implementation

The purpose of this test is to verify that the clock high time is greater than 10 ns.

Modes Supported

- Backwards

PASS Condition

The clock high time is greater than or equal to 10 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a P_{WIDth} measurement on Clock Channel at 50%.
7. Compare the min P_{WIDth} value to the specified value and report pass/fail and margin.

Clock — t_{WL} Clock Low Time Test Method of Implementation

The purpose of this test is to verify that the clock low time is greater than 10 ns.

Modes Supported

- Backwards

PASS Condition

The clock low time is greater than or equal to 10 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform an N_{WIDth} measurement on Clock Channel at 50%.
7. Compare the min N_{WIDth} value to the specified value and report pass/fail and margin.

Clock — t_{TLH} Clock Rise Time Test Method of Implementation

The purpose of this test is to verify that the rise time is less than 10 ns.

Modes Supported

- Backwards

PASS Condition

The clock rise time is less than or equal to 10 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Rise Time measurement on the Clock Channel between V_{IL} to V_{IH} (V_{IL} and V_{IH} are defined by V_{CC}/V_{CCQ} as set in the Configure tab).
7. Compare the max Rise Time value to the specified value and report pass/fail and margin.

Clock — t_{THL} Clock Fall Time Test Method of Implementation

The purpose of this test is to verify that the fall time is less than 10 ns.

Modes Supported

- Backwards

PASS Condition

The clock fall time is less than or equal to 10 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Fall Time measurement on the Clock Channel between V_{IL} to V_{IH} (V_{IL} and V_{IH} are defined by V_{CC}/V_{CCQ} as set in the Configure tab).
7. Compare the max Fall Time value to the specified value and report pass/fail and margin.

t_{ISU} (CMD) Input Setup Time Test Method of Implementation

The purpose of this test is to verify that the input setup time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- Backwards

PASS Condition

The setup time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Measure the rising edge of Function 1 at V_{IH} to Clock rising at 50%.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the falling edge of Function 1 at V_{IL} to Clock rising at 50%.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{IH} (CMD) Input Hold Time Test Method of Implementation

The purpose of this test is to verify that the input hold time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- Backwards

PASS Condition

The hold time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Measure the Clock rising at 50% to the Function 1 rising at V_{IL}.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the Clock rising at 50% to the Function 1 falling at V_{IH}.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{OS} (CMD) Output Setup Time Test Method of Implementation

The purpose of this test is to verify that the output setup time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- Backwards

PASS Condition

The output setup time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 11.7 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low – start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the rising edge of Function 1 at V_{OH} to Clock rising at 50%.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the falling edge of Function 1 at V_{OL} to Clock rising at 50%.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{OH} (CMD) Output Hold Time Test Method of Implementation

The purpose of this test is to verify that the output hold time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- Backwards

PASS Condition

The output hold time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 8.3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low – start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the Clock rising at 50% to the Function 1 rising at V_{OL}.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the Clock rising at 50% to the Function 1 falling at V_{OH}.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{ISU} (DAT) Input Setup Time Test Method of Implementation

The purpose of this test is to verify that the input setup time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Backwards

PASS Condition

The setup time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Measure the rising edge of Function 1 at V_{IH} to Clock rising at 50%.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the falling edge of Function 1 at V_{IL} to Clock rising at 50%.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{IH} (DAT) Input Hold Time Test Method of Implementation

The purpose of this test is to verify that the input hold time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Backwards

PASS Condition

The hold time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Measure the Clock rising at 50% to the Function 1 rising at V_{IL}.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the Clock rising at 50% to the Function 1 falling at V_{IH}.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{OS} (DAT) Output Setup Time Test Method of Implementation

The purpose of this test is to verify that the output setup time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Backwards

PASS Condition

The output setup time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 11.7 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full read cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Measure the rising edge of Function 1 at V_{OH} to Clock rising at 50%.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the falling edge of Function 1 at V_{OL} to Clock rising at 50%.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{OH} (DAT) Output Hold Time Test Method of Implementation

The purpose of this test is to verify that the output hold time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Backwards

PASS Condition

The output hold time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 8.3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Measure the Clock rising at 50% to the Function 1 rising at V_{OL}.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the Clock rising at 50% to the Function 1 falling at V_{OH}.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

5 High-Speed Device Interface Timing Tests

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This section provides the Methods of Implementation (MOIs) for the High-Speed Device Interface Timing tests using an Agilent Infiniium oscilloscope and the N6465A eMMC Compliance Test Application.

Probing and Connection for High-Speed Device Interface Timing Tests

When performing the High-Speed Device Interface Timing tests, the eMMC Compliance Test Application will prompt you to make the proper connections. The connections for the High-Speed Device Interface Timing tests may look similar to the following diagram. Refer to the Connect tab in the eMMC Compliance Test Application for details.

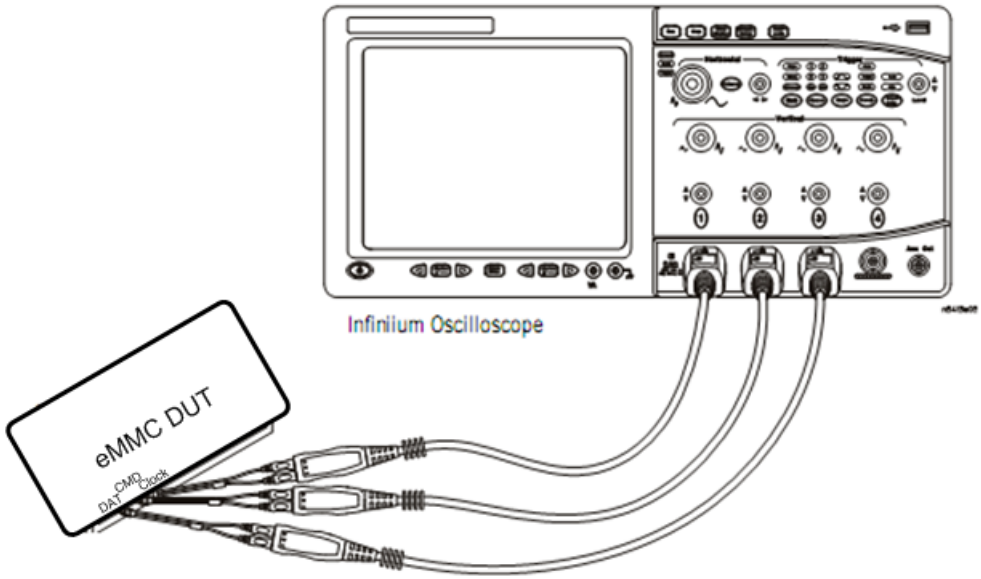

Figure 6 Probing for High-Speed Device Interface Timing Tests

You can use any of the oscilloscope channels as Pin-Under-Test (PUT) source channel. You can identify the channels used for each signal in the Configure tab of the eMMC Compliance Test Application. (The channels shown in Figure 6 are just examples.)

Test Procedure

1. Start the automated test application as described in "Starting the eMMC Compliance Test Application" on page 21.
2. Ensure that the eMMC device-under-test (DUT) is performing read and write operations in the test and speed setup that you plan to test.
3. Connect the probes to the PUTs on the eMMC DUT.
4. Connect the oscilloscope probes to the channels of the oscilloscope that you have set up in the Configure tab.
5. In the eMMC test application, click the Set Up tab.

6 Select the Bus Speed Mode High-speed.

NOTE Selecting Dual-rate will also enable these tests, since they are required to meet specification even on dual-rate devices.

7 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

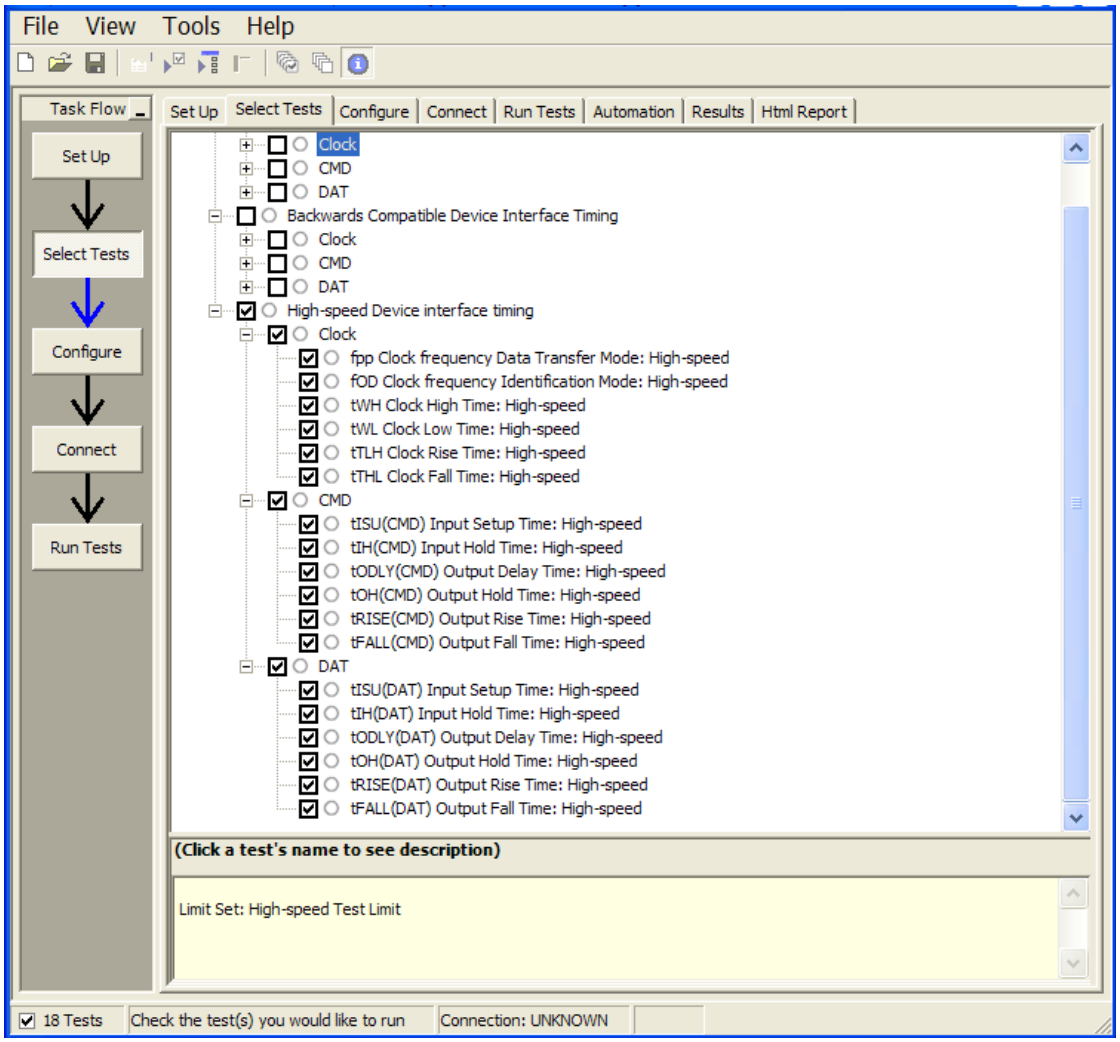

Figure 7 Selecting High-Speed Device Interface Timing Tests

High-Speed Device Interface Timing Specifications

Table 6 High-Speed Device Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	f_{PP}	0	52[3]	MHz	$C_L \leq 30$ pF Tolerance: +100 kHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20 kHz
Clock high time	t_{WH}	6.5		ns	$C_L \leq 30$ pF
Clock low time	t_{WL}	6.5		ns	$C_L \leq 30$ pF
Clock rise time[4]	t_{TLH}		3	ns	$C_L \leq 30$ pF
Clock fall time	t_{THL}		3	ns	$C_L \leq 30$ pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	$C_L \leq 30$ pF
Input hold time	t_{IH}	3		ns	$C_L \leq 30$ pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t_{ODLY}		13.7	ns	$C_L \leq 30$ pF
Output hold time	t_{OH}	2.5		ns	$C_L \leq 30$ pF
Signal rise time[5]	t_{RISE}		3	ns	$C_L \leq 30$ pF
Signal fall time	t_{FALL}		3	ns	$C_L \leq 30$ pF

[1] CLK timing is measured at 50% of V_{DD}.

[2] A *e*•MMC shall support the full frequency range from 0 - 26 MHz, or 0 - 52 MHz.

[3] Device can operate as high-speed Device interface timing at 26 MHz clock frequency.

[4] CLK rise and fall times are measured by min (V_{IH}) and max (V_{IL}).

[5] Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

Clock — f_{pp} Clock Frequency Data Transfer Mode Test Method of Implementation

The purpose of this test is to verify that the clock frequency remains between 0 and 52 MHz in Data Transfer Mode. Ensure that the eMMC DUT is in Data Transfer Mode.

Modes Supported

- High-Speed

PASS Condition

The frequency of the clock is between 0 and 52 MHz across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a FREQuency measurement on Clock Channel at 50% on rising edges.
7. Compare the min FREQuency value to the specified value and report pass/fail and margin.

Clock — f_{OD} Clock Frequency Identification Mode Test Method of Implementation

The purpose of this test is to verify that the clock frequency remains between 0 and 400 kHz in Identification Mode. Ensure that the eMMC DUT is in Identification Mode.

Modes Supported

- High-Speed

PASS Condition

The frequency of the clock is between 0 and 400 kHz across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a FREQuency measurement on Clock Channel at 50%.
7. Compare the min FREQuency value to the specified value and report pass/fail and margin.

Clock — t_{WH} Clock High Time Test Method of Implementation

The purpose of this test is to verify that the clock high time is greater than 6.5 ns.

Modes Supported

- High-Speed

PASS Condition

The clock high time is greater than or equal to 6.5 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a P_{WIDth} measurement on Clock Channel at 50%.
7. Compare the min P_{WIDth} value to the specified value and report pass/fail and margin.

Clock — t_{WL} Clock Low Time Test Method of Implementation

The purpose of this test is to verify that the clock low time is greater than 6.5 ns.

Modes Supported

- High-Speed

PASS Condition

The clock low time is greater than or equal to 6.5 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform an N_{WIDth} measurement on Clock Channel at 50%.
7. Compare the min N_{WIDth} value to the specified value and report pass/fail and margin.

Clock — t_{TLH} Clock Rise Time Test Method of Implementation

The purpose of this test is to verify that the rise time is less than 3 ns.

Modes Supported

- High-Speed

PASS Condition

The clock rise time is less than or equal to 3 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Rise Time measurement on the Clock Channel between V_{IL} to V_{IH} (V_{IL} and V_{IH} are defined by V_{CC}/V_{CCQ} as set in the Configure tab).
7. Compare the max Rise Time value to the specified value and report pass/fail and margin.

Clock — t_{THL} Clock Fall Time Test Method of Implementation

The purpose of this test is to verify that the fall time is less than 3 ns.

Modes Supported

- High-Speed

PASS Condition

The clock fall time is less than or equal to 3 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Fall Time measurement on the Clock Channel between V_{IL} to V_{IH} (V_{IL} and V_{IH} are defined by V_{CC}/V_{CCQ} as set in the Configure tab).
7. Compare the max Fall Time value to the specified value and report pass/fail and margin.

t_{ISU} (CMD) Input Setup Time Test Method of Implementation

The purpose of this test is to verify that the input setup time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- High-Speed

PASS Condition

The setup time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Measure the rising edge of Function 1 at V_{IH} to Clock rising at 50%.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the falling edge of Function 1 at V_{IL} to Clock rising at 50%.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{IH} (CMD) Input Hold Time Test Method of Implementation

The purpose of this test is to verify that the input hold time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- High-Speed

PASS Condition

The hold time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Measure the Clock rising at 50% to the Function 1 rising at V_{IL}.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the Clock rising at 50% to the Function 1 falling at V_{IH}.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{ODLY} (CMD) Output Delay Time Test Method of Implementation

The purpose of this test is to verify that the output delay time of the CMD Test signal relative to the rising edge of the Clock is less than or equal to the specified value.

Modes Supported

- High-Speed

PASS Condition

The output delay time of the CMD test signal relative to the rising edge of the clock is less than or equal to 13.7 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the rising edge of Function 1 at V_{OH} to Clock rising at 50%.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the falling edge of Function 1 at V_{OL} to Clock rising at 50%.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{OH} (CMD) Output Hold Time Test Method of Implementation

The purpose of this test is to verify that the output hold time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- High-Speed

PASS Condition

The output hold time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 2.5 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low – start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the Clock rising at 50% to the Function 1 rising at V_{OL}.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the Clock rising at 50% to the Function 1 falling at V_{OH}.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{RISE} (CMD) Output Rise Time Test Method of Implementation

The purpose of this test is to verify that the output rise time of the CMD Test signal is less than or equal to the specified value.

Modes Supported

- High-Speed

PASS Condition

The output rise time of the CMD test signal is less than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low – start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the Function 1 rise time from V_{OL} to V_{OH}.

NOTE V_{OL} and V_{OH} are defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Compare the max Rise Time value to the specified value and report pass/fail and margin.

t_{FALL} (CMD) Output Fall Time Test Method of Implementation

The purpose of this test is to verify that the output fall time of the CMD Test signal is less than or equal to the specified value.

Modes Supported

- High-Speed

PASS Condition

The output fall time of the CMD test signal is less than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low – start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the Function 1 fall time from V_{OL} to V_{OH}.

NOTE V_{OL} and V_{OH} are defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Compare the max Fall Time value to the specified value and report pass/fail and margin.

t_{ISU} (DAT) Input Setup Time Test Method of Implementation

The purpose of this test is to verify that the input setup time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- High-Speed

PASS Condition

The setup time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Measure the rising edge of Function 1 at V_{IH} to Clock rising at 50%.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the falling edge of Function 1 at V_{IL} to Clock rising at 50%.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{IH} (DAT) Input Hold Time Test Method of Implementation

The purpose of this test is to verify that the input hold time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- High-Speed

PASS Condition

The hold time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Measure the Clock rising at 50% to the Function 1 rising at V_{IL}.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the Clock rising at 50% to the Function 1 falling at V_{IH}.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{ODLY} (DAT) Output Delay Time Test Method of Implementation

The purpose of this test is to verify that the output delay time of the DAT Test signal relative to the rising edge of the Clock is less than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- High-Speed

PASS Condition

The output delay time of the DAT test signal relative to the rising edge of the clock is less than or equal to 13.7 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full read cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Measure the rising edge of Function 1 at V_{OH} to Clock rising at 50%.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the falling edge of Function 1 at V_{OL} to Clock rising at 50%.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{OH} (DAT) Output Hold Time Test Method of Implementation

The purpose of this test is to verify that the output hold time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- High-Speed

PASS Condition

The output hold time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 2.5 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Measure the Clock rising at 50% to the Function 1 rising at V_{OL}.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the Clock rising at 50% to the Function 1 falling at V_{OH}.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{RISE} (DAT) Output Rise Time Test Method of Implementation

The purpose of this test is to verify that the output rise time of the DAT Test signal less than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- High- Speed

PASS Condition

The output rise time of the DAT test signal is less than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low — start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles — six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Measure Rise Time from V_{OL} to V_{OH} on Function 1.

NOTE V_{OL} and V_{OH} are defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the max Rise Time value to the specified value and report pass/fail and margin.

t_{FALL} (DAT) Output Fall Time Test Method of Implementation

The purpose of this test is to verify that the output fall time of the DAT Test signal is less than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- High-Speed

PASS Condition

The output fall time of the DAT test signal is less than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Measure Fall Time from V_{OL} to V_{OH} on Function 1.

NOTE V_{OL} and V_{OH} are defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the max Fall Time value to the specified value and report pass/fail and margin.

6 High-Speed Dual Rate Interface Timing Tests

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This section provides the Methods of Implementation (MOIs) for the High-Speed Dual Rate Interface Timing tests using an Agilent Infiniium oscilloscope and the N6465A eMMC Compliance Test Application.

Probing and Connection for High-Speed Dual Rate Interface Timing Tests

When performing the High-Speed Dual Rate Interface Timing tests, the eMMC Compliance Test Application will prompt you to make the proper connections. The connections for the High-Speed Dual Rate Interface Timing tests may look similar to the following diagram. Refer to the Connect tab in the eMMC Compliance Test Application for details.

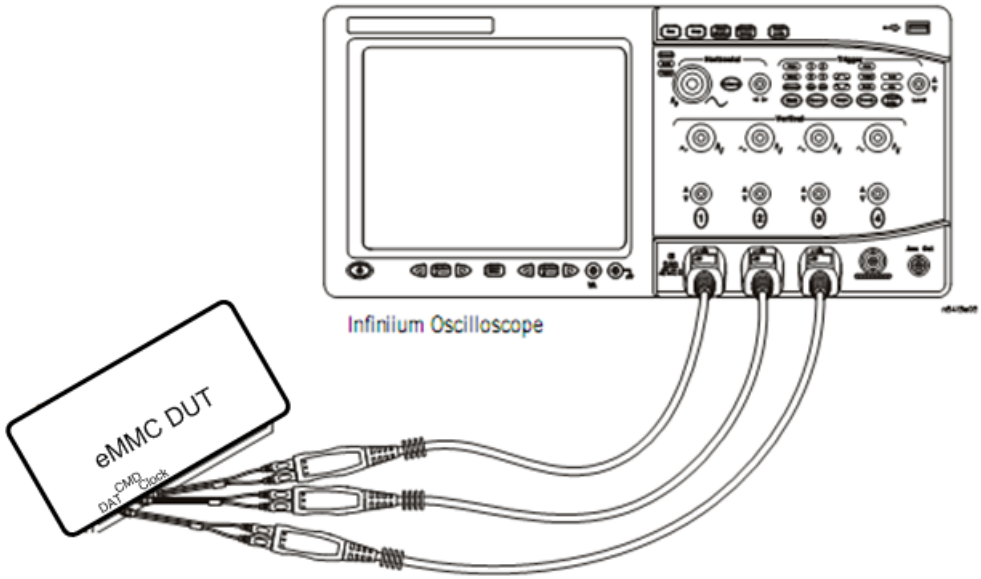

Figure 8 Probing for High-Speed Dual Rate Interface Timing Tests

You can use any of the oscilloscope channels as Pin-Under-Test (PUT) source channel. You can identify the channels used for each signal in the Configure tab of the eMMC Compliance Test Application. (The channels shown in Figure 8 are just examples.)

Test Procedure

1. Start the automated test application as described in "Starting the eMMC Compliance Test Application" on page 21.
2. Ensure that the eMMC device-under-test (DUT) is performing read and write operations in the test and speed setup that you plan to test.
3. Connect the probes to the PUTs on the eMMC DUT.
4. Connect the oscilloscope probes to the channels of the oscilloscope that you have set up in the Configure tab.
5. In the eMMC test application, click the Set Up tab.

6 Select the Bus Speed Mode Dual-rate.

7 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

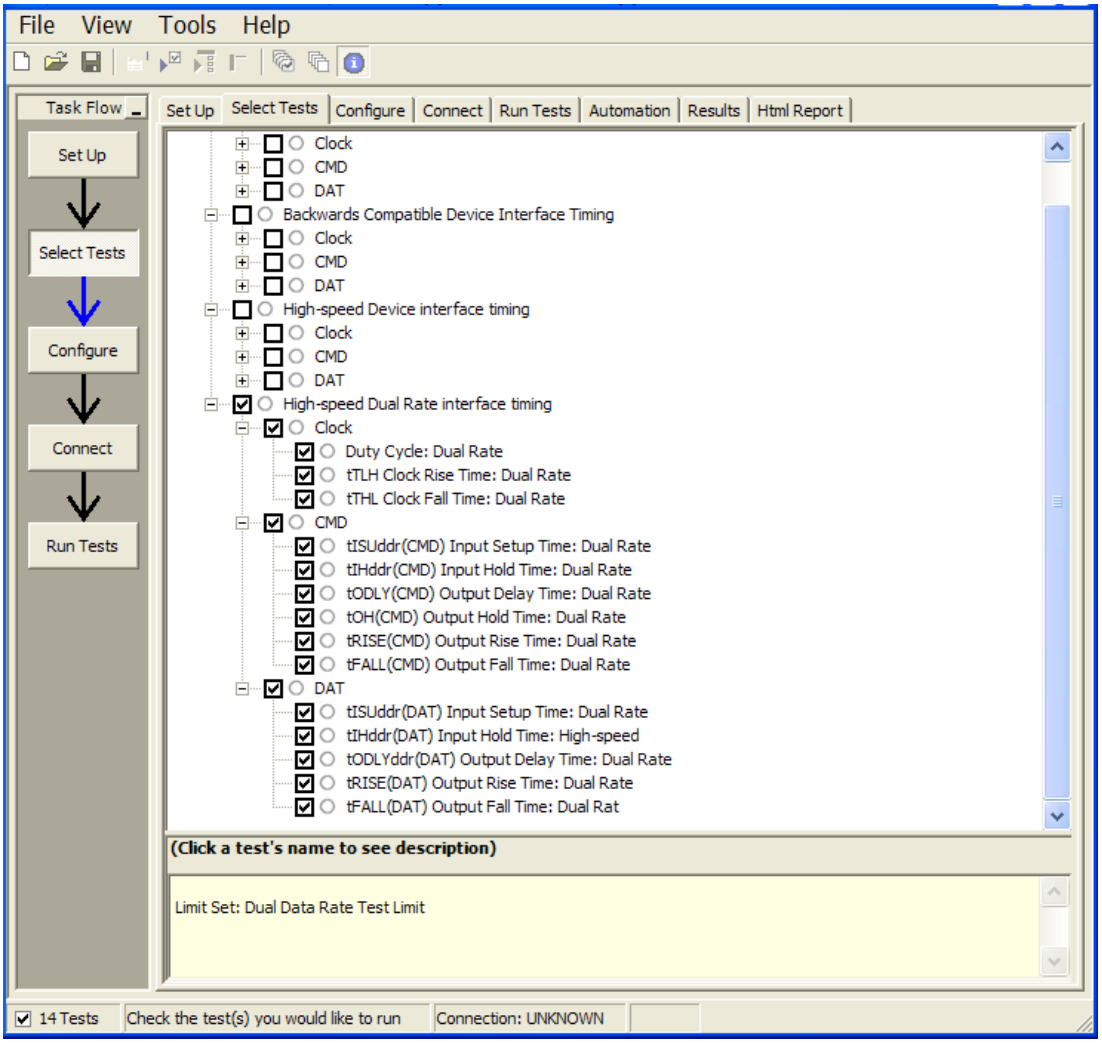

Figure 9 Selecting High-Speed Dual Rate Interface Timing Tests

High-Speed Dual Rate Interface Timing Specifications

Table 7 High-Speed Dual Rate Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Clock rise time	t_{TLH}		3	ns	$C_L \leq 30$ pF
Clock fall time	t_{THL}		3	ns	$C_L \leq 30$ pF
Input CMD (referenced to CLK-SDR mode)					
Input set-up time	t_{ISUddr}	3		ns	$C_L \leq 20$ pF
Input hold time	t_{IHddr}	3		ns	$C_L \leq 20$ pF
Output CMD (referenced to CLK-SDR mode)					
Output delay time during data transfer	t_{ODLY}		13.7	ns	$C_L \leq 20$ pF
Output hold time	t_{OH}	2.5		ns	$C_L \leq 20$ pF
Signal rise time	t_{RISE}		3	ns	$C_L \leq 20$ pF
Signal fall time	t_{FALL}		3	ns	$C_L \leq 20$ pF
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	t_{ISUddr}	2.5		ns	$C_L \leq 20$ pF
Input hold time	t_{IHddr}	2.5		ns	$C_L \leq 20$ pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	$t_{ODLYddr}$	1.5	7	ns	$C_L \leq 20$ pF
Signal rise time (DAT0-7)[2]	t_{RISE}		2	ns	$C_L \leq 20$ pF
Signal fall time (DAT0-7)	t_{FALL}		2	ns	$C_L \leq 20$ pF

[1] CLK timing is measured at 50% of V_{DD}.

[2] Inputs DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

Clock — Duty Cycle Test Method of Implementation

The purpose of this test is to verify that the clock Duty Cycle remains in the specified limits.

Modes Supported

- Dual-Rate

PASS Condition

The duty cycle of the clock is between 45-55% across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Duty Cycle measurement on both edges of the Clock Channel at 50%.
7. Compare the worst case value to the specified value and report pass/fail and margin.

Clock — t_{TLH} Clock Rise Time Test Method of Implementation

The purpose of this test is to verify that the rise time is less than or equal to the specified value.

Modes Supported

- Dual-Rate

PASS Condition

The clock rise time is less than or equal to 3 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Rise Time measurement on the Clock Channel between V_{IL} to V_{IH} (V_{IL} and V_{IH} are defined by V_{CC}/V_{CCQ} as set in the Configure tab).
7. Compare the maximum Rise Time value to the specified value and report pass/fail and margin.

Clock — t_{THL} Clock Fall Time Test Method of Implementation

The purpose of this test is to verify that the fall time is less than or equal to the specified value.

Modes Supported

- Dual-Rate

PASS Condition

The clock fall time is less than or equal to 3 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Fall Time measurement on the Clock Channel between V_{IL} to V_{IH} (V_{IL} and V_{IH} are defined by V_{CC}/V_{CCQ} as set in the Configure tab).
7. Compare the maximum Fall Time value to the specified value and report pass/fail and margin.

t_{ISUddr} (CMD) Input Setup Time Test Method of Implementation

The purpose of this test is to verify that the input setup time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- Dual-Rate

PASS Condition

The setup time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Measure the rising edge of Function 1 at V_{IH} to Clock rising at 50%.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the falling edge of Function 1 at V_{IL} to Clock rising at 50%.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

NOTE Even though the specification name contains "ddr", the command is still sdr.

t_{IHddr} (CMD) Input Hold Time Test Method of Implementation

The purpose of this test is to verify that the input hold time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- Dual-Rate

PASS Condition

The hold time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Measure the Clock rising at 50% to the Function 1 rising at V_{IL}.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the Clock rising at 50% to the Function 1 falling at V_{IH}.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

NOTE Even though the specification name contains "ddr", the command is still sdr.

t_{ODLY} (CMD) Output Delay Time Test Method of Implementation

The purpose of this test is to verify that the output time of the CMD Test signal relative to the rising edge of the Clock is less than or equal to the specified value.

Modes Supported

- Dual-Rate

PASS Condition

The output delay time of the CMD test signal relative to the rising edge of the clock is less than or equal to 13.7 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the rising edge of Function 1 at V_{OH} to Clock rising at 50%.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the falling edge of Function 1 at V_{OL} to Clock rising at 50%.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{OH} (CMD) Output Hold Time Test Method of Implementation

The purpose of this test is to verify that the output hold time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- Dual-Rate

PASS Condition

The output hold time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 2.5 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the Clock rising at 50% to the Function 1 rising at V_{OL}.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the Clock rising at 50% to the Function 1 falling at V_{OH}.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{RISE} (CMD) Output Rise Time Test Method of Implementation

The purpose of this test is to verify that the output rise time of the CMD Test signal is less than or equal to the specified value.

Modes Supported

- Dual-Rate

PASS Condition

The output rise time of the CMD test signal is less than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low – start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the Function 1 rise time from V_{OL} to V_{OH}.

NOTE V_{OL} and V_{OH} are defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Compare the max Rise Time value to the specified value and report pass/fail and margin.

t_{FALL} (CMD) Output Fall Time Test Method of Implementation

The purpose of this test is to verify that the output fall time of the CMD Test signal is less than or equal to the specified value.

Modes Supported

- Dual-Rate

PASS Condition

The output fall time of the CMD test signal is less than or equal to 3 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low – start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the CMD signal.
6. Measure the Function 1 fall time from V_{OL} to V_{OH}.

NOTE V_{OL} and V_{OH} are defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Compare the max Fall Time value to the specified value and report pass/fail and margin.

t_{ISUddr} (DAT) Input Setup Time Test Method of Implementation

The purpose of this test is to verify that the input setup time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Dual-Rate

PASS Condition

The setup time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 2.5 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Measure the rising edge of Function 1 at V_{IH} to BOTH Clock edges at 50%.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the falling edge of Function 1 at V_{IL} to BOTH Clock edges rising at 50%.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{IHddr} (DAT) Input Hold Time Test Method of Implementation

The purpose of this test is to verify that the input hold time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Dual-Rate

PASS Condition

The hold time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 2.5 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Measure BOTH Clock edges at 50% to the Function 1 rising at V_{IL}.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure BOTH Clock edges at 50% to the Function 1 falling at V_{IH}.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

$t_{ODLYddr}$ (DAT) Output Delay Time Test Method of Implementation

The purpose of this test is to verify that the output delay time of the DAT Test signal relative to the rising edge of the Clock is within the specified range.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Dual-Rate

PASS Condition

The output delay time of the DAT test signal relative to the rising edge of the clock is less than or equal to 7 ns and greater than or equal to 1.5 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full read cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Measure the rising edge of Function 1 at V_{OH} to BOTH Clock edges at 50%.

NOTE V_{OH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the falling edge of Function 1 at V_{OL} to BOTH Clock edges at 50%.

NOTE V_{OL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{RISE} (DAT) Output Rise Time Test Method of Implementation

The purpose of this test is to verify that the output rise time of the DAT Test signal less than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Dual-Rate

PASS Condition

The output rise time of the CMD test signal is less than or equal to 2 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Measure Rise Time from V_{OL} to V_{OH} on Function 1.

NOTE V_{OL} and V_{OH} are defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the max Rise Time value to the specified value and report pass/fail and margin.

t_{FALL} (DAT) Output Fall Time Test Method of Implementation

The purpose of this test is to verify that the output fall time of the DAT Test signal less than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- Dual-Rate

PASS Condition

The output fall time of the CMD test signal is less than or equal to 2 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a MUST intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is read and not write.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an output, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the output portion of the DAT signal.
7. Measure Fall Time from V_{OL} to V_{OH} on Function 1.

NOTE V_{OL} and V_{OH} are defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the max Fall Time value to the specified value and report pass/fail and margin.

7
HS200 Device Interface Timing Tests

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This section provides the Methods of Implementation (MOIs) for the HS200 Device Interface Timing tests using an Agilent Infiniium oscilloscope and the N6465A eMMC Compliance Test Application.

Probing and Connection for HS200 Device Interface Timing Tests

When performing the HS200 Device Interface Timing tests, the eMMC Compliance Test Application will prompt you to make the proper connections. The connections for the HS200 Device Interface Timing tests may look similar to the following diagram. Refer to the Connect tab in the eMMC Compliance Test Application for details.

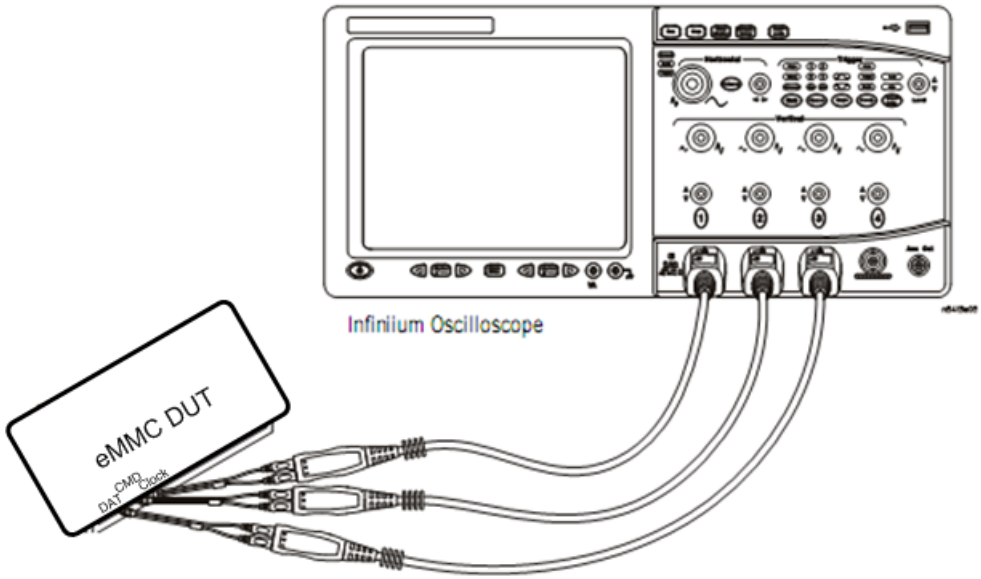

Figure 10 Probing for HS200 Device Interface Timing Tests

You can use any of the oscilloscope channels as Pin-Under-Test (PUT) source channel. You can identify the channels used for each signal in the Configure tab of the eMMC Compliance Test Application. (The channels shown in Figure 10 are just examples.)

Test Procedure

1. Start the automated test application as described in "Starting the eMMC Compliance Test Application" on page 21.
2. Ensure that the eMMC device-under-test (DUT) is performing read and write operations in the test and speed setup that you plan to test.
3. Connect the probes to the PUTs on the eMMC DUT.
4. Connect the oscilloscope probes to the channels of the oscilloscope that you have set up in the Configure tab.
5. In the eMMC test application, click the Set Up tab.

6 Select the Bus Speed Mode HS200.

7 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

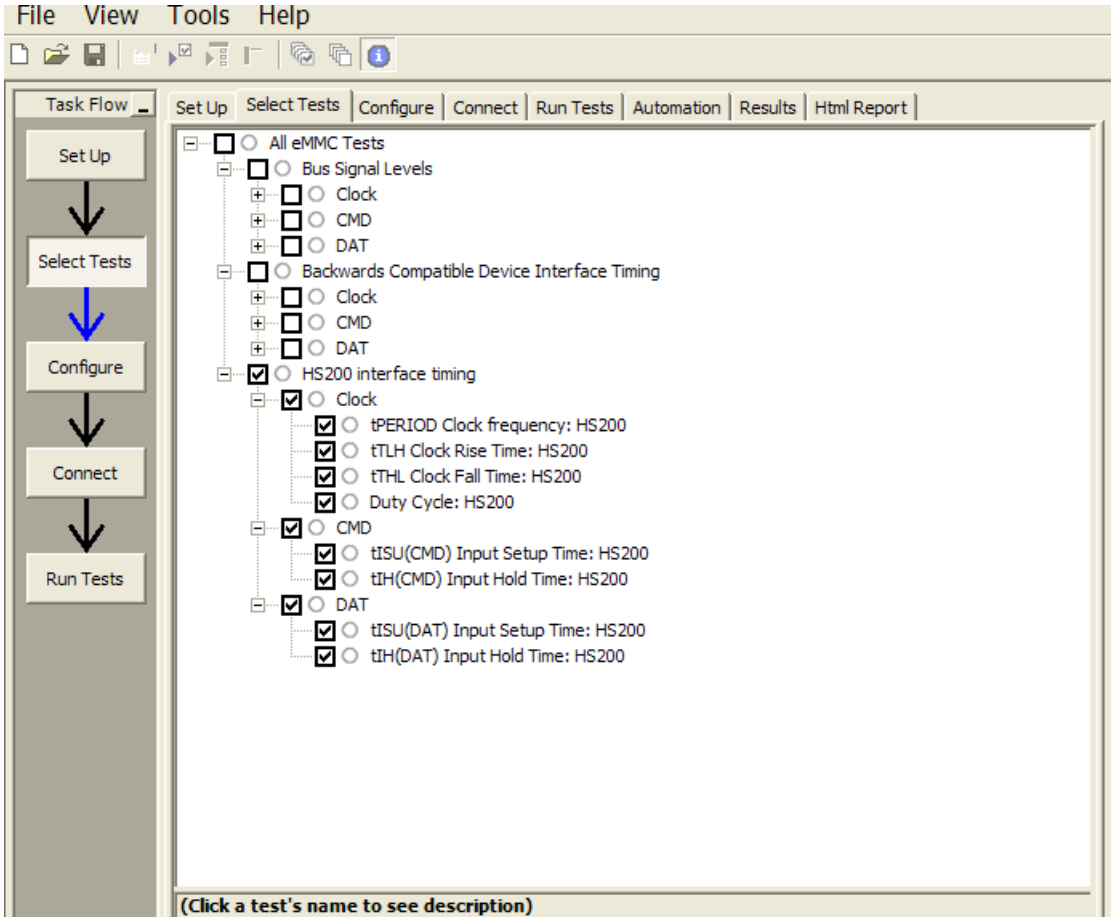

Figure 11 Selecting HS200 Device Interface Timing Tests

HS200 Device Interface Timing Specifications

Table 8 HS200 Device Input Timing

Symbol	Min	Max	Unit	Remark
t_{PERIOD}	5	—	ns	200 MHz (max), between rising edges
t_{TLH}, t_{THL}	—	0.2*t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1 ns (max) at 200 MHz, C_{BGA} = 12 pF, the absolute maximum value of t_{TLH}, t_{THL} is 10 ns regardless of clock frequency
Duty cycle	30	70	%	
t_{ISU}	1.40	—	ns	5 pF ≤ C_{BGA} ≤ 12 pF
t_{IH}	0.8		ns	5 pF ≤ C_{BGA} ≤ 12 pF

t_{PERIOD} Clock Frequency Test Method of Implementation

The purpose of this test is to verify that the minimum clock period is greater than the specified limits.

Modes Supported

- HS200

PASS Condition

The clock period must be greater than or equal to 5 ns across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Period measurement on the rising edges of the Clock Channel at 50%.
7. Compare the min value to the specified value and report pass/fail and margin.

Clock — t_{TLH} Clock Rise Time Test Method of Implementation

The purpose of this test is to verify that the rise time is less than or equal to the specified value.

Modes Supported

- HS200

PASS Condition

The clock rise time is less than or equal to $0.2*t_{PERIOD}$ across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Rise Time measurement on the Clock Channel between V_{IL} to V_{IH} (V_{IL} and V_{IH} are defined by V_{CC}/V_{CCQ} as set in the Configure tab).
7. Compare the maximum Rise Time value to the specified value and report pass/fail and margin.

Clock — t_{THL} Clock Fall Time Test Method of Implementation

The purpose of this test is to verify that the fall time is less than or equal to the specified value.

Modes Supported

- HS200

PASS Condition

The clock fall time is less than or equal to $0.2*t_{PERIOD}$ across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Fall Time measurement on the Clock Channel between V_{IL} to V_{IH} (V_{IL} and V_{IH} are defined by V_{CC}/V_{CCQ} as set in the Configure tab).
7. Compare the maximum Fall Time value to the specified value and report pass/fail and margin.

Clock — Duty Cycle Test Method of Implementation

The purpose of this test is to verify that the clock Duty Cycle remains in the specified limits.

Modes Supported

- HS200

PASS Condition

The duty cycle of the clock is between 30-70% across the cycle count set in the Configure tab.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock and set the memory depth to the cycle number defined in the Configure tab.
3. Single to capture the specified clock cycles.
4. Measure clock swing voltages and thresholds for the UDF.
5. Pass the Clock Channel, Voltages and thresholds from step 4, and clock frequency to the UDF used in Function 1. Function 1 will set a qualifier for the Clock signal to remove any clock off portions from the measurement.
6. Perform a Duty Cycle measurement on both edges of the Clock Channel at 50%.
7. Compare the worst case value to the specified value and report pass/fail and margin.

t_{ISU} (CMD) Input Setup Time Test Method of Implementation

The purpose of this test is to verify that the input setup time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- HS200

PASS Condition

The setup time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 1.4 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Measure the rising edge of Function 1 at V_{IH} to Clock rising at 50%.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the falling edge of Function 1 at V_{IL} to Clock rising at 50%.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{IH} (CMD) Input Hold Time Test Method of Implementation

The purpose of this test is to verify that the input hold time of the CMD Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

Modes Supported

- HS200

PASS Condition

The hold time of the CMD test signal relative to the rising edge of the clock is greater than or equal to 0.8 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output CMD.
3. Set the trigger on CMD going low — start of command sequence.
4. Set the memory depth based on the frequency from step 2 to ensure all command sequence bits are captured.
5. Pass the CMD channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the CMD signal.
6. Measure the Clock rising at 50% to the Function 1 rising at V_{IL}.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

7. Measure the Clock rising at 50% to the Function 1 falling at V_{IH}.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Compare the worst case value to the specified value and report pass/fail and margin.

t_{ISU} (DAT) Input Setup Time Test Method of Implementation

The purpose of this test is to verify that the input setup time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- HS200

PASS Condition

The setup time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 1.4 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Measure the rising edge of Function 1 at V_{IH} to rising Clock edges at 50%.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure the falling edge of Function 1 at V_{IL} to rising Clock edges at 50%.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

t_{IH} (DAT) Input Hold Time Test Method of Implementation

The purpose of this test is to verify that the input hold time of the DAT Test signal relative to the rising edge of the Clock is greater than or equal to the specified value.

NOTE In the Configure tab, Read and Write wait times can be set (in seconds) to increase the time to wait for a trigger before time-out. This enables you to increase the wait time to properly trigger a write or a read when unable to control writes and reads of the DUT. If the application states that it was unable to find a read or a write, please consider the DUT's usage of read and write commands and increase the wait time.

Modes Supported

- HS200

PASS Condition

The hold time of the DAT test signal relative to the rising edge of the clock is greater than or equal to 0.8 ns.

Measurement Algorithm

1. Obtain a sample or acquire signal data.
2. Measure the frequency of the clock to pass into the UDF to help identify the expected range of input and output DAT.
3. Set the trigger on CMD going low – start of command sequence.
4. Set a must NOT intersect zone at 49 clock cycles – six cycles wide, to ensure that the signal is write and not read.
5. Set the memory depth to ensure full write cycle.
6. Pass the CMD channel, DAT channel, signal is an input, V_{IH}/V_{IL} as defined by V_{CC}/V_{CCQ}, and clock frequency to the UDF used in Function 1. Function 1 will be only the input portion of the DAT signal.
7. Measure rising Clock edges at 50% to the Function 1 rising at V_{IL}.

NOTE V_{IL} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

8. Measure rising Clock edges at 50% to the Function 1 falling at V_{IH}.

NOTE V_{IH} is defined by the V_{CC}/V_{CCQ} voltages set in the Configure tab.

9 Compare the worst case value to the specified value and report pass/fail and margin.

8 Debug Mode

Debug mode can be selected to make measurements on saved waveforms.

1 In the Configure tab, select the **Debug** radio button. This will enable the option to use waveform files.

2 Change **Use Waveform Files** from **No** to **Yes** (see Figure 12). This will enable the measurements to use saved waveforms.

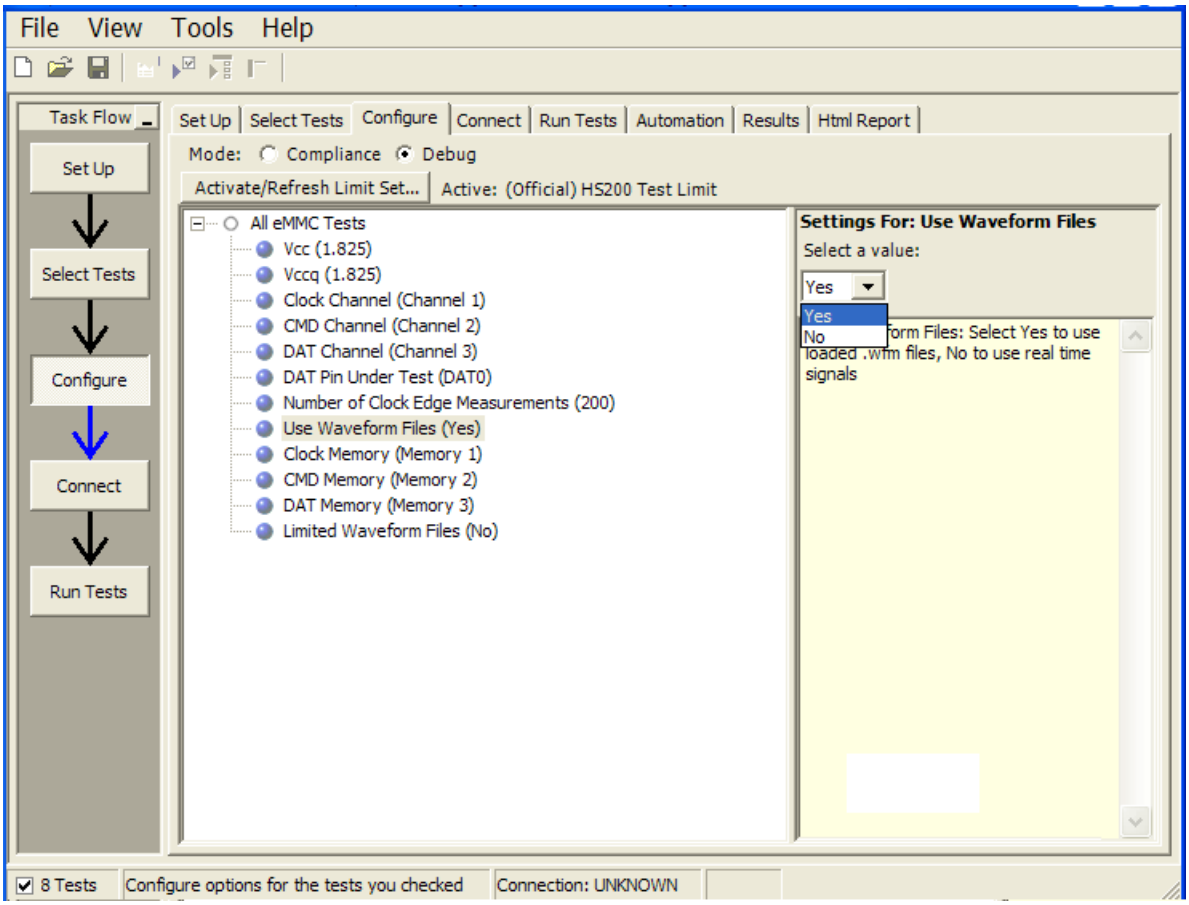

Figure 12 Debug Mode Settings

3 Load the saved waveforms.

4 Set the memory used for each signal.

5 If you have deep captures of all signals, enable and use all three channels to allow the application to use logic to separate input/output data. If you do not have deep captures, but can guarantee that the signals presented are the input or output cmd/data required for the measurement, then change **Limited Waveform Files** from **No** to **Yes**. This will take out the error checking on the signal and assume the signal presented is right for measurement.

6 Select Tests and Run. See previous sections for test and measurement methods.

9 Calibrating the Infiniium Oscilloscope and Probe

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This section describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the eMMC automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the Agilent Infiniium oscilloscope). Use a good quality 50 Ω BNC cable.

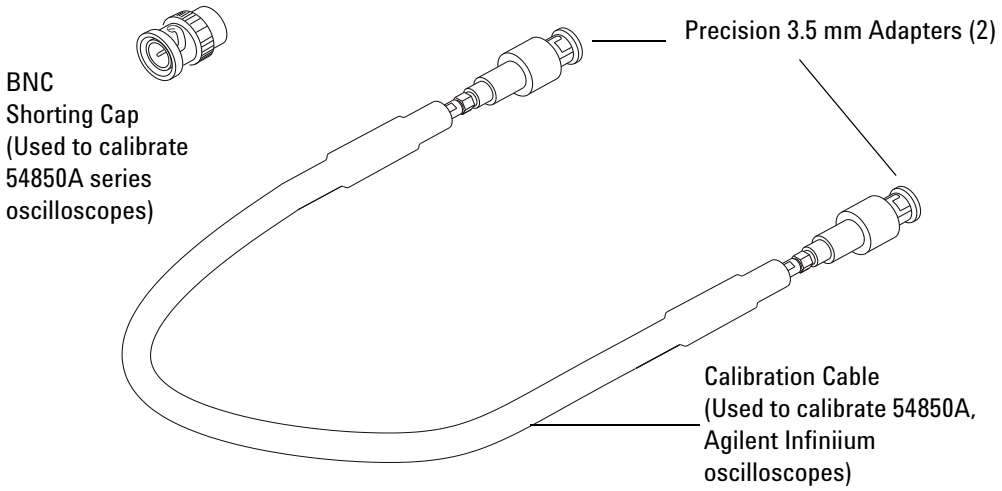

Figure 13 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   b Plug in the power cord.

   c Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   d Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

   a Locate the BNC shorting cap.

   b Locate the calibration cable.

   c Locate the two Agilent precision SMA/BNC adapters.

   d Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

   e Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 14 below, perform the following steps:

   a Click on the Utilities>Calibration menu to open the Calibration dialog box.

Figure 14 Accessing the Calibration Menu

4 Referring to Figure 15 below, perform the following steps to start the calibration:

   b Uncheck the Cal Memory Protect checkbox.

   c Click the Start button to begin the calibration.

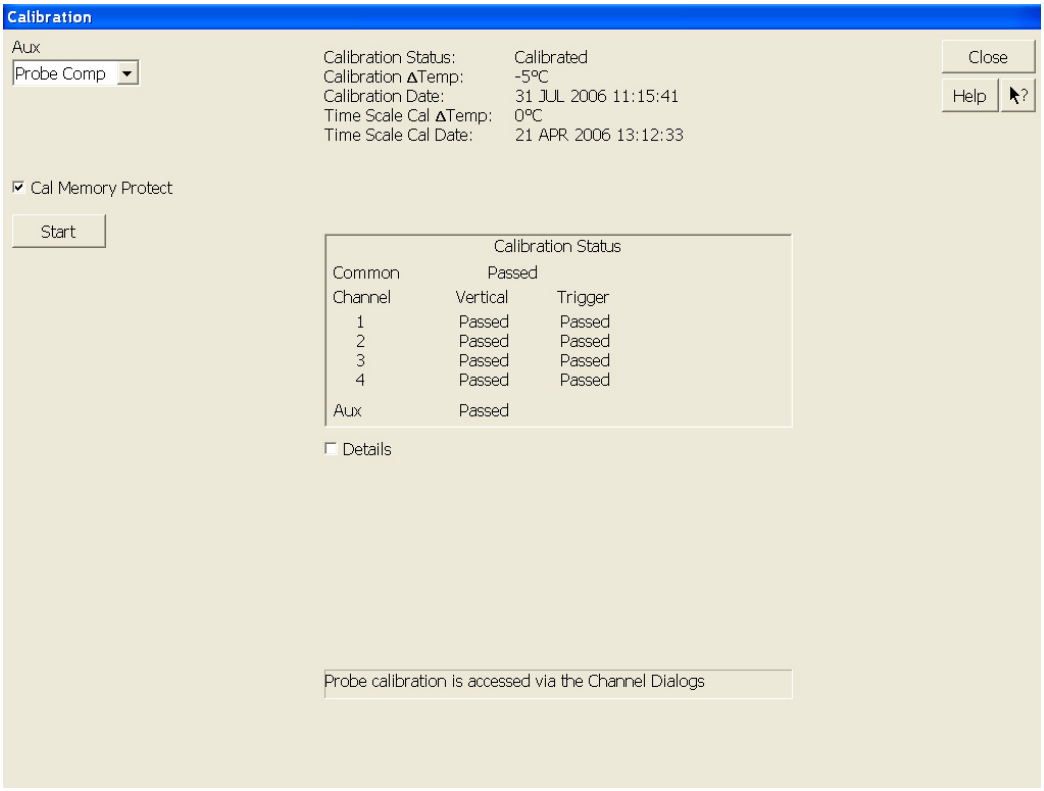

Figure 15 Oscilloscope Calibration Window

d During the calibration of channel 1, if you are prompted to perform a Time Scale Calibration, as shown in Figure 16 below.

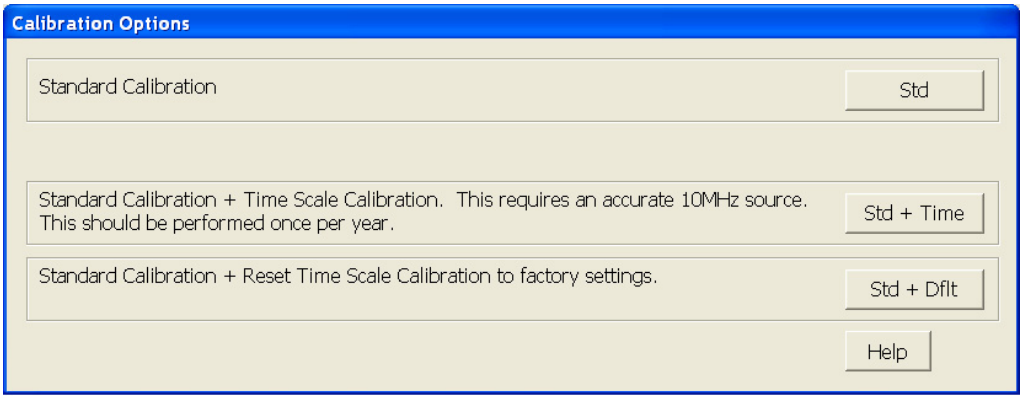

Figure 16 Time Scale Calibration Dialog box

e Click on the Std+Dflt button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

g Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

h Click the Close button to close the calibration window.

i The internal calibration is completed.

j Read NOTE below.

NOTE These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Required Equipment for Probe Calibration

Before performing eMMC tests you should calibrate the probes. Calibration of the solder-in probe heads consists of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adapter
- Deskew fixture
- 50 Ω SMA terminator

Probe Calibration

Connecting the Probe for Calibration

For the following procedure, refer to Figure 17 below.

1 Connect the BNC (male) to SMA (male) adapter to the deskew fixture on the connector closest to the yellow pincher.

2 Connect the 50 Ω SMA terminator to the connector farthest from the yellow pincher.

3 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.

4 Connect the probe to an oscilloscope channel.

5 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.

6 Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.

7 Release the yellow pincher.

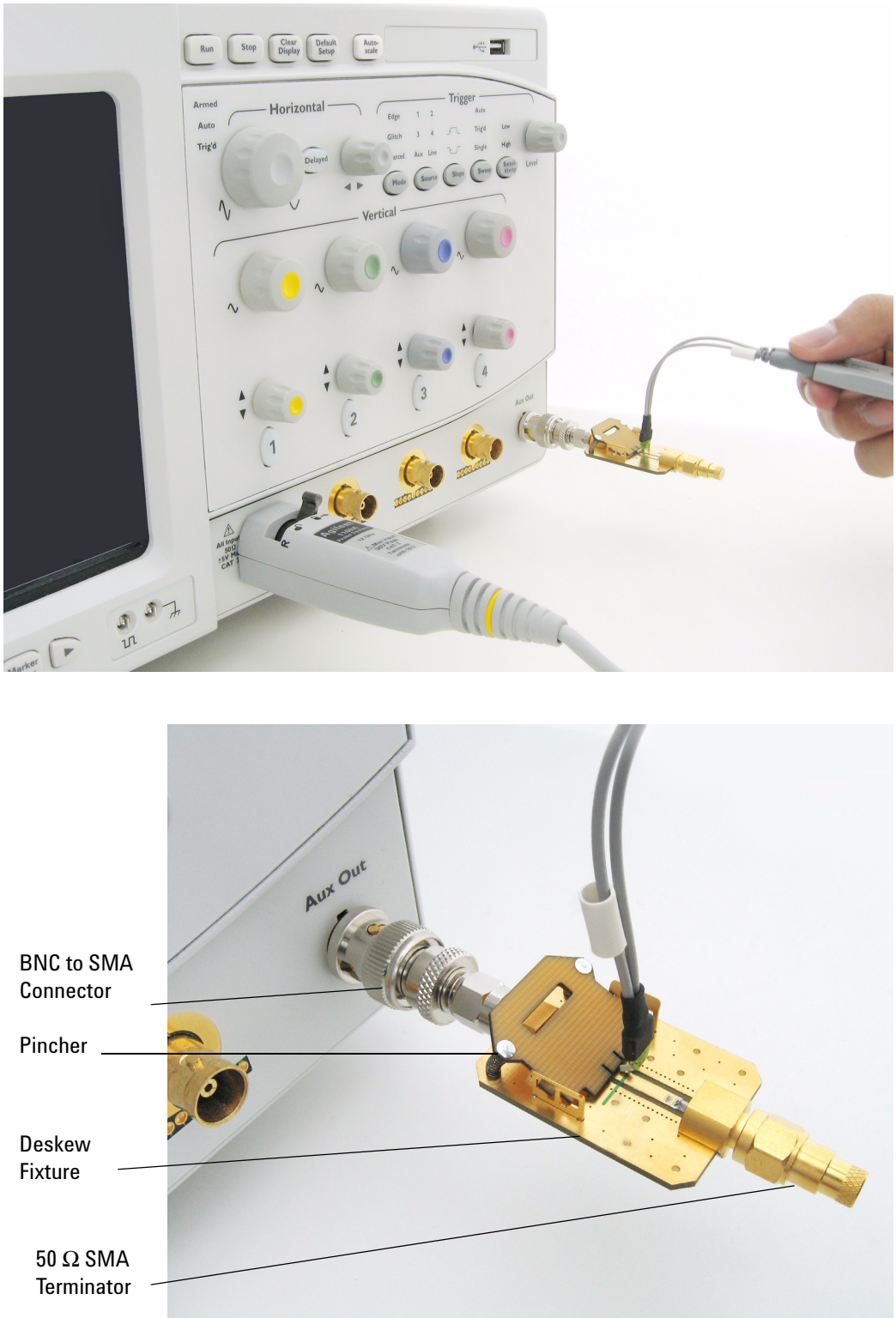

Figure 17 Solder-in Probe Head Calibration Connection Example

Verifying the Connection

1 On the Infiniium oscilloscope, press the autoscale button on the front panel.

2 Set the volts per division to 100 mV/div.

3 Set the horizontal scale to 1.00 ns/div.

4 Set the horizontal position to approximately 3 ns. You should see a waveform similar to that in Figure 18 below.

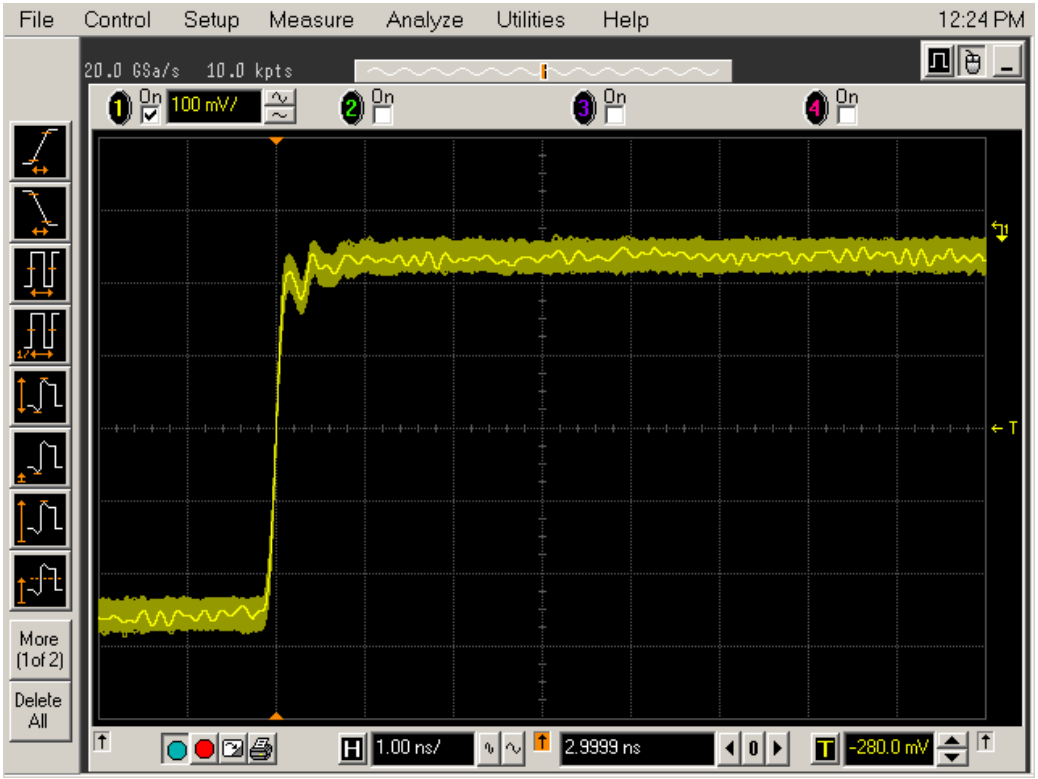

Figure 18 Good Connection Waveform Example

If you see a waveform similar to that of Figure 19 below, then you have a bad connection and should check all of your probe connections.

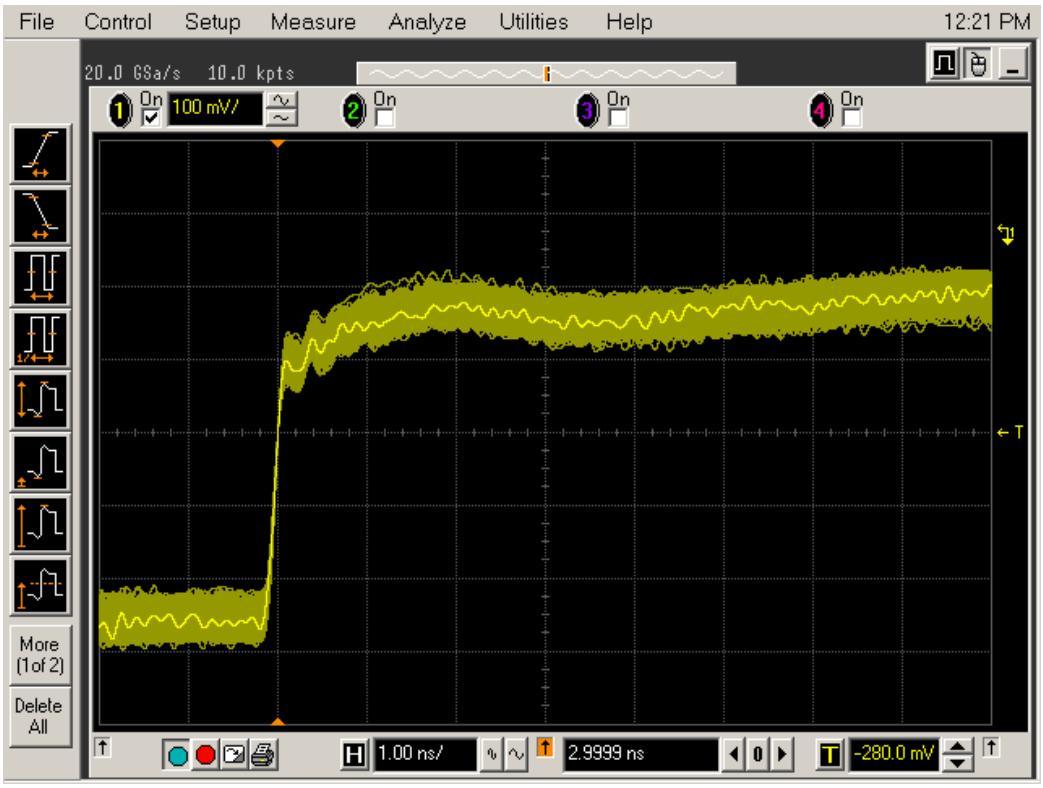

Figure 19 Bad Connection Waveform Example

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe, as shown in Figure 20.

Figure 20 Channel Setup Window

2 In the Channel Setup dialog box, select the Probes... button, as shown in Figure 21.

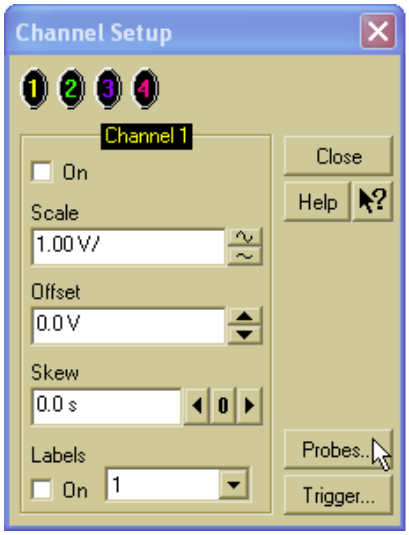

Figure 21 Channel Dialog Box

3 In the Probe Setup dialog box, select the Calibrate Probe... button.

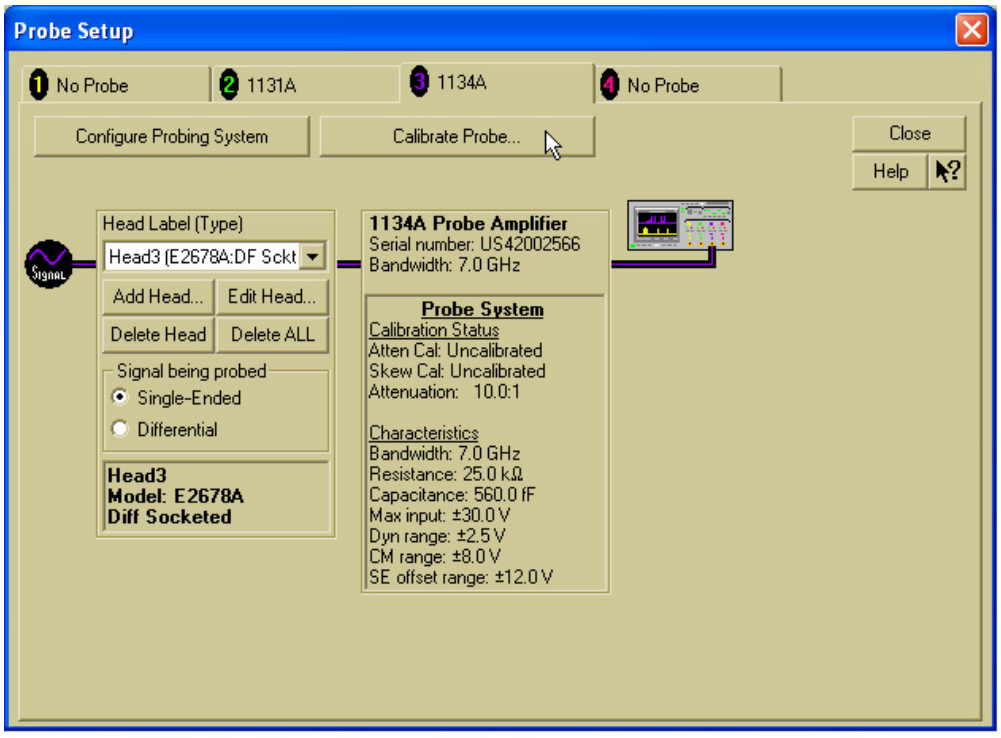

Figure 22 Probe Setup Window

4 In the Probe Calibration dialog box, select the Calibrated Atten/Offset radio button.

5 Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

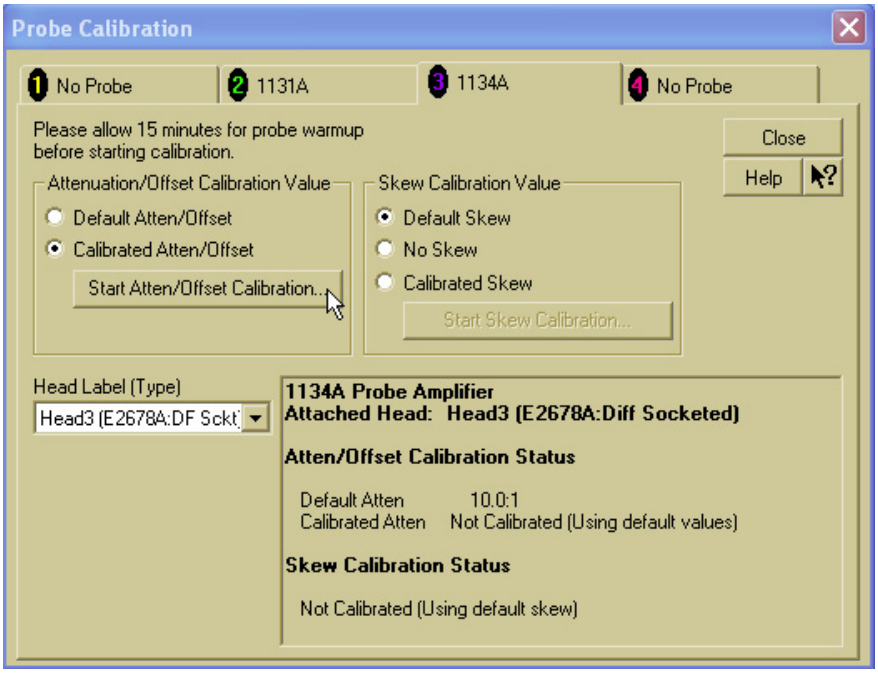

Figure 23 Probe Calibration Window

6 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

7 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adapter
- SMA (male) to BNC (female) adapter
- BNC (male) to BNC (male) 12 inch cable such as the Agilent 8120-1838

- Agilent 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 GHz and greater only)
- Agilent 54855-67604 precision 3.5 mm adapters (Infiniium oscilloscopes with bandwidths of 6 GHz and greater only)
- Deskew fixture

For the following procedure, refer to Figure 24.

1 Connect the BNC (male) to SMA (male) adapter to the deskew fixture on the connector closest to the yellow pincher.

2 Connect the SMA (male) to BNC (female) adapter to the connector farthest from the yellow pincher.

3 Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For Infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adapters.

4 Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.

5 Connect the probe to an oscilloscope channel.

6 To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.

7 Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.

8 Release the yellow pincher.

9 On the oscilloscope, press the autoscale button on the front panel.

10 Select the Setup menu and choose the channel connected to the BNC cable from the pull-down menu.

11 Select the Probes... button.

12 Select the Configure Probe System button.

13 Select User Defined Probe from the pull-down menu.

14 Select the Calibrate Probe... button.

15 Select the Calibrated Skew radio button.

16 Once the skew calibration is completed, close all dialog boxes.

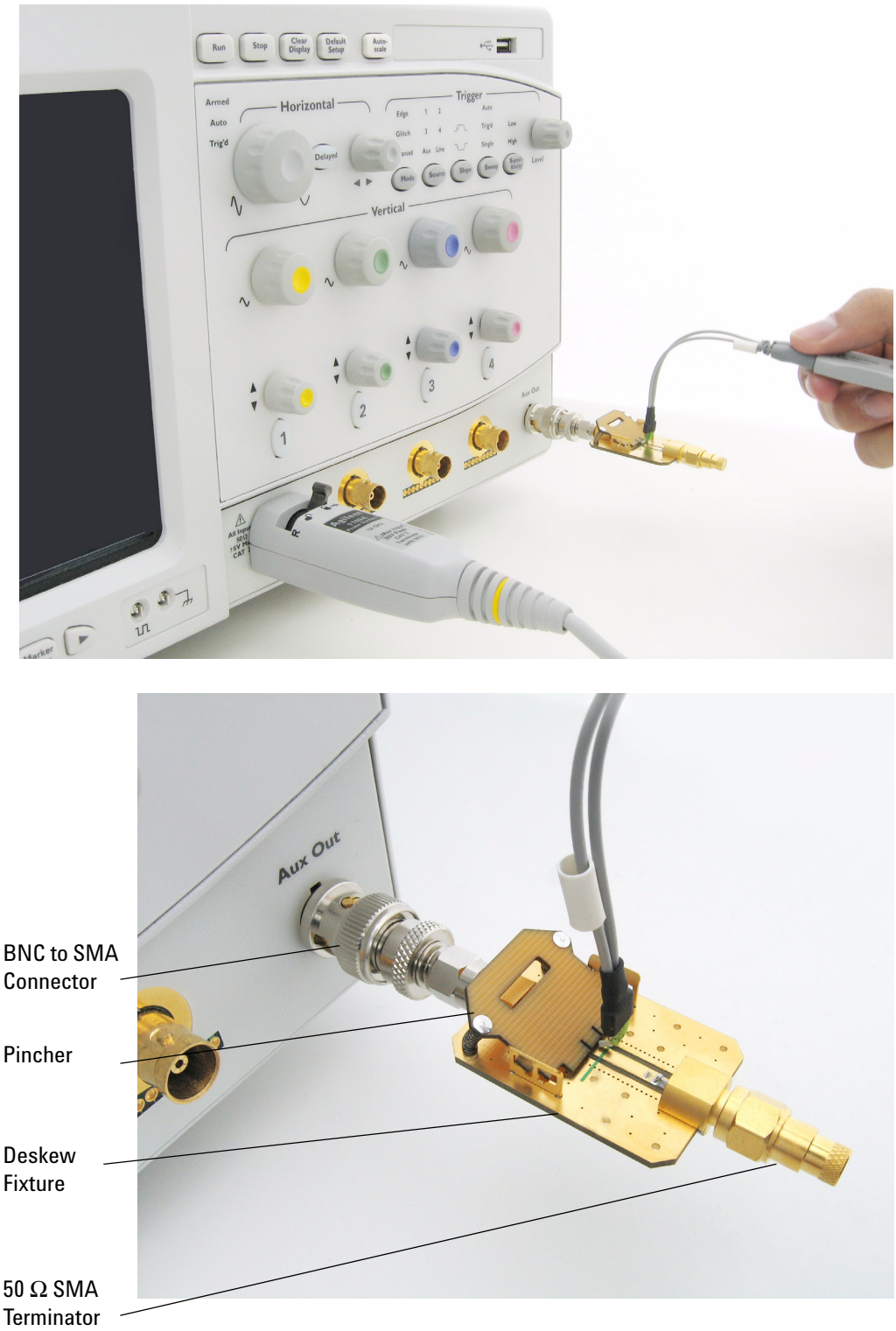

Figure 24 Probe Calibration Verification Connection Example

17 Select the Start Skew Calibration... button and follow the on-screen instructions.

18 Set the vertical scale for the displayed channels to 100 mV/div.

19 Set the horizontal range to 1.00 ns/div.

20 Set the horizontal position to approximately 3 ns.

21 Change the vertical position knobs of both channels until the waveforms overlap each other.

22 Select the Setup menu and choose Acquisition... from the pull-down menu.

23 In the Acquisition Setup dialog box, enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 25.

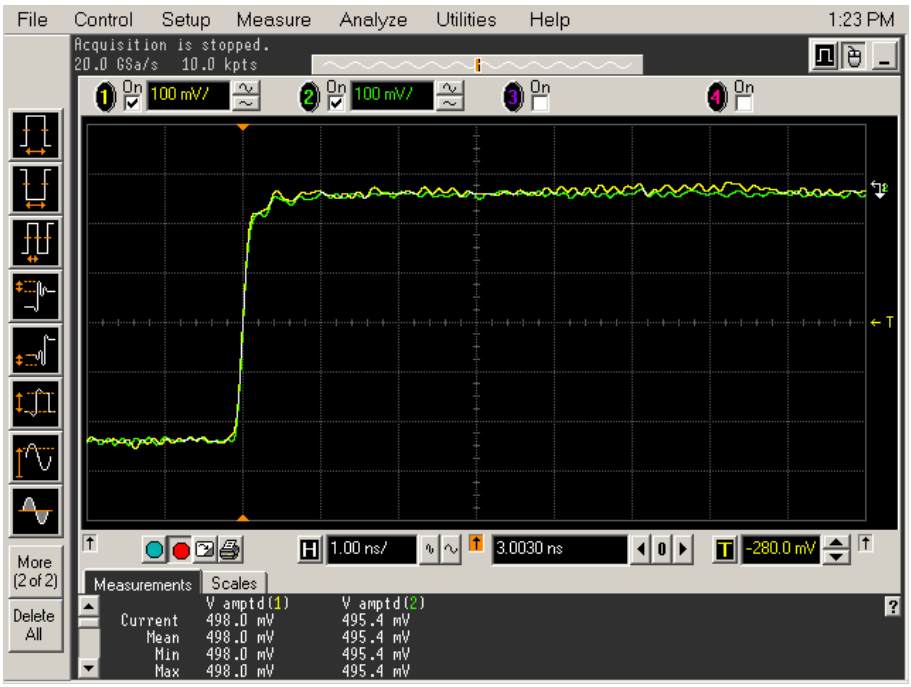

Figure 25 Calibration Probe Waveform Example

NOTE

Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

10 InfiniiMax Probing

Figure 26 1134A InfiniiMax Probe Amplifier

Agilent recommends 116xA or 113xA probe amplifiers, which range from 3.5 GHz to 12 GHz.

Agilent also recommends the E2677A differential solder-in probe head. Other probe head options include N5381A InfiniiMax II 12 GHz differential solder-in probe head, N5425A InfiniiMax ZIF probe head, and N5426A ZIF Tips.

Figure 27 E2677A / N5381A Differential Solder-in Probe Head

Table 9 Probe Head Characteristics (with 1134A probe amplifier)

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential Solder-in	E2677A	7 GHz, 0.27 pF, 50 kΩ	7 GHz, 0.44 pF, 25 kΩ

Used with the 1168A or 1169A probe amplifier, the E2677A differential solder-in probe head provides 10 GHz and 12 GHz bandwidths respectively.