Keysight D9060GDDC GDDR6 Test Application

KEYSIGHT TECHNOLOGIES

Methods of Implementation

Notices

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WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Contents

1 Overview

GDDR6 Automated Testing—At a Glance

The Keysight D9060GDDC GDDR6 Test Application helps you verify that the GDDR6 transmitter device under test (DUT) conforms to the pre-defined limits using the Keysight Infiniium Digital Storage Oscilloscopes. The Keysight D9060GDDC GDDR6 Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope, spectrum analyzer and vector network analyzer connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the Keysight D9060GDDC GDDR6 Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

Required Equipment and Software

In order to run the GDDR6 automated tests, you need the following equipment and software:

Hardware

- Use one of the following Oscilloscope models. Refer to www.keysight.com for the respective bandwidth ranges.
  - DSO9000A-Series, DSO90000A-Series and DSOX90000A/Q/Z/V-Series
    - For data rate up to 16GT/s, a bandwidth of 33 GHz is recommended to get accurate measurements for faster speed grade devices.
  - Keysight UXR Oscilloscopes
- Target Device Under Test (DUT)
- N2803A 30 GHz RCRC probe amplifier(x 4)
- N5445A 30 GHz browser(x4)
- N2787A 3D probe positioner(x4)
- Keyboard, qty = 1, (provided with the Keysight Infiniium Oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium Oscilloscope)
- Keysight also recommends using a second monitor to view the test application.

Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight D9060GDDC GDDR6 Test Application Release Notes)
- Keysight D9060GDDC GDDR6 Test Application software
- InfiniiScan Event Identification Software

Licensing information

Refer to the *Data Sheet* pertaining to GDDR6 Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9060GDDRC" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 13 to see the difference in installing a license key using either of the applications on your machine.

NOTE **To launch the GDDR6 Validation Test Application, you must have the D9060GDDC GDDR6 Test Application software and InfiniiScan Event Identification Software licenses installed.**

Additional Licenses

1 InfiniiSim feature requires the following licenses:
   - InfiniiSim Basic or InfiniiSim Advanced

A Brief on GDDR6 GRAM Testing

Figure 1 shows the ball pin out for the 180-ball BGA GDDR6 GRAM from the JEDEC specification. Measurements can be made on one channel at a time. Channel A is on the right and Channel B is on the right. CK/CK# is common to both the channels.

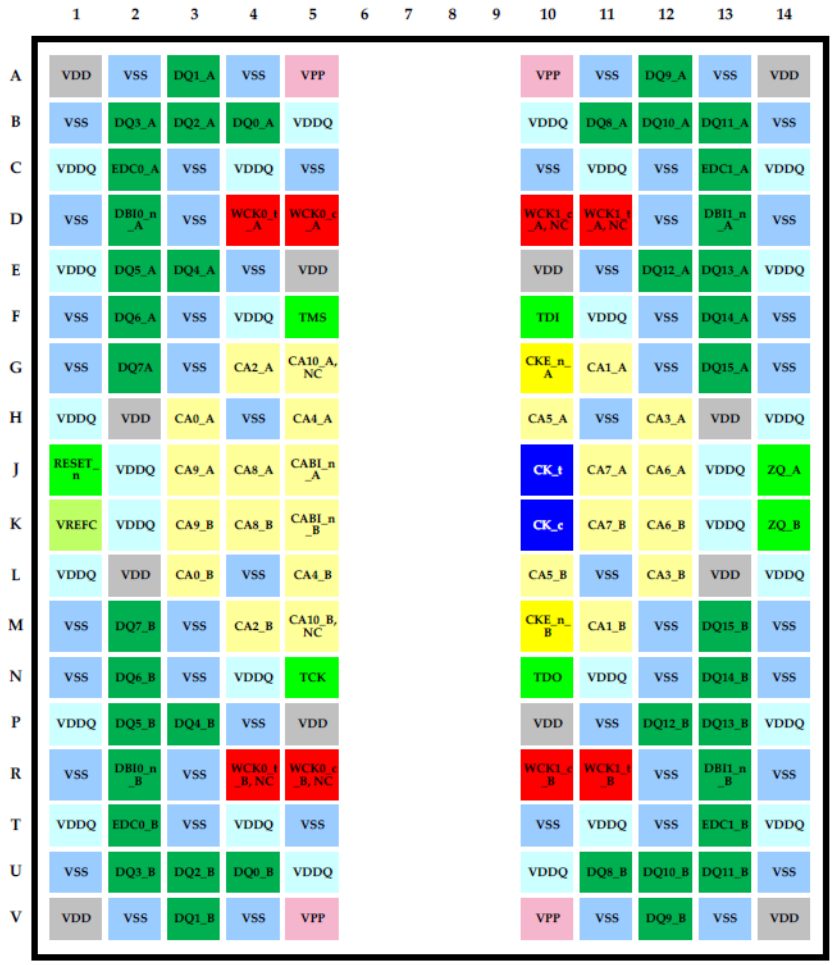

Figure 1 GDDR6 SGRAM 180 Ball BGA Ball-out

In This Book

This manual describes the tests that are performed by the Keysight D9060GDDC GDDR6 Test Application in more detail.

- Chapter 2, “Installing the Test Application and Licenses” shows how to install the automated test application software and licenses (if it was purchased separately).
- Chapter 3, “Preparing to Take Measurements” shows how to start the Keysight D9060GDDC GDDR6 Test Application and gives a brief overview of the required preparation and how the application is used.
- Chapter 4, “AC Timing Tests” describes the methods of implementation for the AC Timing tests.
- Chapter 5, “Input Operating Condition Tests” describes the methods of implementation for the Input Operating Condition tests.
- Chapter 6, “Command Address Input Timings Tests” describes the methods of implementation for Command Address Input Timings tests.
- Chapter 7, “Data Input and Output Timings Tests” describes the methods of implementation for Data Input and Output Timings tests.

See Also

The Keysight D9060GDDC GDDR6 Test Application’s Online Help, which describes:

- Starting the GDDR6 Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

2 Installing the Test Application and Licenses

If you purchased the D9060GDDC GDDR6 Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

Installing the Test Application

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9060GDDC release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.
2. To obtain the GDDR6 Test Application, go to Keysight website: "http://www.keysight.com/find/D9060GDDC".
3. In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

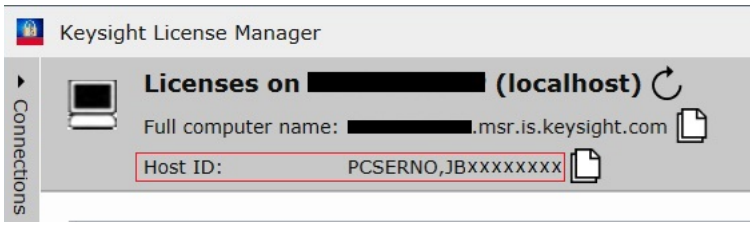

Figure 2 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

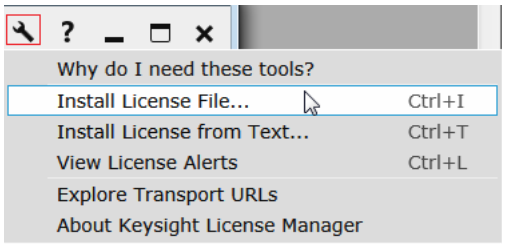

Figure 3 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1. Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 4) that appears in the Environment tab of the application. Note that x indicates numeric values.

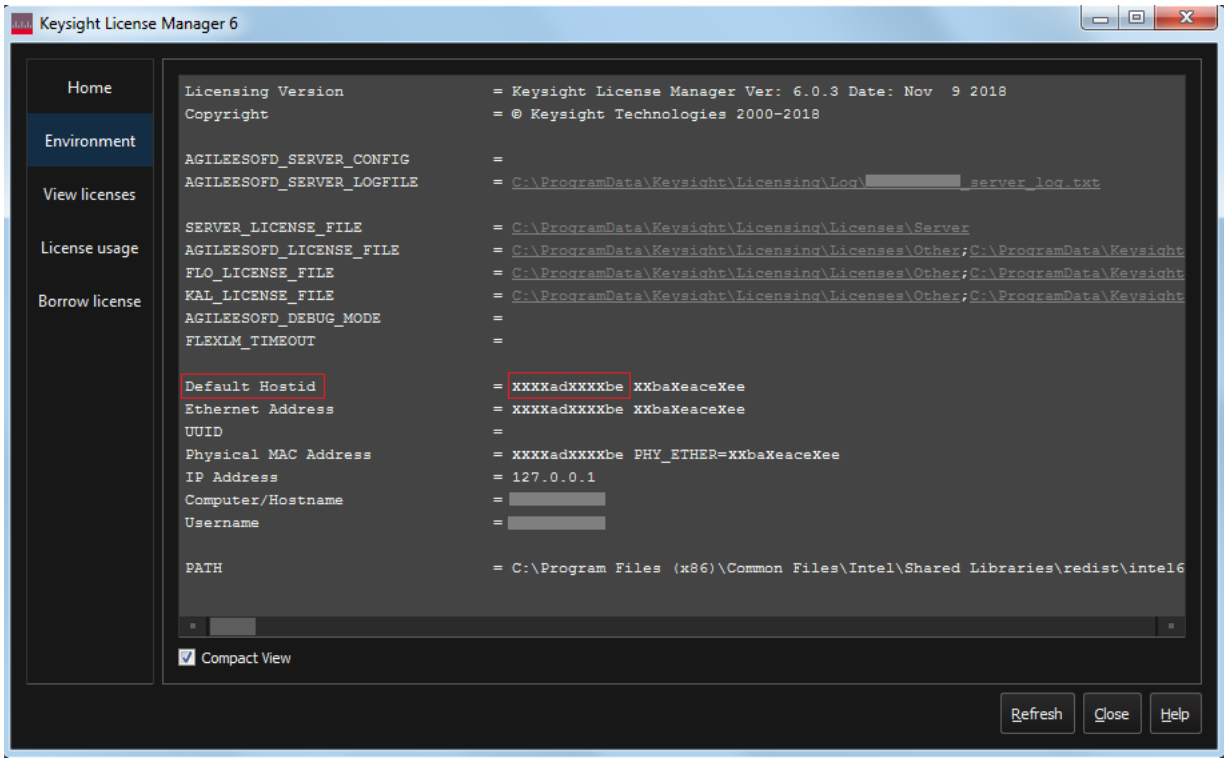

Figure 4 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager 6.

3 From the Home tab, use one of the options to install each license file.

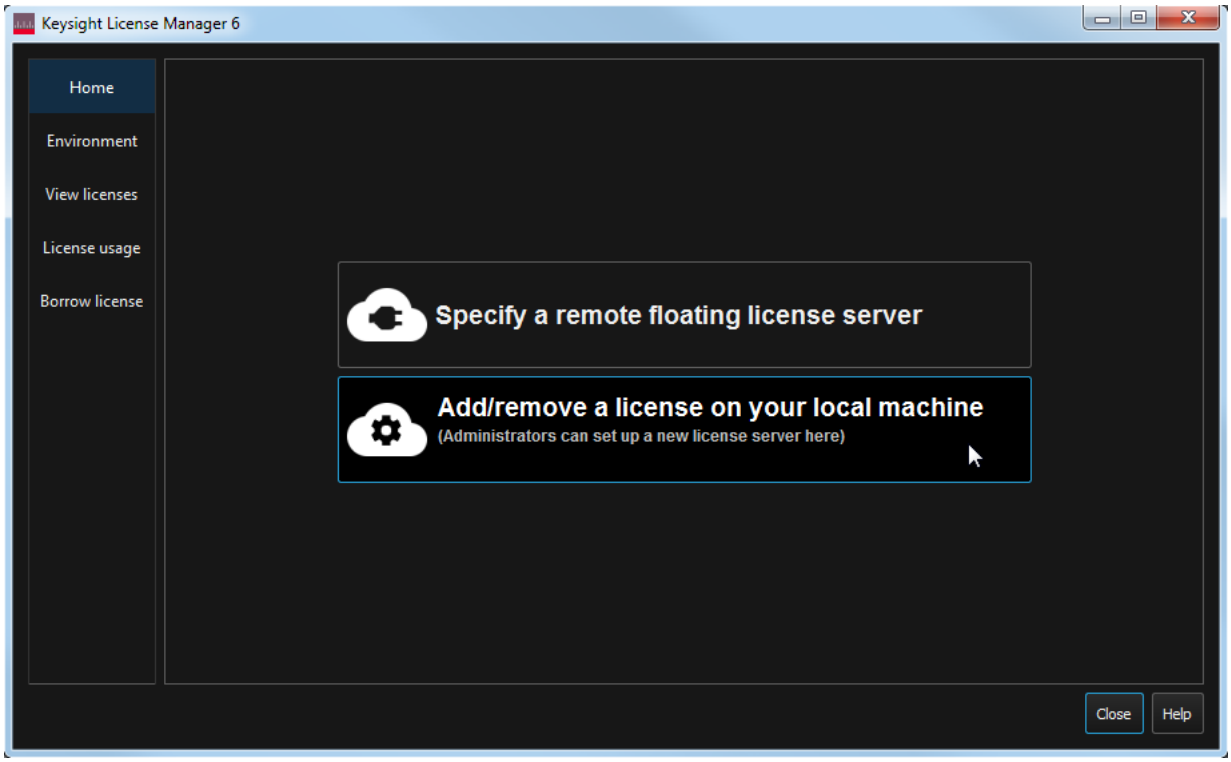

Figure 5 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

3 Preparing to Take Measurements

Before running the automated tests, you should calibrate the oscilloscope and probe. After the oscilloscope and probe have been calibrated, you are ready to start the GDDR6 Test Application and perform the measurements.

Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the GDDR6 Test Application

1 Ensure that the GDDR6 Device Under Test (DUT) is operating and set to desired test modes. To start the GDDR6 Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9060GDDC GDDR6 Test App**.

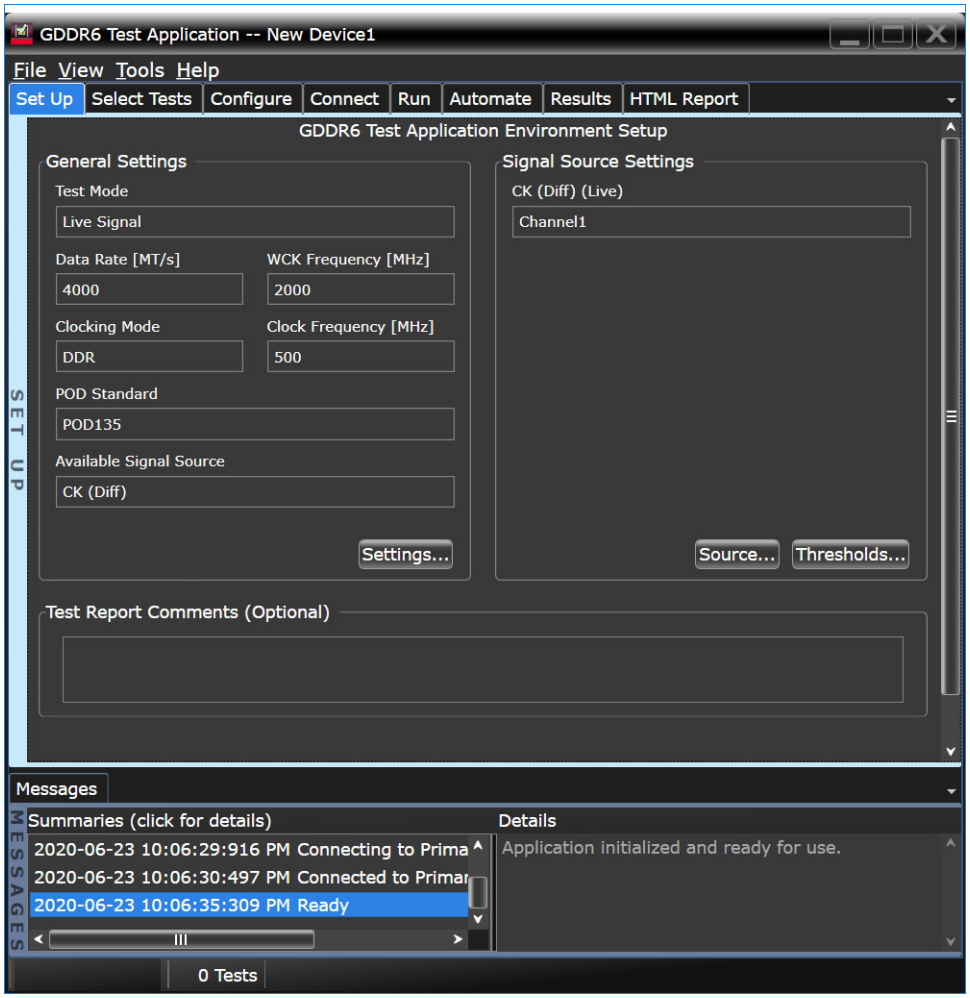

Figure 6 GDDR6 Test Application Main Window

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9060GDDC GDDR6 Test Application Online Help* available in the Help menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

Set Up	Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests that are to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts of commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

Filtering tests in the GDDR6 Test Application

The GDDR6 Test Application filters the list of tests based on the options you select in the **Signal Source** feature.

1 In the **Set Up** tab, click **Settings...**.

2 In the **GDDR6 General Setup** window that appears,

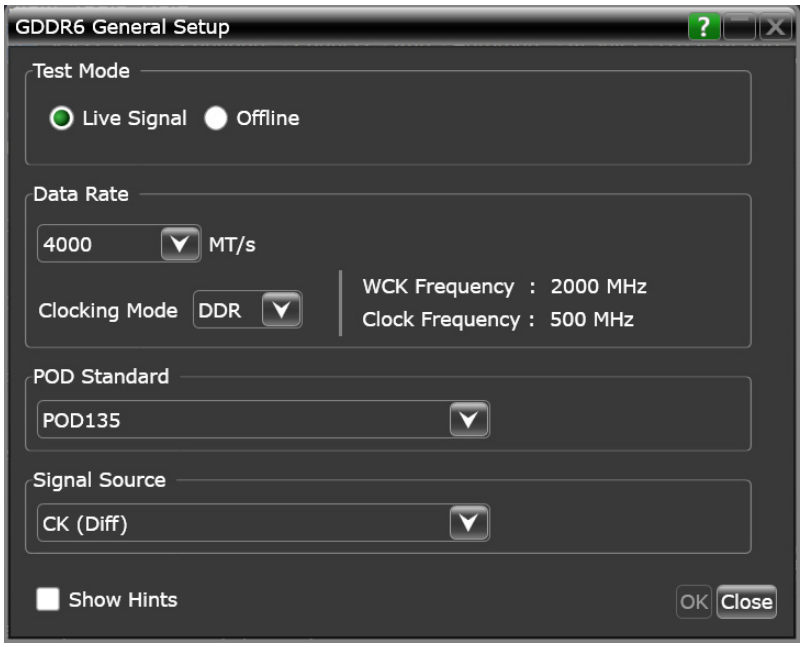

Figure 7 GDDR6 General Setup window

a Select a set of signal combinations from the options that appear in the **Signal Source** drop-down field.

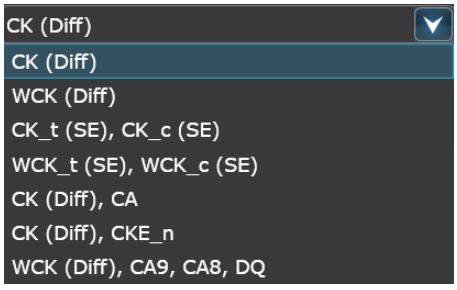

Figure 8 Set of signal combinations in Signal Source drop-down

Connections for Compliance Tests

To run tests using the GDDR6 Test Application, you must make proper connections between the Oscilloscope and the DUT. Once you select the tests that you want to run, refer to the **Connect** tab in the GDDR6 Test Application for connection instructions and the connection diagram, similar to the one shown in Figure 9.

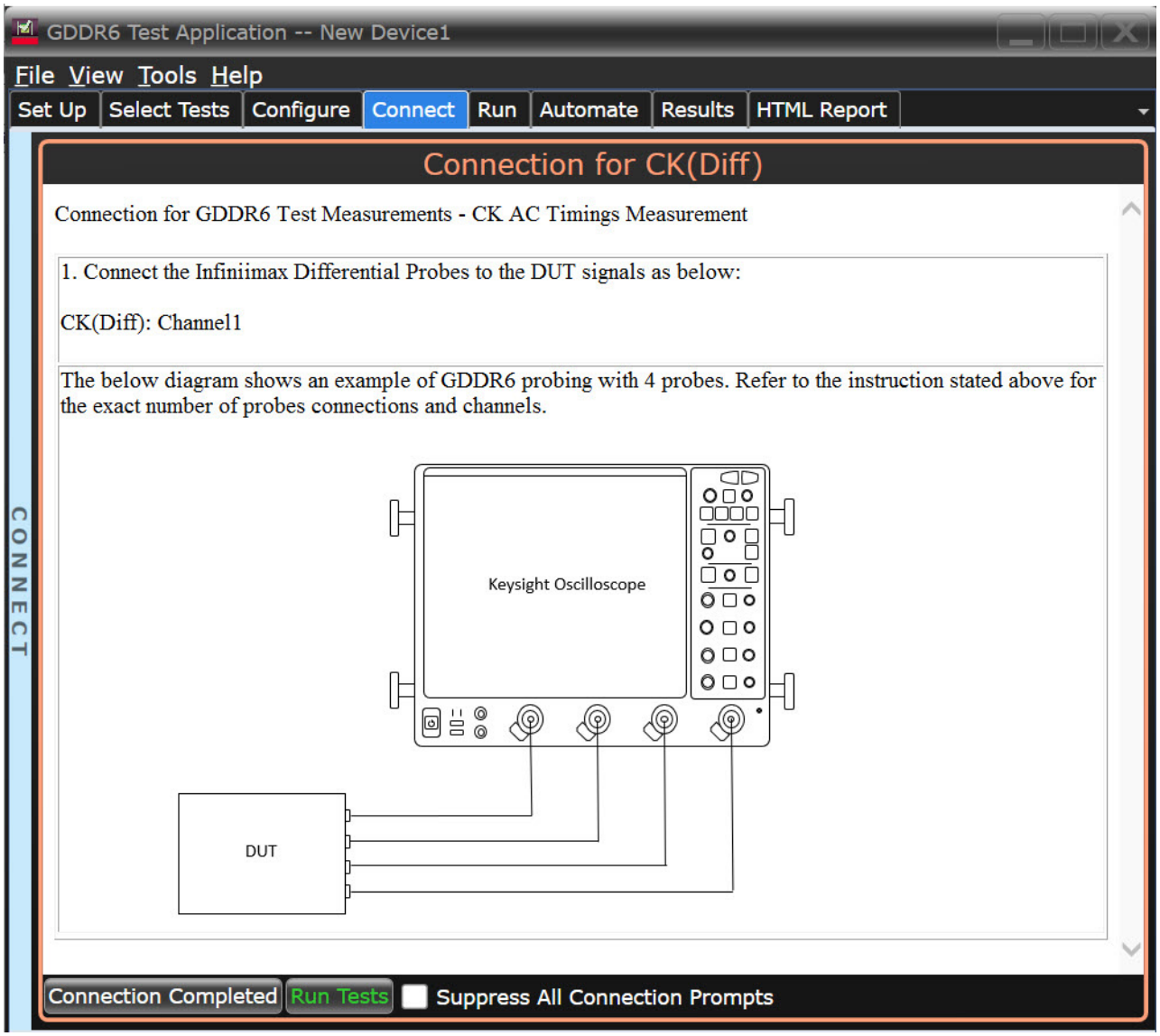

Figure 9 Physical connection diagram and instructions for compliance tests

4 AC Timing Tests

AC Timing Tests

Test Availability Conditions

All tests in this test group appear for the following configuration in GDDR6 General Setup window:

Signal Source:

- Any signal set including CK (Diff) or WCK (Diff)

CK AC Timing Tests

tCK - Rising Edge

Test ID: 10010

Test Overview: The purpose of this test is to measure the average CK cycle time, tCK(Rising Edge) from the rising edge of a cycle to the next rising edge within the waveform window.

Test Procedure:
1. Trigger on the rising edge of the CK(Diff) signal. Acquire CK(Diff) signal.
2. Measure period(rising edge) values for entire CK(Diff) waveform. The CK period(rising edge) value is measured from CK(Diff) rising edge at VREFdiff_CK middle threshold of a cycle to the next rising edge at VREFdiff_CK middle threshold.
   The default "VREFdiff_CK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].
3. Find the mean period value of the period measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

Expected/ Observable Results: The measured value of "tCK-Rising Edge" will be reported as informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

tCK - Falling Edge

Test ID: 10011

Test Overview: The purpose of this test is to measure the average CK cycle time, tCK(Falling Edge) from the falling edge of a cycle to the next falling edge within the waveform window.

Test Procedure:
1. Trigger on the rising edge of the CK(Diff) signal. Acquire CK(Diff) signal.
2. Measure period(falling edge) values for entire CK(Diff) waveform. The CK period(falling edge) is measured from CK(Diff) falling edge at VREFdiff_CK middle threshold of a cycle to the next falling edge at VREFdiff_CK middle threshold.
   The default "VREFdiff_CK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].
3. Find the mean period value of the period measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

Expected/ Observable Results: The measured value of "tCK – Falling Edge" will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

tCH

Test ID: 10020

Test Overview: The purpose of this test is to measure the average CK High-level width, tCH of all the positive pulses within the waveform window.

Test Procedure:
1. Trigger on the rising edge of the CK(Diff) signal. Acquire CK(Diff) signal.
2. Measure high pulse width values for entire CK(Diff) waveform. The CK high pulse width value is measured from CK(Diff) rising edge at VREFdiff_CK middle threshold of a cycle to the next falling edge at VREFdiff_CK middle threshold.
   The default "VREFdiff_CK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].

3 Find the mean high pulse width value of the high pulse width measurements, which will be recorded as the final test result.

4 Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tCH” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

tCL

Test ID: 10030

Test Overview: The purpose of this test is to measure the average CK Low-level width, tCL of all the negative pulses within the waveform window.

Test Procedure:

1 Trigger on the rising edge of the CK(Diff) signal. Acquire CK(Diff) signal.

2 Measure low pulse width values for entire CK(Diff) waveform. The CK low pulse width value is measured from CK(Diff) falling edge at VREFdiff_CK middle threshold of a cycle to the next rising edge at VREFdiff_CK middle threshold.
The default “VREFdiff_CK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].

3 Find the mean low pulse width value of the low pulse width measurements, which will be recorded as the final test result.

4 Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tCL” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

WCK AC Timing Tests

tWCK - Rising Edge

Test ID: 20010

Test Overview: The purpose of this test is to measure the average WCK cycle time, tWCK(Rising Edge) from the rising edge of a cycle to the next rising edge within the waveform window.

Test Procedure:
1. Trigger on the rising edge of the WCK(Diff) signal. Acquire WCK(Diff) signal.
2. Measure period(rising edge) values for entire WCK(Diff) waveform. The WCK period(rising edge) value is measured from WCK(Diff) rising edge at VREFdiff_WCK middle threshold of a cycle to the next rising edge at VREFdiff_WCK middle threshold.
   The default "VREFdiff_WCK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].
3. Find the mean period value of the period measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

Expected/ Observable Results: The measured value of "tWCK – Rising Edge" will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

tWCK - Falling Edge

Test ID: 20011

Test Overview: The purpose of this test is to measure the average WCK cycle time, tWCK(Falling Edge) from the falling edge of a cycle to the next falling edge within the waveform window.

Test Procedure:
1. Trigger on the rising edge of the WCK(Diff) signal. Acquire WCK(Diff) signal.
2. Measure period(falling edge) values for entire WCK(Diff) waveform. The WCK period(falling edge) is measured from WCK(Diff) falling edge at VREFdiff_WCK middle threshold of a cycle to the next falling edge at VREFdiff_WCK middle threshold.
   The default "VREFdiff_WCK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].
3. Find the mean period value of the period measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

Expected/ Observable Results: The measured value of "tWCK – Falling Edge" will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

tWCKH

Test ID: 20020

Test Overview: The purpose of this test is to measure the average WCK High-level width, tWCKH of all the positive pulses within the waveform window.

Test Procedure:
1. Trigger on the rising edge of the WCK(Diff) signal. Acquire WCK(Diff) signal.
2. Measure high pulse width values for entire WCK(Diff) waveform. The WCK high pulse width value is measured from WCK(Diff) rising edge at VREFdiff_WCK middle threshold of a cycle to the next falling edge at VREFdiff_WCK middle threshold.
   The default "VREFdiff_WCK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].

3 Find the mean high pulse width value of the high pulse width measurements, which will be recorded as the final test result.

4 Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tWCKH” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

tWCKL

Test ID: 20030

Test Overview: The purpose of this test is to measure the average WCK Low-level width, tWCKL of all the negative pulses within the waveform window.

Test Procedure:

1 Trigger on the rising edge of the WCK(Diff) signal. Acquire WCK(Diff) signal.

2 Measure low pulse width values for entire WCK(Diff) waveform. The WCK low pulse width value is measured from WCK(Diff) falling edge at VREFdiff_WCK middle threshold of a cycle to the next rising edge at VREFdiff_WCK middle threshold.
The default “VREFdiff_WCK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].

3 Find the mean low pulse width value of the low pulse width measurements, which will be recorded as the final test result.

4 Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tWCKL” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

5 Input Operating Condition Tests

Input Operating Conditions Tests

Test Availability Conditions

All tests in this test group appear for the following configuration in GDDR6 General Setup window:

Signal Source:

- CK_t (SE), CK_c (SE)
- WCK_t (SE), WCK_c (SE)

CK Input Operating Conditions Tests

VIXCK

Test ID: 30010

Test Overview: The purpose of this test is to measure the CK input crossing point voltage, VIXCK of CK_t, CK_c within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CK_t signal. Acquire CK_t and CK_c signals.
2. Find all crossing point voltage of CK_t and CK_c.
3. Find the worst crossing point voltage value of the crossing point voltage measurements, which will be recorded as the final test result.
4. Report the final test result and compare against the compliance test limits.

Expected/ Observable Results: The measured value of VIXCK shall be within the conformance limits as defined in specification mentioned under References section.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

VIDCK (AC)

Test ID: 30020

Test Overview: The purpose of this test is to measure the CK input differential voltage, VIDCK(AC) of CK_t, CK_c within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CK_t signal. Acquire CK_t and CK_c signals.
2. Construct the differential data, CK(Diff) from CK_t and CK_c signals.
3. On CK(Diff) rising edge, find the crossing point at CK(Diff) middle threshold and denoted it as X1 position. Find the position of (X1 + 0.5tCK) and denoted it as X6 position. Measure the maximum voltage of the window within X1 position and X6 position using Infiniium's Histogram feature. If the measured value is less than the VIDCK(AC) Compliance test limit, record this value as "VIDCK(AC)" result for current CK(Diff) positive pulse.
   The default "CK(Diff) middle threshold" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].
4. If the measured value is greater than or equal to the VIDCK(AC) Compliance test limit, by shifting the marker along the rising edge with a user-configured "Increment Time Step" value, find the first point where the voltage crosses the VIDCK(AC) Compliance test limit, denoted this point as X2 position. If the user- configured "tDVAC" value is 0s, record "VIDCK(AC) Compliance test limit" value as the "VIDCK(AC)" result for current CK(Diff) positive pulse.
   The default "tDVAC" value is 0s and this value is configurable in Configure tab using "tDVAC(s)" configurable option.
   The default "Increment Time Step" value is 5ns and this value is configurable in Configure tab using "VIDCK Increment Time Step(s)" configurable option.
5. If the user-configured "tDVAC" value is greater than 0s, from X2 position, by shifting the marker along the edge with a user-configured "Increment Time Step" value, find the first point where the voltage at this position is less than the voltage at previous position and denoted this point as X3 position. Calculate the X position of (X2 + tDVAC) and denoted it as X4 position.
6. Measure the minimum voltage of the window within X3 and X4 using Infiniium's Histogram feature. Record the measured value as "VIDCK(AC)" result for current CK(Diff) positive pulse.
7. Repeat same measurement on CK(Diff) negative pulse.
8. Repeat measurement for total of 200 measurement on CK(Diff) positive and negative pulses.
   The default "Number of measurement" value is 200 and this value is configurable in Configure tab using "Number of Measurement(VIDCK(AC), VIDCK(DC))" configurable option.

9 Find the minimum VIDCK(AC) value of all VIDCK(AC) measurements, which will be recorded as the final test result.

10 Report the final test result and compare against the compliance test limits.

Expected/ Observable Results: The measured value of VIDCK(AC) shall be within the conformance limits as defined in specification mentioned under References section.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

VIDCK (DC)

Test ID: 30021

Test Overview: The purpose of this test is to measure the CK input differential voltage, VIDCK(DC) of CK_t, CK_c within the waveform window.

Test Procedure:

1 Trigger on the rising edge of the CK_t signal. Acquire CK_t and CK_c signals.

2 Construct the differential data, CK(Diff) from CK_t and CK_c signals.

3 On CK(Diff) rising edge, find the crossing point at CK(Diff) middle threshold and denoted it as X1 position. Find the position of (X1 + 0.5tCK) and denoted it as X6 position. Measure the maximum voltage of the window within X1 position and X6 position using Infiniium's Histogram feature. If the measured value is less than the VIDCK(DC) Compliance test limit, record this value as "VIDCK(DC)" result for current CK(Diff) positive pulse.
The default "CK(Diff) middle threshold" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].

4 If the measured value is greater than or equal to the VIDCK(DC) Compliance test limit, by shifting the marker along the rising edge with a user-configured "Increment Time Step" value, find the first point where the voltage crosses the VIDCK(AC) Compliance test limit, denote this point as X2 position.

5 From X2 position, by shifting the marker along the rising edge with a user-configured "Increment Time Step" value, find the first point where the voltage at this position is less than the voltage at previous position and denote this point as X3 position.
The default "Increment Time Step" value is 5ns and this value is configurable in Configure tab using "VIDCK Increment Time Step(s)" configurable option.

6 Calculate X5 position where
X5 position = (X1 +
(tCHtCLRatioMin*tCK)-(VIDCK(DC)ComplianceTestLimit/(CKMaxSlewRate*1e9)))
The "tCHtCLRatioMin" value is configurable in Configure tab using "tCH/tCL(Min)" configurable option.
The default "CKMaxSlewRate" value is 6V/ns and this value is configurable in Configure tab using "CK Max Slew Rate(V/ns)" configurable option.

7 Measure the minimum voltage of the window within X3 and X5 using Infiniium's Histogram feature. Record the measured value as "VIDCK(DC)" result for current CK(Diff) positive pulse.

8 Repeat same measurement on CK(Diff) negative pulse.

9 Repeat measurement for total of 200 measurement on CK(Diff) positive and negative pulses. The default "Number of measurement" value is 200 and this value is configurable in Configure tab using "Number of Measurement(VIDCK(AC), VIDCK(DC))" configurable option.

10 Find the minimum VIDCK(DC) value of all VIDCK(DC) measurements, which will be recorded as the final test result.

11 Report the final test result and compare against the compliance test limits

Expected/ Observable Results: The measured value of VIDCK (DC) shall be within the conformance limits as defined in specification mentioned under References section.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

WCK Input Operating Conditions Tests

VIXWCK

Test ID: 40010

Test Overview: The purpose of this test is to measure the WCK input crossing point voltage, VIXWCK of WCK_t, WCK_c within the waveform window.

Test Procedure:

1 Trigger on the rising edge of the WCK_t signal. Acquire WCK_t and WCK_c signals.

2 Find all crossing point voltage of WCK_t and WCK_c.

3 Find the worst crossing point voltage value of the crossing point voltage measurements, which will be recorded as the final test result.

4 Report the final test result and compare against the compliance test limits.

Expected/ Observable Results: The measured value of VIXWCK shall be within the conformance limits as defined in specification mentioned under References section.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

VIDWCK (AC)

Test ID: 40020

Test Overview: The purpose of this test is to measure the WCK input differential voltage, VIDWCK(AC) of WCK_t, WCK_c within the waveform window.

Test Procedure:

1 Trigger on the rising edge of the WCK_t signal. Acquire WCK_t and WCK_c signals.

2 Construct the differential data, WCK(Diff) from WCK_t and WCK_c signals.

3 On WCK(Diff) rising edge, find the crossing point at WCK(Diff) middle threshold and denoted it as X1 position. Find the position of (X1 + 0.5tWCK) and denoted it as X6 position. Measure the maximum voltage of the window within X1 position and X6 position using Infiniium's Histogram feature. If the measured value is less than the VIDWCK(AC) Compliance test limit, record this value as "VIDWCK(AC)" result for current WCK(Diff) positive pulse.
The default "WCK(Diff) middle threshold" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].

4 If the measured value is greater than or equal to the VIDWCK(AC) Compliance test limit, by shifting the marker along the rising edge with a user-configured "Increment Time Step" value, find the first point where the voltage crosses the VIDWCK(AC) Compliance test limit, denoted this point as X2 position. If the user- configured "tDVAC" value is 0s, record "VIDWCK(AC) Compliance test limit" value as the "VIDWCK(AC)" result for current WCK(Diff) positive pulse.
The default "tDVAC" value is 0s and this value is configurable in Configure tab using "tDVAC(s)" configurable option.
The default "Increment Time Step" value is 5ns and this value is configurable in Configure tab using "VIDWCK Increment Time Step(s)" configurable option.

5 If the user-configured "tDVAC" value is greater than 0s, from X2 position, by shifting the marker along the edge with a user-configured "Increment Time Step" value, find the first point where the voltage at this position is less than the voltage at previous position and denoted this point as X3 position. Calculate the X position of (X2 + tDVAC) and denoted it as X4 position.

6 Measure the minimum voltage of the window within X3 and X4 using Infiniium's Histogram feature. Record the measured value as "VIDWCK(AC)" result for current WCK(Diff) positive pulse.

7 Repeat same measurement on WCK(Diff) negative pulse.

8 Repeat measurement for total of 200 measurement on WCK(Diff) positive and negative pulses. The default "Number of measurement" value is 200 and this value is configurable in Configure tab using "Number of Measurement(VIDWCK(AC), VIDWCK(DC))" configurable option.

9 Find the minimum VIDWCK(AC) value of all VIDWCK(AC) measurements, which will be recorded as the final test result.

10 Report the final test result and compare against the compliance test limits.

Expected/ Observable Results: The measured value of VIDWCK(AC) shall be within the conformance limits as defined in specification mentioned under References section.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

VIDWCK (DC)

Test ID: 40021

Test Overview: The purpose of this test is to measure the WCK input differential voltage, VIDWCK(DC) of WCK_t, WCK_c within the waveform window.

Test Procedure:

1 Trigger on the rising edge of the WCK_t signal. Acquire WCK_t and WCK_c signals.

2 Construct the differential data, WCK(Diff) from WCK_t and WCK_c signals.

3 On WCK(Diff) rising edge, find the crossing point at WCK(Diff) middle threshold and denoted it as X1 position. Find the position of (X1 + 0.5tWCK) and denoted it as X6 position. Measure the maximum voltage of the window within X1 position and X6 position using Infiniium's Histogram feature. If the measured value is less than the VIDWCK(DC) Compliance test limit, record this value as "VIDWCK(DC)" result for current WCK(Diff) positive pulse.
The default "WCK(Diff) middle threshold" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].

4 If the measured value is greater than or equal to the VIDWCK(DC) Compliance test limit, by shifting the marker along the rising edge with a user-configured "Increment Time Step" value, find the first point where the voltage crosses the VIDCK(AC) Compliance test limit, denote this point as X2 position.

5 From X2 position, by shifting the marker along the rising edge with a user-configured "Increment Time Step" value, find the first point where the voltage at this position is less than the voltage at previous position and denote this point as X3 position.
The default "Increment Time Step" value is 5ns and this value is configurable in Configure tab using "VIDWCK Increment Time Step(s)" configurable option.

6 Calculate X5 position where
X5 position = (X1 + (tWCKHtWCKLRatioMin
*tWCK)-(VIDWCK(DC)ComplianceTestLimit/(WCKMaxSlewRate*1e9)))
The "tWCKHtWCKLRatioMin" value is configurable in Configure tab using "tWCKH/tWCKL(min)" configurable option.
The default "WCKMaxSlewRate" value is 6V/ns and this value is configurable in Configure tab using "WCK Max Slew Rate(V/ns)" configurable option.

7 Measure the minimum voltage of the window within X3 and X5 using Infiniium's Histogram feature. Record the measured value as "VIDWCK(DC)" result for current WCK(Diff) positive pulse.

8 Repeat same measurement on WCK(Diff) negative pulse.

9 Repeat measurement for total of 200 measurement on WCK(Diff) positive and negative pulses.
The default "Number of measurement" value is 200 and this value is configurable in Configure tab using "Number of Measurement(VIDWCK(AC), VIDWCK(DC))" configurable option.

10 Find the minimum VIDWCK(DC) value of all VIDWCK(DC) measurements, which will be recorded as the final test result.

11 Report the final test result and compare against the compliance test limits.

Expected/ Observable Results: The measured value of VIDWCK (DC) shall be within the conformance limits as defined in specification mentioned under References section.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification

6 Command Address Input Timings Tests

Command Address Input Timings Tests

Test Availability Conditions

All tests in this test group appear for the following configuration in GDDR6 General Setup window:

Signal Source:

- CK (Diff), CKE_n (for tCKES - Rising, tCKES - Falling, tCKEH - Rising, and tCKEH - Falling tests)
- CK (Diff), CA (for tAS - Rising, tAS - Falling, tAH - Rising, and tAH - Falling tests)

Command Address Input Timings Tests

tCKES-Rising

Test ID: 60010

Test Overview: The purpose of this test is to measure the minimum CKE_n(Rising Edge) input setup time to the associated clock crossing edge within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CKE_n signal. Acquire CKE_n and CK(Diff) signals.
2. Find all crossings on rising edge of the acquired CKE_n signal that cross “VREFC” middle threshold.
   The default “VREFC” value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].
3. For all crossings found, locate the next nearest CK(Diff) rising edge that crosses “VREFdiff_CK”.
   The default “VREFdiff_CK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].
4. Measure the time difference between the CKE_n’s crossing and the corresponding clock crossing as setup time value.
5. Find the minimum setup time value of the setup time measurements, which will be recorded as the final test result.
6. Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tCKES-Rising” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

tCKES-Falling

Test ID: 60011

Test Overview: The purpose of this test is to measure the minimum CKE_n(Falling Edge) input setup time to the associated clock crossing edge within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CKE_n signal. Acquire CKE_n and CK(Diff) signals.
2. Find all crossings on falling edge of the acquired CKE_n signal that cross “VREFC” middle threshold.
   The default “VREFC” value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].
3. For all crossings found, locate the next nearest CK(Diff) rising edge that crosses “VREFdiff_CK”.
   The default “VREFdiff_CK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].
4. Measure the time difference between the CKE_n’s crossing and the corresponding clock crossing as setup time value.
5. Find the minimum setup time value of the setup time measurements, which will be recorded as the final test result.
6. Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tCKES-Falling” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

tCKEH-Rising

Test ID: 60020

Test Overview: The purpose of this test is to measure the minimum CKE_n(Rising Edge) input hold time to the associated clock crossing edge within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CKE_n signal. Acquire CKE_n and CK(Diff) signals.
2. Find all crossings on rising edge of the acquired CKE_n signal that cross “VREFC” middle threshold.
   The default “VREFC” value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].
3. For all crossings found, locate the previous nearest CK(Diff) rising edge that crosses “VREFdiff_CK”.
   The default “VREFdiff_CK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].
4. Measure the time difference between the CKE_n’s crossing and the corresponding clock crossing as hold time value.
5. Find the minimum hold time value of the hold time measurements, which will be recorded as the final test result.
6. Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tCKEH-Rising” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

tCKEH-Falling

Test ID: 60021

Test Overview: The purpose of this test is to measure the minimum CKE_n(Falling Edge) input hold time to the associated clock crossing edge within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CKE_n signal. Acquire CKE_n and CK(Diff) signals.
2. Find all crossings on falling edge of the acquired CKE_n signal that cross “VREFC” middle threshold.
   The default “VREFC” value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].
3. For all crossings found, locate the previous nearest CK(Diff) rising edge that crosses “VREFdiff_CK”.
   The default “VREFdiff_CK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].
4. Measure the time difference between the CKE_n’s crossing and the corresponding clock crossing as hold time value.
5. Find the minimum hold time value of the hold time measurements, which will be recorded as the final test result.
6. Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tCKEH-Falling” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

tAS-Rising

Test ID: 60030

Test Overview: The purpose of this test is to measure the minimum CA(Rising Edge) input setup time to the associated clock crossing edge within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CA signal. Acquire CA and CK(Diff) signals.
2. Find all crossings on rising edge of the acquired CA signal that cross “VREFC” middle threshold. *The default “VREFC” value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].*
3. For all crossings found, locate the next nearest CK(Diff) edge that crosses “VREFdiff_CK”. *The default “VREFdiff_CK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].*
4. Measure the time difference between the CA’s crossing and the corresponding clock crossing as setup time value.
5. Find the minimum setup time value of the setup time measurements, which will be recorded as the final test result.
6. Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tAS-Rising” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

tAS-Falling

Test ID: 60031

Test Overview: The purpose of this test is to measure the minimum CA(Falling Edge) input setup time to the associated clock crossing edge within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CA signal. Acquire CA and CK(Diff) signals.
2. Find all crossings on falling edge of the acquired CA signal that cross “VREFC” middle threshold. *The default “VREFC” value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].*
3. For all crossings found, locate the next nearest CK(Diff) edge that crosses “VREFdiff_CK”. *The default “VREFdiff_CK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].*
4. Measure the time difference between the CA’s crossing and the corresponding clock crossing as setup time value.
5. Find the minimum setup time value of the setup time measurements, which is recorded as the final test result.
6. Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tAS-Falling” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

tAH-Rising

Test ID: 60040

Test Overview: The purpose of this test is to measure the CA(Rising Edge) input hold time to the associated clock crossing edge within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CA signal. Acquire CA and CK(Diff) signals.
2. Find all crossings on rising edge of the acquired CA signal that cross “VREFC” middle threshold. *The default “VREFC” value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].*
3. For all crossings found, locate the previous nearest CK(Diff) edge that crosses “VREFdiff_CK”. *The default “VREFdiff_CK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].*
4. Measure the time difference between the CA’s crossing and the corresponding clock crossing as hold time value.
5. Find the minimum hold time value of the hold time measurements, which will be recorded as the final test result.
6. Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tAH-Rising” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

tAH-Falling

Test ID: 60041

Test Overview: The purpose of this test is to measure the minimum CA(Falling Edge) input hold time to the associated clock crossing edge within the waveform window.

Test Procedure:

1. Trigger on the rising edge of the CA signal. Acquire CA and CK(Diff) signals.
2. Find all crossings on falling edge of the acquired CA signal that cross “VREFC” middle threshold. *The default “VREFC” value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].*
3. For all crossings found, locate the previous nearest CK(Diff) edge that crosses “VREFdiff_CK”. *The default “VREFdiff_CK” value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].*
4. Measure the time difference between the CA’s crossing and the corresponding clock crossing as hold time value.
5. Find the minimum hold time value of the hold time measurements, which will be recorded as the final test result.
6. Report the final test result as informative result.

Expected/ Observable Results: The measured value of “tAH-Falling” will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

7 Data Input and Output Timings Tests

Data Input and Output Timings Tests

Test Availability Conditions

All tests in this test group appear for the following configuration in GDDR6 General Setup window:

Signal Source:

- WCK (Diff), CA9, CA8, DQ

Data Input and Output Timings Tests

tDIPW-Positive

Test ID: 50010

Test Overview: The purpose of this test is to measure the minimum DQ input positive pulse width, tDIPW.

Test Procedure:

1. Separate DQ write data using WCK(Diff), CA8, CA9 and DQ signals by utilizing Infiniium's InfiniiScan - Zone Qualify Triggering feature. The zones' position used for triggering setting is calculated based on user-configured "Write Latency" value.
   The default "Write Latency" value is 5 and this value is configurable in Configure tab using "Write Latency(tCK)". This value must be set according to programmed latency for this test to operate.
2. Measure the positive pulse width of the DQ write data. The positive pulse width is measured from DQ rising edge at "VREFD" middle threshold to the next falling edge at "VREFD" middle threshold for 200 measurements.
   The default "VREFD" value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].
3. Find the minimum positive pulse width value of the positive pulse width measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

Expected/ Observable Results: The "tDIPW-Positive" value will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

tDIPW-Negative

Test ID: 50011

Test Overview: The purpose of this test is to measure the minimum DQ input negative pulse with, tDIPW.

Test Procedure:

1. Perform the following test as a prerequisite:
   50010 [tDIPW-Positive]
2. Measure the negative pulse width of the DQ write data. The negative pulse width is measured from DQ falling edge at "VREFD" middle threshold to the next rising edge at "VREFD" middle threshold for 200 measurements.
   The default "VREFD" value is 0.945V for POD135(or 0.875V for POD125) and this value is configurable in Set Up tab [Threshold Setup Window].
3. Find the minimum negative pulse width value of the negative pulse width measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

Expected/ Observable Results: The "tDIPW-Negative" values will be reported as Informative result.

References: JEDEC 1836.99D Rev 3 GDDR6 SGRAM specification.

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