
N5992MM6E Receiver Debug Tool for MIPI M-PHY® 6

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1 Introduction

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Overview

The N5992MM6E Receiver Debug Tool for MIPI M-PHY® 6 (for short Receiver Debug Tool or N5992MM6E app) is a stand-alone software utility. It provides MIPI M-PHY 6 signals in accordance with the *MIPI Alliance Specification for MIPI M-PHY® Version 6.0* and the *MIPI Alliance Specification for Unified Protocol (MIPI UniPro®) Version 3.0*. The Receiver Debug Tool supports MIPI M-PHY generator hardware based on Keysight XE8-class BERTs, either the M8050A (120 Gbaud) or the M8040A (64 Gbaud).

The N5992MM6E app is a flexible tool for troubleshooting and debugging. The Receiver Debug Tool generates data sequences and allows pattern changes as well as the control of signal levels, data rate, and timing parameters.

The software runs on a standard Windows PC and controls the hardware test resources through appropriate interfaces such as LAN.

NOTE

The definitions of the acronyms and abbreviations used throughout this User Guide are given in **Appendix B: Acronyms and Abbreviations**.

Document History

First Edition (July 2026)

The first edition of this User Guide describes the functionality of software version MPhyG6_Frame Generator_N5992_1.0.0, which is based on the *MIPI Alliance Specification for MIPI M-PHY[®] Version 6.0* and the *MIPI Alliance Specification for Unified Protocol (MIPI UniPro[®]) Version 3.0*.

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2 Test Instrument Setup

Test Instrument Setups	14
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This chapter describes the setups for the different BERTs and how to connect the instruments.

Test Instrument Setups

Setup Workflow

- 1 Select the hardware that you want to use as the pattern generator (M8050A BERT or M8040A BERT).
- 2 Then set up the test instruments and establish the required connections between them (see [Connecting the Instruments](#) on page 16).
- 3 Finally, proceed to the connection tab of the N5992MM6E app ([Connecting to the Instruments](#) on page 51).

Pattern Generator

N5992MM6E supports the M8050A BERT or M8040A BERT as the pattern generator.

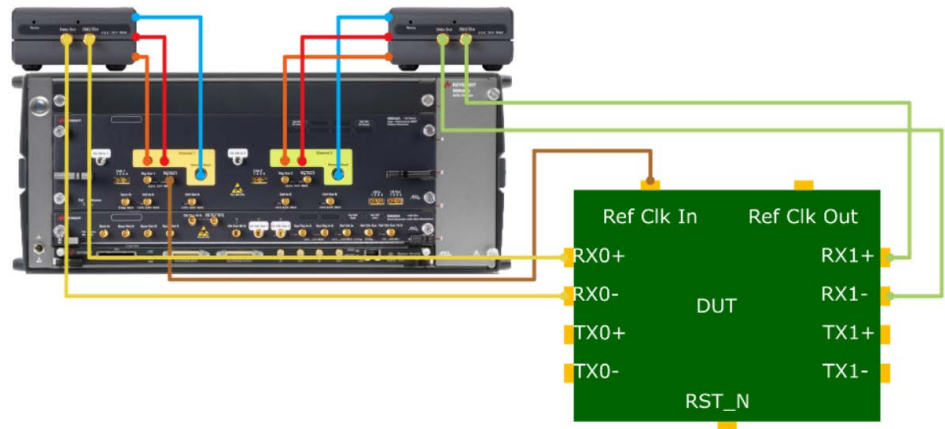


Figure 2-1 M8050A BERT hardware setup, two channels

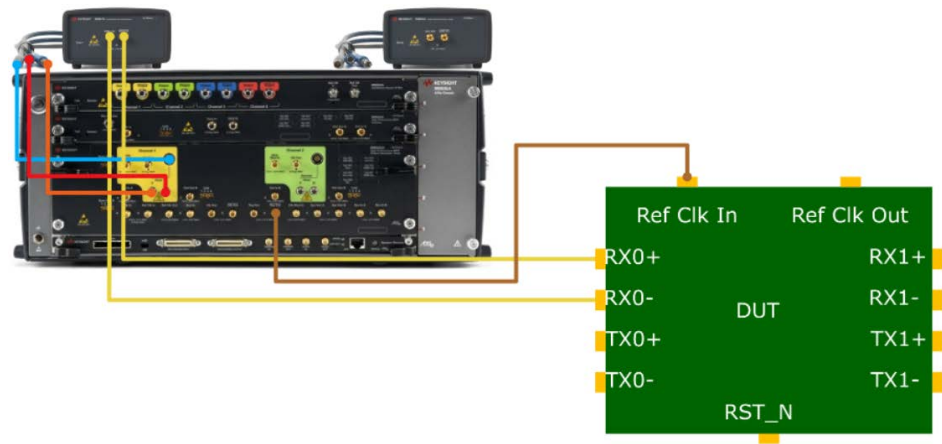


Figure 2-2 M8040A BERT hardware setup, one channel

Connecting the Instruments

Before using the connection part of the N5992MM6E software, set up the test instruments and the device under test (DUT) and establish the required connections between them.

- 1** Connect the test station instruments to the test station controller PC by remote control interfaces, such as LAN or USB.
- 2** Establish all required cable connections between the instruments and the DUT.
- 3** Switch on the PC and instruments.
- 4** Start the *Keysight IO VISA Connection Expert* and check the connections for the instruments. The use of the Connection Expert is described in the [ValiFrame Getting Started Guide](#).

3 Preparing the Software

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This chapter describes how to download and install the N5992MM6E Receiver Debug Tool software. How to obtain a valid license for the software is also explained.

Overview

This chapter describes how to download, install, and start the N5992MM6E Receiver Debug Tool.

Software Prerequisites

Before the N5992MM6E app can be installed, the following software must already be installed on the PC with Windows Operating System:

- Microsoft .NET Framework
- Keysight IO Libraries Suite

The N5992MM6E app changelog lists the required versions. You can download the changelog for the software version that you are going to use from the [BitifEye Download Hub](#).

NOTE

On the BitifEye Download Hub, the N5992MM6E app can be found under the Debug Tool tab of the MIPI M-PHY 6 page as *MIPI M-PHY G6 N5992 Frame Generator*.

Software Download and Installation

- 1 Download the N5992MM6E software installer from the [BitifEye Download Hub](#).
 - a Select MIPI M-PHY G6
 - b Select N5992 Debug Tools
 - c Click  and select Download installer file.

You can download the changelog from there as well.

NOTE

You will need to register for the [BitifEye Download Hub](#) before you can use it.

- 2 Execute the installer file
MPhyG6_Frame Generator_N5992_X.X.X.X_Installer.exe,
where X.X.X.X specifies the version number.
- 3 The welcome page of the setup program will open. The second page of the setup program will show the Keysight Software End-User License Agreement. Read it carefully and select **I accept the terms of the License Agreement**, Click **Next**.
- 4 On the Required Software page:
 - if some of the required software is marked as missing, install the missing software and try again
 - if all required software is installed, click **Next**
- 5 In the Choose Install Location window you have a choice:
 - either
 - confirm the default path (recommended)
 - or
 - click **Browse...** to select the destination folder for the software.
- 6 Click **Install** to install the software.

After the installation, the computer does not need to be rebooted. The *M-PHY Frame Generator (N5992)* icon will be added to the desktop ([Figure 3-1](#)).

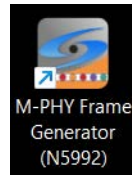


Figure 3-1 Desktop icon

Starting the Software

Start the software by double-clicking the M-PHY Frame Generator (N5992) icon on the desktop. Alternatively, start the application by searching for M-PHY Frame Generator (N5992).

Licenses

If there is a valid license on the PC, the software will open and can be run.

Attempting to start the software without a valid license opens the “No license found!” dialog window. To obtain a valid license, contact your Keysight representative.

Once you have a certificate number for a license, use the BitifEye License Manager (BLM) portal <https://licensing.bitifeye.com/> to add the license to your BLM account and activate it.

For detailed instructions on how to use the BLM, please refer to the [BitifEye License Manager User Guide](#).

4 Using the Software

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This chapter describes how to configure the instrument setup, using the Connection window of the N5992MM6E software, and how to select the MIPI M-PHY 6 signal parameters, using the various tabs in the Signal window.

Overview

This chapter first describes example workflows to configure the frame generator and apply a test pattern to the BERT for MIPI M-PHY receiver testing. This is followed by more details about the various tabs of the frame generator and the parameters to be configured.

General Workflows

This section describes the steps required to configure a setup and apply a test pattern to the BERT for MIPI M-PHY receiver testing. The process guides you first through the instrument connection process and then through a sequence of setup tabs: protocol timing configuration, data rate selection, pattern setup, voltage configuration, and skew adjustment.

The following workflows are described:

- 1 **Configuring the Hardware Connections**
- 2 **Generating an NRZ HS Signal**
- 3 **Generating a PAM4 HS Signal**
- 4 **Generating a Signal with PWM and Multiple HS Gears**

Follow these workflows to ensure that all BERT parameters are configured consistently and that the stimulus applied to the DUT meets the required test conditions before receiver characterization or compliance testing is performed.

The workflows cover:

- 1 Connecting and verifying all required instruments.
- 2 Configuring protocol timing parameters.
- 3 Selecting the required data rates and operating gears.
- 4 Loading and applying the pattern to the BERT.
- 5 Setting the appropriate voltage levels.
- 6 Configuring lane skew parameters.
- 7 Verifying the final test setup before execution.

Configuring the Hardware Connections

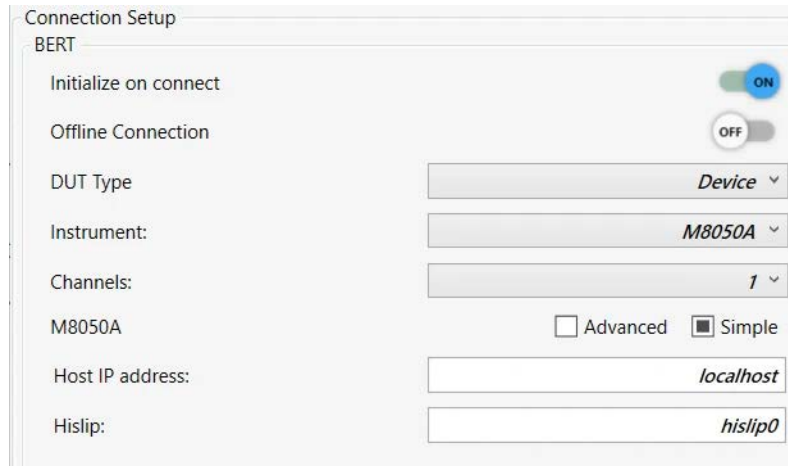


Figure 4-1 Connection Setup pane

In the Connection Setup pane of the CONNECTION window (Figure 4-1):

- 1** Ensure that Offline Connection is set to OFF.
- 2** Select the DUT Type.
- 3** Select the instrument module (BERT).
- 4** Select the number of channels.
- 5** Enter instrument address information.
- 6** Click **Connect**.

If the connection was successful, the message “Connection to instruments successful!” will appear in the log pane and the SIGNAL window will open.

For more details see [Connecting to the Instruments](#) on page 51.

Generating an NRZ HS Signal

This workflow is for just one NRZ HS gear. For multiple gears, see [Generating a Signal with PWM and Multiple HS Gears](#) on page 41.

After the hardware connection (in the CONNECTION window), this workflow progresses through the tabs of the SIGNAL window from left to right:

- 1** In the CONNECTION window: Configure the hardware connections.
 - 2** In the Protocol Tab:
 - a** Configure the M-PHY NRZ protocol parameters.
 - b** Configure the Other Settings protocol parameters.
 - 3** In the Data Rates Tab:
 - a** Select the desired NRZ HS Gear.
 - b** Configure the BERT Settings.
 - 4** In the Pattern Tab: Load or create an NRZ burst sequence.
 - 5** In the Voltage Levels Tab:
 - a** Configure the clock levels.
 - b** Configure the data levels for each data channel.
 - 6** In the Skew Tab: Adjust timing alignment between clock and data.
 - 7** Generate the NRZ HS Signal:
 - a** Verify the protocol settings.
 - b** Verify the selected HS gear.
 - c** Verify the pattern sequence.
 - d** Verify the voltage levels.
 - e** Verify the skew.
 - f** Click **APPLY**.
 - 8** Visualize the NRZ HS signal using the Protocol Decoder on the oscilloscope.
- The following pages provide more details.

1 CONNECTION Window

See [Configuring the Hardware Connections](#) on page 24.

2 Protocol Tab

(See also [Protocol Tab](#) on page 57)

- a Configure the M-PHY NRZ protocol parameters.
- b Configure the Other Settings protocol parameters.

[Figure 4-2](#) shows the default starting values in the High Speed (NRZ) pane of the Protocol Tab.

[Figure 4-3](#) shows the default values in the Other Settings pane.

10-bit words are normally used because M-PHY NRZ utilizes 8b/10b-encoded symbols.

High Speed (NRZ)	
HS Prepare Length:	7
HS Sync Length:	7
Stall Length [UI]:	20
HS Sync Range:	Fine
Initial Adapt Length:	0
Refresh Adapt Length:	0
Initial Adapt Range:	Fine
Refresh Adapt Range:	Fine
Sync Pattern:	D10.5, D26.5

Figure 4-2 Default starting values of M-PHY High Speed (NRZ) protocol parameters

Other Settings

Squelch Pulses:	1
Squelch Pulse Width:	20 ns
Squelch Pulse Distance:	500 ns
Word Size - NRZ (bits):	10

Figure 4-3 Default starting values of M-PHY Other Settings protocol parameters

3 Data Rates Tab

(See also [Data Rates Tab](#) on page 63)

- a Select the desired NRZ HS Gear in the High Speed pane ([Figure 4-4](#)).

High Speed

HS Gear

☐ Gear 4-A

☐ Gear 4-B

☒ Gear 5-A

☐ Gear 5-B

☐ Gear 6-A

HS Data Rate Deviation [ppm]:

0

Figure 4-4 Selecting an HS Gear

NOTE

If the pattern contains @HSG5A, for example, then Gear 5-A must also be selected in the Data Rates Tab, otherwise the sequence validation will fail.

- b Configure the Reference Clock Frequency and the BERT Symbol Rate in the BERT Settings pane ([Figure 4-5](#)).

BERT Settings

Ref. Clock Frequency:	26 MHz
BERT Symbol Rate:	19.968 GBd

Figure 4-5 Configuring BERT Settings

4 Pattern Tab

(See also **Pattern Tab** on page 66)

Load or create an NRZ burst sequence.

Click the folder icon to load MPhyCompliance.seq or your custom sequence.

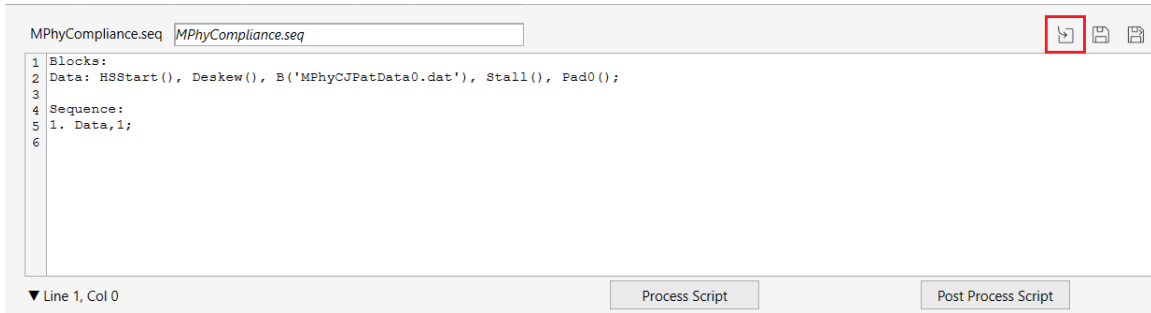


Figure 4-6 Loading the NRZ sequence file MPhyCompliance.seq

This sequence includes:

- A** Start an HS burst.
- B** Apply 8b/10b encoding.
- C** Send markers.
- D** Send payload data.
- E** Apply STALL period.
- F** Pad the end to meet the granularity of the BERT.

If only a single HS Gear is selected, both of the sequences below have the same result.

Example 1

Blocks:

Data: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0();

Sequence:

1. Data,1;

Example 2

Blocks:

```
Data: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0()
@HSG5A;
```

Sequence:

1. Data,1;

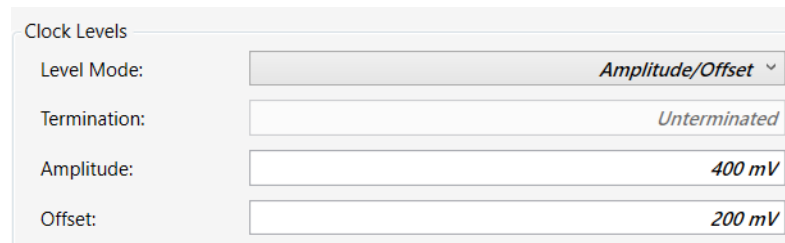
The token must match the gear selected in the Data Rates Tab.

5 Voltage Levels Tab

(See also [Voltage Levels Tab](#) on page 70)

Although the Voltage Levels Tab supports PAM4 level definitions, it is also used to configure NRZ output amplitude and offsets.

- a Configure clock levels:** The supported clock amplitude range is 200 mV to 2 V. [Figure 4-7](#) shows example values for clock levels.



The screenshot shows a 'Clock Levels' configuration window with the following settings:

Parameter	Value
Level Mode:	Amplitude/Offset
Termination:	Unterminated
Amplitude:	400 mV
Offset:	200 mV

Figure 4-7 Example clock level values

b Configure data levels: Figure 4-8 shows example values for data levels.

Remote Head:	M8058A
Data0 Levels	
DIF-P Voltage Level:	270 mV
DIF-IP Voltage Level:	90 mV
DIF-IN Voltage Level:	-90 mV
DIF-N Voltage Level:	-270 mV
Data Offset:	250 mV
Termination Model:	Unbalanced
Apply All Levels	

Figure 4-8 Example data level values

The PAM4 level settings are used to set the NRZ levels. Using the PAM4 example values of Figure 4-8, we have:

- Data Offset 250 mV
- DIF-P (+270 mV) → L3 (385 mV)
- DIF-IP (+90 mV) → L2 (295 mV)
- DIF-IN (-90 mV) → L1 (205 mV)
- DIF-N (-270 mV) → L0 (115 mV)

Therefore, the corresponding NRZ signal levels would be:

- NRZ High Level = L3 = 385 mV
- NRZ Low Level = L0 = 115 mV
- NRZ Amplitude = 270 mV
- NRZ Common Mode (Offset) = 250 mV

c Termination Model (in the Data Levels pane)

If the BERT is connected to the oscilloscope, set the Termination Model to “Unbalanced”.

If the BERT is connected to the DUT, the Termination Model is set to “Balanced” (default value).

d Click **Apply All Levels**.

6 Skew Tab

(See also [Skew Tab](#) on page 74)

Adjust the timing alignment between clock and data. The software allows the range -50 ns to +50 ns skew adjustment. Changes are applied immediately.

7 Generate the NRZ HS signal

After configuration:

- a** Verify Protocol settings.
- b** Verify selected HS Gear.
- c** Verify Pattern sequence.
- d** Verify Voltage Levels.
- e** Verify Skew.
- f** Click **APPLY**.

The software sends all the values from the tabs to the BERT in sequence. If the application is successful, the switches Global Outputs and Sequence State both toggle to ON, and the M8050A/M8040A BERT begins generating the configured M-PHY NRZ HS signal.

8 Visualize the NRZ HS signal

Use the Protocol Decoder on the oscilloscope to visualize the NRZ HS signal ([Figure 4-9](#)).

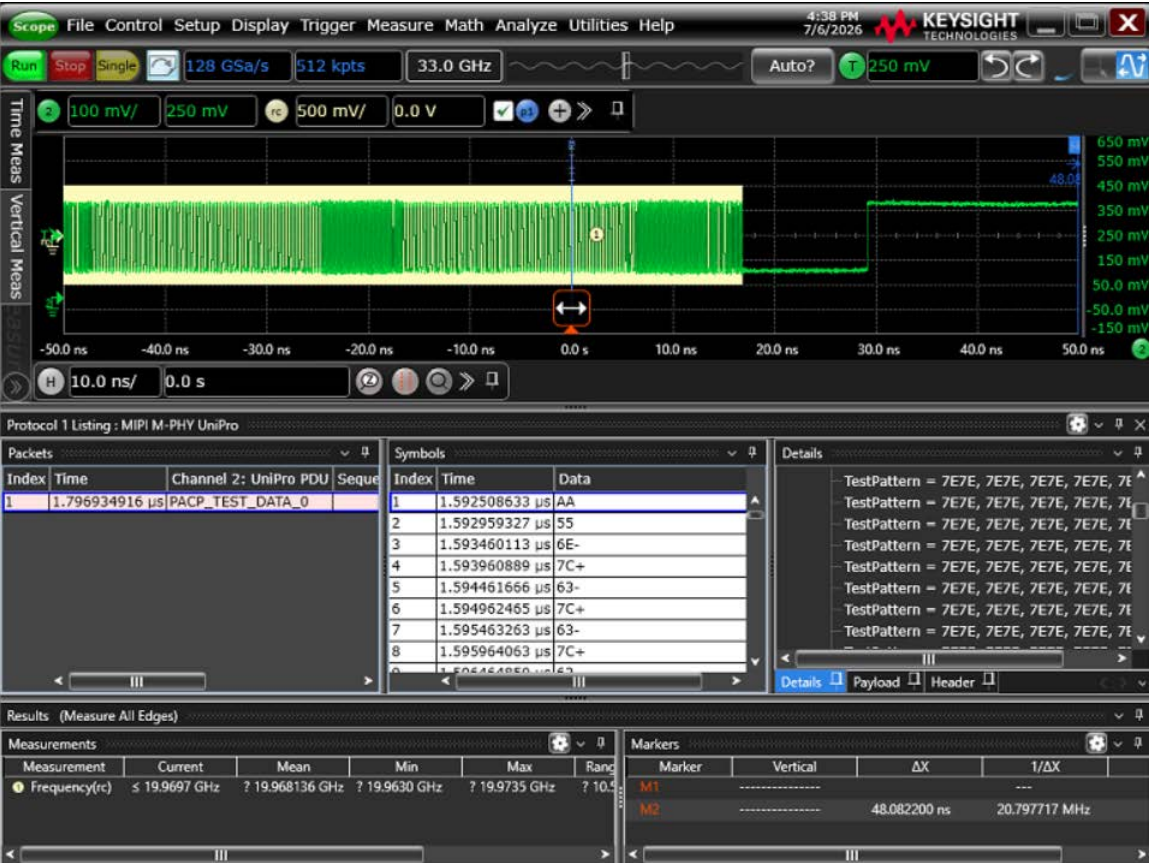


Figure 4-9 Visualization of the NRZ HS signal

Generating a PAM4 HS Signal

After the hardware connection (in the CONNECTION window), this workflow progresses through the tabs of the SIGNAL window from left to right:

- 1** In the CONNECTION window: Configure the hardware connections.
 - 2** In the Protocol Tab:
 - a** Configure the M-PHY PAM4 protocol parameters.
 - b** Configure the Other Settings protocol parameters.
 - 3** In the Data Rates Tab:
 - a** Select the desired PAM4 HS Gear.
 - b** Configure the BERT Settings.
 - 4** In the Pattern Tab: Load or create a PAM4 burst sequence.
 - 5** In the Voltage Levels Tab:
 - a** Configure the clock levels.
 - b** Configure the data levels for each data channel.
 - 6** In the Skew Tab: Adjust timing alignment between clock and data.
 - 7** Generate the PAM4 HS Signal:
 - a** Verify the protocol settings.
 - b** Verify the selected HS gear.
 - c** Verify the pattern sequence.
 - d** Verify the voltage levels.
 - e** Verify the skew.
 - f** Click **APPLY**.
 - 8** Visualize the PAM4 HS signal using the Protocol Decoder on the oscilloscope.
- The following pages provide more details.

1 CONNECTION Window

See [Configuring the Hardware Connections](#) on page 24.

2 Protocol Tab

(See also [Protocol Tab](#) on page 57)

- a** Configure the M-PHY PAM4 protocol parameters.
- b** Configure the Other Settings protocol parameters.

[Figure 4-10](#) shows the default starting values in the High Speed (PAM4) pane of the Protocol Tab.

[Figure 4-11](#) shows the default values in the Other Settings pane.

The PAM4 word size can be either 8 or 16 bits; 16 bits is commonly used.

The image shows a software window titled "High Speed (PAM4)". It contains several configuration parameters, each with a text label and a corresponding input field. The parameters and their values are as follows:

Parameter	Value
HS Prepare Length:	7
HS Sync Length L0_L3:	7
HS Sync Length L0_L1_L2_L3:	7
Align Pattern:	5E993396B6C10CEC
Stall Length [UI (PAM4)]:	128
Initial Adapt Length L0_L1_L2_L3:	0
Refresh Adapt Length L0_L1_L2_L3:	0
Initial Adapt Range L0_L1_L2_L3:	Fine
Refresh Adapt Range L0_L1_L2_L3:	Fine

Figure 4-10 Default starting values of M-PHY High Speed (PAM4) protocol parameters

Other Settings

Squelch Pulses:	1
Squelch Pulse Width:	20 ns
Squelch Pulse Distance:	500 ns
Word Size - NRZ (bits):	10 ▾
Word Size - PAM4 (bits):	16 ▾

Figure 4-11 Default starting values of M-PHY Other Settings protocol parameters

3 Data Rates Tab

(See also [Data Rates Tab](#) on page 63)

- a Select the desired PAM4 HS Gear in the High Speed pane ([Figure 4-12](#)).

High Speed

HS Gear

☐ Gear 4-B

☐ Gear 5-A

☐ Gear 5-B

☒ Gear 6-A

☐ Gear 6-B

HS Data Rate Deviation [ppm]: 0

Figure 4-12 Selecting HS Gear 6-A

NOTE

If the pattern contains @HSG6A, for example, then Gear 6-A must also be selected in the Data Rates Tab, otherwise the sequence validation will fail.

- b Configure the Reference Clock Frequency and the BERT Symbol Rate in the BERT Settings pane ([Figure 4-13](#)).

BERT Settings

Ref. Clock Frequency:	26 MHz ▾
BERT Symbol Rate:	19.968 GBd ▾

Figure 4-13 Configuring BERT Settings

4 Pattern Tab

(See also **Pattern Tab** on page 66)

Load or create a PAM4 burst sequence.

Click the folder icon to load MPhyG6Burst.seq or your custom sequence.

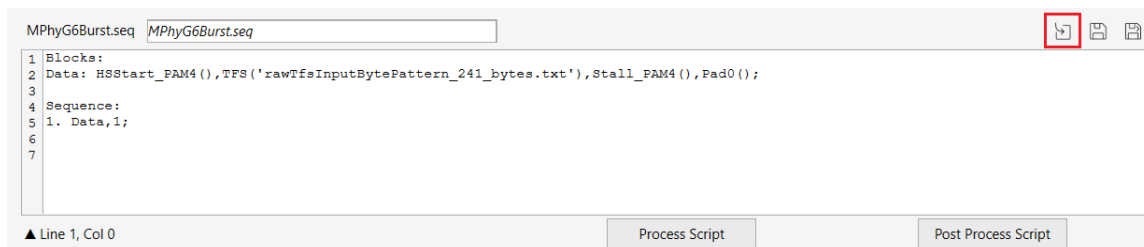


Figure 4-14 Loading the PAM4 sequence file MPhyG6Burst.seq

This sequence includes:

- A** Start a PAM4 HS burst.
- B** Send PAM4 payload data as TFS frames.
- C** Add a PAM4 stall period.
- D** Pad the end to meet the granularity of the BERT.

If only a single HS Gear is selected, both of the sequences below have the same result.

Example 1

Blocks:

```
Data: HSStart_PAM4(), TFS('rawTfsInputBytePattern_241_bytes.txt'),
Stall_PAM4(), Pad0();
```

Sequence:

```
1. Data, 1;
```

Example 2

Blocks:

```
Data: HSStart_PAM4(), TFS('rawTfsInputBytePattern_241_bytes.txt'),
Stall_PAM4(), Pad0() @HSG6A;
```

Sequence:

1. Data,1;

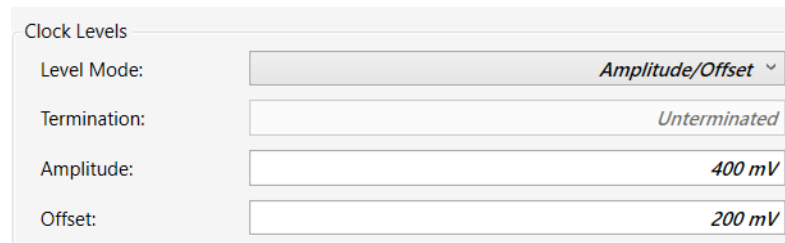
The token must match the gear selected in the Data Rates Tab.

5 Voltage Levels Tab

(See also [Voltage Levels Tab](#) on page 70)

The Voltage Level Tab defines PAM4 levels, but it is also used to configure PAM4 output amplitude and offsets.

a Configure clock levels: The supported clock amplitude range is 200 mV to 2 V. [Figure 4-15](#) shows recommended starting values for clock levels.



The screenshot shows a software interface for configuring clock levels. It has a title bar 'Clock Levels' and four rows of configuration options. Each row has a label on the left and a value in a text box on the right. The values are italicized. The first row is 'Level Mode' with a dropdown menu showing 'Amplitude/Offset'. The second row is 'Termination' with the value 'Unterminated'. The third row is 'Amplitude' with the value '400 mV'. The fourth row is 'Offset' with the value '200 mV'.

Label	Value
Level Mode:	<i>Amplitude/Offset</i>
Termination:	<i>Unterminated</i>
Amplitude:	<i>400 mV</i>
Offset:	<i>200 mV</i>

Figure 4-15 Example clock level values

b Configure data levels: Figure 4-16 shows example values for data levels.

Remote Head:	M8058A
Data0 Levels	
DIF-P Voltage Level:	270 mV
DIF-IP Voltage Level:	90 mV
DIF-IN Voltage Level:	-90 mV
DIF-N Voltage Level:	-270 mV
Data Offset:	250 mV
Termination Model:	Unbalanced ▾
Apply All Levels	

Figure 4-16 Example data level values

This gives the following values for L0, L1, L2, and L3:

- Data Offset 250 mV
- DIF-P (+270 mV) → L3 (385 mV)
- DIF-IP (+90 mV) → L2 (295 mV)
- DIF-IN (-90 mV) → L1 (205 mV)
- DIF-N (-270 mV) → L0 (115 mV)

c Termination Model (in the Data Levels pane)

If the BERT is connected to the oscilloscope, set the Termination Model to “Unbalanced”.

If the BERT is connected to the DUT, the Termination Model is set to “Balanced” (default value).

d Click Apply All Levels.

6 Skew Tab

(See also [Skew Tab](#) on page 74)

Adjust the timing alignment between clock and data. The software allows the range -50 ns to +50 ns skew adjustment. Changes are applied immediately.

7 Generate the PAM4 HS signal

After configuration:

- a** Verify Protocol settings.
- b** Verify selected HS Gear.
- c** Verify Pattern sequence.
- d** Verify Voltage Levels.
- e** Verify Skew.
- f** Click **APPLY**.

The software sends all the values from the tabs to the BERT in sequence. If the application is successful, the switches Global Outputs and Sequence State both toggle to ON, and the M8050A/M8040A BERT begins generating the configured M-PHY PAM4 HS signal.

8 Visualize the PAM4 HS signal

Use the Protocol Decoder on the oscilloscope to visualize the PAM4 HS signal ([Figure 4-17](#)).

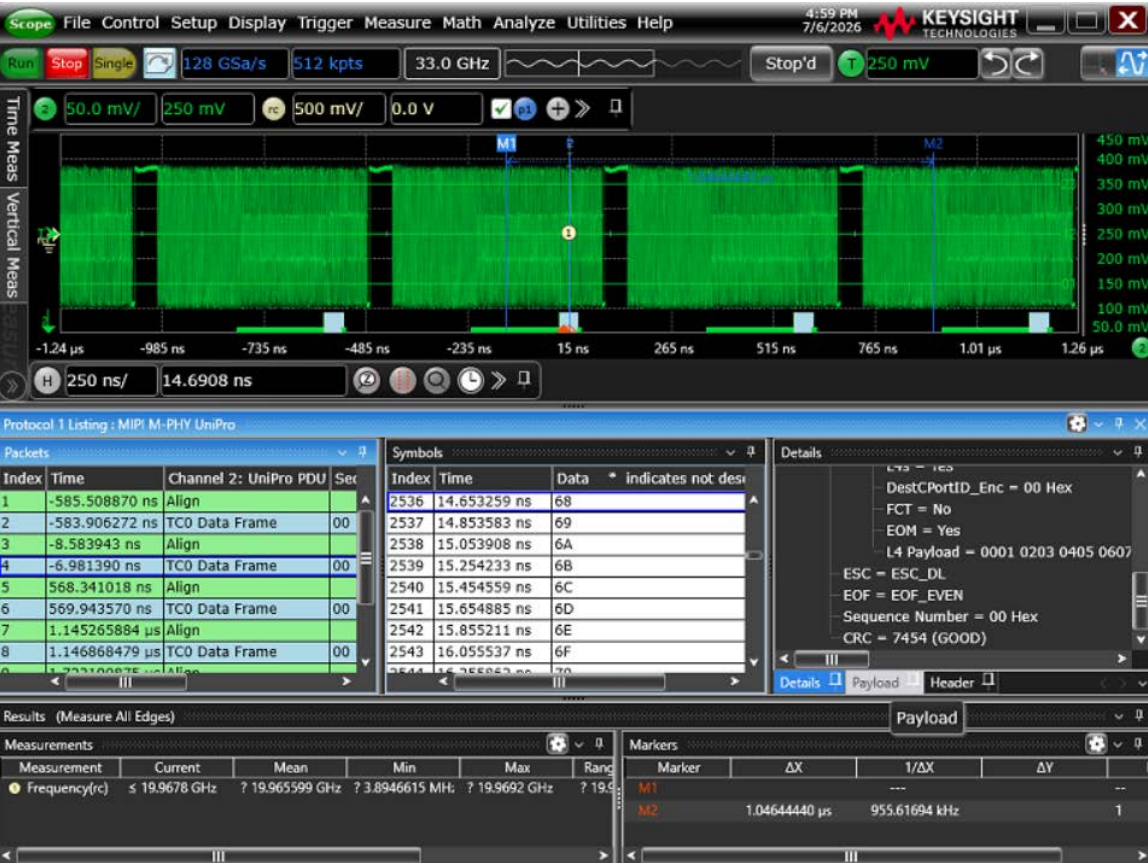


Figure 4-17 Visualization of the PAM4 HS signal

Generating a Signal with PWM and Multiple HS Gears

After the hardware connection (in the CONNECTION window), this workflow progresses through the tabs of the SIGNAL window from left to right:

- 1 In the CONNECTION window: Configure the hardware connections.
- 2 In the Protocol Tab:
 - a Configure the Low Speed (PWM) protocol parameters.
 - b Configure the High Speed (NRZ) protocol parameters.
 - c Configure the High Speed (PAM4) protocol parameters.
 - d Configure the Other Settings protocol parameters.
- 3 In the Data Rates Tab:
 - a Select the desired NRZ HS Gears, PAM4 Gear, and PWM.
 - b Configure the BERT Settings.
- 4 In the Pattern Tab: Load or create a multiple-data-rate burst sequence.
- 5 In the Voltage Levels Tab:
 - a Configure the clock levels.
 - b Configure the data levels for each data channel.
- 6 In the Skew Tab: Adjust timing alignment between clock and data.
- 7 Generate the multiple-data-rate signal:
 - a Verify the protocol settings.
 - b Verify the selected PWM and HS gears.
 - c Verify the pattern sequence.
 - d Verify the voltage levels.
 - e Verify the skew.
 - f Click **APPLY**.
- 8 Visualize the multiple-data-rate signal using the Protocol Decoder on the oscilloscope.

The following pages provide more details.

1 CONNECTION Window

See [Configuring the Hardware Connections](#) on page 24.

2 Protocol Tab

(See also [Protocol Tab](#) on page 57)

- a Configure the Low Speed (PWM) protocol parameters.
- b Configure the High Speed (NRZ) protocol parameters.
- c Configure the High Speed (PAM4) protocol parameters.
- d Configure the Other Settings protocol parameters.

[Figure 4-18](#) shows default values in the Low Speed (PWM) parameters pane of the Protocol Tab.

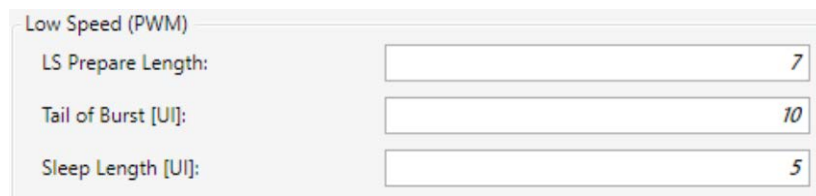
[Figure 4-19](#) shows the default starting values in the High Speed (NRZ) pane.

[Figure 4-20](#) shows the default starting values in the High Speed (PAM4) pane.

[Figure 4-21](#) shows the default values in the Other Settings pane.

10 bits is normally used for NRZ Word Size because M-PHY NRZ utilizes 8b/10b-encoded symbols.

16 bits is commonly used for PAM4 Word Size.



Low Speed (PWM)	
LS Prepare Length:	7
Tail of Burst [UI]:	10
Sleep Length [UI]:	5

Figure 4-18 Default values of M-PHY Low Speed (PWM) protocol parameters

High Speed (NRZ)	
HS Prepare Length:	7
HS Sync Length:	7
Stall Length [UI]:	20
HS Sync Range:	Fine ▾
Initial Adapt Length:	0
Refresh Adapt Length:	0
Initial Adapt Range:	Fine ▾
Refresh Adapt Range:	Fine ▾
Sync Pattern:	D10.5, D26.5

Figure 4-19 Default starting values of M-PHY High Speed (NRZ) protocol parameters

High Speed (PAM4)	
HS Prepare Length:	7
HS Sync Length L0_L3:	7
HS Sync Length L0_L1_L2_L3:	7
Align Pattern:	5E993396B6C10CEC
Stall Length [UI (PAM4)]:	128
Initial Adapt Length L0_L1_L2_L3:	0
Refresh Adapt Length L0_L1_L2_L3:	0
Initial Adapt Range L0_L1_L2_L3:	Fine ▾
Refresh Adapt Range L0_L1_L2_L3:	Fine ▾

Figure 4-20 Default starting values of M-PHY High Speed (PAM4) protocol parameters

Other Settings	
Squelch Pulses:	1
Squelch Pulse Width:	20 ns
Squelch Pulse Distance:	500 ns
Word Size - NRZ (bits):	10 ▾
Word Size - PAM4 (bits):	16 ▾

Figure 4-21 Default starting values of M-PHY Other Settings protocol parameters

3 Data Rates Tab

(See also [Data Rates Tab](#) on page 63)

- a Select the desired NRZ HS Gears, PAM4 Gear, and PWM. See [Figure 4-22](#).

High Speed		Low Speed	
HS Gear	☐ Gear 4-B ☒ Gear 5-A ☐ Gear 5-B ☒ Gear 6-A ☐ Gear 6-B	Support PWM	☒
HS Data Rate Deviation [ppm]:	0	PWM Data Rate:	4.4973 MBit/s
		PWM Bit Resolution:	4440

Figure 4-22 Selecting multiple gears

NOTE

If the pattern contains @HSG1A, @HSG2A, @HSG3A, @HSG4A, @HSG5A, and @HSG6A, for example, then the options Gear 1-A, Gear 2-A, Gear 3-A, Gear 4-A, Gear 5-A, and Gear6-A must also be selected in the Data Rates Tab, otherwise the sequence validation will fail.

If the pattern includes a PWM block, **Support PWM** must be selected.

- b** Configure the BERT Settings. See [Figure 4-23](#).

BERT Settings

Ref. Clock Frequency: 26 MHz

BERT Symbol Rate: 19.968 GBd

Figure 4-23 Configuring BERT Settings

4 Pattern Tab

(See also [Pattern Tab](#) on page 66)

Load or create a multiple-data-rate burst sequence.

Click the folder icon to load MPhyCompliance.seq or your custom sequence.

```

1 Blocks:
2
3 DataPWM: LSStart(), Deskew(), LB('MPhyCJPatData0.dat'), LSStall(), Pad0();
4 DataHSG1A: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0() @HSG1A;
5 DataHSG2A: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0() @HSG2A;
6 DataHSG3A: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0() @HSG3A;
7 DataHSG4A: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0() @HSG4A;
8 DataHSG5A: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0() @HSG5A;
9 DataHSG6A: HSStart_PAM4(), TFS('rawTfsInputBytePattern_24i_bytes.txt'), Stall_PAM4(), Pad0() @HSG6A;
10
11 Sequence:
12
13 1. DataPWM, 1;
14 2. DataHSG1A, 1;
15 3. DataHSG2A, 1;
16 4. DataHSG3A, 1;
17 5. DataHSG4A, 1;
18 6. DataHSG5A, 1;
19 7. DataHSG6A, 1;
20

```

Figure 4-24 Loading the sequence file MPhyAllGearsBurst.seq

This sequence includes the following:

- A** Low Speed transmission mode.
 - i** Send the Low-Speed start sequence.
 - ii** Send deskew/alignment symbols.
 - iii** Load and transmit the pattern from file.
 - iv** Send a Low-Speed idle/stall sequence.
 - v** Pad the end to meet the granularity of the BERT.

- B** High Speed NRZ HSG1A–HSG5A transmission mode.
 - i** Start an HS burst.
 - ii** Apply 8b/10b encoding.
 - iii** Send markers.
 - iv** Send payload data.
 - v** Apply STALL period.
 - vi** Pad the end to meet the granularity of the BERT.
- C** High Speed PAM4 HSG6A transmission mode.
 - i** Start a PAM4 HS burst.
 - ii** Send PAM4 payload data as TFS frames.
 - iii** Add a PAM4 stall period.
 - iv** Pad the end to meet the granularity of the BERT.

5 Voltage Levels Tab

(See also [Voltage Levels Tab](#) on page 70)

Although the Voltage Levels Tab supports PAM4 level definitions, it is also used to configure NRZ output amplitude and offsets.

- a Configure clock levels:** The supported clock amplitude range is 200 mV to 2 V. [Figure 4-7](#) shows example values for clock levels.

The screenshot shows a 'Clock Levels' configuration window with the following settings:

Level Mode:	Amplitude/Offset ▾
Termination:	Unterminated
Amplitude:	400 mV
Offset:	200 mV

Figure 4-25 Example clock level values

b Configure data levels: Figure 4-8 shows example values for data levels.

Remote Head:	M8058A
Data0 Levels	
DIF-P Voltage Level:	270 mV
DIF-IP Voltage Level:	90 mV
DIF-IN Voltage Level:	-90 mV
DIF-N Voltage Level:	-270 mV
Data Offset:	250 mV
Termination Model:	Balanced ▾
Apply All Levels	

Figure 4-26 Example data level values

The PAM4 level settings are used to set the NRZ levels. Using the PAM4 example values of Figure 4-26, we have:

- Data Offset 250 mV
- DIF-P (+270 mV) → L3 (385 mV)
- DIF-IP (+90 mV) → L2 (295 mV)
- DIF-IN (-90 mV) → L1 (205 mV)
- DIF-N (-270 mV) → L0 (115 mV)

Therefore, the corresponding NRZ signal levels would be:

- NRZ High Level = L3 = 385 mV
- NRZ Low Level = L0 = 115 mV
- NRZ Amplitude = 270 mV
- NRZ Common Mode (Offset) = 250 mV

c Termination Model (in the Data Levels pane)

If the BERT is connected to the oscilloscope, set the Termination Model to “Unbalanced”.

If the BERT is connected to the DUT, the Termination Model is set to “Balanced” (default value).

- d** Click **Apply All Levels**.

NOTE

The NRZ levels are applied for PWM and all HS gears, HSG1–HSG5.

6 Skew Tab

(See also **Skew Tab** on page 74)

Adjust the timing alignment between clock and data. The software allows the range –50 ns to +50 ns skew adjustment. Changes are applied immediately.

7 Generate the multiple-data-rate signal

After configuration:

- a** Verify Protocol settings.
- b** Verify the selected PWM and HS gears.
- c** Verify Pattern sequence.
- d** Verify Voltage Levels.
- e** Verify Skew.
- f** Click **APPLY**.

The software sends all the values from the tabs to the BERT in sequence. If the application is successful, the switches Global Outputs and Sequence State both toggle to ON, and the M8050A/M8040A BERT begins generating the configured M-PHY multiple-data-rate signal.

8 Visualize the multiple-data-rate signal

Use the oscilloscope to visualize the multiple-data-rate signal (**Figure 4-27**).

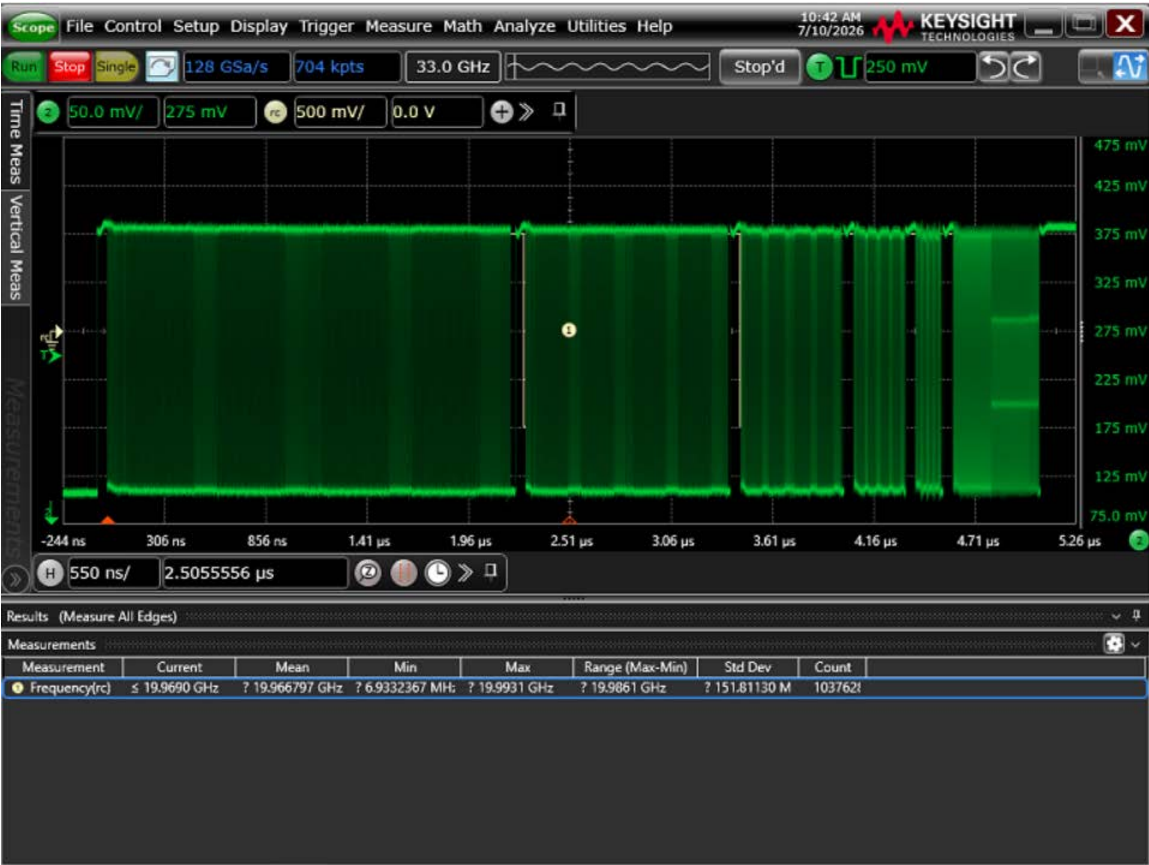


Figure 4-27 Visualization of the multiple-data-rate signal

Main Parts of the GUI

The N5992MM6E Receiver Debug Tool GUI has the following main parts:

- **Connection Window:** The first window that opens is the connection window, which is used to configure the connection setup. See [Connecting to the Instruments](#) on page 51.
- **Signal Window:** The signal window is used to configure the signal. It is described more fully in [Signal Settings](#) on page 54.
- **Message Log:** When the N5992MM6E app is open, a message log can be displayed at the bottom of the window. The class (severity) of the message (e.g., Info, Warning, Error) is listed on the left and the message is followed by the date and time on the right. Click the small black triangle in the bottom-left corner of the main window to hide the message log.
- **About Window:** Click ABOUT in the top-right corner of the main window to open a panel giving details of the version of N5992MM6E that is running and the corresponding software license (see [Figure 4-28](#)).

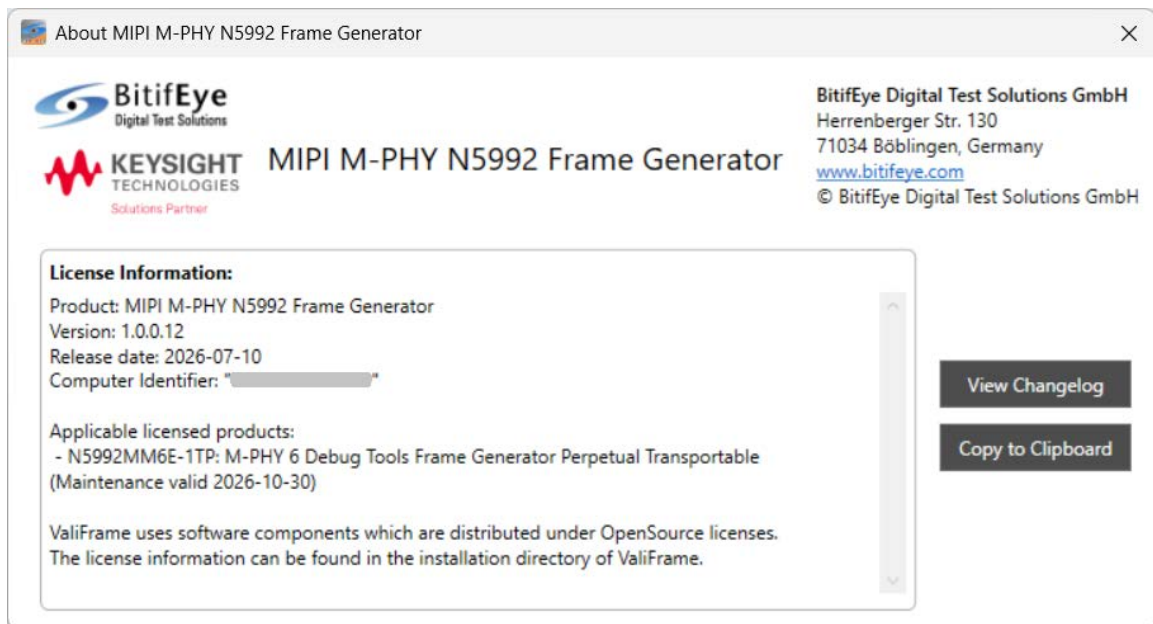


Figure 4-28 Example About window

Connecting to the Instruments

In the first window that opens, the CONNECTION window (Figure 4-29):

- 1 Choose the instrument (BERT) that is going to be used.
- 2 Set the connection setup parameters. For details, see Table 4-1.
- 3 Click **Connect** (lower red frame in Figure 4-29) to finish configuring the setup.

The log will display the message “Connection to instruments successful!” The signal window will open and the SIGNAL button on the task bar will turn blue (Figure 4-30).

NOTE

After connection, all parameters return to their default values.

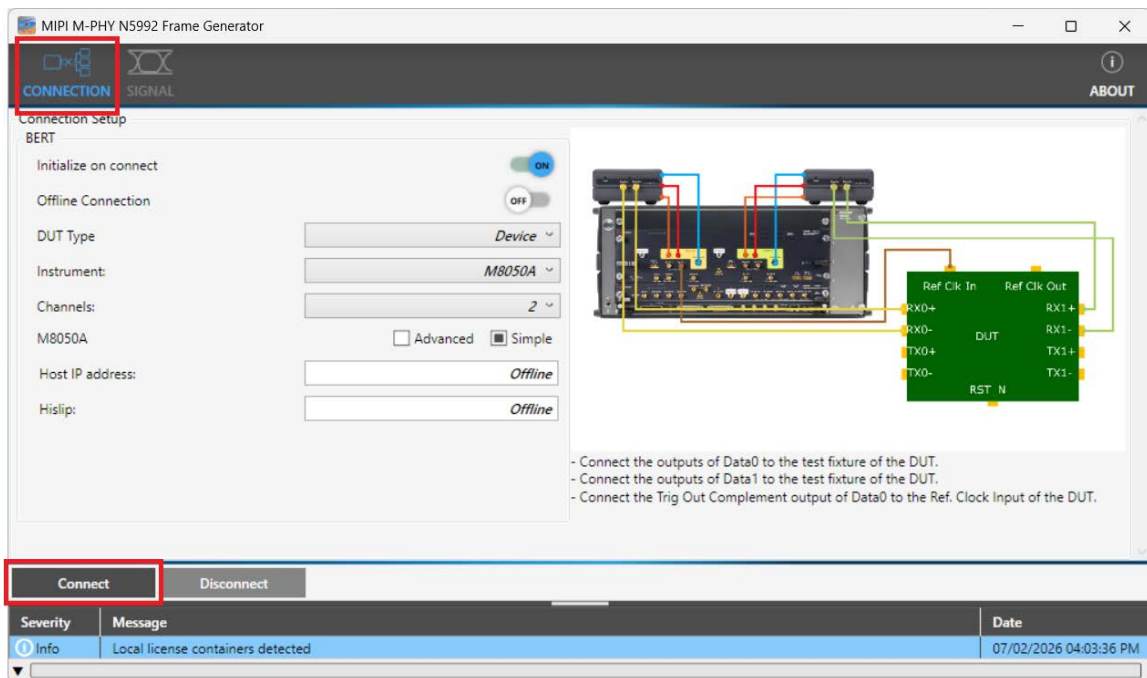


Figure 4-29 Example N5992MM6E Connection window

NOTE

If Offline Connection is set to ON, the N5992MM6E software does not connect to any instrument. This mode can be used for demonstrations or checks only. **No valid data is produced.**

Connection Diagram

The right half of the Connection window shows the connection diagram and connection instructions. The details of the diagram depend on the values selected for the parameters shown in the left half of the Connection window.

Connection Setup Parameters

The connection setup parameters are listed and described in [Table 4-1](#).

Table 4-1 Connection Setup Parameters

Parameter Name	Description
Initialize on Connect	– ON: The instruments will be initialized when you click Connect (see Figure 4-29, lower red frame). – OFF: The instruments will be initialized the first time that you click APPLY.
Offline Connection	– OFF: Use this when you want to take measurements. You can specify the connection of the software to the BERT, that is, how it is addressed. – ON: This is intended for simulation/demonstration purposes only. It does not produce valid data.
DUT Type	Select either Device or Host, depending on the DUT.
Instrument	Select the BERT you are using: M8050A or M8040A.
Channels	Set to '2' to test two receiver channels of the DUT simultaneously. The Connection Diagram will indicate the connections needed. The connections are shown in yellow for Channel 1 and green for Channel 2.
M8050A / M8040A	– Advanced: Type in the TCP/IP address of the BERT in the 'Instrument Address' field. – Simple: Type in the Host IP address and the HiSLIP sub-address.
Instrument Address	TCP/IP address of the BERT. This field is visible when 'Advanced' is selected.
Host IP Address	Host IP address of the BERT. This field is visible when 'Simple' is selected.
Hislip	HiSLIP sub-address of the BERT. This field is visible when 'Simple' is selected.

Disconnecting from the Instruments

When you want to change the configuration after running some tests, proceed as follows:

- 1** Click the **CONNECTION** button (at the top). This returns you to the connection window.
- 2** Click **Disconnect** (at the bottom).

The message “Disconnection from instruments successful!” should appear in the log.

Signal Settings

General Description

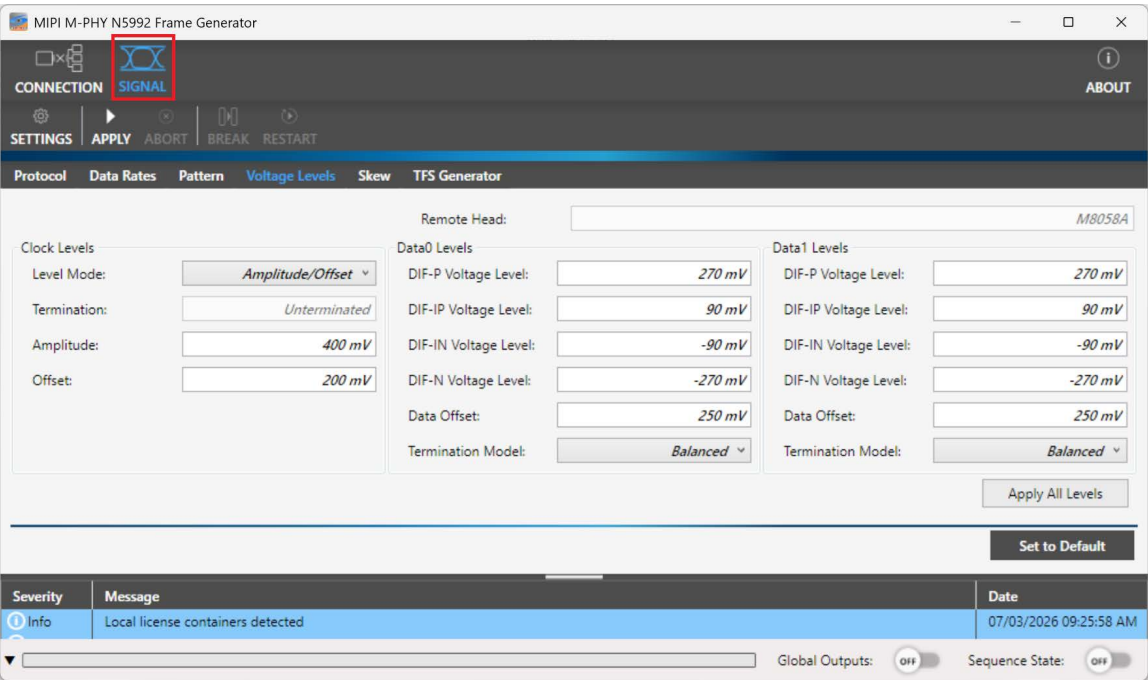


Figure 4-30 SIGNAL window, showing the Voltage Levels tab

The icons in the Signal window toolbar (just above the tabs in [Figure 4-30](#)) are mainly concerned with how the program runs, whereas each tab allows you to configure a particular part of the setup, either with respect to the instruments that are connected to the software or with respect to the MIPI M-PHY 6 standard. Finally, beside the progression bar at the bottom of the window, there are two switches: Global Outputs and Sequence State.

The toolbar, tabs, and switches are considered in more detail below.

Toolbar

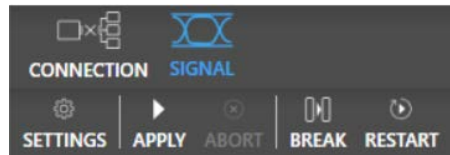


Figure 4-31 Toolbar in the Signal window

SETTINGS

Click SETTINGS to save, load, or reset particular settings. For example, if you have configured the setup for a particular task or DUT, you can save this configuration for future use. Similarly, if you have already saved a particular configuration, you can load it to use it again, thus saving time. It is also possible to reset the configuration to the default values.

APPLY

Once the configuration is completed, that is, all the required values have been configured in the tabs, click APPLY to apply all the tabs one after the other to the instruments.

ABORT

ABORT can be used to abort application of the tabs to the instruments if necessary. ABORT is grayed out (disabled) until APPLY has been clicked.

BREAK

The function of BREAK is related to the Pattern tab.

In some patterns, the first block of the generator sequence is

1. Sleep, manual;

This means that the instrument does not step into the link training until manually forced to. This is achieved by clicking BREAK. The instrument moves on to the second block in the generator sequence.

BREAK is grayed out (disabled) until APPLY has been clicked.

RESTART

The function of RESTART is related to the Pattern tab.

If you want to interrupt the sequence and start it again from the beginning, click RESTART. The instrument goes back to the first block in the generator sequence. In many cases this is

1. Sleep, manual;

and link training will not resume until forced to with BREAK.

This icon is grayed out (disabled) until APPLY has been clicked.

Protocol Tab

The Protocol Tab (Figure 4-32) provides access to the M-PHY-specific settings that you can change. The values of the parameters will vary according to the DUT. The parameters are described below.

Protocol	Data Rates	Pattern	Voltage Levels	Skew	TFS Generator
High Speed (NRZ)					
HS Prepare Length:					7
HS Sync Length:					7
Stall Length [UI]:					20
HS Sync Range:					Fine
Initial Adapt Length:					0
Refresh Adapt Length:					0
Initial Adapt Range:					Fine
Refresh Adapt Range:					Fine
Sync Pattern:					D10.5, D26.5
Low Speed (PWM)					
LS Prepare Length:					7
Tail of Burst [UI]:					10
Sleep Length [UI]:					5
High Speed (PAM4)					
HS Prepare Length:					7
HS Sync Length L0_L3:					7
HS Sync Length L0_L1_L2_L3:					7
Align Pattern:					5E993396B6C10CEC
Stall Length [UI (PAM4)]:					128
Initial Adapt Length L0_L1_L2_L3:					0
Refresh Adapt Length L0_L1_L2_L3:					0
Initial Adapt Range L0_L1_L2_L3:					Fine
Refresh Adapt Range L0_L1_L2_L3:					Fine
Other Settings					
Squelch Pulses:					1
Squelch Pulse Width:					20 ns
Squelch Pulse Distance:					500 ns
Word Size - NRZ (bits):					10
Word Size - PAM4 (bits):					16

Set to Default

Figure 4-32 Protocol Tab

High Speed (NRZ) Settings

High Speed (NRZ)	
HS Prepare Length:	7
HS Sync Length:	7
Stall Length [UI]:	20
HS Sync Range:	Fine ▼
Initial Adapt Length:	0
Refresh Adapt Length:	0
Initial Adapt Range:	Fine ▼
Refresh Adapt Range:	Fine ▼
Sync Pattern:	D10.5, D26.5

Figure 4-33 Protocol Tab – High Speed (NRZ) Settings

- **HS Prepare Length:** PREPARE is the initial sub-state before the HS-burst starts and HS Prepare Length defines the number of DIFP (Differential Positive Voltage) states before the bit stream is started.

The actual HS Prepare Length can be calculated with the formulas given in Table 8 “PREPARE, SYNC, and ADAPT Attribute and Dependent Parameter Values” of the *MIPI® Alliance Specification for M-PHY® Version 6.0* document.

- **HS Sync Length:** This defines the number of SYNC pattern symbols before the burst starts. For HS mode, the Prepare Length will be followed by the default SYNC sequence (D10.5, D26.5). In HS burst and PWM burst modes, the SYNC sequence is followed by the payload. The payload starts with MARKER0 (MK0).
- **Stall Length [UI]:** This defines the number of DIFN (Differential Negative Voltage) states after a data burst. This parameter only affects the data output when the sequence file (see [Pattern Tab](#) on page 66) contains a STALL entry in the data block definition.
- **HS Sync Range:** Select either Fine or Coarse for the HS Sync Range.
For Fine, the duration of the HS sync sequence T_{SYNC} is equal to the HS Sync Length: $T_{\text{SYNC}} = \text{SYNC_length}$ in units of SI.

For Coarse, $T_{\text{SYNC}} = \min(2^{\text{SYNC_length}}, 2^{14})$ in units of SI.

For more details see Table 8 “PREPARE, SYNC, and ADAPT Attribute and Dependent Parameter Values” of the *MIPI® Alliance Specification for M-PHY® Version 6.0* document and the text just before that table.

- **Initial Adapt Length:** The ADAPT sub-state is intended to allow the DUT equalizer training to adapt to the channel characteristic when receiving an HS data stream. The ADAPT sequence starts with a MK0 followed by an 8b10b-encoded PRBS9 pattern completed by one b0 bit. The Initial Adapt Length parameter defines the duration of the Initial ADAPT sequence after power-up.

Initial Adapt Length is also used for the Initial Adapt LOL3 pattern of the ADAPT PAM4 sequence.

- **Refresh Adapt Length:** This defines the duration of the refresh ADAPT sequence during link operation.

Refresh Adapt Length is also used for the Refresh Adapt LOL3 pattern of the ADAPT PAM4 sequence.

- **Initial Adapt Range:** Select either Fine or Coarse.

For Fine, the duration of the Initial ADAPT sequence is calculated as $T_{\text{ADAPT}} = 650 * (\text{ADAPT_length} + 1)$ in units of UI.

For Coarse, $T_{\text{ADAPT}} = 650 * 2^{\text{ADAPT_length}}$ in units of UI, where $\text{ADAPT_length} < 18$ UI.

Initial Adapt Range is also used for the Initial Adapt LOL3 pattern of the ADAPT PAM4 sequence.

- **Refresh Adapt Range:** Select either Fine or Coarse.

For Fine, the duration of the Refresh ADAPT sequence is calculated as $T_{\text{ADAPT}} = 650 * (\text{ADAPT_length} + 1)$ in units of UI.

For Coarse, $T_{\text{ADAPT}} = 650 * 2^{\text{ADAPT_length}}$ in units of UI.

Refresh Adapt Range is also used for the Refresh Adapt LOL3 pattern of the ADAPT PAM4 sequence.

- **Sync Pattern:** The pattern that is sent for synchronization. Sync Pattern is editable in the GUI, but only D-code values (10-bit code word, e.g., D10.2) are accepted.

High Speed (PAM4) Settings

High Speed (PAM4)	
HS Prepare Length:	7
HS Sync Length L0_L3:	7
HS Sync Length L0_L1_L2_L3:	7
Align Pattern:	5E993396B6C10CEC
Stall Length [UI (PAM4)]:	128
Initial Adapt Length L0_L1_L2_L3:	0
Refresh Adapt Length L0_L1_L2_L3:	0
Initial Adapt Range L0_L1_L2_L3:	Fine
Refresh Adapt Range L0_L1_L2_L3:	Fine

Figure 4-34 Protocol Tab – High Speed (PAM4) Settings

- **HS Prepare Length:** PREPARE is the initial sub-state before the HS-burst starts, and HS Prepare Length defines the number of DIFP (Differential Positive Voltage) states before the bit stream is started.

The actual HS Prepare Length can be calculated with the formulas given in Table 8 “PREPARE, SYNC, and ADAPT Attribute and Dependent Parameter Values” of the *MIPI® Alliance Specification for M-PHY® Version 6.0* document.
- **HS Sync Length L0_L3:** This defines the number of SYNC pattern symbols before the burst starts.
- **HS Sync Length L0_L1_L2_L3:** This defines the number of SYNC pattern symbols before the burst starts.
- **Align Pattern:** This defines the Align Pattern. The default value is taken from the specification: ALIGN = 0x5E993396B6C10CEC. It is editable in the GUI, but only hex strings are accepted.
- **Stall Length [UI (PAM4)]:** This defines the number of DIFN (Differential Negative Voltage) states after a data burst. This parameter only affects the data output when the sequence file (see **Pattern Tab** on page 66) contains a Stall_PAM4 entry in the data block definition.

- **Initial Adapt Length L0_L1_L2_L3:** The ADAPT sub-state is intended to allow the DUT equalizer training to adapt to the channel characteristic when receiving an HS data stream.
- **Refresh Adapt Length L0_L1_L2_L3:** This defines the duration of the refresh ADAPT sequence during link operation.
- **Initial Adapt Range L0_L1_L2_L3:** Select either Fine or Coarse. The duration of the Initial ADAPT sequence is calculated as given in Table 8 “PREPARE, SYNC, and ADAPT Attribute and Dependent Parameter Values” of the *MIPI® Alliance Specification for M-PHY® Version 6.0* document.
- **Refresh Adapt Range L0_L1_L2_L3:** Select either Fine or Coarse. The duration of the Refresh ADAPT sequence is calculated as given in Table 8 “PREPARE, SYNC, and ADAPT Attribute and Dependent Parameter Values” of the *MIPI® Alliance Specification for M-PHY® Version 6.0* document.

Low Speed (PWM) Settings



Low Speed (PWM)

LS Prepare Length:	7
Tail of Burst [UI]:	10
Sleep Length [UI]:	5

Figure 4-35 Protocol Tab – Low Speed (PWM) Settings

- **LS Prepare Length:** This defines the number of DIFP states before the PWM burst starts. The actual PWM Prepare Length can be calculated with the formulas given in Table 8 “PREPARE, SYNC, and ADAPT Attribute and Dependent Parameter Values” of the *MIPI® Alliance Specification for M-PHY® Version 6.0* document.
- **Tail of Burst [UI]:** This is defined as the transmission of a series of either zeros or ones after the last 8b10b symbol of the burst.
- **Sleep Length [UI]:** Sleep is the power-saving state in the LS mode. It will add as many DIFN (0) states as given by the Sleep Length in unit intervals. For a PWM burst, LS Sleep adds all PWM zeros and one PWM one. Example: The LS Sleep of PWM (10) will be nine PWM zeros and one PWM one.

Other Settings

Other Settings	
Squelch Pulses:	1
Squelch Pulse Width:	20 ns
Squelch Pulse Distance:	500 ns
Word Size - NRZ (bits):	10 ▾
Word Size - PAM4 (bits):	16 ▾

Figure 4-36 Protocol Tab – Other Settings

- **Squelch Pulses:** This defines the number of pulses in the squelch data block. This parameter only affects the data output when the sequence file contains a “SQUELCH” entry in the data block definition (see [Pattern Tab](#) on page 66).
- **Squelch Pulse Width:** This is the width of the DIFN pulse in the squelch data block.
- **Squelch Pulse Distance:** This is the distance between DIFN pulses in the squelch data block.
- **Word Size – NRZ (bits):** The Word Size for NRZ can be selected as 8, 10, 16 or 20 bits.
- **Word Size – PAM4 (bits):** The Word Size for PAM4 can be selected as 8 or 16 bits.

Data Rates Tab

Use the Data Rates Tab (see [Figure 4-37](#)) to modify parameters for the Reference Clock, High-Speed Gears, and Low-Speed Data Rate.

The screenshot shows the 'Data Rates' tab selected in the software. The 'High Speed' section includes a list of gears where 'Gear 6-A' is selected, and an 'HS Data Rate Deviation [ppm]' field set to 0. The 'Low Speed' section includes a 'Support PWM' toggle set to ON, a 'PWM Data Rate' field set to 4.4973 MB/s, and a 'PWM Bit Resolution' field set to 4440. The 'BERT Settings' section at the bottom shows 'Ref. Clock Frequency' set to 26 MHz and 'BERT Symbol rate' set to 19.968 GBd. A 'Set to Default' button is located at the bottom right.

Figure 4-37 Data Rates Tab

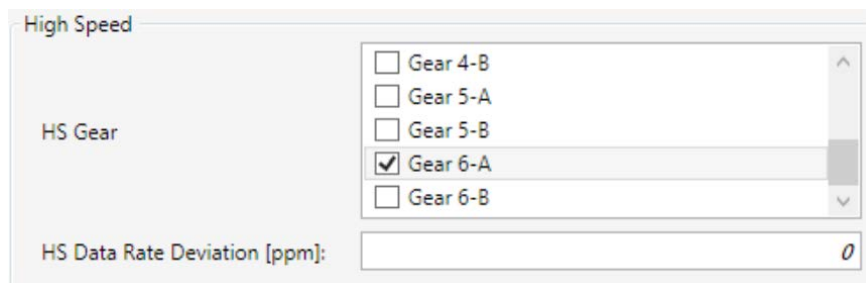
NOTE

For details about the relationship between data rates selected in the Data Rates Tab and those specified in a sequence file, see [Appendix A: Data Rate Validation](#).

NOTE

For details of which M-PHY HS Gears and combinations thereof are available for a particular Base Reference Clock and BERT Baud rate, refer to Table 1 and Table 2 of the *N5992MM6E Data Sheet*, which can be found on the [N5992MM6E product page](#).

High Speed Settings



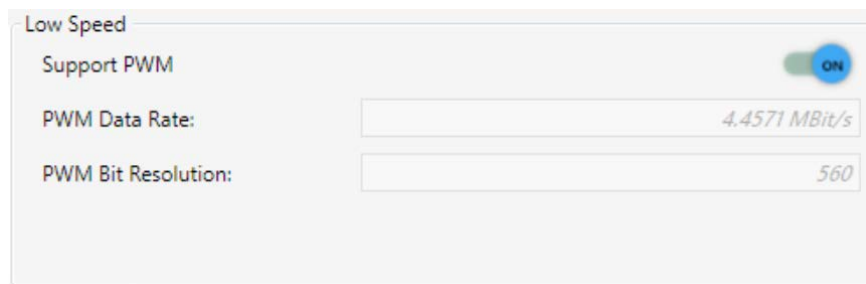
The screenshot shows a 'High Speed' settings window. On the left, there is a label 'HS Gear'. To the right is a list box containing five items: 'Gear 4-B', 'Gear 5-A', 'Gear 5-B', 'Gear 6-A' (which is selected with a checkmark), and 'Gear 6-B'. Below the list box is a text field labeled 'HS Data Rate Deviation [ppm]:' with the value '0'.

Figure 4-38 Data Rates Tab – High Speed Settings

- **HS Gear:** You can select multiple HS Gears (Gear 1-A and 1-B to Gear 6-A and 6-B). A minimum of one HS Gear must be selected, and the maximum number of HS Gears is limited by the BERT baud rate.
- **HS Data Rate Deviation [ppm]:** The deviation of the HS Data Rate from the nominal value. Min: -5000 ppm; Default: 0; Max: +5000 ppm.

If the DUT Type is Host, it is not possible to set the HS Data Rate Deviation.

Low Speed Settings



The screenshot shows a 'Low Speed' settings window. At the top, there is a toggle switch for 'Support PWM' which is turned ON. Below this are two text fields: 'PWM Data Rate:' with the value '4.4571 MBit/s' and 'PWM Bit Resolution:' with the value '560'.

Figure 4-39 Data Rates Tab – Low Speed Settings

- **Support PWM:** Enable this option to accept a PWM block in a sequence. When Support PWM is enabled, the maximum supported BERT Symbol Rate will be limited to HS Gear 5-B (around 24 GBaud).

- **PWM Data Rate:** This is read-only, and visible only if PWM is enabled.
- **PWM Bit Resolution:** This is read-only, and visible only if PWM is enabled.

BERT Settings



The screenshot shows a software interface titled "BERT Settings". It contains two rows of settings, each with a label on the left and a value in a box on the right. The first row is labeled "Ref. Clock Frequency:" and shows a value of "26 MHz" with a small downward arrow indicating a drop-down menu. The second row is labeled "BERT Symbol rate:" and shows a value of "19.968 GBd" with a similar drop-down arrow.

Setting	Value
Ref. Clock Frequency:	26 MHz
BERT Symbol rate:	19.968 GBd

Figure 4-40 Data Rates Tab – BERT Settings

- **Ref. Clock Frequency:** Select the reference clock frequency from the drop-down menu.
- **BERT Symbol Rate:** Select the rate from the drop-down menu.

Pattern Tab

The Pattern tab makes it possible to load different sequence files, which define the data that is going to be uploaded to the instruments.

NOTE

For details about the validation and processing of data rates within a sequence file, see [Appendix A: Data Rate Validation](#).

Use the small icon marked 1 in [Figure 4-41](#) to load a sequence file (extension .seq). The default location of the sequence files is C:\ProgramData\BitifEye\ValiFrameK2\MPhyG6\Pattern. Each file defines one sequence, which is built up of one or more blocks.

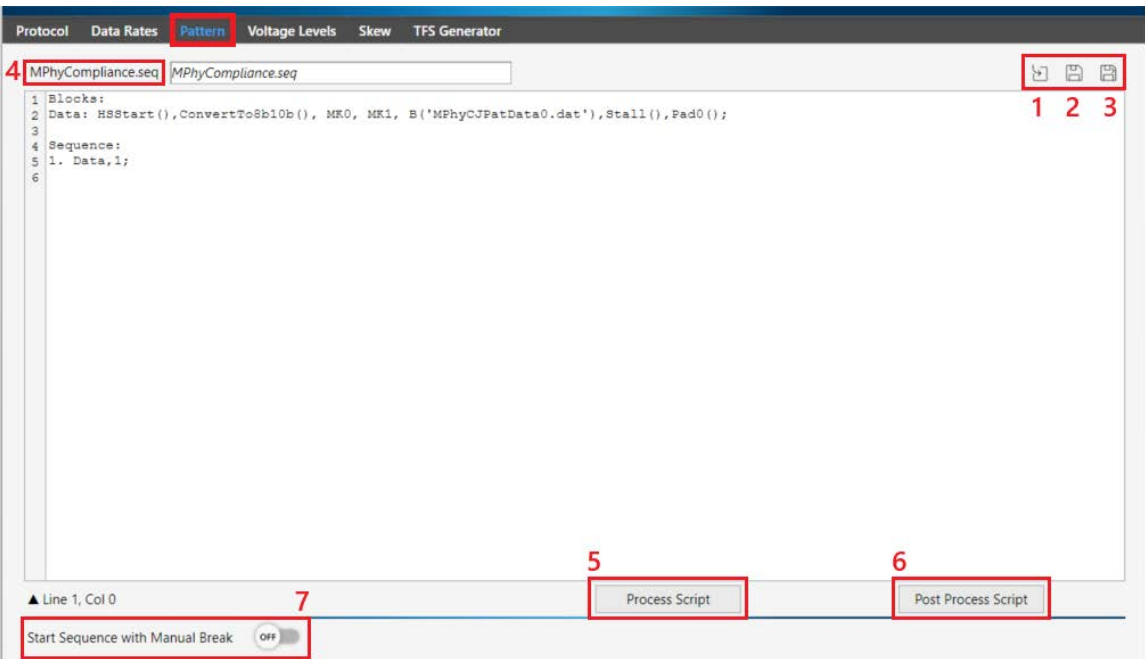


Figure 4-41 Pattern Tab

The large text field (script editor field) in the Pattern Tab contains the script corresponding to the selected sequence, once it has been loaded. The file name of the sequence is displayed in Frame 4. You can edit this script and save the edited sequence using icons 2 and 3, which have the functions Save and Save As, respectively. The default location of the script file is C:\ProgramData\BitifEye\ValiFrameK2\MPhyG6\Pattern. Every time the sequence is changed, for example by loading a new sequence, the edited script is overwritten.

If a sequence calls a file and the path is not specified, the default location where the macro processor searches will be the same directory as the location of the sequence file.

You can edit the training sequences and patterns using a unified syntax. For details of this language, refer to the [N5992MM6E Language Guide](#).

If you mark data and right-click in the script editor field, a list of possible conversions will pop up (see [Figure 4-42](#)). This is a handy conversion tool if you want to convert numbers between different numbering systems. “Binary to Hex” and “Hex to Binary” are just generally useful. In M-PHY the numbering system is 8b/10b; the remaining entries in the tool allow you to convert numbers between this and other systems instantly, in both directions.



Figure 4-42 Pattern Tab – Pop-up list of conversions

In the script editor window, the data blocks are described in terms of macros, which are described in the [N5992MM6E Language Guide](#). Clicking the **Process Script** button (labeled 5 in [Figure 4-41](#)) opens an additional pane (see [Figure 4-43](#)), in which the blocks are listed in terms of commands and data instead of macros.

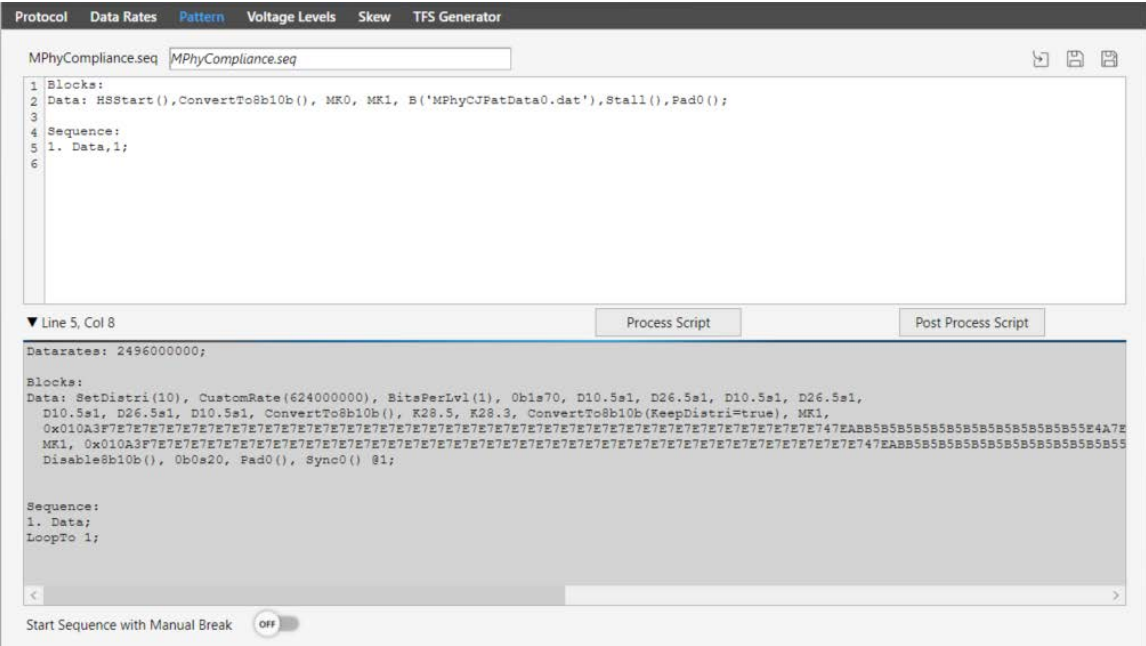


Figure 4-43 Pattern Tab – Process Script pane

If you mark part of the content of the Process Script or Post Process Script field and then right-click, a menu pops up that you can use to cut, copy or paste the marked part of the script.

Clicking the **Post Process Script** button (labeled 6 in [Figure 4-41](#)) opens another pane (see [Figure 4-44](#)), in which the blocks are listed as data; you can see exactly what the data that will be sent to the instruments looks like (in hexadecimal notation).

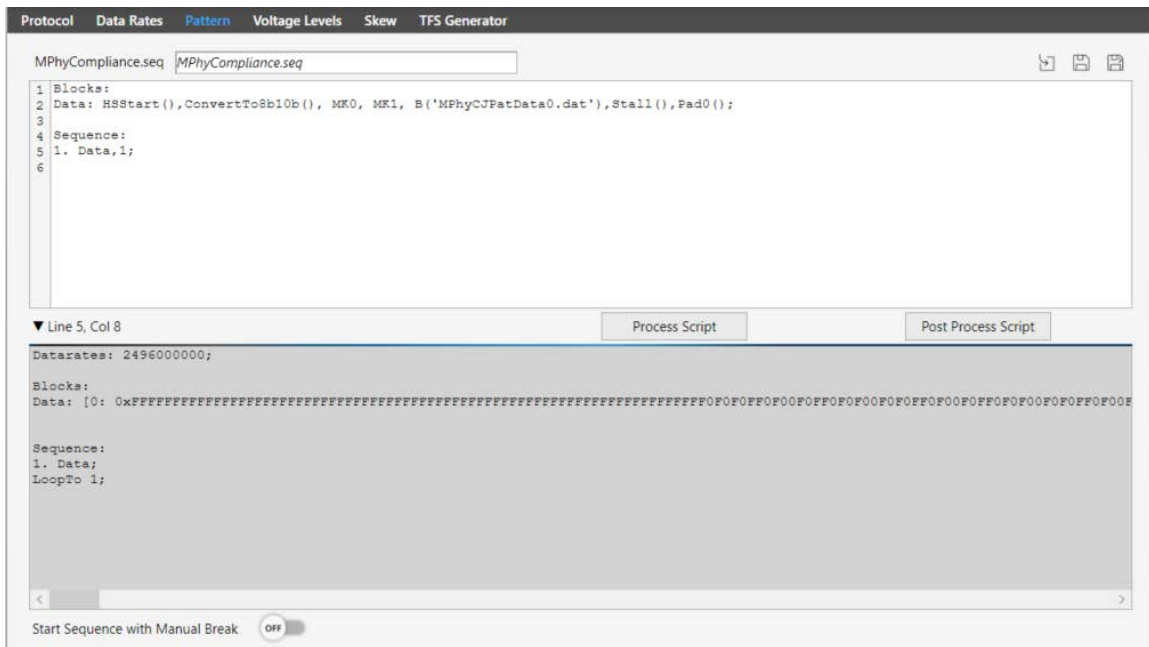


Figure 4-44 Pattern Tab – Post Process Script pane

If **Start Sequence with Manual Break** is enabled (labeled 7 in [Figure 4-41](#)), the first block of the generator sequence is

0. PAUSE_BERT, manual;

where PAUSE_BERT is a single block of PadIdlePam4, which will create an empty squelch block in the sequence. This means that the instrument does not step into the link training until manually forced to. This is achieved by clicking **BREAK**. Then the instrument moves on to the next block in the generator sequence.

Voltage Levels Tab

The reference clock and data channel levels can be modified in the Voltage Levels Tab. The levels can be set for each data channel individually and also for the reference clock.

When you make changes in the Voltage Levels Tab, there is an option to apply only the changes of the voltage levels made in this tab. Click 'Apply All Levels'.

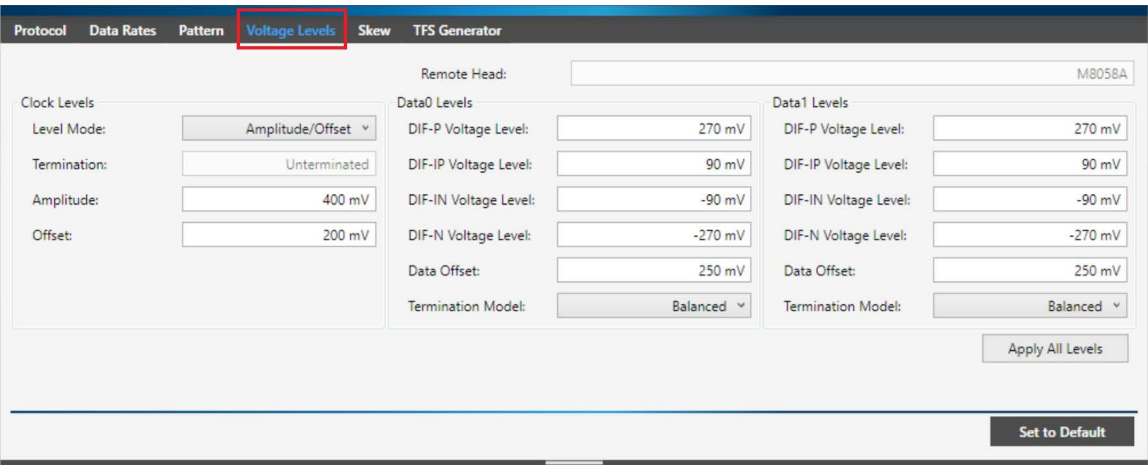


Figure 4-45 Voltage Levels Tab

Remote Head

The model number of the Remote Head is displayed (read-only) in the top right corner. The maximum amplitude that can be set will depend on the limitations of the connected Remote Head.

The set PAM4 levels are limited by the BERT, since the PAM4 levels have a maximum resolution of 1% for the M8040A and 0.1% for the M8050A. Therefore, the set values in the GUI are updated based on the actual set values with these limitations.

Clock Level Settings

Figure 4-46 Clock level settings – Amplitude/Offset

- **Level Mode:** Select whether the levels should be set in terms of High Level/ Low Level or Amplitude/Offset.
- **Termination:** This is set as Unterminated for the clock channel.
- **Amplitude, Offset or High Level, Low Level:** Enter the required values. See [Table 4-2](#) for allowed values.

Table 4-2 Clock Settings – Ranges of Levels

Level	Minimum	Maximum	Default
Amplitude	200 mV	2 V	400 mV
High Level	Low Level + 200 mV	Low Level + 2 V	
Low Level	High Level – 2 V	High Level – 200 mV	
Offset			200 mV

Data0/Data1 Levels

If two channels are selected during connection configuration, there are separate sections for Data0 Levels and Data1 Levels. The options are exactly the same in each case.

Data0 Levels	
DIF-P Voltage Level:	270 mV
DIF-IP Voltage Level:	90 mV
DIF-IN Voltage Level:	-90 mV
DIF-N Voltage Level:	-270 mV
Data Offset:	250 mV
Termination Model:	Balanced ▼

Figure 4-47 Data level settings

- **DIF-P Voltage level:** Voltage level of the highest PAM4 level (L3).
 - **DIF-IP Voltage level:** Voltage level of the second-highest PAM4 level (L2).
 - **DIF-IN Voltage level:** Voltage level of the second-lowest PAM4 level (L1).
 - **DIF-N Voltage level:** Voltage level of the lowest PAM4 level (L0).
 - **Data offset:** Offset of the data levels.
 - **Termination Model:** Select Balanced (into 100 Ω) or Unbalanced (into 50 Ω).
- Click **Apply All Levels** to apply the configured level values.

PAM4 to NRZ Conversion in the Data Levels Section

The PAM4 line coding is always enabled, but when a block that is not an HS-G6 block, i.e., not a PAM4 gear, the values set in the Data Levels section define the NRZ levels.

To obtain the NRZ levels, the Data Offset, DIF-P, and DIF-N voltages are used in the following way:

- $\text{NRZ Amplitude (Single-Ended)} = (\text{DIF-P} - \text{DIF-N}) / 2$
- $\text{NRZ Offset} = (\text{DIF-P} + \text{DIF-N}) / 2 + \text{Data Offset}$

Example

If we have the following PAM4 values:

- DIF-P: 300 mV
- DIF-N: 100 mV
- Data Offset: 250 mV

the corresponding NRZ values are:

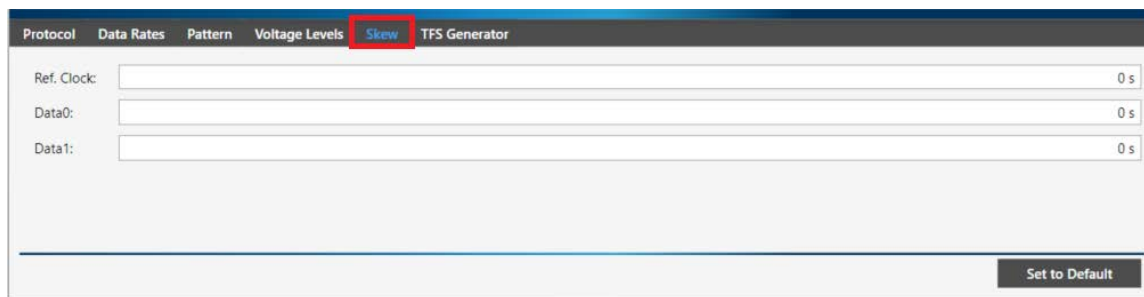
- NRZ Amplitude = $(300 - 100) / 2 = 100$ mV
- NRZ Offset = $(300 + 100) / 2 + 250 = 450$ mV

Skew Tab

In the Skew Tab (see [Figure 4-48](#)), you can set the skew values for the reference clock and for the data channels.

Min: -50 ns; Default: 0; Max: +50 ns

Changes that you make in the Skew Tab are applied immediately. You do not have to click APPLY.



The screenshot shows the 'Skew' tab selected in a software interface. The tab bar at the top includes 'Protocol', 'Data Rates', 'Pattern', 'Voltage Levels', 'Skew' (highlighted with a red box), and 'TFS Generator'. Below the tab bar, there are three input fields: 'Ref. Clock:', 'Data0:', and 'Data1:'. Each field has a text input area and a unit selector set to '0 s'. At the bottom right of the tab, there is a 'Set to Default' button.

Figure 4-48 Skew Tab

TFS Generator Tab

In the TFS Generator Tab (see [Figure 4-49](#)), you can set parameters that govern the mapping to TFS data blocks, as introduced in *MIPI Alliance Specification for Unified Protocol (MIPI UniPro®) Version 3.0, Section 5.5.4 Transport Framing Structure (TFS)*, and various generator options.

The screenshot shows the 'TFS Generator' tab in a software application. The interface is divided into two main sections: 'Mapping to TFS Data Blocks' on the left and 'Generator Options' on the right.

Mapping to TFS Data Blocks:

- Block 0 to Block 7: Each block has a text input field and a small button to its right.
- Output Raw Data File: A text input field containing 'TFSRawData_0Block.txt'.
- HS Burst Output Sequence: A text input field containing 'TFSBurst.seq'.

Generator Options:

- Input Data Unit: A dropdown menu set to 'PA_SDU'.
- Output TFS frame: A dropdown menu set to 'DL Frame'.
- Finish TFS Frame with EoB: A toggle switch set to 'OFF'.
- Number of Loops: A text input field set to '1'.
- Scramble TFS Frame: A toggle switch set to 'ON'.
- Gray-Code TFS Frame: A toggle switch set to 'ON'.
- Pre-Code TFS Frame: A toggle switch set to 'ON'.
- Add CRC Errors: A text input field set to '0'.
- Add FEC Error: A toggle switch set to 'OFF'.

A 'Generate' button is located at the bottom right of the 'Generator Options' section.

Figure 4-49 TFS Generator Tab

Mapping to TFS Data Blocks

Figure 4-50 TFS Generator Tab – Mapping to TFS Data Blocks

The software requires data blocks to be filled in order, beginning with Block 0 and then proceeding to Blocks 1, 2, and so forth. Leaving empty blocks between populated blocks is not supported and will produce unexpected results.

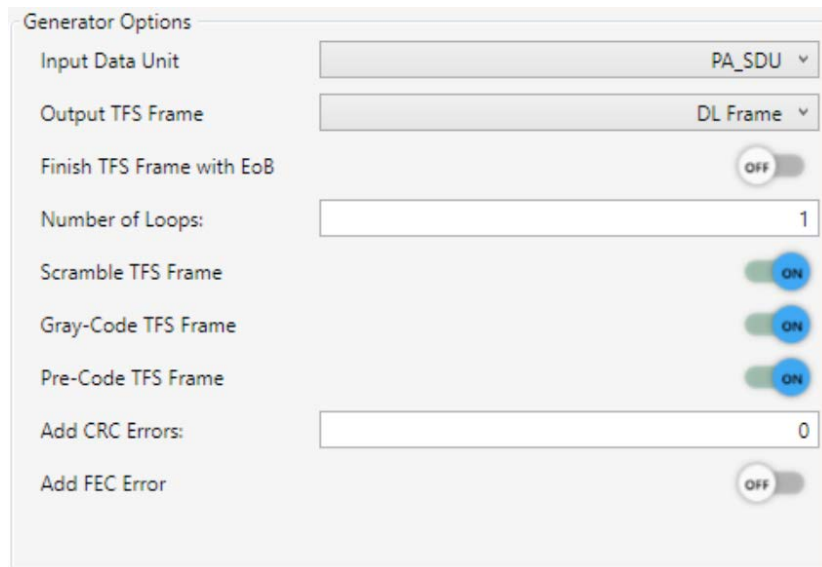
Packing of symbols into TFS frames is performed in accordance with Section 5.5.4.5 of the *UniPro v3.0* specification. During this process, the data intended for a given block may exceed the available capacity of that TFS block. In such cases, the input symbols that cannot be accommodated in Block *N* are carried over and become the first inputs symbols of Block *N*+1. The packing algorithm then continues processing Block *N*+1 using the updated input.

Whenever a carry-over occurs, the software records the event in the log. This mechanism is applied consistently to all subsequent blocks until the packing process is complete. If the input data cannot fit into a normal TFS frame, the software reports an error indicating that the TFS block capacity has been exceeded and no TFS frame is created.

- **Block *N*:** *N* = 0, 1, ..., 7. Data is accepted as 8 PA_SDU or PA_PDU symbols that fulfill the following conditions:

- the size of each block is a multiple of a PA_SDU symbol, i.e., a multiple of 17 bits, or of a PA_PDU symbol, i.e., a multiple of 16 bits
- **Output Raw Data File:** The default file name is *TFSRawData_OBlocks.txt*. If you select *N* block input, the file name will change to *TFSRawData_NBlocks.txt*.
- **HS Burst Output Sequence:** The path and name of the HS Burst Output Sequence. Default file name: *TFSBurst.seq*.

Generator Options



The screenshot shows a 'Generator Options' dialog box with the following settings:

- Input Data Unit:** PA_SDU (selected from a dropdown)
- Output TFS Frame:** DL Frame (selected from a dropdown)
- Finish TFS Frame with EoB:** OFF (toggle switch)
- Number of Loops:** 1 (text input)
- Scramble TFS Frame:** ON (toggle switch)
- Gray-Code TFS Frame:** ON (toggle switch)
- Pre-Code TFS Frame:** ON (toggle switch)
- Add CRC Errors:** 0 (text input)
- Add FEC Error:** OFF (toggle switch)

Figure 4-51 TFS Generator Tab – Generator Options

- **Input Data Unit:** Select either PA_SDU or PA_PDU.
- **Output TFS Frame:** Select either PACP frame or DL. PA_SDUs/PA_PDUs belonging to PACP frames and PA_SDUs/PA_PDUs belonging to DL frames are not allowed in the same TFS frame. A maximum of one PACP frame is allowed in a single TFS frame.
- **Finish TFS Frame with EoB:** If you select this option, TFS End-of-Block (EOB) control symbols will be added to finish the frame if the input data is not sufficient to fill a whole TFS frame. The EOB symbols are added after the last packed TFS symbol.

If you do not select this option, the TFS frame is finished instead with TFS FILLER control symbols.

- **Number of Loops:** The number of times it is required to loop the full TFS frame (256 bytes after CRC and FEC calculations). Maximum: 10 000.
- **Scramble TFS Frame:** Toggle ON to apply scrambling to the data.
- **Gray-Code TFS Frame:** Toggle ON to apply gray coding to the data.
- **Pre-Code TFS Frame:** Toggle ON to apply pre-coding to the data.
- **Add CRC Errors:** Specify 1, 2, or 3. If you specify 1 or 2, the frame generator will invalidate 1 or 2 bytes of data after FEC encoding. This means that, depending on your selection, 1 or 2 bytes of data will have a different output. If you select 3, one CRC byte will be made invalid.
- **Add FEC Error:** If you toggle this ON, more than 3 bytes will be made invalid after FEC encoding. Therefore, a random number of bytes, between 3 and 256, will be modified to a random byte value.

Generate Button

Click the **Generate** button to do the following:

- 1 Create the raw TFS frame, which is a text file with 241 bytes in hexadecimal format. The frame is created following the rules laid out in Section 5.5.4.5 of the *UniPro v3.0* specification.

To respect ESC_DL symbol's proximity rules, FILLERs will be added to the TFS data blocks while packing.

To finish the frame, either FILLERs or EoB control symbols will be added, depending on whether Finish TFS Frame with EoB is selected.

- 2 Generate *TFSBurst.seq*: This sequence is a PAM4 Burst that includes the Output Raw Data File.

Example Sequence**Blocks:**

```
Data: HSStart_PAM4(),TFS('TFSRawData_NBlocks.txt', 1, true, true,
true, 0, false),Stall_PAM4(),Pad0();
```

Sequence:

```
Data,1;
```

The generation takes into account all of the Generator Options set in the TFS tab.

The default locations of the output files are:

- Raw Data File: *C:\ProgramData\BitifEye\ValiFrameK2\MPhyG6\Pattern\TFSRawData_NBlock.txt*
- Burst Sequence: *C:\ProgramData\BitifEye\ValiFrameK2\MPhyG6\Pattern\TFSBurst.seq*

Switches

Global Outputs Switch

Once all the parameters have been set, click **APPLY** (in the toolbar) to apply the parameter values to the instrument. Then the Global Outputs switch toggles ON and the progress bar to the left will turn green, orange or red, depending on whether any problems have been encountered. A description of any problem found will appear in the log window.

Sequence State Switch

If you toggle the Sequence State switch ON, another parameter field opens on the right that shows the current state of the setup. For example, if the first block of the sequence is “1. Sleep”, the Sequence State might show “1. Sleep”, so you know which block of the sequence has been reached.

The Sequence State switch toggles ON automatically when you click APPLY in the toolbar.

5 Troubleshooting and Support

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Troubleshooting

The message log pane at the bottom of the main window displays error messages that should help you discover what has gone wrong. They are explained in the following section. Further details of the run will be saved in the [Log File](#).

Error Messages

Table 5-1 Error Messages, Issues, and Actions

Error Message	Cause of Issue	What To Do
Connection to BERT system at <IP-address> failed! Please verify instrument address and HiSLIP.	Connection to the BERT failed.	Check that the correct instrument is selected in the Connection Setup pane (CONNECTION window), the instrument is correctly set up, and the address is correctly inserted in the Connection Setup pane.
Could not set the Termination Model <TerminationModelType> on <ChannelId>. Please check the setup.	The BERT driver was not able to set the Termination Model configured in the Voltage Levels Tab.	Check that the Termination Model is correctly set for the desired application.
<ChannelId> was turned off when turning on global outputs. Check setup and BERT.	The channel output was turned off when the global output was enabled.	Check that the Termination Model is correctly set for the desired application.
CRC and FEC errors cannot be added simultaneously.	When using TFS, it is not allowed to add CRC errors and FEC errors at the same time.	Choose either CRC errors or FEC errors (not both).
Cannot save Data Rates settings. The selected combination of <invalid fields>, does not allow any valid BERT Symbol rate with the current instrument settings. Please select a valid combination of HS Gears, PWM and Reference Clock Frequency that generates at least one valid BERT Symbol rate.	The selected HS gears, reference clock, and PWM settings do not produce any valid BERT symbol rate.	Adjust the HS gears, reference clock, or PWM settings until at least one valid BERT symbol rate is available. Refer to Table 1 and Table 2 of the N5992MM6E Data Sheet on the N5992MM6E product page .
The Macro Processor expects the Raw TFS file to be composed of hexadecimal and/or binary symbols only.	The raw TFS input contains non-hex/ binary data or an invalid hex pair.	Fix the source file so it contains only valid raw hexadecimal/binary data.

Table 5-1 Error Messages, Issues, and Actions (cont.)

Error Message	Cause of Issue	What To Do
Unexpected size of the input raw TFS. It must contain only full blocks + a BTF byte.	The TFS data length is not one of the accepted block lengths, or the full-frame conversion does not receive the expected 241-byte raw payload.	Make sure that the input contains full blocks plus the BTF byte, and that the raw payload is the expected size, before creating the full frame.
It is not permitted to change TFS encoding parameters between TFS frames in the same burst. Changed parameters: <ifferences>.	Scramble, gray code, or pre-code settings were changed in the middle of a burst.	Keep the TFS encoding settings constant for the whole burst.
There is no selected HS Gear.	A block does not define a data rate, and no selected HS gear is available as fallback.	Select at least one HS gear before generating the sequence.
Error in M-Phy Macro Processor: Argument <ArgumentName> must be ...	An M-PHY macro was called with an argument with a non-supported value. To avoid incorrect results and/or to comply with the specification, the macro processor limits the values of some arguments.	Check the log message to see which argument is incorrectly set and adjust accordingly.
Error in Script Processor: Macro <MacroName> invoked with invalid arguments.	A macro was called using an argument of unsupported type or with an incorrect number of arguments.	Check the macro's signature in the N5992MM6E Language Guide to confirm which arguments the macro supports.
8b10b-exclusive macro <MacroName> cannot be invoked in PAM4 HS Gear ... OR PAM4-exclusive macro <MacroName> cannot be invoked in NRZ HS Gears ... OR Block contains 8b10b symbol <SymbolName> cannot be used in PAM4 HS Gear ...	To not mix encodings in the same block, G1-G5 blocks do not output 1b1b-encoded patterns, and G6 blocks do not output 8b10b-encoded patterns.	Check in the N5992MM6E Language Guide whether the macro is supported in the desired Gear/Encoding and adjust accordingly.
Not able to detect an external clock source with Host setup selected. Please check the setup.	No external clock source could be detected when in Host mode.	Check the external clock cabling, source, and host setup before applying the settings again.

Table 5-1 Error Messages, Issues, and Actions (cont.)

Error Message	Cause of Issue	What To Do
Was not able to detect a valid reference clock frequency in Host Configuration. Detected frequency: <RefClkFreq>.	In the Host setup, the external clock source is set to a reference clock frequency outside of the supported values of 19.2, 26, 52, 76.8, or 104 MHz.	Set the output of the external clock source to one of the supported frequencies.
Pattern Generator is not supported.	The connected hardware configuration does not match the supported M8040/ M8050 channel setup, or the pattern generator is not supported.	Verify the installed channel modules and use a supported generator configuration.
The instrument is not jumping to the first block of the sequence!	The instrument did not reach the first sequence block within the allowed wait time.	Check the instrument state and the sequence start condition; then try again.

Log File

The log file can be viewed by right-clicking within the log list section and selecting Show Log File (see lower red frame in [Figure 5-1](#)). The log file is temporarily saved at C:\ProgramData\BitifEye\ValiFrameK2\Tmp. Note that all log information will be lost when the N5992MM6E application is terminated unless you save the log file.

Support

If the information in the **Troubleshooting** section cannot help you solve the issue you are facing, proceed as follows:

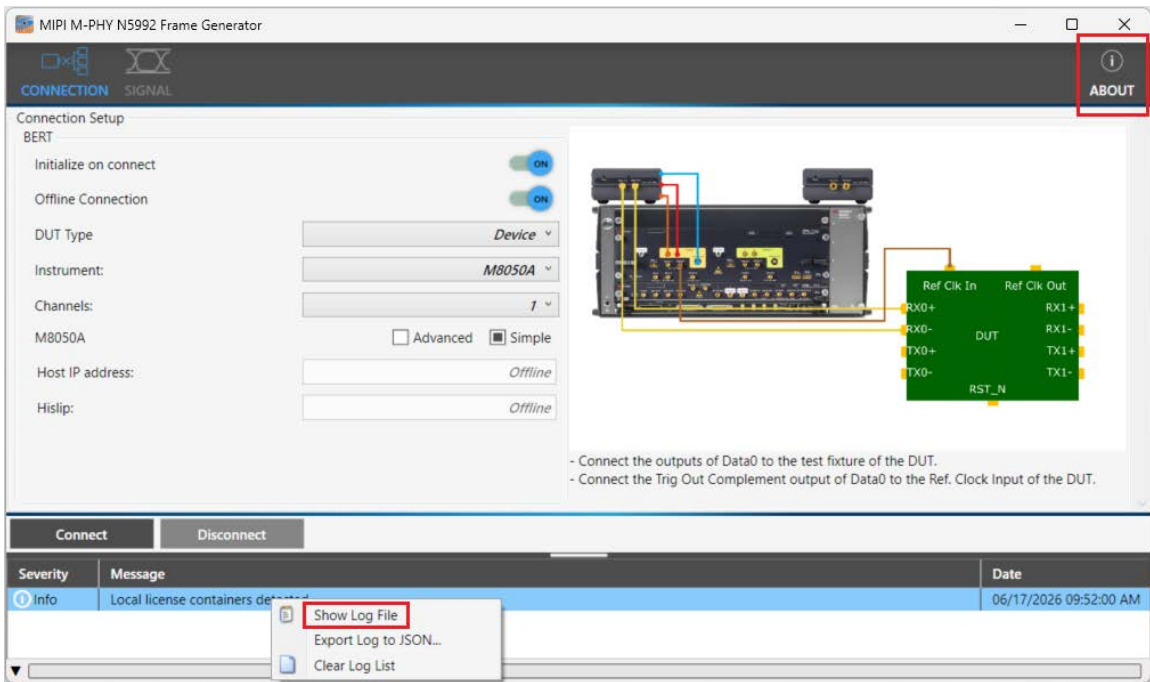


Figure 5-1 Accessing the log file

- 1 Save the log file.
 - a Right-click on the log list section of the main window.
 - b Select **Show Log File** (Figure 5-1).
 - c Save the log file.
- 2 Click the **ABOUT** button in the main window (Figure 5-1).
- 3 Click the **Copy to Clipboard** button in the About window (Figure 5-2).
- 4 Send this copied information and the log file to your Keysight support contact.

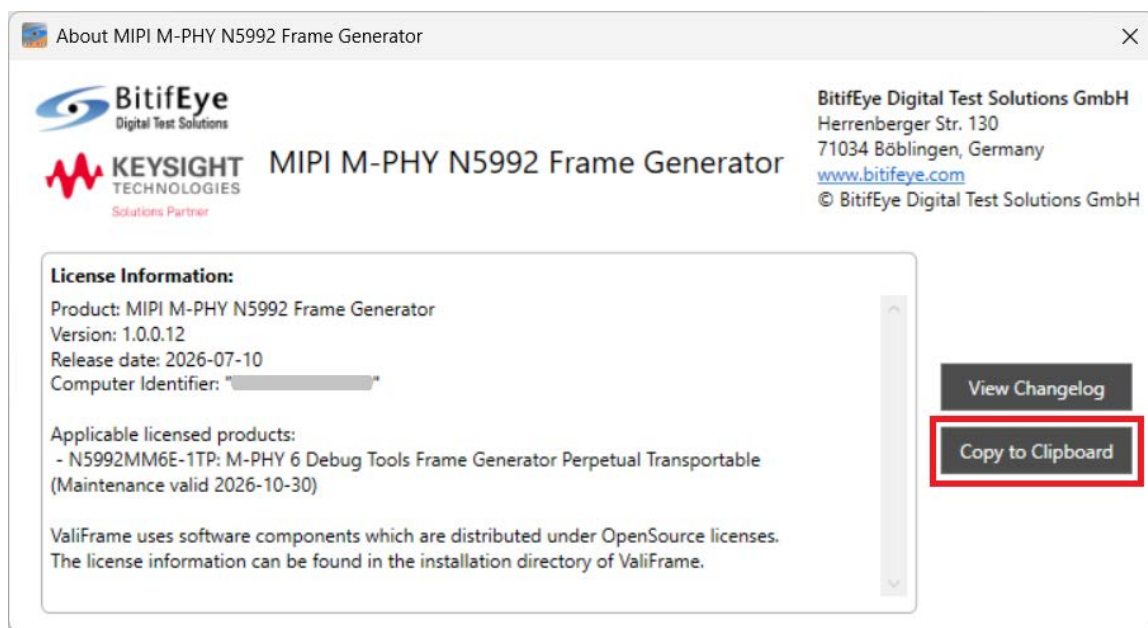


Figure 5-2 About window

The Keysight support team is also happy to help you should you require further information about a particular application.

For support options, visit www.keysight.com/find/contactus.

A Data Rate Validation

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This appendix describes how data rates are validated and processed within a sequence.

Overview

Data rates can appear in a sequence and also be set in the Data Rates Tab. This means that it is necessary to ensure that all data rate references in the sequence are consistent with the configuration defined in the Data Rates Tab.

Data Rate Validation Rule

All HS Gears referenced in the sequence must be selected in the Data Rates Tab selection.

Supported Scenarios

Data rate tokens have the format @HSG<number><series>

Examples

@HSG1A, @HSG6B

Only the following tokens are allowed in the sequence:

@HSG1A, @HSG1B,

@HSG2A, @HSG2B,

@HSG3A, @HSG3B,

@HSG4A, @HSG4B,

@HSG5A, @HSG5B,

@HSG6A, @HSG6B

Block Without an @HSG<number><series> Token

A block without an HS data rate token is acceptable only if you select just one HS gear in the Data Rates Tab.

If a block does not contain an @HSG<number><series> token

- and only one HS Gear is selected in the Data Rates Tab:
this block will be accepted
- and multiple HS Gears are selected in the Data Rates Tab:
this will lead to an error or unexpected result

Example

Data: `HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0();`

If you select only one HS Gear in the Data Rates Tab, this block will be accepted.

If you select multiple HS Gears in the Data Rates Tab, for example, Gear 1-A and Gear 1-B, this block will not be accepted.

NOTE

See also **PWM Blocks** on page 90.

Block with an @HSG<number><series> Token

If the block contains an @HSG<number><series> token, there are three possibilities:

- Both <number> and <series> match with the HS Gears selected in the Data Rates Tab
The block will be accepted.
- Token format is invalid
This will lead to an error.
- <number> or <series> (or both) does not match with the HS Gears selected in the Data Rates Tab
This will lead to an error.

Example

Selecting Gear 1-A and Gear 1-B as HS Gears in the Data Rates Tab will lead to the following results: Both

```
Data: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0()
@HSG1A;
```

and

```
Data: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0()
@HSG1B;
```

will be accepted, whereas

```
Data: HSStart(), Deskew(), B('MPhyCJPatData0.dat'), Stall(), Pad0()
@HSG3B;
```

will not be accepted because the token @HSG3B would require Gear 3B to be selected in the Data Rates Tab.

PWM Blocks

A *PWM block* is a block that contains MIPI M-PHY PWM macros and does not contain any macros applicable only to HS-NRZ and HS-PAM4 gears. See Table 2-1 in the [N5992MM6E Language Guide](#).

A PWM block should not have a token. If you select multiple HS Gears in the Data Rates Tab, a PWM block must be accompanied by at least one properly identified HS gear block.

Example

```
DataPwM: LSStart(), Deskew(), LB('MPhyCJPatData0.dat'), LSStall(),  
Pad0();
```

This block does not contain an HS data rate token, and it does not contain any macros applicable only to HS-NRZ and HS-PAM4 gears. Therefore, it will be accepted, provided only one HS Gear is selected in the Data Rates Tab. If the user has selected more than one HS gear in the Data Rates tab, a second block that contains the relevant HS data rate tokens will be required.

Sequence Consistency Check

The system verifies that all HS Gears referenced in the sequence are included in the Data Rates Tab.

- If all of the HS Gears mentioned in the Pattern are selected in the Data Rates Tab, the sequence is accepted.
- If any HS Gear is missing in the Data Rates tab, an error will be logged.

B Acronyms and Abbreviations

List of Acronyms 94

This Appendix contains a list of acronyms and abbreviations used in this User Guide.

List of Acronyms

Acronym	Definition
B	
BERT	Bit Error Ratio Tester
BLM	BitifEye License Manager
BTF	Block Type Flag
C	
CJTPAT	Compliant Jitter Tolerance Pattern
CRC	Cyclic Redundancy Check
CRPAT	Compliant Random Pattern
D	
DIFN	Voltage level of the lowest PAM4 level (L0)
DIF-IN	Voltage level of the second-lowest PAM4 level (L1)
DIF-IP	Voltage level of the second-highest PAM4 level (L2)
DIFP	Voltage level of the highest PAM4 level (L3)
DL	Data Link
DUT	Device Under Test
E	
EOB	End of Burst
ESC_DL	Data Link Layer Control Symbol Identifier
F	
FEC	Forward Error Correction
G	
GUI	Graphical User Interface
H	
HiSLIP	High-Speed LAN Instrument Protocol
HS	High Speed

Acronym	Definition
I	
IO	Input-Output, Interface
IP	Internet Protocol
L	
LAN	Local Area Network
LS	Low Speed
M	
MK0	Marker Zero
P	
PA	PHY Adapter layer
PACP	PHY Adapter Control Protocol
PC	Personal Computer
PDU	Protocol Data Unit
PWM	Pulse-Width Modulation
R	
RX, Rx	Receiver
S	
SDU	Service Data Unit
SI	Symbol Interval
T	
T_{ADAPT}	Duration of ADAPT Sequence
TCP	Transmission Control Protocol
TFS	Transport Frame Structure
T_{SYNC}	Duration of HS SYNC Sequence
TX, Tx	Transmitter
U	
UI	Unit Interval

Acronym	Definition
UniPro	Unified Protocol
V	
VISA	Virtual Instrument System Architecture
V _{term}	Terminated Voltage

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without notice.

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