# D9370GDDC GDDR7
# Compliance Test Application

KEYSIGHT

METHODS OF IMPLEMENTATION

# Notices



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**CAUTION**

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# 1 Overview

## GDDR7 Automated Testing—At a Glance

The Keysight D9370GDDC GDDR7 Compliance Test Application helps you verify that the GDDR7 transmitter device under test (DUT) is compliant to the pre-defined limits using the Keysight Infiniium Oscilloscopes. The Keysight D9370GDDC GDDR7 Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope, spectrum analyzer and vector network analyzer connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

**NOTE**

**The tests performed by the Keysight D9370GDDC GDDR7 Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.**

## Required Equipment and Software

In order to run the GDDR7 automated tests, you need the following equipment and software:

### Hardware

- Use one of the following Oscilloscope models. Refer to www.keysight.com for the respective bandwidth ranges.
  - Keysight UXR Oscilloscopes
- Target Device Under Test (DUT)
- N2803A 30 GHz RCRC probe amplifier(x 4)
- N5445A 30 GHz browser(x4)
- N2787A 3D probe positioner(x4)
- Keyboard, qty = 1, (provided with the Keysight Infiniium Oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium Oscilloscope)
- Keysight also recommends using a second monitor to view the test application.

### Software

- The minimum version of Infiniium Oscilloscope Software (see the Keysight D9370GDDC GDDR7 Compliance Test Application Release Notes)
- Keysight D9370GDDC GDDR7 Compliance Test Application software
- InfiniiScan Event Identification Software

### Licensing information

Refer to the *Data Sheet* pertaining to GDDR7 Test Application to know about the licenses you must install along with other optional licenses. Visit "http://www.keysight.com/find/D9370GDDC" and in the web page's **Document Library** tab, you may view the associated Data Sheet.

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

The licensing format for Keysight License Manager 6 differs from its predecessors. See "Installing the License Key" on page 17 to see the difference in installing a license key using either of the applications on your machine.

**NOTE** **To launch the GDDR7 Compliance Test Application, you must have the D9370GDDC GDDR7 Test Application software and InfiniiScan Event Identification Software licenses installed.**

#### Additional Licenses

1 InfiniiSim feature requires the following licenses:
   - InfiniiSim Basic or InfiniiSim Advanced

## A Brief on GDDR7 GRAM Testing

GDDR7 SGRAMs support a vendor defined mapping of logical DQ[9:0] signals to physical package pins. The ball-out as shown in Figure 1 uses the term DQp[9:0]_[A:D] with letter “p” referring to the physical locations of the 10 DQ pins per channel. The correspondence between these pin locations and the logical DQ[9:0] signals will be found in a vendor specific mapping table (TABLE 154). It is pointed out that the location of the 10 DQ and their mapping to logical signals is the same for the 4 channels, which preserves the symmetry across the channels.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VSS | VSS | DQp1_A | VSS | DQE_A | VSS | DQp0_A | A | DQp0_B | VSS | DQE_B | VSS | DQp1_B | VSS | VSS |
| DQp2 A | VSS | VSS | VDDQ | VSS | VDD | VSS | B | VSS | VDD | VSS | VDDQ | VSS | VSS | DQp2 B |
| VSS | VSS | DQp3_A | VSS | DQp4_A | VSS | DQp5_A | C | DQp5_B | VSS | DQp4_B | VSS | DQp3_B | VSS | VSS |
| RCK c A | VDDQ | VSS | VDDQ | VSS | VDDQ | VSS | D | VSS | VDDQ | VSS | VDDQ | VSS | VDDQ | RCK c B |
| RCK t A | VSS | DQp7_A | VSS | DQp6_A | VSS | WCK c A | E | WCK c B | VSS | DQp6_B | VSS | DQp7_B | VSS | RCK t B |
| VSS | VDDQ | VSS | VDDQ | VSS | VSS | WCK t A | F | WCK t B | VSS | VSS | VDDQ | VSS | VDDQ | VSS |
| DQp8 A | VSS | DQp9 A | VSS | ERR A | VDDQ | VSS | G | VSS | VDDQ | ERR B | VSS | DQp9 B | VSS | DQp8 B |
| VSS | VSS | VSS | VDD | VSS | VDD | CA0_A | H | CA0_B | VDD | VSS | VDD | VSS | VSS | VSS |
| VPP | CA4_A | VDD | CA3_A | CA2_A | VDD | CA1_A | J | CA1_B | VDD | CA2_B | CA3_B | VDD | CA4_B | VPP |
| ZQ AB | RESET n | VSS | VSS | VDD | VSS | VSS | K | VSS | VSS | VDD | VSS | VSS | VSS | ZQ CD |
| VPP | CA4 D | VDD | CA3 D | CA2 D | VDD | CA1 D | L | CA1 C | VDD | CA2 C | CA3 C | VDD | CA4 C | VPP |
| VSS | VSS | VSS | VDD | VSS | VDD | CA0_D | M | CA0_C | VDD | VSS | VDD | VSS | VSS | VSS |
| DQp8_D | VSS | DQp9_D | VSS | ERR_D | VDDQ | VSS | N | VSS | VDDQ | ERR_C | VSS | DQp9_C | VSS | DQp8_C |
| VSS | VDDQ | VSS | VDDQ | VSS | VSS | WCK_t_D | P | WCK_t_C | VSS | VSS | VDDQ | VSS | VDDQ | VSS |
| RCK t_D | VSS | DQp7_D | VSS | DQp6_D | VSS | WCK c_D | R | WCK c_C | VSS | DQp6_C | VSS | DQp7_C | VSS | RCK t_C |
| RCK c_D | VDDQ | VSS | VDDQ | VSS | VDDQ | VSS | T | VSS | VDDQ | VSS | VDDQ | VSS | VDDQ | RCK c_C |
| VSS | VSS | DQp3_D | VSS | DQp4_D | VSS | DQp5_D | U | DQp5_C | VSS | DQp4_C | VSS | DQp3_C | VSS | VSS |
| DQp2_D | VSS | VSS | VDDQ | VSS | VDD | VSS | V | VSS | VDD | VSS | VDDQ | VSS | VSS | DQp2_C |
| VSS | VSS | DQp1 D | VSS | DQE D | VSS | DQp0 D | W | DQp0 C | VSS | DQE C | VSS | DQp1 C | VSS | VSS |



Figure 1 GDDR7 SGRAM 266 Ball BGA Ball-out

| PIN | Ball Channel A | Ball Channel B | Ball Channel C | Ball Channel D | Logical Signal |
|---|---|---|---|---|---|
| DQp0 | A7 | A8 | W8 | W7 | DQ9 |
| DQp1 | A3 | A12 | W12 | W3 | DQ8 |
| DQp2 | B1 | B14 | V14 | V1 | DQ7 |
| DQp3 | C3 | C12 | U12 | U3 | DQ6 |
| DQp4 | C5 | C10 | U10 | U5 | DQ5 |
| DQp5 | C7 | C8 | U8 | U7 | DQ0 |
| DQp6 | E5 | E10 | R10 | R5 | DQ1 |
| DQp7 | E3 | E12 | R12 | R3 | DQ2 |
| DQp8 | G1 | G14 | N14 | N1 | DQ3 |
| DQp9 | G3 | G12 | N12 | N3 | DQ4 |

NOTE 1 The ball coordinates reflect the fixed locations of the DQp[9:0] pins in channels A to D. The mapping to logical signals as in the “Logical Signal” column is customizable as required; the mapping shown in the table is provided as an example and applies to all 4 channels.

**Table 1 Example Logical Signal to Physical Pin Mapping for DQ[9:0]**

## In This Book

This manual describes the tests that are performed by the Keysight D9370GDDC GDDR7 Compliance Test Application in more detail.

- Chapter 2, “Installing the Test Application and Licenses” shows how to install the automated test application software and licenses (if it was purchased separately).
- Chapter 3, “Preparing to Take Measurements” shows how to start the Keysight D9370GDDC GDDR7 Compliance Test Application and gives a brief overview of the required preparation and how the application is used.
- Chapter 4, “AC Timing Tests” describes the methods of implementation for the AC Timing tests.
- Chapter 5, “Input Operating Condition Tests” describes the methods of implementation for the Input Operating Condition tests.
- Chapter 6, “Command Address Input Timings Tests” describes the methods of implementation for Command Address Input Timings tests.
- Chapter 7, “Data Input and Output Timings Tests” describes the methods of implementation for Data Input and Output Timings tests.

### See Also

The Keysight D9370GDDC GDDR7 Compliance Test Application’s Online Help, which describes:

- Starting the GDDR7 Test Application
- Creating or Opening a Test Project
- Setting Up the Test Environment
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
- Configuring Automation in the Test Application
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App

# 2 Installing the Test Application and Licenses



If you purchased the D9370GDDC GDDR7 Test Application separate from your Infiniium oscilloscope, you must install the software and license key.

## Installing the Test Application

1. Make sure you have the minimum version of Infiniium Oscilloscope software (see the D9370GDDC release notes). To ensure that you have the minimum version, select **Help > About Infiniium...** from the main menu.
2. To obtain the GDDR7 Test Application, go to Keysight website: "http://www.keysight.com/find/D9370GDDC".
3. In the web page's **Trials & Licenses** tab, click the **Details and Download** button to view instructions for downloading and installing the application software.

## Installing the License Key

To procure a license, you require the Ethernet Address information that is displayed in the Keysight Software Manager Utility installed on the same machine where you wish to install the license.

### Using Keysight Software Manager Utility

To view and copy the Ethernet Address from Keysight Software Manager Utility:

1. Launch **Keysight Software Manager Utility** on the machine where you wish to run the Test Application and its features.
2. Copy the **Ethernet Address**, which is a set of alphanumeric values (as highlighted in Figure 2) that appears in the **Add License** tab of the application.

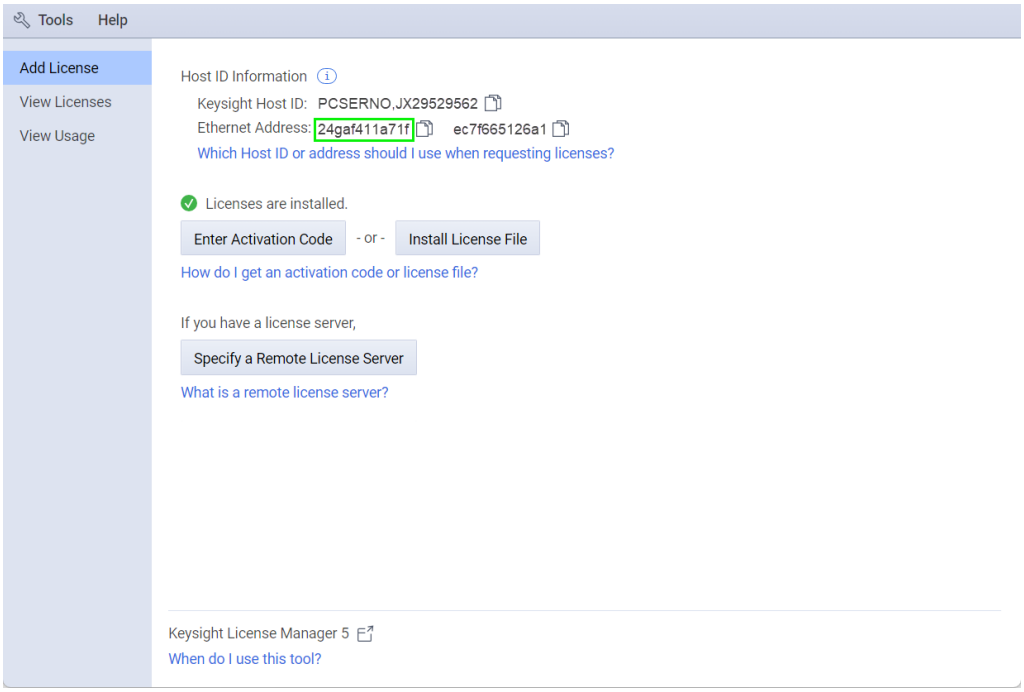


Figure 2 Viewing the Ethernet Address

To install one of the procured licenses using the Keysight Software Manager Utility application:

1 Save the license files on the machine where you wish to run the Test Application and its features.

2 Launch Keysight Software Manager Utility.

3 In the **Add License** tab (Figure 3), use one of the options to install the license file.

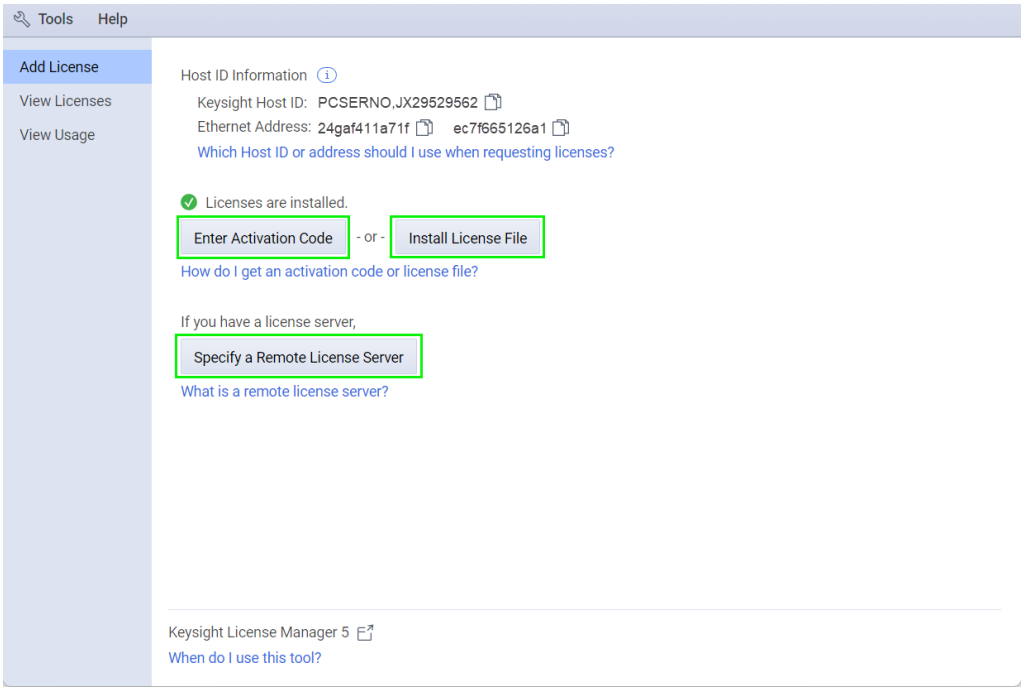


Figure 3 License installation options

For more information regarding installation of procured licenses in Keysight Software Manager Utility, refer to **Supporting Documentation** section on the Keysight Software Manager Utility web page.

# 3 Preparing to Take Measurements



Before running the automated tests, you should calibrate the oscilloscope and probe. After the oscilloscope and probe have been calibrated, you are ready to start the GDDR7 Test Application and perform the measurements.

## Calibrating the Oscilloscope

If you have not already calibrated the oscilloscope, refer to the *User Guide* for the respective Oscilloscope you are using.

**NOTE** If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

**NOTE** If you switch cables between channels or other Oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

## Starting the GDDR7 Test Application

1 Ensure that the GDDR7 Device Under Test (DUT) is operating and set to desired test modes. To start the GDDR7 Test Application: From the Infiniium Oscilloscope's main menu, select **Analyze > Automated Test Apps > D9370GDDC GDDR7 Test App**.

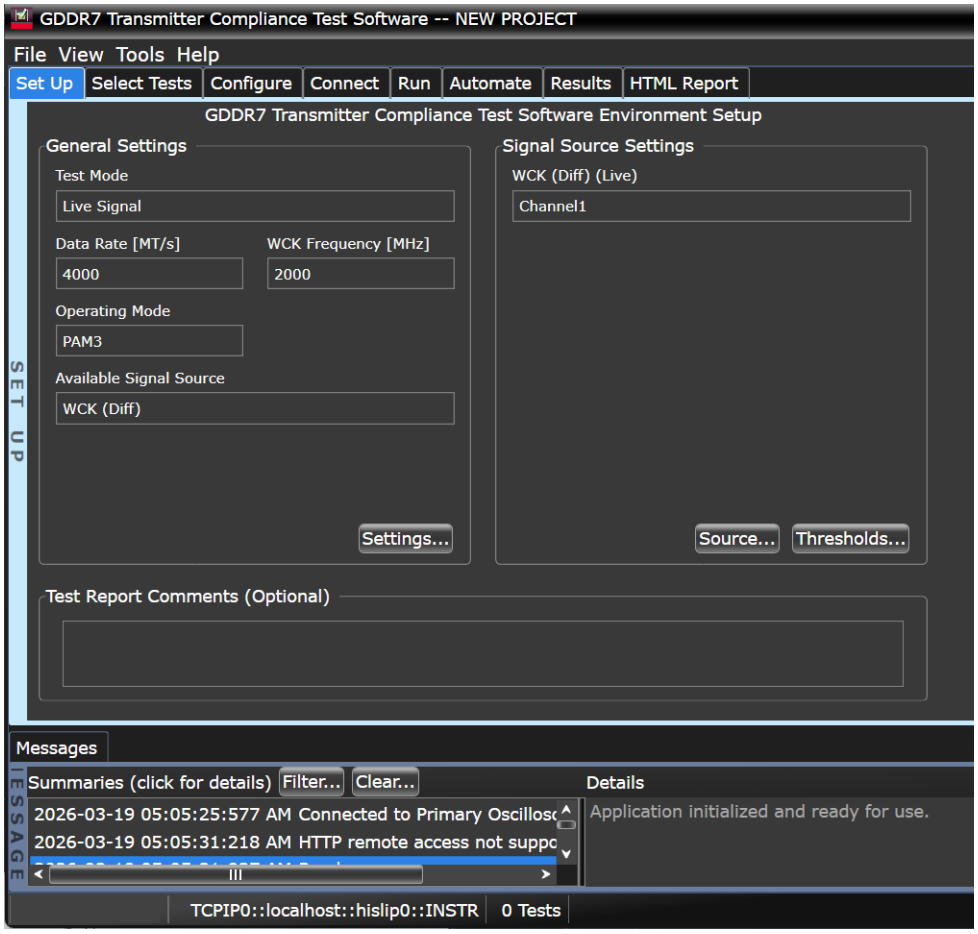


Figure 4 GDDR7 Test Application Main Window

To understand the functionality of the various features in the user interface of the Test Application, refer to the *Keysight D9370GDDC GDDR7 Compliance Test Application Online Help* available in the Help menu.

The task flow pane and the tabs in the main pane show the steps you take in running the automated tests:

| | |
|---|---|
| **Set Up** | Lets you identify and set up the test environment, including information about the device under test. The Test App includes relevant information in the final HTML report. |
| **Select Tests** | Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups. |
| **Configure** | Lets you configure test parameters (for example, channels used in test, voltage levels, etc.). |
| **Connect** | Shows you how to connect the oscilloscope to the device under test for the tests that are to be run. |
| **Run** | Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing. |
| **Automate** | Lets you construct scripts of commands that drive execution of the application. |
| **Results** | Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear. |
| **HTML Report** | Shows a compliance test report that can be printed. |

**NOTE**

In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), where you are running the Test Application.

## Filtering tests in the GDDR7 Test Application

The GDDR7 Test Application filters the list of tests based on the options you select in the **Signal Source** feature.

1 In the **Set Up** tab, click **Settings...**.

2 In the **GDDR7 General Setup** window that appears,

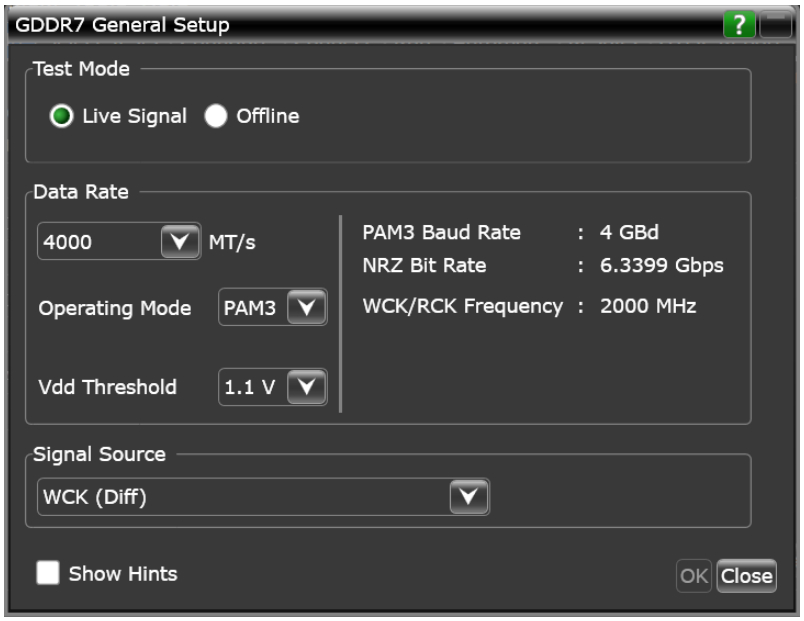


Figure 5 GDDR7 General Setup window

*a* Select a set of signal combinations from the options that appear in the **Signal Source** drop-down field.

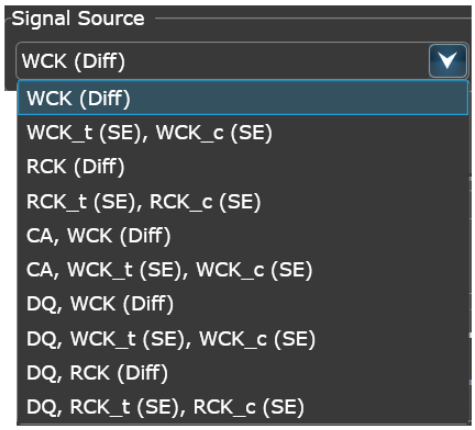


Figure 6 Set of signal combinations in Signal Source drop-down

## Connections for Compliance Tests

To run tests using the GDDR7 Test Application, you must make proper connections between the Oscilloscope and the DUT. Once you select the tests that you want to run, refer to the **Connect** tab in the GDDR7 Test Application for connection instructions and the connection diagram, similar to the one shown in Figure 7.

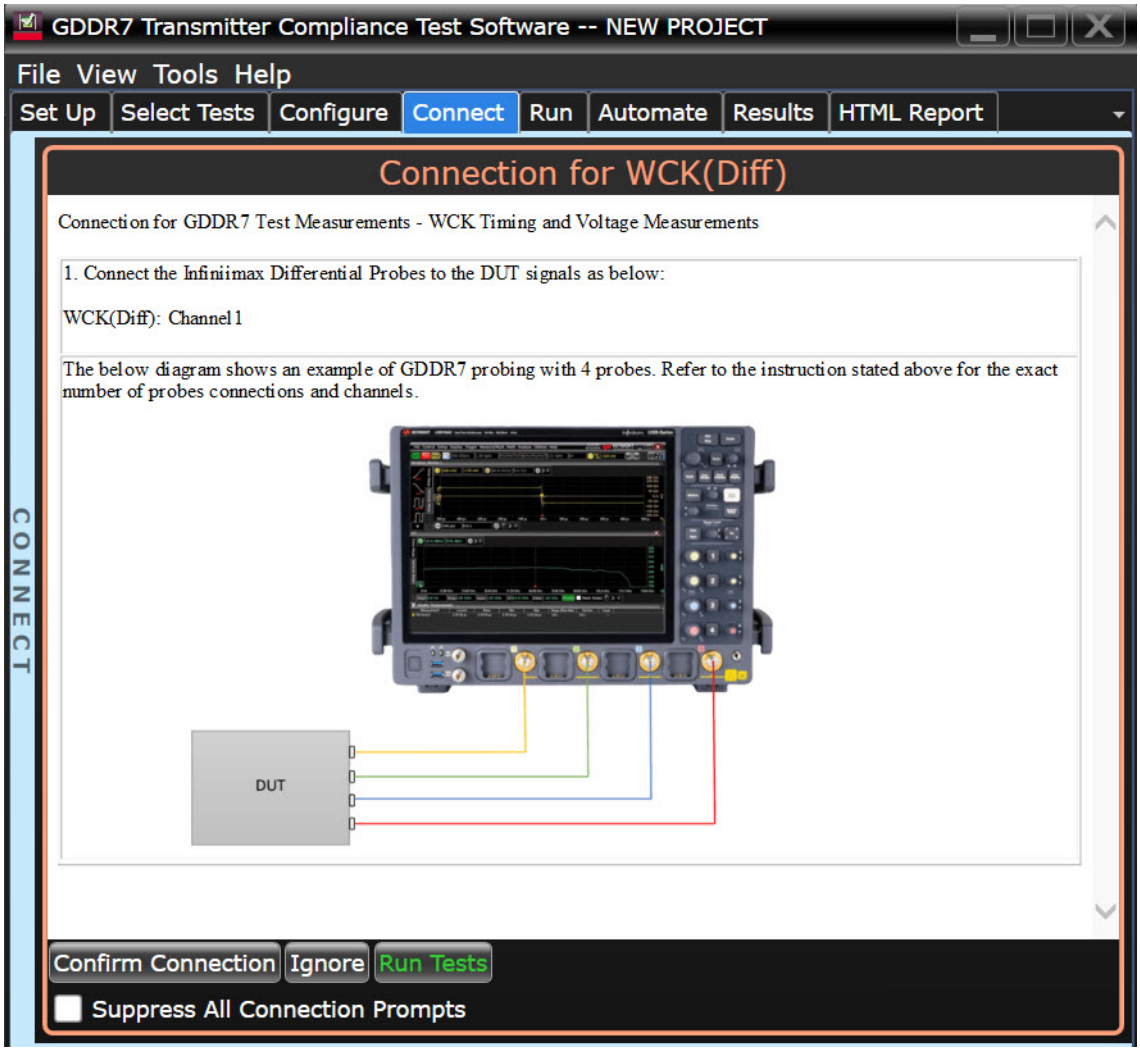


Figure 7 Physical connection diagram and instructions for compliance tests

# 4 AC Timing Tests

# AC Timing Tests

## Test Availability Conditions

All tests in this test group appear for the following configuration in GDDR7 General Setup window:

Signal Source:

- Any signal set including RCK or WCK

**NOTE**

**Following tests support Continuous signal only:**

1. tRCK(abs) High (Information Only)
2. tRCK(abs) Low (Information Only)
3. tRCK(avg) High (Information Only)
4. tRCK(avg) Low (Information Only)
5. tWCK(abs) High (Information Only)
6. tWCK(abs) Low (Information Only)
7. tWCK(avg) High (Information Only)
8. tWCK(avg) Low (Information Only)

## RCK AC Timing Tests

### tRCK - Rising Edge (Information Only)

**Test ID:** 11000

**Test Overview:** The purpose of this test is to measure the RCK clock cycle time from rising edge to rising edge. The RCK clock period is measured from the RCK(Diff) rising edge at 0V middle threshold to the next rising edge at 0V middle threshold. The average value of the period measurements obtained will be reported as final "tRCK - Rising Edge" result.

**Test Procedure:**

1. Trigger on the rising edge of the RCK(Diff) signal. Acquire RCK(Diff) signal.
2. Measure period(rising edge) values for entire RCK(Diff) waveform. The RCK period(rising edge) value is measured from RCK(Diff) rising edge at VREFdiff_RCK middle threshold of a cycle to the next rising edge at VREFdiff_RCK middle threshold.
   *The default "VREFdiff_RCK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].*
3. Find the mean period value of the period measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

**Expected/ Observable Results:** The measured value of "tRCK-Rising Edge" will be reported as informative result.

**References:** JESD239A GDDR7 SGRAM specification

### tRCK - Falling Edge (Information Only)

**Test ID:** 11001

**Test Overview:** The purpose of this test is to measure the RCK clock cycle time from falling edge to falling edge. The RCK clock period is measured from the RCK(Diff) falling edge at 0V middle threshold to the next falling edge at 0V middle threshold. The average value of the period measurements obtained will be reported as final "tRCK - Falling Edge" result.

**Test Procedure:**

1. Trigger on the rising edge of the RCK(Diff) signal. Acquire RCK(Diff) signal.
2. Measure period(falling edge) values for entire RCK(Diff) waveform. The RCK period(falling edge) is measured from RCK(Diff) falling edge at VREFdiff_RCK middle threshold of a cycle to the next falling edge at VREFdiff_RCK middle threshold.
   *The default "VREFdiff_RCK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].*
3. Find the average value of the period measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

**Expected/ Observable Results:** The average value of the period measurements obtained will be reported as final "tRCK - Falling Edge" result.

**References:** JESD239A GDDR7 SGRAM specification

tRCK(abs) High (Information Only)

**Test ID:** 11002

**Test Overview:** The purpose of this test is to measure the RCK clock absolute High Pulse Width.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth
   - set interpolation
2 Prepare display
   - label display with operation
3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
4 Prepare Trigger
   - set Edge Trigger (different between rising and falling)
   - set trigger threshold (based on customer GUI settings)
   - use "Single"
5 Check Signal Requirement
   - verify clock frequency
6 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals and test configurations parameters
      - e.g. wck_t load from optSignalSrc_Live_WCK_t_SE
      - e.g. signal's threshold
2 Use Scope Measurement
   - Set Threshold
   - Set ML Pulse Width measurement
   - Setup measurement trend
3 Able to handle differential and single ended (conversion)
4 Store results with dedicated key within Measurement Collector.

**Expected/ Observable Results:** The average value of the pulse width measurements obtained will be reported as final "tRCK(abs) High Clk Pulse Width" result.

**References:** JESD239A GDDR7 SGRAM specification

tRCK(abs) Low (Information Only)

**Test ID:** 11003

**Test Overview:** The purpose of this test is to measure the RCK clock absolute Low Pulse Width.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth
   - set interpolation
2 Prepare display
   - label display with operation
3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
4 Prepare Trigger
   - set Edge Trigger (different between rising and falling)
   - set trigger threshold (based on customer GUI settings)
   - use "Single"
5 Check Signal Requirement
   - verify clock frequency
6 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals and test configurations parameters
      - e.g. wck_t load from optSignalSrc_Live_WCK_t_SE
      - e.g. signal's threshold
2 Use Scope Measurement
   - Set Threshold
   - Set ML Pulse Width measurement
   - Setup measurement trend
3 Able to handle differential and single ended (conversion)
4 Store results with dedicated key within Measurement Collector.

**Expected/ Observable Results:** The average value of the pulse width measurements obtained will be reported as final "tRCK(abs) Low Clk Pulse Width" result.

**References:** JESD239A GDDR7 SGRAM specification

tRCK(avg) High (Information Only)

**Test ID:** 11004

**Test Overview:** The purpose of this test is to measure the RCK clock average High Pulse Width.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth
   - set interpolation
2 Prepare display
   - label display with operation
3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
4 Prepare Trigger
   - set Edge Trigger (different between rising and falling)
   - set trigger threshold (based on customer GUI settings)
   - use "Single"
5 Check Signal Requirement
   - verify clock frequency
6 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals and test configurations parameters
      - e.g. wck_t load from optSignalSrc_Live_WCK_t_SE
      - e.g. signal's threshold
2 Use Scope Measurement
   - Set Threshold
   - Set ML Pulse Width measurement
   - Setup measurement trend
3 Setup window size (Default 500 according to JESD239A Spec)
4 Able to handle differential and single ended (conversion)
5 Store results with dedicated key within Measurement Collector

**Expected/ Observable Results:** The average value of the pulse width measurements obtained will be reported as final "tRCK(avg) High Clk Pulse Width" result.

**References:** JESD239A GDDR7 SGRAM specification

tRCK(avg) Low (Information Only)

**Test ID:** 11005

**Test Overview:** The purpose of this test is to measure the RCK clock average Low Pulse Width.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth
   - set interpolation
2 Prepare display
   - label display with operation
3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
4 Prepare Trigger
   - set Edge Trigger (different between rising and falling)
   - set trigger threshold (based on customer GUI settings)
   - use "Single"
5 Check Signal Requirement
   - verify clock frequency
6 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals and test configurations parameters
      - e.g. wck_t load from optSignalSrc_Live_WCK_t_SE
      - e.g. signal's threshold
2 Use Scope Measurement
   - Set Threshold
   - Set ML Pulse Width measurement
   - Setup measurement trend
3 Setup window size (Default 500 according to JESD239A Spec)
4 Able to handle differential and single ended (conversion)
5 Store results with dedicated key within Measurement Collector

**Expected/ Observable Results:** The average value of the pulse width measurements obtained will be reported as final "tRCK(avg) Low Clk Pulse Width" result.

**References:** JESD239A GDDR7 SGRAM specification

## WCK AC Timing Tests

### tWCK - Rising Edge (Information Only)

**Test ID:** 10000

**Test Overview:** The purpose of this test is to measure the WCK clock cycle time from rising edge to rising edge. The WCK clock period is measured from the WCK(Diff) rising edge at 0V middle threshold to the next rising edge at 0V middle threshold. The average value of the period measurements obtained will be reported as final "tWCK - Rising Edge" result.

**Test Procedure:**

1. Trigger on the rising edge of the WCK(Diff) signal. Acquire WCK(Diff) signal.
2. Measure period(rising edge) values for entire WCK(Diff) waveform. The WCK period(rising edge) value is measured from WCK(Diff) rising edge at VREFdiff_WCK middle threshold of a cycle to the next rising edge at VREFdiff_WCK middle threshold.
   *The default "VREFdiff_WCK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].*
3. Find the mean period value of the period measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

**Expected/ Observable Results:** The measured value of "tWCK-Rising Edge" will be reported as informative result.

**References:** JESD239A GDDR7 SGRAM specification

### tWCK - Falling Edge (Information Only)

**Test ID:** 10001

**Test Overview:** The purpose of this test is to measure the WCK clock cycle time from falling edge to falling edge. The WCK clock period is measured from the WCK(Diff) falling edge at 0V middle threshold to the next falling edge at 0V middle threshold. The average value of the period measurements obtained will be reported as final "tWCK - Falling Edge" result.

**Test Procedure:**

1. Trigger on the rising edge of the WCK(Diff) signal. Acquire WCK(Diff) signal.
2. Measure period(falling edge) values for entire WCK(Diff) waveform. The WCK period(falling edge) is measured from WCK(Diff) falling edge at VREFdiff_WCK middle threshold of a cycle to the next falling edge at VREFdiff_WCK middle threshold.
   *The default "VREFdiff_WCK" value is 0V and this value is configurable in Set Up tab [Threshold Setup Window].*
3. Find the average value of the period measurements, which will be recorded as the final test result.
4. Report the final test result as informative result.

**Expected/ Observable Results:** The average value of the period measurements obtained will be reported as final "tWCK - Falling Edge" result.

**References:** JESD239A GDDR7 SGRAM specification

tWCK(abs) High (Information Only)

**Test ID:** 10002

**Test Overview:** The purpose of this test is to measure the WCK clock absolute High Pulse Width.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth
   - set interpolation
2 Prepare display
   - label display with operation
3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
4 Prepare Trigger
   - set Edge Trigger (different between rising and falling)
   - set trigger threshold (based on customer GUI settings)
   - use "Single"
5 Check Signal Requirement
   - verify clock frequency
6 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals and test configurations parameters
      - e.g. wck_t load from optSignalSrc_Live_WCK_t_SE
      - e.g. signal's threshold
2 Use Scope Measurement
   - Set Threshold
   - Set ML Pulse Width measurement
   - Setup measurement trend
3 Able to handle differential and single ended (conversion)
4 Store results with dedicated key within Measurement Collector.

**Expected/ Observable Results:** The average value of the pulse width measurements obtained will be reported as final "tWCK(abs) High Clk Pulse Width" result.

**References:** JESD239A GDDR7 SGRAM specification

tWCK(abs) Low (Information Only)

**Test ID:** 10003

**Test Overview:** The purpose of this test is to measure the WCK clock absolute Low Pulse Width.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth
   - set interpolation
2 Prepare display
   - label display with operation
3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
4 Prepare Trigger
   - set Edge Trigger (different between rising and falling)
   - set trigger threshold (based on customer GUI settings)
   - use "Single"
5 Check Signal Requirement
   - verify clock frequency
6 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals and test configurations parameters
      - e.g. wck_t load from optSignalSrc_Live_WCK_t_SE
      - e.g. signal's threshold
2 Use Scope Measurement
   - Set Threshold
   - Set ML Pulse Width measurement
   - Setup measurement trend
3 Able to handle differential and single ended (conversion)
4 Store results with dedicated key within Measurement Collector.

**Expected/ Observable Results:** The average value of the pulse width measurements obtained will be reported as final "tWCK(abs) Low Clk Pulse Width" result.

**References:** JESD239A GDDR7 SGRAM specification

tWCK(avg) High (Information Only)

**Test ID:** 10004

**Test Overview:** The purpose of this test is to measure the WCK clock average High Pulse Width.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth
   - set interpolation
2 Prepare display
   - label display with operation
3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
4 Prepare Trigger
   - set Edge Trigger (different between rising and falling)
   - set trigger threshold (based on customer GUI settings)
   - use "Single"
5 Check Signal Requirement
   - verify clock frequency
6 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals and test configurations parameters
      - e.g. wck_t load from optSignalSrc_Live_WCK_t_SE
      - e.g. signal's threshold
2 Use Scope Measurement
   - Set Threshold
   - Set ML Pulse Width measurement
   - Setup measurement trend
3 Setup window size (Default 500 according to JESD239A Spec)
4 Able to handle differential and single ended (conversion)
5 Store results with dedicated key within Measurement Collector

**Expected/ Observable Results:** The average value of the pulse width measurements obtained will be reported as final "tWCK(avg) High Clk Pulse Width" result.

**References:** JESD239A GDDR7 SGRAM specification

tWCK(avg) Low (Information Only)

**Test ID:** 10005

**Test Overview:** The purpose of this test is to measure the WCK clock average Low Pulse Width.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth
   - set interpolation
2 Prepare display
   - label display with operation
3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
4 Prepare Trigger
   - set Edge Trigger (different between rising and falling)
   - set trigger threshold (based on customer GUI settings)
   - use "Single"
5 Check Signal Requirement
   - verify clock frequency
6 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals and test configurations parameters
      - e.g. wck_t load from optSignalSrc_Live_WCK_t_SE
      - e.g. signal's threshold
2 Use Scope Measurement
   - Set Threshold
   - Set ML Pulse Width measurement
   - Setup measurement trend
3 Setup window size (Default 500 according to JESD239A Spec)
4 Able to handle differential and single ended (conversion)
5 Store results with dedicated key within Measurement Collector

**Expected/ Observable Results:** The average value of the pulse width measurements obtained will be reported as final "tWCK(avg) Low Clk Pulse Width" result.

**References:** JESD239A GDDR7 SGRAM specification

# 5 Electrical Tests

# Electrical Tests

## Test Availability Conditions

All tests in this test group appear for the following configuration in GDDR7 General Setup window:

Signal Source:

- Any signal set including RCK or WCK

**NOTE**

**Following tests support Continuous signal only:**

1. VID_RCK
2. VID_WCK
3. VIX_RCK_Ratio
4. VIX_WCK_Ratio

## RCK Electrical Tests

### VID_RCK (Information Only)

**Test ID:** 21001

**Test Overview:** This test is to measure the RCK Differential input voltage.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scopeRCK
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth based on SNDR test specific config variable
   - set interpolation

2 Prepare display
   - label display with operation

3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)

4 Prepare Trigger
   - set Edge Trigger
   - set trigger threshold (based on customer GUI settings)
   - try to use "Single" to capture signal instead of "Digitize"

5 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals and test configurations parameters
      - e.g. rck_t load from optSignalSrc_Live_RCK_t_SE
      - e.g. signal's threshold

2 Use Scope Measurement
   - Set Threshold
   - Locate all edges within the waveform via FindAllEdge
   - Find the pulse from the Edges located
   - Calculate the voltage difference for series of measured pulse.

3 Able to handle differential and single ended (conversion)

4 Store results with dedicated key within Measurement Collector.

**Expected/ Observable Results:** The value of the input voltage measurements obtained will be reported as final "Vid_RCK" result.

**References:** JESD239A GDDR7 SGRAM specification

VIX_RCK_Ratio (Information Only)

**Test ID:** 20000

**Test Overview:** This test is performed to measure the RCK input crosspoint voltage ratio.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth based on SNDR test specific config variable
   - set interpolation

2 Prepare display
   - label display with operation

3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
   - Set Signal as Single Ended (To measure the crosspoint between the signals)

4 Prepare Trigger
   - set Edge Trigger
   - set trigger threshold (based on customer GUI settings)
   - try to use "Single" to capture signal instead of "Digitize"

5 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals (For single-ended Signals)
   - Load test parameters (Thresholds, etc.)

2 Use Scope Measurement
   - Set Threshold
   - Set Crosspoint Measurement in Vertical Measurement
   - Setup measurement trend

3 Store results with dedicated key within Measurement Collector.

**Expected/ Observable Results:** The value of the input voltage ratio measurements obtained will be reported as final "Vix_RCK" result.

**References:** JESD239A GDDR7 SGRAM specification

## WCK Electrical Tests

### VID_WCK (Information Only)

**Test ID:** 21001

**Test Overview:** This test is to measure the WCK Differential input voltage.

**Test Procedure:** Acquisition:

1 Initialize Scope
- preset scope
- turn off all channels
- set sampling rate
- set global bandwidth
- set memory depth based on SNDR test specific config variable
- set interpolation

2 Prepare display
- label display with operation

3 Prepare Signal
- Horizontal scaling (use ML enhanced dynamic range)
- Vertical scaling (use ML enhanced dynamic range)

4 Prepare Trigger
- set Edge Trigger
- set trigger threshold (based on customer GUI settings)
- try to use "Single" to capture signal instead of "Digitize"

5 Prepare Waveform
- save waveform as H5

Measurement:

1 Translate Parameters function
- Load signals and test configurations parameters
  - e.g. wck_t load from optSignalSrc_Live_WCK_t_SE
  - e.g. signal's threshold

2 Use Scope Measurement
- Set Threshold
- Locate all edges within the waveform via FindAllEdge
- Find the pulse from the Edges located
- Calculate the voltage difference for series of measured pulse.

3 Able to handle differential and single ended (conversion)

4 Store results with dedicated key within Measurement Collector.

**Expected/ Observable Results:** The value of the input voltage measurements obtained will be reported as final "Vid_WCK" result.

**References:** JESD239A GDDR7 SGRAM specification

VIX_WCK_Ratio (Information Only)

**Test ID:** 20000

**Test Overview:** This test is performed to measure the WCK input crosspoint voltage ratio.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth based on SNDR test specific config variable
   - set interpolation

2 Prepare display
   - label display with operation

3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
   - Set Signal as Single Ended (To measure the crosspoint between the signals)

4 Prepare Trigger
   - set Edge Trigger
   - set trigger threshold (based on customer GUI settings)
   - try to use "Single" to capture signal instead of "Digitize"

5 Prepare Waveform
   - save waveform as H5

Measurement:

1 Translate Parameters function
   - Load signals (For single-ended Signals)
   - Load test parameters (Thresholds, etc.)

2 Use Scope Measurement
   - Set Threshold
   - Set Crosspoint Measurement in Vertical Measurement
   - Setup measurement trend

3 Store results with dedicated key within Measurement Collector.

**Expected/ Observable Results:** The value of the input voltage ratio measurements obtained will be reported as final "Vix_WCK" result.

**References:** JESD239A GDDR7 SGRAM specification

# 6 Jitter Tests

# Jitter Tests

## Test Availability Conditions

All tests in this test group appear for the following configuration in GDDR7 General Setup window:

Signal Source:

- Any signal set including RCK, WCK, CA, or DQ

**NOTE**

**Following tests support Continuous signal only:**

1. **RCK Jitter**
2. **WCK Jitter**
3. **CA Jitter**
4. **DQ Jitter**

## Clock Jitter Tests

### WCK Jitter (Information Only)

**Test ID:** 30000

**Test Overview:** This test is to measure the Jitter for WCK.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth based on SNDR test specific config variable
   - set interpolation

2 Prepare display
   - label display with operation

3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)

4 Prepare Trigger
   - set Edge Trigger
   - set trigger threshold (based on customer GUI settings)
   - try to use "Single" to capture signal instead of "Digitize"

5 Prepare Waveform
   - save waveform as H5

Measurement:

1 Configure WCK clock recovery as "Constant Frequency" "Semi-Automatic"

2 Configure measurement threshold for WCK (diff).

3 Enable Jitter with the settings below:
   - Measurement: TIE (Phase) [ Reason: for DCD result ]
   - RJ Bandwidth: Narrow (Pink)
   - Display Unit: Unit Interval
   - RJ Method: Spectral Only [ Reason: able to support all required Jitter measurement and faster]
   - Pattern Length: Periodic (Auto)
   - BER Level: based on Config Tab (default: 1E-9)

**Expected/ Observable Results:** The value of the jitter measurements obtained will be reported as the final result.

**References:** JESD239A GDDR7 SGRAM specification

## Command/Address Jitter Tests

### CA Jitter (Information Only)

**Test ID:** 33000

**Test Overview:** This test is to measure the Jitter for CA.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth based on SNDR test specific config variable
   - set interpolation

2 Prepare display
   - label display with operation

3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)

4 Prepare Trigger
   - set Edge Trigger
   - set trigger threshold (based on customer GUI settings)
   - try to use "Single" to capture signal instead of "Digitize"

5 Prepare Waveform
   - save waveform as H5

Measurement:

1 Configure WCK clock recovery as "Constant Frequency" "Semi-Automatic"

2 Configure measurement threshold for WCK (diff).

3 Enable Jitter with the settings below:
   - Measurement: TIE (Phase) [ Reason: for DCD result ]
   - RJ Bandwidth: Narrow (Pink)
   - Display Unit: Unit Interval
   - RJ Method: Spectral Only [Reason: able to support all required Jitter measurement and faster]
   - Pattern Length: Periodic (Auto)
   - BER Level: based on Config Tab (default: 1E-9)

**Expected/ Observable Results:** The value of the jitter measurements obtained will be reported as the final result.

**References:** JESD239A GDDR7 SGRAM specification

## Data Jitter Tests

### DQJitter (Information Only)

**Test ID:** 32000

**Test Overview:** This test is to measure the Jitter for DQ.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth based on SNDR test specific config variable
   - set interpolation

2 Prepare display
   - label display with operation

3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)

4 Prepare Trigger
   - set Edge Trigger
   - set trigger threshold (based on customer GUI settings)
   - try to use "Single" to capture signal instead of "Digitize"

5 Prepare Waveform
   - save waveform as H5

Measurement:

1 Configure WCK clock recovery as "Constant Frequency" "Semi-Automatic"

2 Configure measurement threshold for WCK (diff).

3 Enable Jitter with the settings below:
   - Measurement: TIE (Phase) [ Reason: for DCD result ]
   - RJ Bandwidth: Narrow (Pink)
   - Display Unit: Unit Interval
   - RJ Method: Spectral Only [Reason: able to support all required Jitter measurement and faster]
   - Pattern Length: Periodic (Auto)
   - BER Level: based on Config Tab (default: 1E-9)

**Expected/ Observable Results:** The value of the jitter measurements obtained will be reported as the final result.

**References:** JESD239A GDDR7 SGRAM specification

# 7 Eye Diagram Tests

# Eye Diagram Tests

## Test Availability Conditions

All tests in this test group appear for the following configuration in GDDR7 General Setup window:

Signal Source:

- Any signal set including CA or DQ

**NOTE**

**Following tests support Continuous signal only:**

1. **CA Eye Diagram**
2. **DQ Eye Diagram**

## CA Eye Diagram Tests

### CA Eye Diagram (Information Only)

**Test ID:** 41000

**Test Overview:** This test is to measure the eye diagram for Command Address Signal.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth based on SNDR test specific config variable
   - set interpolation

2 Prepare display
   - label display with operation

3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)

4 Prepare Trigger
   - set Edge Trigger
   - set trigger threshold (based on customer GUI settings)
   - try to use "Single" to capture signal instead of "Digitize"

5 Prepare Waveform
   - save waveform as H5

Measurement:

1 Configure clock recovery as "Constant Frequency" "Semi-Automatic"
2 Setup Explicit Clock Recovery with clock source WCK(diff)/ RCK(diff) for DQ channel
3 Configure measurement threshold for WCK (diff).
4 Setup Hysteresis Threshold for DQ Channel
5 Configure CTLE & DFE options and set the Channel measure to Equalized1 channel
6 Turn on Real Time Eye for Equalized1 channel
7 Setup measurement for Eye Height and Eye Width:
   - Obtain the Vertical Eye Center Position
   - Locate the Horizontal Eye Center Position
      - When Eye opening is found:
         - Search for left eye crossing using Histogram.Mode
         - Add 0.5UI from left eye crossing to get "rough" Eye Center Position
   - Rescale Eye to center for better screenshot.
   - Measure the Eye Width and the Eye Height
      - After Eye Width is measured, recalculate left and right eye crossing using Histogram.Mean to get "true" Eye Center Position

**Expected/ Observable Results:** The value of the eye measurements obtained will be reported as the final result.

**References:** JESD239A GDDR7 SGRAM specification

## DQ Eye Diagram Tests

### DQ Eye Diagram (Information Only)

**Test ID:** 40000

**Test Overview:** This test is to measure the eye diagram for PAM3 DQ Signal.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth based on SNDR test specific config variable
   - set interpolation
2 Prepare display
   - label display with operation
3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)
4 Prepare Trigger
   - set Edge Trigger
   - set trigger threshold (based on customer GUI settings)
   - try to use "Single" to capture signal instead of "Digitize"
5 Prepare Waveform
   - save waveform as H5

Measurement:

1 Configure clock recovery as "Constant Frequency" "Semi-Automatic"
2 Setup Explicit Clock Recovery with clock source WCK(diff)/ RCK(diff) for DQ channel
3 Configure DQ channel as PAM3 signal
4 Configure measurement threshold for WCK (diff).
5 Setup Hysteresis Threshold for DQ Channel
6 Configure CTLE & DFE options and set the Channel measure to Equalized1 channel
7 Turn on Real Time Eye for Equalized1 channel
8 Setup measurement for Eye Height and Eye Width:
   - Obtain the Vertical Eye Center Position
   - Locate the Horizontal Eye Center Position
      - When Eye opening is found:
         - Search for left eye crossing using Histogram.Mode
         - Add 0.5UI from left eye crossing to get "rough" Eye Center Position
   - Rescale Eye to center for better screenshot.
   - Measure the Eye Width and the Eye Height
      - After Eye Width is measured, recalculate left and right eye crossing using Histogram.Mean to get "true" Eye Center Position

**Expected/ Observable Results:** The value of the eye measurements obtained will be reported as the final result.

**References:** JESD239A GDDR7 SGRAM specification

# 8 PAM3 SNDR Tests

# PAM3 SNDR Tests

## Test Availability Conditions

All tests in this test group appear for the following configuration in GDDR7 General Setup window:

Signal Source:

- Any signal set including DQ

**NOTE**

**Following tests support Continuous signal only:**

**1. PAM3 SNDR (DQ)**

# PAM3 SNDR (DQ) Tests

PAM3 SNDR (DQ) (Information Only)

**Test ID:** 50000

**Test Overview:** This test is to measure the PAM3 SNDR for DQ.

**Test Procedure:** Acquisition:

1 Initialize Scope
   - preset scope
   - turn off all channels
   - set sampling rate
   - set global bandwidth
   - set memory depth based on SNDR test specific config variable
   - set interpolation

2 Prepare display
   - label display with operation

3 Prepare Signal
   - Horizontal scaling (use ML enhanced dynamic range)
   - Vertical scaling (use ML enhanced dynamic range)

4 Prepare Trigger
   - set Edge Trigger
   - set trigger threshold (based on customer GUI settings)
   - try to use "Single" to capture signal instead of "Digitize"

5 Prepare Waveform
   - save waveform as H5

Measurement:

1 Configure DQ channel Coding as "PAM-3" in signal type.
2 Configure DQ channel Nominal Symbol Rate in Signal Type Setup.
3 Configure DQ channel clock recovery to explicit clock with clock source WCK (diff).
4 Configure measurement threshold for DQ channel and WCK (diff).
5 Load pattern file based on config variable for DQ channel.
6 Turn on Real Time Eye for Channel 1.
7 In Signal Type SNDR Setup, load SNDR Standard file based on config variable.
8 In Signal Type SNDR Setup, Tick "SNDR Input" Waveforms and Add "SNDR" measurement.

**Expected/ Observable Results:** The value of the PAM3 SNDR obtained will be reported as the final result.

**References:** JESD239A GDDR7 SGRAM specification

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