RELEASE NOTES

D9050PCIC PCI Express Automated Test Application Software

Keysight D9050PCIC Software Version 5.4.1.0

Release Date:	December 5, 2025
Operating System:	Microsoft Windows 10 /11 (UXR/UXR-B Series) Microsoft Windows 10 (Z-Series)
Instrument Software Version:	11.71.00021 (UXR/UXR-B Series) 06.74.01101 (Z-Series)
File Name:	SetupInfPCIE505040001.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issues Fixed

- Fixed incorrect measurement procedure for the following tests:
    - Full Swing Tx Voltage with no TxEQ Test
    - Reduced Swing Tx Voltage with no TxEQ Test
- Fixed incorrect measurement procedure for the following Reference Clock test, now it will use median cross point and edge rate as per the specification.
    - Clock Rise-Fall Matching test
- Fixed the wide variation in 64.0 GT/s Equalization Preset Tests' results.
- Fixed missing eye diagrams in Template tests.
- Fixed an issue where application overwrites the user set InfiniiSim bandwidth.
- Fixed an issue where, with lane reversal enabled, wrong pattern file was used.

Keysight D9050PCIC Software Version 5.4.0.0

Release Date:	August 4, 2025
Operating System:	Microsoft Windows 10 /11 (UXR/UXR-B Series) Microsoft Windows 10 (Z-Series)
Instrument Software Version:	11.70.00015 (UXR/UXR-B Series) 06.74.01101 (Z-Series)
File Name:	SetupInfPCIE505040000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Added Gen5 M.2 End Point and M.2 Root Complex (8.0 GT/s, 16.0 GT/s, and 32.0 GT/s) tests.
- Added support for SigTest version 5.1.08.
- Added “Link Widths” selection.
- Added additional pre-requisites during installation.
- Added SSC Deviation and SSC Frequency options in Debug Mode for Gen6 64.0 GT/s tests. These settings apply when SSC or SRIS is enabled in Device Definition. Users will be notified if changes to these settings are reverted to default after modifying SSC or SRIS settings in Device Definition.

KEYSIGHT

Modifications / Changes

- Modified “64.0 GT/s Full swing Tx voltage with no TxEQ” test to measure at the waveform UI location.
- Modified PS21 measurement method for “64.0 GT/s Pseudo package loss (No-Root and Root Device)” test according to ECN.
- When “Global InfiniiSim” is enabled:
    - the “Global Bandwidth Limit” setting will be auto-configured according to the value used in the InfiniiSim settings.
    - “Bandwidth Limit” setting in the **Configure** tab will be ignore in this case, and a message will be displayed to mark the same.
- Modified Reference Clock, Rise/Fall Matching to use slowest edge rates for result computation.
- Modified PCIE 4.0 2.5 GT/s and 5.0 GT/s Base TX Template Test to become informative test.
- Modified the bandwidth limit value used in InfiniiSim settings.

Issues Fixed

- Fixed PCIe Gen6 64.0 GT/s test to use the correct “Clock Recovery” setting when SSC or SRIS is enabled.
- Fixed incorrect VTx result.
- Fixed missing lane handling in Gen6 compliance pattern.
- Fixed incorrect bandwidth limit setting for 64.0 GT/s “Unit Interval” test.
- Fixed incorrect selected preset reported for “32.0 GT/s and 64.0 GT/s Maximum nominal Tx boost ratio” test when “Collective Preset Data Acquisition” option was enabled.
- Fixed incorrect result reported for “32.0 GT/s Maximum nominal Tx boost ratio” test when “Collective Preset Data Acquisition” option was enabled.
    - This test will no longer report Overall Results that contain AC/DC method measurement results as well.

- Fixed incorrect bandwidth limit setting when applying InfiniiSim function in CEM – End Point and CEM – Root Complex (8.0 GT/s and 16GT/s) tests.
- Fixed incorrect Bandwidth filter type used for 64.0 GT/s Reference clock tests.
- Fixed the issue wherein all CTLE values were unselected after test run, in case user selected “All” or “Autotune” option.

Keysight D9050PCIC Software Version 5.2.1.0

Release Date:	October 18, 2024
Operating System:	Microsoft Windows 10 /11 (UXR/UXR-B Series) Microsoft Windows 10 (Z-Series)
Instrument Software Version:	11.70.00015 (UXR/UXR-B Series) 06.74.01101 (Z-Series)
File Name:	SetupInfPCIE505020001.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Added prompt to remind the user to install the required MATLAB version, if not installed already.

Modification / Change

- Updated Keysight License Manager 5, Keysight License Service, Keysight Host Processor Platform, PathWave License Manager, and Keysight Bootstrap Service.

Issue Fixed

- Fixed the issue wherein Test ID “6061050” for the test “Auto Tune Optimized CTLE” will prompt an error message upon completion of the run.

Note / Recommendation

- It is recommended to install “IO Libraries Suite” version 2024 (update 1 or above).

Keysight D9050PCIC Software Version 5.2.0.0

Release Date:	September 13, 2024
Operating System:	Microsoft Windows 10
Instrument Software Version:	06.74.01101 (Z-Series) 11.60.00115 (UXR/UXR-B Series)
File Name:	SetupInfPCIE505020000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Support provided for Intel Clock Jitter Tool 6.0.0.
- Support provided for following fixtures (on all data rates):
  - CEM Fixture 4.0
  - CEM Fixture 5.0

Modifications / Changes

- Test ID “4034024” for the test “Reference Clock, Clock Frequency” has been removed.
- Test ID “4044024” for the test “Reference Clock, Clock Frequency (Common Clk) (16.0 GT/s)” has been changed to “4014024”.
- Updated the test app to report the negative jitter values (returned from SigTest) as zero values for workshop mode.
- PCI-SIG Reference Clock Jitter tests updated to report additional RMS Max jitter value.
- PCIE 6.0 Tx, Signal-to-Noise-Distortion Ratio test updated to report additional Effective Pmax and Sigma-e values.
- The following PCIe5.0, 32.0 GT/s, CEM-Root Complex tests have been changed to “Informative Test” only:
  - Uncorrelated Total Jitter test (Test ID 5053012)
  - Uncorrelated Deterministic Jitter test (Test ID 5053013)
  - Uncorrelated Total Pulse Width Jitter test (Test ID 5053010)
  - Uncorrelated Deterministic Pulse Width Jitter test (Test ID 5053011)

    - Workshop Mode Test – Min Channel - Base Jitter test (Test ID 5059100)

- Reference Clock tests have now been set to the maximum sample rate when using UXR oscilloscope.

Issues Fixed

- Fixed the issue wherein the compliance app was unable to launch in certain environments.
- Fixed abort issue with 32.0 GT/s tests on certain Z-Series scopes.
- Fixed wrong values reported by tests in specific conditions.
- Fixed abort issue with “AC Common Mode Voltage” test in certain conditions.
- Fixed non-generation of test results in measurement server mode.
- Fixed incorrect limit for Reference Clock, Clock Frequency test.
- Fixed the exception that occurred on running tests after creating a new project.
- Fixed incorrect toggle settings for 64.0 GT/s PWJ test.
- Fixed invalid results for preset tests (without Collective Preset Data Acquisition enabled).
- Fixed malfunctioning of DUT automation manual toggle in certain conditions.
- Fixed an issue wherein DUT automation with 16.0 GT/s CEM Root Complex tests toggled to incorrect preset value in workshop mode.
- Fixed an issue wherein EQ Preset test workshop mode (with Collective Preset Data Acquisition enabled) impacted the application responsiveness.

Keysight D9050PCIC Software Version 5.1.3.0

Release Date:	August 1, 2024
Operating System:	Microsoft Windows 10
Instrument Software Version:	06.74.01101 (Z-Series) 11.51.00102 (UXR/UXR-B Series)
File Name:	SetupInfPCIE505010003.exe
Licenses:	Please see the product data sheet on Keysight.com.

Modifications / Changes

- Updated Keysight License Manager 5.
- Updated Keysight License Service.
- Updated Keysight Host Processor Platform.

Issue Fixed

- Fixed an issue that appeared while saving a project with waveforms.

Keysight D9050PCIC Software Version 5.1.2.0

Release Date:	May 24, 2024
Operating System:	Microsoft Windows 10
Instrument Software Version:	06.74.01101 (Z-Series) 11.51.00102 (UXR/UXR-B Series)
File Name:	SetupInfPCIE505010002.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issues Fixed

- Fixed incorrect limit for VTX-BOOST for data rates 8 GT/s and above as per spec.

Keysight D9050PCIC Software Version 5.1.1.0

Release Date:	March 29, 2024
Operating System:	Microsoft Windows 10
Instrument Software Version:	06.74.01101 (Z-Series) 11.51.00102 (UXR/UXR-B Series)
File Name:	SetupInfPCIE505010001.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issues Fixed

- Fixed the closed eye diagram issue in 5.0 GT/s, 8.0 GT/s, and 16.0 GT/s CEM-Root Complex tests.
- Fixed the incorrect PLL function applied to 64.0 GT/s Reference Clock's RMS Jitter (Common Clk) test.

KEYSIGHT

Keysight D9050PCIC Software Version 5.1.0.0

Release Date:	October 6, 2023
Requirements Category (e.g., operating system):	Microsoft Windows 10
Requirements Category (e.g., instrument software version):	06.74.00402 (Z-Series) 11.51.00102 (UXR/UXR-B Series)
File Name:	SetupInfPCIE505010000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- 64 GT/s **Auto Tune Optimized CTLE** tests are now available under **Utilities** test list that allow users to find the optimized CTLE values for both 52 UI Jitter Pattern and PWJ Pattern automatically. The optimized CTLE values are determined with the following criteria:
    - 64 GT/s 52 UI Jitter Pattern: The lowest $T_{TX\text{-}RJ}$ value found in range of CTLE Equalization values (-5 dB to -15 dB).
    - 64 GT/s PWJ Pattern: The lowest $T_{TX\text{-}UPW\text{-}TJ}$ value found in range of CTLE Equalization values (-5 dB to -15 dB).
- Introduced new tests as stated below:

  Gen4:

    - Test ID: 4031039; Test Name: Tx, Maximum nominal Tx boost ratio for reduced swing (8.0 GT/s)
    - Test ID: 4031040; Test Name: Tx, Maximum nominal Tx boost ratio for full swing (8.0 GT/s)
    - Test ID: 4041039; Test Name: Tx, Maximum nominal Tx boost ratio for reduced swing (16.0 GT/s)
    - Test ID: 4041040; Test Name: Tx, Maximum nominal Tx boost ratio for full swing (16.0 GT/s)

  Gen5:

    - Test ID: 5031039; Test Name: Tx, Maximum nominal Tx boost ratio for reduced swing (8.0 GT/s)

- Test ID: 5031040; Test Name: Tx, Maximum nominal Tx boost ratio for full swing (8.0 GT/s)
- Test ID: 5041039; Test Name: Tx, Maximum nominal Tx boost ratio for reduced swing (16.0 GT/s)
- Test ID: 5041040; Test Name: Tx, Maximum nominal Tx boost ratio for full swing (16.0 GT/s)
- Test ID: 5051039; Test Name: Tx, Maximum nominal Tx boost ratio for reduced swing (32.0 GT/s)
- Test ID: 5051040; Test Name: Tx, Maximum nominal Tx boost ratio for full swing (32.0 GT/s)

Gen6:

- Test ID: 6031039; Test Name: Tx, Maximum nominal Tx boost ratio for reduced swing (8.0 GT/s)
- Test ID: 6031040; Test Name: Tx, Maximum nominal Tx boost ratio for full swing (8.0 GT/s)
- Test ID: 6041039; Test Name: Tx, Maximum nominal Tx boost ratio for reduced swing (16.0 GT/s)
- Test ID: 6041040; Test Name: Tx, Maximum nominal Tx boost ratio for full swing (16.0 GT/s)
- Test ID: 6051039; Test Name: Tx, Maximum nominal Tx boost ratio for reduced swing (32.0 GT/s)
- Test ID: 6051040; Test Name: Tx, Maximum nominal Tx boost ratio for full swing (32.0 GT/s)
- Test ID: 6061039; Test Name: Tx, Maximum nominal Tx boost ratio for reduced swing (64.0 GT/s)
- Test ID: 6061040; Test Name: Tx, Maximum nominal Tx boost ratio for full swing (64.0 GT/s)

Modifications / Changes

- Enhanced the algorithm to handle close eye scenario in:
  - Tx, Full swing voltage with no Tx EQ (64.0 GT/s)
  - Tx, Reduced swing voltage with no Tx EQ (64.0 GT/s)
  - Tx, Pseudo package loss, Non-Root Device (64.0 GT/s)
  - Tx, Pseudo package loss, Root Device (64.0 GT/s)
- 64 GT/s PWJ Pattern is now offering 4 levels of RNrms instead of 2 levels.
- Improved the sequence to iterate the test permutations in ascending order when multiple data rates and presets are selected.

- The following tests are changed to Informative Test only:
    - 32.0 GT/s CEM – End Point's Unit Interval test (Test ID = 5052000).
    - 32.0 GT/s CEM – Root Complex's Unit Interval test (Test ID = 5053000).
- The following tests report additional result without scope random jitter removed in reporting section:
    - Tx, Total uncorrelated PWJ (64.0 GT/s)
    - Tx, Deterministic DjDD uncorrelated PWJ (64.0 GT/s)
- Scope Noise Compensation button in main GUI will be disabled when PCIE 4.0 or PCIE 5.0 is selected as this feature is not applicable to the mentioned PCIE generations.
- Updated Reference Clock Tests, CEM – End Point Tests (32.0 GT/s), CEM – Root Complex Tests (32.0 GT/s) and Base – Transmitter Tests (32.0 GT/s) connection diagrams.
- Includes additional general reporting items to most of 64.0 GT/s tests:
    - Bandwidth Response
    - Clock Recovery Method
    - Threshold Setting and Value
- Included additional reporting items to Tx, Signal-to-Noise-Distortion-Ratio (64.0 GT/s) test:
    - Linear Fit Pulse Length (Np)
    - Linear Fit Pulse Delay (Dp)
    - Points Per UI (M)
- Included Eye Height and Eye Width reporting items in report when running multi-trials for the following tests:
    - RootComplex Tests – Workshop Mode Test – Max Channel – Signal Quality Test (32.0 GT/s)
    - EndPoints Tests – Workshop Mode Test – Max Channel – Signal Quality Test (32.0 GT/s)
- Included actual values in report when running multi-trials in workshop mode's 32.0 GT/s Equalization Preset tests.
- The reporting items (Bandwidth and Sample Rate) report the actual values used in Infiniium instead of the selected config values in application's Configure tab.
- In Z-series scope, the setting Sine(x)/x Interpolation default value is set to INT2 when Real Edge connection is disabled, and the setting Sine(x)/x Interpolation default value is set to OFF when Read Edge connection is enabled.
- Maximum available sample rate of the scope will be used in Reference Cock Tests in signal acquisition and the setting Sine(x)/x Interpolation is removed.
- The following tests will report Invalid Result when analyzing distorted waveform:
    - Tx, Full swing Tx voltage with no TxEQ (64.0 GT/s)
    - Tx, Reduced swing Tx voltage with no TxEQ (64.0 GT/s)

- Tx, Pseudo package loss, Non-Root Device (64.0 GT/s)
- Tx, Pseudo package loss, Root Device (64.0 GT/s)

Issues Fixed

- In PCI-SIG Reference Clock Jitter tests (all data rates), same vertical scaling will be used to capture noise floor signal if **Noise Floor Deembed** config is enabled.
- Fixed Keysight U3020A S26 functionality to be used as part of supported Switch Matrix instruments.
- Fixed the signal check issue on second pair's reference clock signal in CEM – Root Complex tests.
- Updated Reference Clock Test lists as per specifications:

PCIE Gen	Data Rates	Test ID	Test Name	New Name in Select tests list and Test Name
4.0	16.0 GT/s	4044019	Reference Clock, SSC frequency range	Reference Clock, SSC frequency range **(Common Clk)**
4.0	16.0 GT/s	4044020	Reference Clock, SSC deviation	Reference Clock, SSC deviation **(Common Clk)**
5.0	All Data Rate Tests	5014019	Reference Clock, SSC frequency range	Reference Clock, SSC frequency range **(Common Clk)**
5.0	All Data Rate Tests	5014020	Reference Clock, SSC deviation	Reference Clock, SSC deviation **(Common Clk)**
5.0	All Data Rate Tests	5014021	Reference Clock, Max SSC df/dt	Reference Clock, Max SSC df/dt **(Common Clk)**
5.0	32.0 GT/s	5054020	Reference Clock, SSC deviation (32.0 GT/s)	**Removed** as IR testing is not supported
6.0	All Data Rate Tests	6014019	Reference Clock, SSC frequency range	Reference Clock, SSC frequency range **(Common Clk)**
6.0	All Data Rate Tests	6014020	Reference Clock, SSC deviation	Reference Clock, SSC deviation **(Common Clk)**

6.0	All Data Rate Tests	6014021	Reference Clock, Max SSC df/dt	Reference Clock, Max SSC df/dt **(Common Clk)**
6.0	32.0 GT/s	6054020	Reference Clock, SSC deviation (32.0 GT/s)	**Removed** as IR testing is not supported
6.0	64.0 GT/s	6064020	Reference Clock, SSC deviation (64.0 GT/s)	**Removed** as IR testing is not supported

Known Issues

- In measurement server mode, after running 32 GT/s tests with all CTLE check boxes selected, error is thrown intermittently which restricts the application to proceed to new trial.

  Workaround: Please restart the application when error is thrown at the beginning of a new trial.

- When running 8 GT/s CEM EndPoint tests on Real Edge channel, SigTest throws “Memory allocation failed” error intermittently.

  Workaround 1: Use normal channel instead of Real Edge channel.

  Workaround 2: Use smaller “Number of UI” (parameter can be found in **Configure** Tab) if Real Edge channel is used.

Keysight D9050PCIC Software Version 5.0.0.0

Release Date:	June 23, 2023
Requirements Category (e.g., operating system):	Microsoft Windows 10
Requirements Category (e.g., instrument software version):	06.73.00102 (Z-Series) 11.50.00401 (UXR/UXR-B Series)
File Name:	SetupInfPCIE505000000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- When tests are executed in MR (Measure, Report) mode, the application checks for required waveforms to run all the selected tests. If any of the waveforms are missing, the application will take an action based on the selected Test Abort Action.
- Implemented “DC preset calculation method” as an alternative measurement method to “AC fit method” for 32.0 GT/s Equalization Preset Tests according to ECN by PCI-SIG.
- Supports new Sigtest version 4.0.52.
- Supports UXR-B Series oscilloscope.

Modifications / Changes

- Removed 64.0 GT/s tests from the test list, when following two criteria are met:
  - App running in offline mode.
  - App running on 6.xx version of Infiniium baseline.

Issues Fixed

- 64.0 GT/s tests' availability issue fixed. Now, 64.0 GT/s tests will remain disabled in an application not licensed for 64.0 GT/s data rate even when a 64.0 GT/s project file is loaded in the test application.
- Issue fixed where-in app presented empty result from SigTest as 0.0 (marked as Pass) in the result and report section. The fix now allows to report empty result as "No results" (marked as Fail).

- Fixed DUT automation's **Manual Toggle** exception issue which appeared when user tried to toggle manually without a pulse generator connection.

Known Issues

- In measurement server mode, after running 32 GT/s tests with all CTLE check boxes selected, error is thrown intermittently which restricts the application to proceed to new trial.

  Workaround: Please restart the application when error is thrown at the beginning of a new trial.

- When running 8 GT/s CEM EndPoint tests on Real Edge channel, SigTest throws "Memory allocation failed" error intermittently.

  Workaround 1: Use normal channel instead of Real Edge channel.

  Workaround 2: Use smaller "Number of UI" (parameter can be found in **Configure** Tab) if Real Edge channel is used.

Keysight D9050PCIC Software Version 4.1.0.0

Release Date:	April 12, 2023
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	06.73.00102 (Z-Series) 11.50.00102 (UXR-Series)
File Name:	SetupInfPCIE504010000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Support provided for multiselect presets in **Device Definition** dialog box to allow tests to run with multiple preset settings in single trial for 8 GT/s, 16 GT/s, 32 GT/s and 64 GT/s.
- Enhanced application to run Equalization Preset Tests on multiple lanes by using Switch Matrix.
- Enabled support for alternate measurement method to get average eye amplitude at 0.5 UI location by using Infiniium software. Impacted tests are Peak Differential Output Voltage and Deemphasized Voltage Ratio for all generations and data rates.
- Included Extrapolated Eye Height as additional test item in test report for 16 GT/s Template Tests.
- Included option for offline waveforms in project file during project saving.
- Offered other Clock Recovery Method for 64GT/s tests in Debug Mode.

Modifications / Changes

- Updated Keysight License Manager 5.
- Updated new Gen 6's 64 GT/s compliance pattern files in application.
- Updated app to report SigTest returned negative jitter values as zero values.
- Modified **Test Mode** section of the **Set Up** tab, some functionality moved to **View** menu > **Preferences** option > **Preferences** dialog box > **Run** tab > **Test Execution** section
- Modified the required pattern wording from 1010 to 3030 in 64 GT/s PWJ measurement's instructions.

Issues Fixed

- Fixed the exception thrown when performing Scope Noise Compensation with DUT Automation feature on.
- Fixed the issue where application was unable to locate transfer function files in 8.0 GT/s workshop mode.

Known Issue

- In Disaggregation mode, after running 32 GT/s tests with all CTLE check boxes selected, error is thrown intermittently which causes the application to be unable to proceed to new trial.

  Workaround: Please restart the application when error is thrown at the beginning of new trial.

- When running 8 GT/s CEM EndPoint tests on Real Edge channel, SigTest throws "Memory allocation failed" error intermittently.

  Workaround 1: Use normal channel instead of Real Edge channel.

  Workaround 2: Use smaller "Number of UI" (parameter can be found in **Configure** Tab) if Real Edge channel is used.

Keysight D9050PCIC Software Version 4.0.0.0

Release Date:	December 12, 2022
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	06.73.00102 (Z-Series) 11.40.00105 (UXR-Series)
File Name:	SetupInfPCIE504000000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Supports PCIe Gen 6 specification.
- Supports new Sigtest Phoenix version 5.1.04.
- Supports 64 GT/s “Scope Noise Compensation” feature.
- Supports Clock Jitter Tool in PCIe Gen 5 “Reference Clock” test point.
- Implemented Infiniium gated features.

KEYSIGHT

Modifications / Changes

- Application name is changed from “PCI-Express Gen5 Test Application” to “PCIE Test Application”.
- Included Equalization Preset Tests’ Boost, Preshoot, and De-emphasis in Gen 5’s 32 GT/s, Gen 6’s 32 GT/s, and 64 GT/s.
- Updated 8 GT/s – 32 GT/s default number of UI values in **Configure** tab to acquire at least 500 pattern repetitions.
- Implemented hardware differential to replace math function differential. Hence, the channel selection is modified to align with hardware differential capability.
- Turned on waveform display for user to visualize the waveform during DUT Manual Toggle operation.
- Added missing Gen 5 Reference Clock – Clock Frequency (Common Clk) tests with test ID:
    - 5014024
    - 5054024
- Added missing Gen 5 Reference Clock – SSC Deviation tests with test ID:
    - 5054020
- Support provided for 32 GT/s Equalization Preset Tests to run individually (without enabling Collective Preset Data Acquisition) by using Sigtest Phoenix 5.1.04.
- Included toggle setting number in signal configuration prompt.
- Rearranged informative CAL OUT message into a separated message prompt in DUT manual toggle usage.

Issues Fixed

- Fixed the missing reference image in 5.0 GT/s Reference Clock RMS Jitter tests.
- Fixed the missing reference eye diagram image in 8 GT/s and 16 GT/s CEM End Point/Root Complex's Template tests.
- Fixed 32 GT/s CEM End Point and Root Complex's Max Channel tests that didn't apply embedding in worker PC in measurement server mode.
- Fixed the incorrect channel shown issue in connection diagram. Now, it is shown as per the selected channel in **Connection Setup** dialog box.
- Fixed the incorrect list of required presets to acquire for half power equalization preset test in **Collective Preset Data Acquisition** mode:
    - 8 GT/s: P01, P03, P04, P05, P06, and P09
    - 16 GT/s: P01, P03, P04, P05, P06, and P09
    - 64 GT/s: Q00, Q01, Q02, Q03, and Q04
- Fixed test abort issue when **Equalization Preset Tests** are re-run in workshop mode.
- Fixed the issue that application cannot set to 33 GHz bandwidth in Z-series scope as per the specification.
- Fixed 16 GT/s PWJ tests' "memory allocation failed" issue thrown by SigTest if the waveform is captured with maximum number of UI, maximum noise reduction BW, and maximum sample rate by creating a new config "Number of UI for PWJ Tests" with limited editable range.

Known Issue

- In 32 GT/s, Half Power Equalization Preset Tests will not be able to run with "Collective Preset Data Acquisition" due to Sigtest Phoenix 5.1.04 limitation to run without full list of presets.

Keysight D9050PCIC Software Version 3.20.3.0

Release Date:	July 26, 2022
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.71.00001 (90000-Series, Q-Series, or Z-Series) 11.30.00406 (UXR-Series)
File Name:	SetupInfPCIE503200003.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issues Fixed

- Fixed incorrect reported results for:
    - EndPoint Tests, Peak Differential Output Voltage (Transition)(32.0 GT/s)
    - EndPoint Tests, Peak Differential Output Voltage (Non-Transition)(32.0 GT/s)
    - RootComplex Tests, Peak Differential Output Voltage (Transition)(32.0 GT/s)
    - RootComplex Tests, Peak Differential Output Voltage (Non-Transition)(32.0 GT/s)

Keysight D9050PCIC Software Version 3.20.2.0

Release Date:	July 04, 2022
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.71.00001 (90000-Series, Q-Series, or Z-Series) 11.25.00202 (UXR-Series)
File Name:	SetupInfPCIE503200002.exe
Licenses:	Please see the product data sheet on Keysight.com.

Modification / Changes

- Increase the number of attempts to reset the DUT during DUT Automation.

Keysight D9050PCIC Software Version 3.20.0.0

Release Date:	March 04, 2022
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.71.00001 (90000-Series, Q-Series, or Z-Series) 11.25.00202 (UXR-Series)
File Name:	SetupInfPCIE503200000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Added CEM End Point and CEM Root Complex tests.
- Added DUT Automation features with 81150A/81160A as toggle source.
- Added lane reversal DUT capability.
- Enabled differential connection for two channels UXR oscilloscope.
- Each test points now have their own bandwidth configuration options.
- Each data rates now have their own interpolation configuration options.

Modifications / Changes

- Required MATLAB runtime version R2021a (9.10).
- Updated default SigTest version; see SigTest Version Configuration Overview
- Removed support for SigTest version 4.0.46
- Test Mode selection will only be available in “Acquire,Measure,Report” test execution phases.
- 32.0 GT/s Equalization Preset Test must run with “Collective Preset Data Acquisition” option enabled.
- Equalization Preset Tests will be enabled automatically when “Analyze Captured Waveforms” mode or “Workshop Compliance Mode” is enabled.
- Updated 32.0 GT/s jitter tests in Base - Transmitter Tests to use PWJ (toggle 1010 pattern).
- Updated 16.0 GT/s PWJ tests in Base - Transmitter Tests to use PWJ (toggle 1010 pattern).
- SigTest version 5.1.01 reports 0 (zero) for jitter result when the jitter value is very small.
- Increased the number of Waveform Point setting to 64000000 in SigTest Phoenix to ensure that the analysis is done on entire waveform when interpolation option is enabled.
- Individual test status will report “Invalid result” or “No result” when there are invalid test results or unable to find the waveform required to perform measurement.
- Missing test result from SigTest tools will be reported as “NA”.
- Revised compliance pattern checking mechanism for Reference Clock Tests.
- Allowed CTLE selection for running test with CTLE option using SigTest tools.
- Displayed all diagrams generated by SigTest Phoenix tools in Template Test.
- Reported Eye Height and Eye Width value in Template Test.
- Template Test now have same set of reporting items across all data rates.
- For each test, the report displays: Connection Type, Channel, Sample Rate, Bandwidth, Selected Preset, Data Lane, Selected SigTest Version (if applicable), Reference Clock, S4P file used, CTLE Embedding and SigTest Status (if applicable).
- Updated the content of signal change message.
- Prompt added to alert the user when switch matrix changes are required.

- Captions for all the images in the report will be appended with “(Image)”
- Waveforms and test results in worker machine will be store in test application device folder in Measurement Server run. Please see the Hard Disk Consumption Notes
- Re-arrange test list for Base Transmitter Tests to optimize the test flow for DUT Automation toggling.
- Increased “Max Store Files Trial” limit to 100 trials.
- Removed “Force New Waveform Acquisition” configuration because the test application will decide to either reuse the existing waveform or acquire a new one.
- Disabled GUI during test run.
- Added PWJ (toggle 1010 pattern) as one of the preset selections in “User Defined Waveform Directory”.
- Added deemphasis selection in “User Defined Waveform Directory”.

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Issues Fixed

- Fixed incorrect label for Peak Differential Output Voltage (Non-Transition) & Peak Differential Output Voltage (Transition) test.
- Fixed the test result for Base – Transmitter Test – Absolute delta of DC common mode voltage during L0 and Idle to become an absolute value.
- Fixed inconsistent signal scaling between the conventional and the Measurement Server run. • Corrected pass/fail reporting for Template Test.
- Fixed the issue in which the tests were not running properly with the CTLE option while using remote commands.
- Fixed the issue wherein 32.0 GT/s Reference Clock Tests were reporting wrong transfer function.
- Fixed the general Reference Clock Tests error in Measurement Server run.
- Fixed the PCIE4.0 Reference Clock Tests error that occurred while using remote commands.
- Fixed missing Filter Response images in Reference Clock Tests.
- Fixed general Switch Matrix test flow and improved error handling.

- Fixed general issue in Measurement Server test flow.
- Fixed the test completion status/display error in Measurement Server mode.
- Fixed general test plan issue.
- Fixed general “Workshop Compliance Mode” test error.
- Fixed “User Defined Waveform Directory” GUI bugs.
- General GUI improvement and fixed bugs.Fixed the issue that application cannot set to 33GHz bandwidth in Z-series scope as according to specification.

Notes / Recommendations

- 5.0 GT/s, 8.0 GT/s, and 16.0 GT/s CEM Root Complex Tests (except Unit Interval Test) does not support real edge connection.
- Measurement Server mode requires same version of the test application to be installed on all participating PCs.
- Using GPIB-USB connection for DUT Automation, in Measurement Server mode – it will only work when the toggle source is connected to the Manager PC.
- Using CAL OUT as toggle source for DUT Automation will have a longer test time as compared to the 81150/60A toggle source.

Keysight D9050PCIC Software Version 3.2.0.0

Release Date:	October 26, 2021
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.60.00403 (90000-Series, Q-Series, or Z-Series) 11.10.00105 (UXR-Series)
File Name:	SetupInfPCIE503020000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Supports the Keysight Infiniium applications' bundle license for PCIe. The PCI Express bundle license provides access to the following applications:

  1. Keysight D9040PCIC PCI Express Compliance Test Application
  2. Keysight D9050PCIC PCI Express Gen 5 Compliance Test Application

Keysight D9050PCIC Software Version 3.0.0.0

Release Date:	December 2020
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.55.00504 (90000-Series, Q-Series, or Z-Series) 10.25.01001 (UXR-Series)
File Name:	SetupInfPCIE503000000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Supports Keysight D9010AGGC Compliance Test Software Measurement Server for using multiple machines/PCs over a network as processing engines in order to significantly enhance the test execution speed. To know more, please visit the D9010AGGC product page at https://www.keysight.com.
- Supports Switch Matrix for up to 8 lanes testing.
- Supports PCIE 4.0 Base Specification tests, in addition to existing PCIE 5.0 tests.
- Includes CTLE iteration for 32.0 GT/s jitter tests.

Issues Fixed

- Fixed collective data acquisition sequence for Equalization Preset Tests.
- Removed largest transition amplitude (outer eye) and smallest transition amplitude (inner eye) reporting from Full Swing Tx Voltage with no TxEQ Test.
- Fixed incorrect limit for Unit Interval Test at 8.0 GT/s as per PCIE 5.0 spec.
- Fixed the issue – SSC Deviation returns 0 value when the test is run in SRIS mode.
- Updated the RMS AC Peak Common Mode Output Voltage (2.5 GT/s) test as info-only.
- Updated correct template file (PCIE_2_0_CARD\TX_CON_6.0dB.dat) to be used in Gen4's 5GT/s -6dB template test.

Keysight D9050PCIC Software Version 1.11.2.0

Release Date:	July 2020
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.55.00504 (90000-Series, Q-Series, or Z-Series) 10.25.00607 (UXR-Series)
File Name:	SetupInfPCIE501110002.exe
Licenses:	Please see the product data sheet on Keysight.com.

Issues Fixed

- Hide the selection of Channel 3 & 4 when running in two-channel scope setup.
- Fix two-channel handling SSC Modulation Frequency test which will turn off Channel 3 display.
- Accept any folder by ignoring additional non-waveform files in folder when copying waveform from external disk.
- Increase time out during setting up measurement trend.
- Removed 256GSa/s choice from sampling rate selection in 2.5GT/s and 5.0GT/s tests due to unreasonably high sampling rate in low data rate.

Keysight D9050PCIC Software Version 1.11.1.0

Release Date:	April 2020
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.55.00401 (90000-Series, Q-Series, or Z-Series) 10.20.00503 (UXR-Series)
File Name:	SetupInfPCIE501110001.exe
Licenses:	Please see the product data sheet on Keysight.com.

Modifications / Changes

- Compliance application versioning format is changed to 1.11.1.0. This format will be used for all future releases.

Issues Fixed

- Fixed the behavior to force acquiring waveform if Force New Acquisition option is checked during Equalization Preset Test.
- Increased the timeout duration dynamically according to Interpolation Integer.
- Updated the correct test limit of Pseudo Package Loss Test for 8, 16 & 32GT/s.
- Fixed the precision level of DDJ and RJ tests for all data rates.
- Fixed the RJ test to report in RMS instead of p-p value.
- Updated the correct limit used in Absolute Min Input Voltage from MAX_INCLUSIVE to MIN_INCLUSIVE.
- Updated the sampling rate selection for each data rate in Configure Tab.

Known Issues

- With data speed of 2.5GT/s, 1.6M UI and INT4 of Sine(x)/x Interpolation configuration, Infiniium might not able to capture the required waveform intermittently.

Keysight D9050PCIC Software Version 1.11.0000

Release Date:	December 06, 2019
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.50.00906 (90000-Series, Q-Series, or Z-Series) 10.12.05302 (UXR-Series)
File Name:	SetupInfPCIE501110000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Supports Infiniium Oscilloscope Software version 6.50 for non UXR-Series oscilloscope.
- Supports Infiniium Oscilloscope Software version 10.12 for UXR-Series oscilloscope.
- Supports non Real Edge connection in Q-Series and Z-Series oscilloscope (for data rate 16GT/s and below only).

Modifications / Changes

- App will prompt reacquire-waveform-confirmation message if the previous waveform exists in the same device folder.
- Rephrase the choices in Sample Rate, GSa/s of all data rates by removing "E+9" in Configure tab.
- Remove Equalization Preset Tests when running Base-RefClk Test.
- Rephrase Noise Reduction BW, GHz to Noise Reduction BW, Hz in Configure tab.
- Remove additional RemoteHint that will cause duplicated description in Remote Programming Reference.

Keysight D9050PCIC Software Version 1.10.0000

Release Date:	September 27, 2019
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.40.01101 (90000-Series, Q-Series, or Z-Series) 10.11.04711 (UXR-Series)
File Name:	SetupInfPCIE501100000.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Supports 2.5GT/s and 5.0GT/s data rate tests.
- Provides Waveform Management GUI to manage waveform folders effectively.

Modifications / Changes

- SigTest application version 4.0.46 is packaged and supported in compliance application.
- In the absence of EZJIT/EZJIT PLUS license, several tests across all data rates will be disabled as stated below:
    - Unit Interval
    - SSC Modulation Frequency
    - SSC Peak Deviation (Max)
    - SSC Peak Deviation (Min)
    - SSC Df/Dt (Max)
    - RefClk SSC Frequency Range
    - RefClk SSC Deviation
    - RefClk Max SSC df/dt
    - Peak to Peak Jitter (Common Clk)
    - RMS Jitter (Common Clk)

Known Issues

- Real Edge license checking is unavailable in Q-Series & Z-Series scopes.

Keysight D9050PCIC Software Version 01.00.0001

Release Date:	June 07, 2019
Requirements Category (e.g., operating system):	Microsoft Windows 10 and Windows 7
Requirements Category (e.g., instrument software version):	6.40.00714 (90000-Series, Q-Series, or Z-Series) 10.10.04419 (UXR-Series)
File Name:	SetupInfPCIE501000001.exe
Licenses:	Please see the product data sheet on Keysight.com.

New Features / Additions

- Supports PCI Express Base Specification Revision 5.0
- Supports Base - Transmitter Tests, Base - References Clock Tests, and Equalization Preset Tests
- Supports 8 GT/s, 16 GT/s and 32 GT/s data rate tests
- Supports updated SigTest version
- Provides ANPL (Analyze Now; Process Later)
- Supports UXR Oscilloscopes with 50GHz bandwidth or higher
- Supports Real Edge connection on Z-Series & Q-Series Oscilloscopes with 50 GHz bandwidth or higher

Known Issues

- SigTest executables GUI may not reflect the actual configuration during measurements.
- Enabling **Interpolation** option (in **Configure** tab) will lead to longer test time

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SigTest Version Configuration Overview

PCIE Gen 5.0 & SigTest

Gen	Data Speed (GT/s)	Test Point	SigTest Configuration
5.0	2.5	Base – Tx	4.0.51
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		Reference Clock	N/A
	5.0	Base – Tx	4.0.51
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		Reference Clock	N/A
	8.0	Base – Tx	4.0.51
		CEM – End Point	3.2.0.3
		CEM – Root Complex	3.2.0.3
		Reference Clock	N/A
		Equalization Preset	4.0.51
	16.0	Base – Tx	4.0.51
		CEM – End Point	4.0.51
		CEM – Root Complex	4.0.51
		Reference Clock	N/A
		Equalization Preset	4.0.51
	32.0	Base – Tx	5.1.01 (all Jitter Tests) 5.0.24 (Others)
		CEM – End Point	5.1.01
		CEM – Root Complex	5.1.01
		Reference Clock	N/A
		Equalization Preset	5.1.01

SigTest Installation

It is recommended to install all the supported SigTest application versions as mentioned in the Table above. See more details in Keysight D9050PCIC PCI Express Gen5 Automated Test Application - Compliance Testing Methods of Implementation.

Download the required SigTest application version(s) from the following link:
https://www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html?grouping=rdc%20Content%20Types&sort=title:asc

Hard Disk Consumption Notes

The table below illustrate a few test setups and their approximate total hard disk space consumption while running test.

Test Setup	Approximate hard disk consumes
32G/s Base TX - Selected all tests (no Equalization Preset Tests) + enabled all CTLE using Infiniium	1.2GB
32G/s CEM End Point - Selected all tests (no Equalization Preset Tests) + enabled all CTLE using Infiniium	915MB
32G/s CEM Root Complex - Selected all tests (no Equalization Preset Tests) + enabled all CTLE using Infiniium	915MB
32GT/s CEM Root Complex - Selected all tests (no PWJ Tests and Equalization Preset Tests) + enabled all CTLE using Infiniium + 8 Data Lanes using switch matrix	8.4GB
32GT/s Base - Selected all tests (no Equalization Preset Tests) + enabled all CTLE using Infiniium + 8 Data Lanes using switch matrix	14GB
32GT/s CEM End Point - Selected only Max Channel tests (with Equalization Preset Tests) + enabled all CTLE using Infiniium + 8 Data Lanes using switch matrix	9GB

Initial Release