RELEASE NOTES

Keysight PCIe 6 Protocol Testing

This document contains the latest information on the Keysight P5573A/P5574A/P5575A PCIe 6 Protocol Exerciser, P5570A/P5571A/P5572A PCIe 6 Protocol Analyzer, P5563B/P5563C PCIe 6 Test Backplane hardware, and the accompanying P5500 PCIe Traffic Analysis software.

Note: The P5563B Test Backplane model is scheduled for discontinuation in June 2026 and will be succeeded by the P5563C Test Backplane model.

Keysight P5573A/P5574A/P5575A PCIe 6 Protocol Exerciser, P5570A/P5571A/P5572A PCIe 6 Protocol Analyzer, P5563B/P5563C PCIe 6 Test Backplane Hardware, and P5500 PCIe Traffic Analysis Software

Version 1.218.1

Released Date:	March, 2026
Release Version:	1.218.1
Release Type	Minor Release
Operating System	Microsoft Windows 11 (64 bit)
Exerciser Requirements	Refer to Hardware Requirements
Analyzer Requirements	Refer to Hardware Requirements
Controller Requirements	Refer to Controller Requirements
License Requirements	Refer to License Requirements

Maintenance Updates

This minor release of the P5500 PCIe Traffic Analysis software includes general bug fixes and internal improvements to enhance overall stability and reliability.

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Special Notes:

- Software Automation API users
  Make sure to use the correct binding associated with the Software Release. With each release the binding needs adoption. This is also needed, even if you do not require a new API feature of the release.
  - C# users: take the Interop files fresh from C:\ProgramFiles\Keysight\PCIeAnalysis\Install\Bin\Release
  - Python: re-run "C:\Program Files\Keysight\PCIeAnalysis\Samples\Python\setup-python-for-automation.bat"
  - C++: recompile

Known Issues

Known Issues – General

- After power cycling a module, run the Cleanup utility
  The Cleanup utility is available from Windows Start menu > Keysight PCIe Traffic Analysis > Cleanup
- Link up might not establish when the software GUI for the Analyzer module is launched after the software GUI for the Exerciser module, or if the test setup includes an Endpoint DUT on top of the Analyzer.
  Workaround: First, launch the software GUI for the Analyzer module and then the software GUI for the Exerciser module. You can also select both the Analyzer module and the Exerciser module during the module selection in the Module Setup screen, which will launch the software GUI's for both the Analyzer and Exerciser in the same window.

Known Issues – Exerciser

- The following clock configurations are partially supported.
  Note: The external clock must be available before launching the session.
  - FLIT mode: CC with SSC and SRNS for 64 GT/s data rate
  - Non FLIT mode: CC with SSC and SRNS for 32 GT/s data rate.
- Polarity inversion might not work as expected in Non-FLIT mode when bifurcation settings are applied.

Known Issues – Analyzer

- The following clock configurations are partially supported.
  Note: The external clock must be available before launching the session.
  - FLIT mode: CC with SSC and SRNS for 64 GT/s data rate
  - Non FLIT mode: CC with SSC for 32 GT/s data rate
- Performance Overview feature is not supported in FLIT mode.
- Analyzer might enter an undefined state if powered on before the reference clock is available, or if the reference clock is lost (e.g., due to server reboot or backplane power-off).

Workaround: To avoid this issue, ensure that the reference clock is active before powering on the Analyzer. If the clock is interrupted, close the GUI → perform cleanup → relaunch GUI to reprogram the FPGA.
For more details, please refer to the "Exerciser or Analyzer Initialization with Reference Clock Dependency" section in the *Keysight P5500 PCIe and CXL Traffic Analysis User Guide*.

- The Activity per Lane status in the Link Status tab does not update correctly, even when a proper link-up established in non-FLIT mode.
- Analyzer GUI crashes intermittently while performing packet capture with SDS triggers in FLIT mode.
- L0p captures might have issues in FLIT mode.
- Non-FLIT mode captures of 16GB might crash the Analyzer GUI.

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Version 1.218.0

Released Date:	January, 2026
Software Version:	1.218.0
Operating System	Microsoft Windows 11 (64 bit)
Exerciser Requirements	Refer to Hardware Requirements
Analyzer Requirements	Refer to Hardware Requirements
Controller Requirements	Refer to Controller Requirements
License Requirements	Refer to License Requirements

Important Notes:

- Software Automation API users
  Make sure to use the correct binding associated with the Software Release. With each release the binding needs adoption. This is also needed, even if you do not require a new API feature of the release.
    - C# users: take the Interop files fresh from C:\ProgramFiles\Keysight\PCIeAnalysis\Install\Bin\Release
    - Python: re-run "C:\Program Files\Keysight\PCIeAnalysis\Samples\Python\setup-python-for-automation.bat"
    - C++: recompile

New Features and Enhancements

This release of the P5500 PCIe Traffic Analysis Application introduces the following features and enhancements:

Exerciser

- Tag configuration is supported in both FLIT and Non-FLIT modes:
    - Request Behavior packet enables configuration of Automatic or Manual Tag
    - Completion Behavior packet enables configuration of Software Completion Tag

      Note: In FLIT mode, tag configuration is supported only in the Block Transfer mode.
- Hierarchy ID message is supported for Message Request packet with data in both FLIT and Non-FLIT modes.
- Virtual Channel page provides the Device Readiness Status (DRS) message settings and the Hardware Status pane displays the status of the DRS message received from the DUT in FLIT mode.

- Modify DLLP tab on the Error Insertion page allows you to specify the number of DLLPs that the Exerciser will identify and replace with another predefined DLLPs in FLIT mode.
- CRC and FEC errors tab supports Bit wise insertion of FEC errors in FLIT mode.
- Compliance tab in the Built-In Self-Test (BIST) mode allows you to configure and run TX and RX compliance tests to validate the DUT's transmitter (TX) behavior and the DUT's receiver (RX) behavior. The following modes are supported:
    - RX Compliance Mode: Exerciser transmits a 100 MHz signal to trigger the DUT to send the compliance pattern at the specified speed and de-emphasis level. The Exerciser then synchronizes to the compliance pattern sent by the DUT and checks BER counters.
    - TX Compliance Mode: In this mode, the Exerciser transmits compliance patterns at selected speed and de-emphasis level, and DUT synchronizes to that pattern and checks BER counters.
- L0p power state supported for Gen1 and Gen2.
- Completion Behavior is supported in FLIT mode. Currently, only 'Queue Shared' completion queue is available.

Analyzer:

- Compute on Run feature is supported in both FLIT and Non-FLIT modes.
- L0p transitions are captured in both upstream and downstream directions, and the LTSSM Viewer displays the L0p transitions.

Fixed Issues

- In Exerciser, when using 14-bit tag mode, the DUT config scan fails.
- Sometimes, on application startup, an error message "License is not available" appears.
- For P5575A & P5574A Exerciser:
    - Link width is incorrectly defaulting to x16, while the hardware supports only up to x8 or x4.
    - In Self-Test, two voltages are reported as failing incorrectly.
- Analyzer Transaction Viewer sometimes aborts computation without results. If part of Compute all, then all computations stop without results. In this case, exclude Transaction Viewer from computations.
- In the event of speed transitions and depending on the speed change time of the devices under test, captures might have the following limitations:
    - Packets might be missing
    - Packets might have bit errors (shown as red)
    - Wrong state transitions might be shown in the LTSSM viewer (transitions to L0)
    - LTSSM decoding does not work with SKP OS or any TS filtered
    - FLITs might be corrupted on entry to L0. This recovers while staying in L0

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Known Issues

Known Issues – General

- After power cycling a module, run the Cleanup utility
  The Cleanup utility is available from Windows Start menu > Keysight PCIe Traffic Analysis > Cleanup
- Link up might not establish when the software GUI for the Analyzer module is launched after the software GUI for the Exerciser module, or if the test setup includes an Endpoint DUT on top of the Analyzer.
  Workaround: First, launch the software GUI for the Analyzer module and then the software GUI for the Exerciser module. You can also select both the Analyzer module and the Exerciser module during the module selection in the Module Setup screen, which will launch the software GUI's for both the Analyzer and Exerciser in the same window.

Known Issues – Exerciser

- The following clock configurations are partially supported.
  Note: The external clock must be available before launching the session.
  - FLIT mode: CC with SSC and SRNS for 64 GT/s data rate
  - Non FLIT mode: CC with SSC and SRNS for 32 GT/s data rate.
- Polarity inversion might not work as expected in Non-FLIT mode when bifurcation settings are applied.

Known Issues – Analyzer

- The following clock configurations are partially supported.
  Note: The external clock must be available before launching the session.
  - FLIT mode: CC with SSC and SRNS for 64 GT/s data rate
  - Non FLIT mode: CC with SSC for 32 GT/s data rate
- Performance Overview feature is not supported in FLIT mode.
- Analyzer might enter an undefined state if powered on before the reference clock is available, or if the reference clock is lost (e.g., due to server reboot or backplane power-off).
  Workaround: To avoid this issue, ensure that the reference clock is active before powering on the Analyzer. If the clock is interrupted, close the GUI → perform cleanup → relaunch GUI to reprogram the FPGA.
  For more details, please refer to the "Exerciser or Analyzer Initialization with Reference Clock Dependency" section in the *Keysight P5500 PCIe and CXL Traffic Analysis User Guide*.
- The Activity per Lane status in the Link Status tab does not update correctly, even when a proper link-up established in Non-FLIT mode.
- Analyzer GUI crashes intermittently while performing packet capture with SDS triggers in FLIT mode.
- L0p captures might have issues in FLIT mode.
- Non-FLIT mode captures of 16GB might crash the Analyzer GUI.

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Version 1.217.0

Released Date:	September, 2025
Software Version:	1.217.0
Operating System	Microsoft Windows 11 (64 bit)
Exerciser Requirements	Refer to Hardware Requirements
Analyzer Requirements	Refer to Hardware Requirements
Controller Requirements	Refer to Controller Requirements
License Requirements	Refer to License Requirements

New Features and Enhancements

This release of the P5500 PCIe Traffic Analysis Application introduces the following features and enhancements:

General

- P5500 PCIe Traffic Analysis Application now supports Windows 11.
- Keysight Pathwave License Manager rebranded to Keysight Software Manager Utility.
- FLIT spelling updated to FLIT (in uppercase) across the GUI and product documentation.

Exerciser

- Power Management mode now supports the following features in FLIT mode:
    - L0p Upsizing, with the Hardware Status pane displaying the status of the negotiated link width.
    - L1 power state
- Auto Equalization feature implemented for 8.0GT/s, 16.0GT/s, and 32.0GT/s data rates in both FLIT and Non-FLIT modes.
- Implemented Transceiver cursor settings for 64.0GT/s data rate (Pre Cursor 2, Pre Cursor 1, and Post Cursor).
- DUT can request cursors from the Exerciser once the PCIe link is established.
- Supports the following Error Insertion capabilities in FLIT mode:
    - Data Link Layer Errors:
        - Modify FLIT DLLP data by comparing and replacing it with another predefined DLLP values
        - Send arbitrary DLLP packets
        - Send Immediate selective or standard NACK, or Sequence Triggered NACK
        - Disable ACK transmissions

        - Insert CRC and FEC errors
    - Transaction Layer errors:
        - Insertion of TLP Poisoned, TLP Nullified, TLP Poisoned (Phy), and Malformed TLP errors in Request Behavior packets
- Request Behavior records can be added for packets added to a function in FLIT mode.
- Introduced '*.pacap' file format for Analyzer captures. Files saved in this format can be analyzed via API or software GUI.
- Redesigned the GUI layout of the 'Config Space' and 'DUT Config Space' to enhance readability and improve user experience.

Analyzer:

- Advanced Trigger supported in FLIT mode.
- L1 power state capture supported in FLIT mode.
- Auto Lane Polarity Inversion supported in FLIT mode.
  Note: After selecting 'Auto' mode for Lane Polarity Inversion, you must retrain the link or initiate a new linkup for the Analyzer module to correctly detect lane polarities.
- Auto Lane Reversal supported in Non-FLIT mode.
  Note: After selecting 'Auto' mode for Lane Reversal, you must retrain the link or initiate a new linkup for the Analyzer module to correctly detect lane reversal.

Fixed Issues

- Fixed issues to improve the accuracy of LTSSM state capture during PCIe link training.
- Upon linkup at 64.0 GT/s, it can happen that the Exerciser module only reaches up to 32.0 GT/s. In this case, use the "Initiate Speed Change" button to reattempt switching to 64.0 GT/s
- The Voltage Monitor self-tests might sometimes fail for the Exerciser module.
- In Exerciser FLIT mode, the Exerciser/DUT Initiates Lower Speed Change LTSSM tests are failing when the link speed transitions from 64.0 GT/s to other speeds.

Known Issues

Important Note:

- Software Automation API users
  Make sure to use the correct binding associated with the Software Release. With each release the binding needs adoption. This is also needed, even if you do not require a new API feature of the release.
    - C# users: take the Interop files fresh from C:\ProgramFiles\Keysight\PCIeAnalysis\Install\Bin\Release
    - Python: re-run "C:\Program Files\Keysight\PCIeAnalysis\Samples\Python\setup-python-for-automation.bat"
    - C++: recompile

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Known Issues – General

- Sometimes, on application startup, an error message “License is not available” appears. In this case, perform a cleanup and restart the application.
- L0p power state is not supported in Gen1 and Gen2.
- After power cycling a module, run the Cleanup utility
  The Cleanup utility is available from Windows Start menu > Keysight PCIe Traffic Analysis > Cleanup
- Link up might not establish when the software GUI for the Analyzer module is launched after the software GUI for the Exerciser module, or if the test setup includes an Endpoint DUT on top of the Analyzer.
  Workaround: First, launch the software GUI for the Analyzer module and then the software GUI for the Exerciser module. You can also select both the Analyzer module and the Exerciser module during the module selection in the Module Setup screen, which will launch the software GUI’s for both the Analyzer and Exerciser in the same window.

Known Issues – Exerciser

- When using 14 bit tag mode, the DUT config scan fails.
- Exerciser might enter an undefined state if powered on before the reference clock is available, or if the reference clock is lost (e.g., due to server reboot or backplane power-off).
  Workaround: To avoid this issue, ensure that the reference clock is active before powering on the Exerciser. If the clock is interrupted, close the GUI → perform cleanup → relaunch GUI to reprogram the FPGA.
  For more details, please refer to the "Exerciser Initialization with Reference Clock Dependency" section in the *Keysight P5500 PCIe and CXL Traffic Analysis User Guide*.

- For P5575A & P5574A Exerciser:
  - Link width is incorrectly defaulting to x16, while the hardware supports only up to x8 or x4.
    Workaround: Please use only with maximum link width the module supports.
  - In Self-Test, two voltages are reported as failing incorrectly.

Known Issues – Analyzer

- Auto Link Width detection not supported in this release.
- Compute on Run feature not supported in this release.
- Non-FLIT mode captures of 16GB might crash the Analyzer GUI.
- Transaction Viewer sometimes aborts computation without results. If part of Compute all, then all computations stop without results. In this case, exclude Transaction Viewer from computations.
- In the event of speed transitions and depending on the speed change time of the devices under test, captures might have the following limitations:
  - Packets might be missing
  - Packets might have bit errors (shown as red)
  - Wrong state transitions might be shown in the LTSSM viewer (transitions to L0)

- LTSSM decoding does not work with SKP OS or any TS filtered
- FLITs might be corrupted on entry to L0. This recovers while staying in L0

Because of the above-listed limitations, some of the states might be missed during Hot Reset or Disable/Enable or Power-up capture.

Workarounds:

- Manual stop when status remains in "Filling Memory"
- Retry LTSSM capture
- Reduce link width
- Capture individual LTSSM state transitions 2.5 GT/s->8.0 GT/s, 8.0 GT/s ->16.0 GT/s, 16.0 GT/s ->32.0 GT/s, 32.0 GT/s ->64.0 GT/s

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Version 1.216.0

Released Date:	April, 2025
Software Version:	1.216.0
Exerciser Requirements	Refer to Hardware Requirements
Analyzer Requirements	Refer to Hardware Requirements
Controller Requirements	Refer to Controller Requirements
License Requirements	Refer to License Requirements

New Features and Enhancements

This release of the P5500 PCIe Traffic Analysis Application introduces the following features and enhancements:

General

- The programming guide " PCIE_Traffic_Analysis_API_Help" now available in PDF format under the following location:
  C:\Program Files\Keysight\PCIeAnalysis\Docs

Exerciser

- Power Management mode now supports the L0p (Downsizing) feature in FLIT mode, with the Hardware Status pane displaying the status of the negotiated link width.
- Virtual Channels now support Merge Credit feature in FLIT mode.
- Auto Equalization feature implemented for 64.0 GT/s data rate in FLIT mode.

Analyzer:

- Link Status viewer implemented, providing real-time monitoring of the PCIe link (upstream and/or downstream) tracked by Analyzer.
- Supports EDSSF adapter for device testing. The Analyzer software enables you to configure the adapter used for device testing in the Lane tab of the Setup dialog.
- Single FLIT Viewer now allows you to customize the layout with color options such as No Color, FLIT Color, Marked TLP Packets, and Colored TLP Packets, available in the Display Option drop-down list.

Test Backplane:

An important fix made around the PERST signal behavior on power-on of the Test Backplane. To get this fix implemented, you must perform a Test Backplane firmware update, followed by a power cycle, before establishing link-up.

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For more details on the Test Backplane Firmware update, please refer to the "Running the Test Backplane Self-Test" section in the *Keysight P5500 PCIe and CXL Traffic Analysis User Guide*.

Fixed Issues

- The P5500 PCIe Traffic Analysis software startup can take up to a few minutes.
- Link up might not establish when the software GUI for the Analyzer module is launched after the software GUI for the Exerciser module.
- Exerciser traffic generation may get stuck when configured with incorrect BAR address.
- Analyzer in LTSSM mode may not decode L0 state correctly. For L0 capturing, use TLP mode.
- The Memory Read Write self-test might fail for the Exerciser module.
- In Analyzer FLIT mode, the TLP packet is not visible in the packet viewer; however, the payload FLIT is observable in the FLIT Viewer at the Gen5 data rate.

Known Issues

- Upon linkup at 64.0 GT/s, it can happen that the Exerciser module only reaches up to 32.0 GT/s. In this case, use the “Initiate Speed Change” button to reattempt switching to 64.0 GT/s
- After power cycling a module, run the Cleanup utility
  The Cleanup utility is available from Windows Start menu > Keysight PCIe Traffic Analysis > Cleanup
- In the event of speed transitions and depending on the speed change time of the devices under test, captures might have the following limitations:
  - Packets might be missing
  - Packets might have bit errors (shown as red)
  - Wrong state transitions might be shown in the LTSSM viewer (transitions to L0)
  - LTSSM decoding does not work with SKP OS or any TS filtered
  - FLITs might be corrupted on entry to L0. This recovers while staying in L0

  Because of the above-listed limitations, some of the states might be missed during Hot Reset or Disable/Enable or Power-up capture.

  Workarounds:
  - Manual stop when status remains in "Filling Memory"
  - Retry LTSSM capture
  - Reduce link width
  - Capture individual LTSSM state transitions 2.5 GT/s->8.0 GT/s, 8.0 GT/s ->16.0 GT/s, 16.0 GT/s ->32.0 GT/s, 32.0 GT/s ->64.0 GT/s
- LTSSM decoding may not work correctly if hardware filters for SKP OS and TS are enabled
- The Voltage Monitor self-tests might sometimes fail for the Exerciser module
- In Exerciser FLIT mode, the Exerciser/DUT Initiates Lower Speed Change LTSSM tests are failing when the link speed transitions from 64.0 GT/s to other speeds

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Version 1.215.0

Released Date:	March, 2025
Software Version:	1.215.0
Exerciser Requirements	Refer to Hardware Requirements
Analyzer Requirements	Refer to Hardware Requirements
Controller Requirements	Refer to Controller Requirements
License Requirements	Refer to License Requirements

New Features and Enhancements

This release of the P5500 PCIe Traffic Analysis Application introduces the following software enhancement:

Analyzer:

- P5570A module now supporting x16 captures:
  - FLIT-Mode x1 to x8: Supports link widths ranging from x1 to x8
  - FLIT-Mode x16 only: Supports only the x16 link width.
    Note: when the actual link traffic is not x16, the FLIT-Mode x1 to x8 must be used.

Known Issues

- The P5500 PCIe Traffic Analysis software startup can take up to a few minutes.
- Upon linkup at 64.0 GT/s, it can happen that the Exerciser module only reaches up to 32.0 GT/s. In this case, use the “Initiate Speed Change” button to reattempt switching to 64.0 GT/s
- After power cycling a module, run the Cleanup utility
  The Cleanup utility is available from Windows Start menu > Keysight PCIe Traffic Analysis > Cleanup
- Link up might not establish when the software GUI for the Analyzer module is launched after the software GUI for the Exerciser module
  Workaround: First, launch the software GUI for the Analyzer module and then the software GUI for the Exerciser module. You can also select both the Analyzer module and the Exerciser module during the module selection in the Module Setup screen, which will launch the software GUI’s for both the Analyzer and Exerciser in the same window.
- In the event of speed transitions and depending on the speed change time of the devices under test, captures might have the following limitations:
  - Packets might be missing
  - Packets might have bit errors (shown as red)

  - Wrong state transitions might be shown in the LTSSM viewer (transitions to L0, Config.LW.Accept)
  - LTSSM decoding does not work with SKP OS or any TS filtered
  - FLITs might be corrupted on entry to L0. This recovers while staying in L0

  Because of the above-listed limitations, it might not be possible to capture complete Hot Reset or Disable/Enable or Power up LTSSM traffic.

  Workarounds:
  - Manual stop when status remains in "Filling Memory"
  - Retry LTSSM capture
  - Reduce link width
  - Capture individual LTSSM state transitions 2.5 GT/s->8.0 GT/s, 8.0 GT/s ->16.0 GT/s, 16.0 GT/s ->32.0 GT/s, 32.0 GT/s ->64.0 GT/s

- Exerciser traffic generation may get stuck when configured with incorrect BAR address
- Analyzer in LTSSM mode may not decode L0 state correctly. For L0 capturing, use TLP mode
- LTSSM decoding may not work correctly if hardware filters for SKP OS and TS are enabled
- The Memory Read Write and Voltage Monitor self-tests might fail for the Exerciser module
- In Exerciser FLIT mode, the Exerciser/DUT Initiates Lower Speed Change LTSSM tests are failing when the link speed transitions from 64.0 GT/s to other speeds
- In Analyzer FLIT mode, the TLP packet is not visible in the packet viewer; however, the payload FLIT is observable in the FLIT Viewer at the Gen5 data rate

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Version 1.214.0

Released Date:	January, 2025
Software Version:	1.214.0
Exerciser Requirements	Refer to Hardware Requirements
Analyzer Requirements	Refer to Hardware Requirements
Controller Requirements	Refer to Controller Requirements
License Requirements	Refer to License Requirements

New Features and Enhancements

This release of the P5500 PCIe Traffic Analysis Application introduces the following features and enhancements:

General:

- The P5500 PCIe Traffic Analysis software now supports both Keysight PCIe 5.0 and PCIe 6 hardware modules.
- The Load File tab in the Module Setup dialog allows you to directly load Traffic Capture (.paans) files.

Analyzer:

- Supports up to x16 link width in Non-FLIT mode and up to x8 link width in FLIT mode.
- Supports capture of power management states (L0s/L1) in Non-FLIT mode.
- Supports auto link width detection feature in Non-FLIT mode.
- New Lane Viewer in FLIT mode allows you to customize the layout according to FLIT Color, ECC Group, Marked TLP Packets, and Colored TLP Packets using the Display Options in the right-click menu.
- FLIT Viewer supports the Lane Viewer column. This column can be added to the FLIT Viewer layout using the Show Column option in the right-click menu of a column header.
- Supports the Bifurcation feature in Non-FLIT mode.
- Improved packet capture and upload speeds.
- Implemented the Compute on Run feature, which allows you to configure auto-compute settings for Transaction Decode, Performance Overview, LTSSM Overview, and Traffic Overview.
- The Capture tab in Non-FLIT mode allows you to select either PCIe5 or PCIe6 spec compliance standard for decoding of captured packets.
- Improved the Export/Import pattern, enhancing usability and performance.
- Improved packet coloring in FLIT mode.

- Improved decoding of the TS0 packets, as bit groups are decoded with half scrambling.

Exerciser:

- Supports up to x16 link width in FLIT mode.
- Enhancements in Python Programming examples.
- FLIT mode supports the transfer of I/O Request and Message Request packets in Single Packet and Block Transfer modes.
- FLIT mode supports cursors for data rates 8.0GT/s, 16.0GT/s, and 32.0GT/s.
- In FLIT mode, trigger out event generates when the LTSSM state transitions out of L0.
- Implemented new layout for the Config Space and DUT Config Space.
- Supports the Bifurcation feature in Non-FLIT mode.
- Improved the Export/Import pattern, enhancing usability and performance.
- Supports Optimized Flow Control in FLIT mode.

Known Issues

- The P5500 PCIe Traffic Analysis software startup can take up to a few minutes.
- Upon linkup at 64.0 GT/s, it can happen that the Exerciser module only reaches up to 32.0 GT/s. In this case, use the “Initiate Speed Change” button to reattempt switching to 64.0 GT/s
- After power cycling a module, run the Cleanup utility
  The Cleanup utility is available from Windows Start menu > Keysight PCIe Traffic Analysis > Cleanup
- Link up might not establish when the software GUI for the Analyzer module is launched after the software GUI for the Exerciser module
  Workaround: First, launch the software GUI for the Analyzer module and then the software GUI for the Exerciser module. You can also select both the Analyzer module and the Exerciser module during the module selection in the Module Setup screen, which will launch the software GUI’s for both the Analyzer and Exerciser in the same window.
- In the event of speed transitions and depending on the speed change time of the devices under test, captures might have the following limitations:
  - Packets might be missing
  - Packets might have bit errors (shown as red)
  - Wrong state transitions might be shown in the LTSSM viewer (transitions to L0, Config.LW.Accept)
  - LTSSM decoding does not work with SKP OS or any TS filtered
  - FLITs might be corrupted on entry to L0. This recovers while staying in L0

  Because of the above-listed limitations, it might not be possible to capture complete Hot Reset or Disable/Enable or Power up LTSSM traffic.

  Workarounds:
  - Manual stop when status remains in "Filling Memory"
  - Retry LTSSM capture

    - Reduce link width
    - Capture individual LTSSM state transitions 2.5 GT/s->8.0 GT/s, 8.0 GT/s ->16.0 GT/s, 16.0 GT/s ->32.0 GT/s, 32.0 GT/s ->64.0 GT/s
- Exerciser traffic generation may get stuck when configured with incorrect BAR address
- Analyzer in LTSSM mode may not decode L0 state correctly. For L0 capturing, use TLP mode
- LTSSM decoding may not work correctly if hardware filters for SKP OS and TS are enabled
- The Memory Read Write and Voltage Monitor self-tests might fail for the Exerciser module
- In Exerciser FLIT mode, the Exerciser/DUT Initiates Lower Speed Change LTSSM tests are failing when the link speed transitions from 64.0 GT/s to other speeds
- In Analyzer FLIT mode, the TLP packet is not visible in the packet viewer; however, the payload FLIT is observable in the FLIT Viewer at the Gen5 data rate
- In Exerciser FLIT mode, the Last DW BE of the Config Read defaults to 0010 instead of 0000

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Version 1.213.0

Released Date:	October, 2024
Software Version:	1.213.0
Exerciser Requirements	Refer to Hardware Requirements
Analyzer Requirements	Refer to Hardware Requirements
Controller Requirements	Refer to Controller Requirements
License Requirements	Refer to License Requirements

Note: While the P5500 PCIe Traffic Analysis software described in this document is likely to be compatible with the Keysight PCIe 5.0 hardware modules (P5551A and P5552A), it is strongly recommended to use the P5500 PCIe 5.0 Traffic Analysis software to work with the PCIe 5.0 hardware. Use the version mentioned in this document with the PCIe 6 hardware (described below) only. New Features and Enhancements

This release of the P5500 PCIe Traffic Analysis Application introduces the following features and enhancements:

- Support for P5570A (Analyzer with x16 link width).
  Note: For this release, the functionality in FLIT mode and Non-FLIT mode is limited to x8 link width.

Known Issues

- The P5500 PCIe Traffic Analysis software startup can take up to a few minutes.
- Upon linkup at 64.0 GT/s, it can happen that the Exerciser module only reaches up to 32.0 GT/s. In this case, use the “Initiate Speed Change” button to reattempt switching to 64.0 GT/s
- After power cycling a module, run the Cleanup utility
  The Cleanup utility is available from Windows Start menu > Keysight PCIe Traffic Analysis > Cleanup
- Link up might not establish when the software GUI for the Analyzer module is launched after the software GUI for the Exerciser module
  Workaround: First, launch the software GUI for the Analyzer module and then the software GUI for the Exerciser module. You can also select both the Analyzer module and the Exerciser module during the module selection in the Module Setup screen, which will launch the software GUI’s for both the Analyzer and Exerciser in the same window.

- In the event of speed transitions and depending on the speed change time of the devices under test, captures might have the following limitations:
    - Packets might be missing
    - Packets might have bit errors (shown as red)
    - Wrong state transitions might be shown in the LTSSM viewer (transitions to L0, Config.LW.Accept)
    - LTSSM decoding does not work with SKP OS or any TS filtered
    - FLITs might be corrupted on entry to L0. This recovers while staying in L0

  Because of the above-listed limitations, it might not be possible to capture complete Hot Reset or Disable/Enable or Power up LTSSM traffic.

  Workarounds:
    - Manual stop when status remains in "Filling Memory"
    - Retry LTSSM capture
    - Reduce link width
    - Capture individual LTSSM state transitions 2.5 GT/s->8.0 GT/s, 8.0 GT/s ->16.0 GT/s, 16.0 GT/s ->32.0 GT/s, 32.0 GT/s ->64.0 GT/s
- Exerciser traffic generation may get stuck when configured with incorrect BAR address
- Analyzer in LTSSM mode may not decode L0 state correctly. For L0 capturing, use TLP mode
- LTSSM decoding may not work correctly if hardware filters for SKP OS and TS are enabled

KEYSIGHT

Version 1.212.0

Released Date:	August 23, 2024
Software Version:	1.212.0
Exerciser Requirements	Refer to Hardware Requirements
Analyzer Requirements	Refer to Hardware Requirements
Controller Requirements	Refer to Controller Requirements
License Requirements	Refer to License Requirements

Note: While the P5500 PCIe Traffic Analysis software described in this document is likely to be compatible with the Keysight PCIe 5.0 hardware modules (P5551A and P5552A), it is strongly recommended to use the P5500 PCIe 5.0 Traffic Analysis software to work with the PCIe 5.0 hardware. Use the version mentioned in this document with the PCIe 6 hardware (described below) only.

New Features and Enhancements

This release of P5500 PCIe Traffic Analysis Application introduces the following Protocol Exerciser and Analyzer features.

- General:
  - Support the storage of all FPGA images, eliminating the need for reprogramming when switching between FLIT-Mode and Non-FLIT-Mode
    Note: Initial update takes longer, as there is a conversion to multi-FPGA storage needed.
- Exerciser Non-FLIT Mode
  - Support of Pre Cursors/Post Cursors in Equalization and Transceiver modes
  - Support of L0s and L1 states in Power Management mode
- Exerciser FLIT-Mode
  - Block Transfer of packets in Single Mode and Continuous Mode
  - Flow control credit updates in the Hardware Status pane under the Flow Control tab
- Analyzer Non-FLIT Mode
  - Performance improvements in Packet and FLIT upload, and processing

- Analyzer FLIT-Mode
    - Support of FLIT Replay scenarios

Known Issues

- The P5500 PCIe Traffic Analysis software startup can take up to a few minutes.
- Upon linkup at 64.0 GT/s, it can happen that the Exerciser module only reaches up to 32.0 GT/s. In this case, use the “Initiate Speed Change” button to reattempt switching to 64.0 GT/s
- After power cycling a module, run the Cleanup utility
  The Cleanup utility is available from Windows Start menu > Keysight PCIe Traffic Analysis > Cleanup
- Link up might not establish when the software GUI for the Analyzer module is launched after the software GUI for the Exerciser module
  Workaround: First, launch the software GUI for the Analyzer module and then the software GUI for the Exerciser module. You can also select both the Analyzer module and the Exerciser module during the module selection in the Module Setup screen, which will launch the software GUI’s for both the Analyzer and Exerciser in the same window.
- In the event of speed transitions and depending on the speed change time of the devices under test, captures might have the following limitations:
    - Packets might be missing
    - Packets might have bit errors (shown as red)
    - Wrong state transitions might be shown in the LTSSM viewer (transitions to L0, Config.LW.Accept)
    - LTSSM decoding does not work with SKP OS or any TS filtered
    - FLITs might be corrupted on entry to L0. This recovers while staying in L0

  Because of the above-listed limitations, it might not be possible to capture complete Hot Reset or Disable/Enable or Power up LTSSM traffic.

  Workarounds:
    - Manual stop when status remains in "Filling Memory"
    - Retry LTSSM capture
    - Reduce link width
    - Capture individual LTSSM state transitions 2.5 GT/s->8.0 GT/s, 8.0 GT/s ->16.0 GT/s, 16.0 GT/s ->32.0 GT/s, 32.0 GT/s ->64.0 GT/s
- Exerciser traffic generation may get stuck when configured with incorrect BAR address
- Analyzer in LTSSM mode may not decode L0 state correctly. For L0 capturing, use TLP mode
- LTSSM decoding may not work correctly if hardware filters for SKP OS and TS are enabled

KEYSIGHT

Version 1.211.0

Released Date:	June 28, 2024
Software Version:	1.211.0
Exerciser Requirements	Refer to Hardware Requirements
Analyzer Requirements	Refer to Hardware Requirements
Controller Requirements	Refer to Controller Requirements
License Requirements	Refer to License Requirements

Note: While the P5500 PCIe Traffic Analysis software described in this document is likely to be compatible with the Keysight PCIe 5.0 hardware modules (P5551A and P5552A), it is strongly recommended to use the P5500 PCIe 5.0 Traffic Analysis software to work with the PCIe 5.0 hardware. Use the version mentioned in this document with the PCIe 6 hardware (described below) only.

New Features

P5573A/P5574A/P5575A PCIe 6 Protocol Exerciser hardware

Keysight Protocol Exerciser for PCI Express (PCIe) provides a test and debug solution for PCI Express to test up to the sixth generation of PCI Express technology. Keysight Protocol Exerciser for PCIe is an advanced traffic generator that you can use to send and respond to the TLP and DLLP packets to stimulate PCIe devices and systems. In addition, it can also test LTSSM state transitions.

P5571A/P5572A PCIe 6 Protocol Analyzer hardware

The P5571A/P5572A PCIe 6 Protocol Analyzer is an advanced traffic analyzer that enables you to capture the incoming traffic from the PCIe devices including the DUT and Protocol Exerciser modules for analysis. The captured traffic can be computed to view decoded transactions and summarized LTSSM information.

P5563B PCIe 6 Test Backplane

The P5563B PCIe 6 Test Backplane is a test platform that primarily supports two x16 slots for PCIe add-in cards. It provides a mechanical fixture to support the add-in cards.

KEYSIGHT

P5500 Traffic Analysis software

The P5500 Traffic Analysis Application enables you to:

- Manage the P5573A/P5574A/P5575A PCIe 6 Protocol Exerciser and the P5571A/P5572A PCIe 6 Protocol Analyzer hardware modules from a single user interface
- Conduct self-tests for the P5573A/P5574A/P5575A, P5571A/P5572A, and P5563B modules before starting the traffic generation and analysis operations
- Update the firmware for the hardware modules

As a software application for the P5573A/P5574A/P5575A Protocol Exerciser, the P5500 PCIe Traffic Analysis Application enables you to:

- Create and manage setup files for Protocol Exerciser
- Create a link between DUT and Protocol Exerciser
- Run LTSSM tests provided to test DUT's LTSSM functions
- View and update the link and Exerciser hardware status
- Define stimulus traffic
- Start the Stimulus and view results
- Perform protocol checks on the incoming traffic

The 1.211.0 version currently supports the following Protocol Exerciser features:

- Up to 64.0 GT/s LTSSM up to x8 linkwidths
- Full Protocol Exerciser functionality as Keysight PCIe 5.0 Protocol Testing solution, for up to 32.0 GT/s speeds, in non-FLIT mode, except Port Bifurcation, Autonomous Equalization, support for low power states, and Lane Margining
- Sending of a single Memory Request (Memory Read/Memory Write) at a time for up to 64.0 GT/s
- Sending of a single Config Request (Config Read/Config Write) at a time for 64.0 GT/s in FLIT Mode
- Exerciser Configuration Space and DUT Configuration Space
- Saving and loading of configuration files
- Supports device-based licensing, which enables the saving of licenses onto the device (hardware module) itself rather than being saved on the controller PC or host PC.

As a software application for the P5571A/P5572A Protocol Analyzer, the P5500 PCIe Traffic Analysis Application enables you to:

- Set the connection and traffic capture options for the Protocol Analyzer
- Set up simple triggers for capturing the incoming traffic
- Capture incoming traffic for analysis
- View incoming traffic using refined filtering and searching techniques
- View LTSSM states, state transitions, and equalization summary
- Compute and view decoded transactions (including Lane Margining traffic decode)

- Compute and view offline performance summary from the captured PCIe data

The 1.211.0 version currently supports the following Protocol Analyzer features:

- Full Protocol Analyzer functionality as Keysight PCIe 5.0 Protocol Testing solution, for up to 32.0 GT/s speeds, in non-FLIT mode, except Port Bifurcation, low power state capturing, and Lane Margining
- It supports device-based licensing, which enables the saving of licenses onto the device (hardware module) itself rather than being saved on the controller PC or host PC.

For up to 64.0 GT/s speeds, x8 linkwidth, in FLIT Mode

- LTSSM state decoding
- Detailed trigger capabilities for Ordered Sets (OSs)
- Capture of DLLPs (UpdateFC, InitFC, and Ack/Nak) using Any DLLP trigger
- Viewing of DLLPs (UpdateFC, InitFC, and Ack/Nak) in Packet Viewer, Header tab, and Details tab
- Capture of TLPs using Any TLP trigger
- Viewing of TLPs in Packet Viewer, Header tab, and Details tab
- FLIT Viewer to visualize FLITs and Ordered Sets, including searching and Filtering and full cross linking to Packet Viewer
- Single FLIT View tab to view specific FLIT selected under the FLITs tab
- With Global Filter, you can avoid storing NOP FLITs or Ordered Sets, reducing the capture memory needed

For more information about these features, refer to the *Keysight P5500 PCIe and CXL Traffic Analysis User Guide*.

Known Issues

- The P5500 PCIe Traffic Analysis software startup can take up to a few minutes.
- Upon linkup at 64 GT/s, it can happen that the Exerciser module only reaches up to 32 GT/s. In this case, use the “Initiate Speed Change” button to reattempt switching to 64 GT/s
- After power cycling a module, run the Cleanup utility
  The Cleanup utility is available from Windows Start menu > Keysight PCIe Traffic Analysis > Cleanup
- Link up might not establish when the software GUI for the Analyzer module is launched after the software GUI for the Exerciser module
  Workaround: First, launch the software GUI for the Analyzer module and then the software GUI for the Exerciser module. You can also select both the Analyzer module and the Exerciser module during the module selection in the Module Setup screen, which will launch the software GUI’s for both the Analyzer and Exerciser in the same window.
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Workarounds:

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- Retry LTSSM capture
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Requirements

Hardware Requirements

Before installing the P5573A/P5574A/P5575A PCIe 6 Exerciser and P5571A/P5572A PCIe 6 Analyzer hardware, carefully study the hardware and environmental specifications and requirements listed in the product Datasheet or the Hardware Guides accompanying this product.

Controller Requirements

The controller system is a computer that hosts the supported PCIe 6 Protocol Exerciser and Protocol Analyzer functionality, including all required software components and hardware support services. The controller system connects to the Exerciser and/or Analyzer card(s) through USB and communicates with the card(s) using protocol Exerciser and Analyzer sessions created in the P5500 PCIe Traffic Analysis software.

The Controller PC must meet the following system requirements:

- Microsoft Windows 11, 64-bit operating system
- Minimum 16 GB RAM (32 GB or higher recommended for optimal performance).
- At least 32 GB free disk space on the C: drive
- USB 3.0 interface for each Exerciser/Analyzer card
- Monitor resolution of 1920 x 1080

License Requirements

The following licenses are required to run the P5500 PCIe Traffic Analysis software:

- P5577PSWA (one for each Exerciser module)

- P5576PSWA (one for each Analyzer module)

Supported license types include device-based, node-locked, transportable, USB portable, and floating licenses

Further, any of the above license types can be installed for these durations: 6 months, 12 months, 24 months, 36 months, or perpetual.

The above licenses can be installed using the Keysight Software Manager Utility that gets installed when you install the P5500 PCIe Traffic Analysis software. For steps on installing the licenses using the Keysight Software Manager Utility, refer to its Online Help.

Installation Steps and Getting Started Information

For installation information for the PCIe 6 Protocol Exerciser and PCIe 6 Protocol Analyzer hardware, refer to the *Keysight PCIe 6 Exerciser and Analyzer Installation Guide* or the respective Hardware Guides for the Protocol Exerciser and Protocol Analyzer modules. For installation information for the P5500 PCIe Traffic Analysis software, refer to *PCIe and CXL Traffic Analysis User Guide*.

Related Documents

For detailed information, refer to the Datasheet or the following documents:

- P557XA_PCIe6_Exerciser_HardwareGuide.pdf
- P557XA_PCIe6_Analyzer_HardwareGuide.pdf
- P5563X_PCIe6_TestBackplane_HardwareGuide.pdf
- PCIe6_Exerciser_Analyzer_Installation_Guide.pdf
- PCIe_and_CXL_Traffic_Analysis_UserGuide.pdf
- PCIe_Traffic_Analysis_API_Online_Help.pdf

These documents are also available at the following location after installation of the P5500 PCIe Traffic Analysis application:

%Program Files%\Keysight\PCIeAnalysis\Docs