M80885RCA DDR5 Receiver Test Application

KEYSIGHT

USER GUIDE

Notices

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https://www.keysight.com/in/en/support/M80885RCA

User Documentation

Our user documentation includes comprehensive information on features that may impact the secure deployment, use, and decommissioning of our products. This includes details on exposed network ports, the use of cryptography and authentication, and firmware security settings, if necessary.

Additional Resources

- Network Security Solutions: Learn how Keysight helps protect your network from threats.
- Creating a More Connected and Secure World: Discover Keysight's commitment to cybersecurity.

Contents

1 Introduction

This chapter provides an introduction to the Keysight M80885RCA DDR5 Receiver Test Application and the related documents that can be consulted to gather more background information.

M80885RCA DDR5 Receiver Test Application—At a Glance

In conformance with the current requirements, DDR5 promises to reduce power consumption and considerably increase bandwidth and capacity in comparison to the earlier generations of DDR SDRAM devices. The DDR5 Full Spec by JEDEC provides a series of guidelines for testing the correct operation and characterization of digital receiver interfaces of DDR5 SDRAM devices including DIMM, DRAM, RCD, Buffer, and Host devices at the physical layer to ensure minimum required performance and interoperability. In particular, the Standard defines the minimum set of requirements for JEDEC compliant 8Gb through 32Gb for x4, x8, and x16 DDR5 SDRAM devices. Keysight's M80885RCA DDR5 Receiver test solution provides the required equipment, test fixtures, and software application to ensure reliable and automated calibration of signal parameters in addition to complete and conformant receiver test procedures. (see Figure 1)

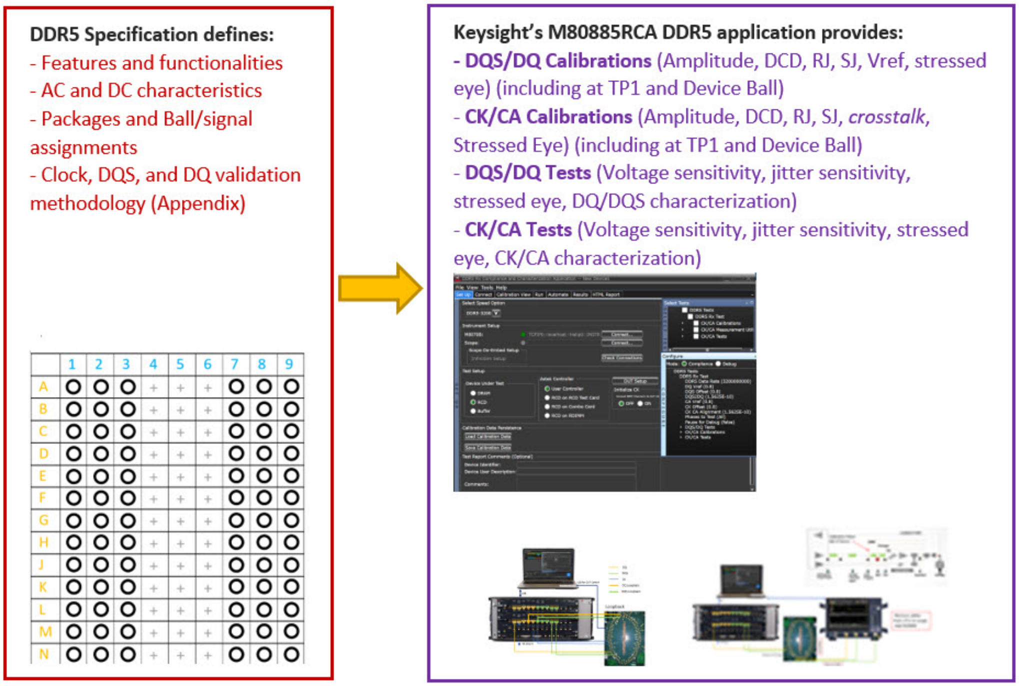


Figure 1 Overview of physical layer compliance tests for a typical DDR5 SDRAM receiver

In particular, the purpose of the receiver testing is to test the receiver sensitivity with a stress signal, whose characteristics are defined by the standard.

M80885RCA DDR5 Receiver Stress Test

M80885RCA DDR5 Receiver Test Application provides a platform for stressed receiver sensitivity test and characterization, which is conformant to standards for DDR5 DUT Testing. The solution consists of several test instruments and fixtures, such as a Bit Error Ratio Tester (BERT), Oscilloscope, Compliance Test Card, and Device Test Card operating together with the M80885RCA software package.

Salient features of the M80885RCA DDR5 Receiver Test Application include:

- Remote control of the main test instrumentation

- Automated calibration following the procedure recommended in the specification
- Automatic and unattended conformance testing and characterization measurements
- Control of a switch matrix hardware to automatically connect the appropriate pin of the DUT to the test equipment
- Quick and easy measurement results to assess the performance of your DUT without expertise in BERT and DDR5 standard
- Support for Data Analytics using *Keysight KS6800A Series Analytics Software*

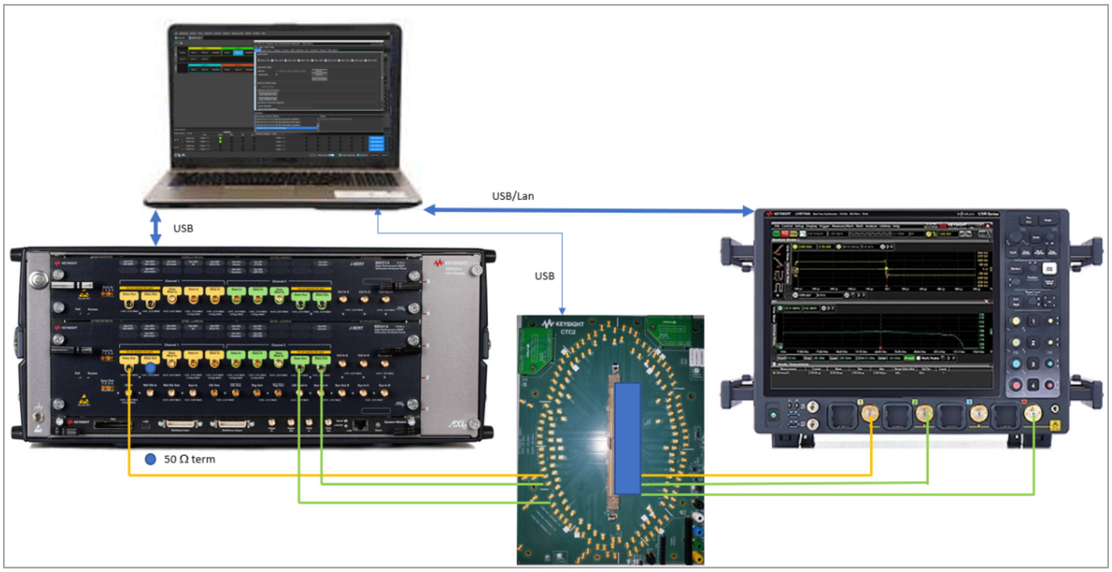


Figure 2 M80885RCA equipment configuration

Applicable Standards

The M80885RCA DDR5 Receiver Test Application supports automated DDR5 receiver tests, based on the following standards:

- DDR5 Full Spec JESD79-5C_v1.30
- DDR5 Registering Clock Driver Definition (DDR5RCD03) - JESD82-513

NOTE MRDIMM and 6 Taps DEFE are yet to be supported by the test application.

System Description

The M80885RCA DDR5 Test Solution consists of:

- M8040A 64 GBaud High-Performance BERT setup: Modules M8045A + M8046A + M8054 installed in M9505A AXIe 5-Slot Chassis
- M8020A J-BERT High-Performance BERT setup: Modules M8041A installed in an M9505A AXIe 5-Slot Chassis
- Real time oscilloscope for signal calibrations
- Test fixtures:
  - CTC2 Board with one slot for the Test card
  - Test card or DIMM
- Power Supplies:
  - RDIMM: 12V, 3.3V, 1.1V (optional)
  - UDIMM: 5V, 5V, 1.1V (optional)
  - Test Fixtures: 1.8V, 1.1V
- The M80885RCA DDR5 Receiver Test Application

Contacting Keysight Technologies

For more information on products, applications or services associated with Keysight Technologies, contact your local Keysight office.

The complete list is available at: www.keysight.com/find/contactus.

2 Installing the M80885RCA DDR5 Receiver Test Application

As a prerequisite for installing the M80885RCA DDR5 Receiver Test Application, you require the necessary hardware and software along with various licenses. This chapter describes these requirements and steps for installing the application.

Hardware and Software Requirements

BERT

- M8040A 64 GBaud High-Performance BERT setup: Modules M8045A + M8046A + M8054 installed in M9505A AXIe 5-Slot Chassis
- M8020A J-BERT High-Performance BERT setup: Modules M8041A installed in an M9505A AXIe 5-Slot Chassis

NOTE

Please note that there are hardware limitations between M8020A and M8040A, which limit the following settings for M8040A:

1. M8020A PG Channel Amplitude is 0-12V, whereas M8040A PG Channel Amplitude is 50mV-900mV.
2. M8040A requires TRIG-OUT to generate DCD.
3. M8040A requires AWG to generate Noise Interference.
4. M8040A requires an external ISI board.

Infiniium Oscilloscope

- Infiniium UXR Series, V-Series or Z-Series (16GHz for testing up to 6400 and 25GHz for testing up to 8800)

Test Fixtures

- CTC2 Board with one slot for the Test Card
- Test Card

CTC2 Board

The CTC2 board provides SMPs for all DDR signals. The board also includes provision for loopback signals for Rx testing. Further, the board includes external 12 V and 3.3 V (VIN_MGMT) power connections and one socket for the test card. The CTC2 test board is connected to the controller PC via USB.

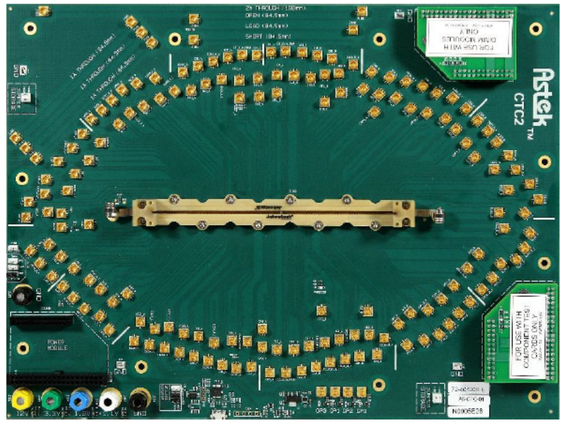


Figure 3 CTC2 Board

Accessories

The following table lists the accessories accompanying the M80885RCA DDR5 Receiver Test solution.

Table 1 Rx Compliance App & Accessories

Product	Description
M80885RCA	DDR5 RX Compliance and Characterization Tests
M8088A-802	Coaxial Cable SMA to SMP 1000 mm matched pair
M8088A-803	Coaxial Cable SMP to SMP 400 mm single cable
	SMA to SMP 80 cm cable
	SMA to SMP 100 cm cable
	SMA-SMP adapters, qty=3
M8046A-804	Matched Cable Pair, 2.4 mm to 2.92 mm, 2 ps match, 40 GHz, Length 914 mm
M8088A-801	Coax Cable SMA to SMP 800mm Matched Pair
M8046A-801	Cable, 2.92 mm (m) to 2.92 mm (m), Length 0.5 m
N1027A-2P2	Microwave Pick-Off Tee 2.4mm connectors, matched pair
11904C	Adapter 2.4 mm male to 2.92 mm female
85138A	Male connector, 2.4mm 50 ohm termination

Shortest cables are recommended.

Controller PC Hardware Requirements

Operating system

- Microsoft Windows 10 (64 bit)

Memory

- 8 GB RAM [minimum]

Monitor Resolution

- WXGA+ (1440 x 900) [minimum]

PC Software Requirements

Keysight IO Libraries Suite (Software)

- Ver. 18.1 or later

M8070B system software for M8000 series

- Ver. 10.5.180.6

M8070ADVB Advanced Measurement Package for M8000 Series

- Ver. 1.11.80.6

Infiniium Oscilloscope software

- Ver. 11.51.00302

MATLAB compiler runtime

- R2017a

PC Interfaces

- USB
- LAN

License Requirements

The M80885RCA DDR5 Receiver Test Application is a BERT compliance test application which requires a valid license installed in Keysight License Manager and an active VISA connection to an M8070B session connected to a M8020A/M8040A 32 or 64 GBaud High-performance BERT with the module licenses shown below installed. For a comprehensive list, refer to the *M80885RCA DDR5 Receiver Test Application - Data Sheet*.

M80885RCA DDR5 Receiver Test Application Configuration

Table 2 License Requirements for M80885RCA

Product	Description
M80885RCA-1xx	M80885RCA DDR5 Receiver Test Application (node-locked, transportable, floating, or USB license)
M80885RCA-TRL	M80885RCA DDR5 Receiver Test Application, 30 days free trial license

Table 3 License Option for M8070B System Software and Platform

Product	Description
M8070A-0TP	System Software for M8000 Series of BER Test Solutions, Transportable, Perpetual License
M8070A-1TP	DUT Control Interface, Transportable, Perpetual License
M8020A-BU2	Bundle consisting of one M9505A 5-slot AXIe chassis with USB

Table 4 on page 22 shows licenses available for M8070ADVB Advanced Measurement Package for M8000 Series:

Table 4 Advanced Measurement Package Licenses

License	Description
M8070ADVB	Advanced Measurement Package for M8000 Series BERT Test Solutions (node-locked license, transportable license, floating (single site) license, or USB portable license)
M8070ADVB-TRL	Advanced Measurement Package for M8000 Series BERT Test Solutions, 30 days free Trial

Table 5 License Options for M8020A and M8041A

Product	Description
M8020A-BU2	Bundle consisting of one M9505A 5-slot AXIe Chassis with USB option
M8041A-C08 or M8041A-C16	BERT one Channel Data Rate up to 8.5 Gb/s or BERT one Channel Data Rate up to 16.2 Gb/s
M8041A-0A2	Second Channel for Analyzer, License
M8041A-0A3	Analyzer Equalization, Module-wide License
M8041A-0G2	Second Channel for Pattern Generator, License
M8041A-0G3	Advanced Jitter Sources for Receiver Characterization, Module-wide License
M8041A-0G4	Multi-tap De-emphasis, Module Wide License
M8041A-0G5	Adjustable Intersymbol Interference (ISI), Module Wide License
M8041A-0G6	Reference Clock Input with Multiplying PLL, Clockgroup-wide L=icense
M8041A-0G7	Advanced Interference Sources for Receiver Characterization, Module-wide License

Table 6 License Options for M8040A

Product	Description
M8040A-BU2	High-performance BERT 64 Gbaud
M8057A/B	Remote Head
M8045A-G32	Pattern generator one channel NRZ, data rate up to 32 Gbaud
M8045A-0G2	Second Channel, hardware and license
M8045A-0G3	Advanced jitter sources for receiver characterization, module-wide license
M8045A-0G4	De-emphasis, module-wide license
M8046A-A32	Analyzer (error detector)
M8049A-002	External ISI board
M8054A	External level interference sources RI/SI

Table 7 License Options for the Infiniium Oscilloscope

License	Description
D9020JITA	EZJIT Complete - Jitter and Vertical Noise Analysis Software for V/Z/UXR-Series
N8823X-1XX	EZJIT Complete Vertical Noise Analysis Software
D9010DMBA	De-embedding Software (Precision Probe, InfiniiSim Basic)
D9020ASIA	Advanced Signal Integrity Software (EQ, InfiniiSimAdv, Crosstalk)
N5465X-1XX	InfiniiSim Advanced Software
D9020ASIA	Advanced Signal Integrity Software (EQ, InfiniiSimAdv, Crosstalk)
N5461X-1XX	Equalization Emulation Software
E2688X-1XX, N5384A	High-speed SDA and Clock Recovery

You can install the required licenses for the M80885RCA DDR5 application using Keysight License Manager.

Keysight License Manager

Keysight License Manager is a software utility that enables end users to easily manage right-to-use licenses for software and hardware capabilities on Keysight instruments or systems. The graphical user interface (GUI) gives you a visual representation of the licenses installed on your Keysight Technologies systems and provides access to the following features:

- View the licenses installed on a system
- Install licenses for new capabilities
- Transport licenses from one controller to another
- Borrow the licenses
- Remove licenses for capabilities no longer needed

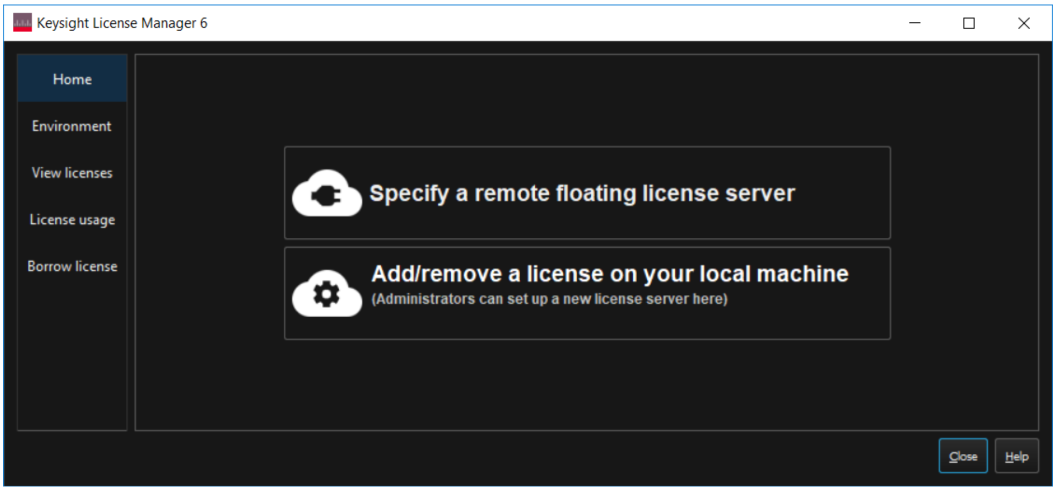
For detailed information on **Keysight License Manager**, refer to the *Keysight License Manager Help*. You can access the *Keysight License Manager Help* from the **Keysight License Manager** web page: http://www.keysight.com/find/LicenseManager

NOTE Please note that the Keysight License Manager 6 and Keysight License Manager 5 are installed on your system when you install M80885RCA software.

There are two versions of Keysight License Manager, which can be used to manage the licenses:

Keysight License Manager 6

This license management application allows you to manage floating and USB portable licenses for a variety of software products and instruments.



USB portable licenses:	Install, view, delete
Floating licenses:	Install, view, delete, borrow, and configure license server

You can use the Keysight License Manager 6 to configure remote license servers for sharing licenses across a network, or to configure a local license server (used with certain types of node-locked licenses) on the computer or instrument where your Keysight software is installed.

Although, the Keysight License Manager 6 is installed on your system when you install the M80885RCA DDR5 software, however, you can download it at: Keysight License Manager 6.

Keysight License Manager 5

This license management application allows you to manage node-locked and transportable licenses for a variety of software products and instruments.

Node-locked licenses:	Install, view, delete
Transportable licenses:	Install, view, delete, and transport

Although, the Keysight License Manager 5 is installed on your system when you install the M80885RCA DDR5 software, however, you can download it at: Keysight License Manager 5.

Installing the Licenses

Adding License using Keysight License Manager 6

Adding a Floating License

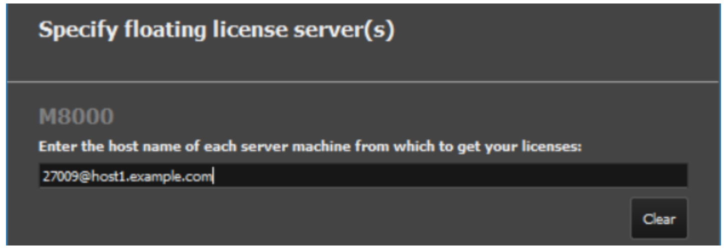
1 On the license server machine, start **Keysight License Manager 6** from your computer's **Start** screen or **Start** menu.
2 Click **Add a license to your local machine**.
3 Select **Add a license to this floating license server**.
4 In the **Add (install) a license window**, click **Browse...** and browse to the location of your license file. You can repeat this as many times as needed to install all your licenses.
5 If you want the license server process to start automatically each time the server machine is restarted, make sure that **Automatically start license server after every reboot** is selected.

For more information, you can also refer the *Keysight Licensing Administrator's Guide*:
https://literature.cdn.keysight.com/litweb/pdf/5951-5739.pdf

Specify remote license servers

To tell your Keysight product where to get its floating (network) licenses, do the following.

1 From the **Keysight License Manager 6** home screen, click Specify remote license server(s).
2 If you did not run **License Manager** from a menu in a Keysight product, you will see a product selection dialog box. Select the product to be licensed from the drop-down list.
3 In the **License Setup Wizard** for <Product Name> dialog box, type in the port_number@host_name of each server. If you have more than one server, separate them with semicolons (;). For example:



4 Once you've entered your server name(s), click **Next** to complete your setup.

Adding a USB License

Before adding a USB license, you must ensure that:

- Your Keysight product software is installed on this machine.
- You have a license file on this machine. If you don't have a license file, go to **Keysight Software Manager** to get one.
- If your license is locked to a dongle (USB key) rather than to a host ID:
  - The dongle driver is installed on this machine. To install:
    - Run Setup64.exe and accept the defaults.
    - Get the FLEXID10 USB Dongle Driver from http://www.keysight.com/find/LicensingUsbDriver.
    - Extract the .zip file to this machine.
  - The dongle is connected to a USB port on this machine.

To license a Keysight product for use on this machine, select the product from the drop-down menu. Once you have selected your product, browse to the license file, then click **Next** to add the license.

Counted node-locked or USB portable licenses require a license server process: your local machine is both server and client for this license type. If your local machine was not already running a license server process, that process will be started when you click **Next** to complete the operation. To make sure the server process starts automatically each time you reboot the machine, ensure that **Automatically start license server after every reboot** is selected.

For more information, you can also refer the *Keysight Licensing Administrator's Guide*: https://literature.cdn.keysight.com/litweb/pdf/5951-5739.pdf

Adding License using Keysight License Manager 5

Adding a Node-Locked License

You can add a license to your system by installing a license (*.lic) file if you receive one from Keysight.

1 Select the > **Install License File...** menu option. This displays a Windows file selection window.

2 Use the file window to browse to and select the license file (<filename>.lic) that you want to add.

3 Click **Open**. License Manager automatically installs the license file in the folder and notifies you with a pop-up that the license has been stored in your license directory. The license now appears on the main license view.

For more information, you can also refer the *Keysight Licensing Administrator's Guide*: https://literature.cdn.keysight.com/litweb/pdf/5951-5739.pdf

Transporting a License

Transportable licenses are licenses that can be moved from one host controller to another using the **Keysight License Manager**.

1 Start the **Keysight License Manager** by double clicking the **Keysight License Notifier** icon or click **Start** > **(All) Programs** > **Keysight License Manager** > **Keysight License Manager**.

2 In the **Keysight License Manager**, click on **Help** > **Keysight License Manager Help** and perform the procedure in the **Transporting Licenses** help topic.

3 Additionally, you can also refer the *Keysight Licensing Administrator's Guide*: https://literature.cdn.keysight.com/litweb/pdf/5951-5739.pdf

Installing the Software

The installer for the M80885RCA DDR5 Receiver Test Application can be downloaded from the Keysight website.

To install the M80885RCA DDR5 Receiver Test Application, perform the following steps:

1. Double-click the downloaded installer file on your PC. If your computer does not have Keysight License Manager 5.3 or 6.0 installed, the M80885RCA DDR5 installer prompts you to install it as a requirement.
2. Click **Install** to install Keysight License Manager (if not already available on your machine). After the installation of Keysight License Manager is finished, the installation of M80885RCA software is resumed. The following screen is displayed.

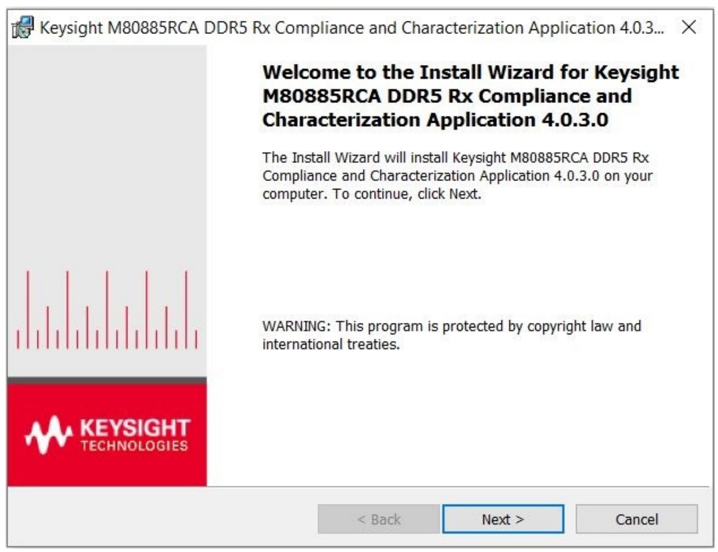


Figure 4 Welcome screen

NOTE The installer version displayed on your **Welcome** screen will depend on the version of the M80885RCA software you have downloaded from the Keysight website.

3 Click **Next**. The **Keysight Software End-User License Agreement** window is displayed.

4 Select **Agree** to agree to the license agreement and to enable the **Next** button.

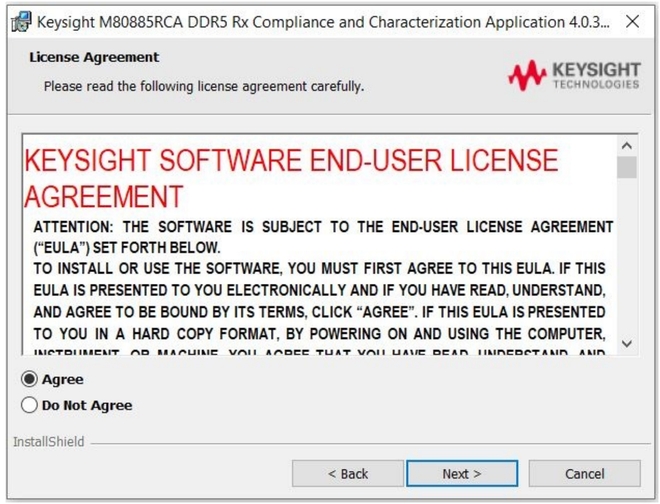


Figure 5 License Agreement window

5 Click **Install**.

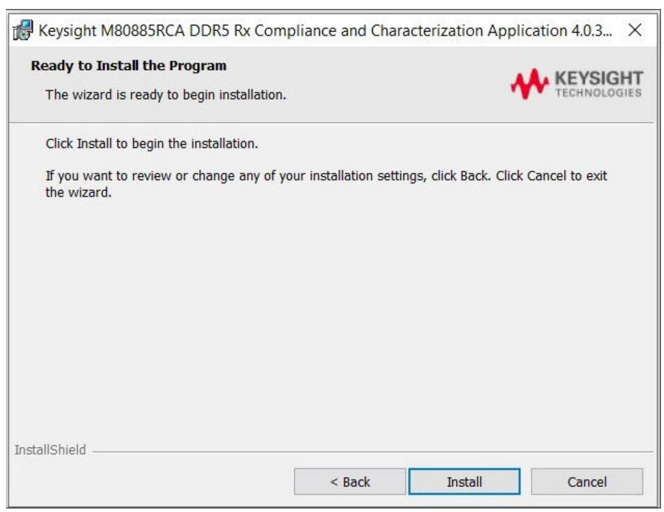


Figure 6 Ready to install window

6 Once the installation of the M80885RCA DDR5 Receiver Test Application begins, its status is displayed.

7 Once the installation is complete, the following window is displayed. Click **Finish** to complete the installation and exit the wizard.

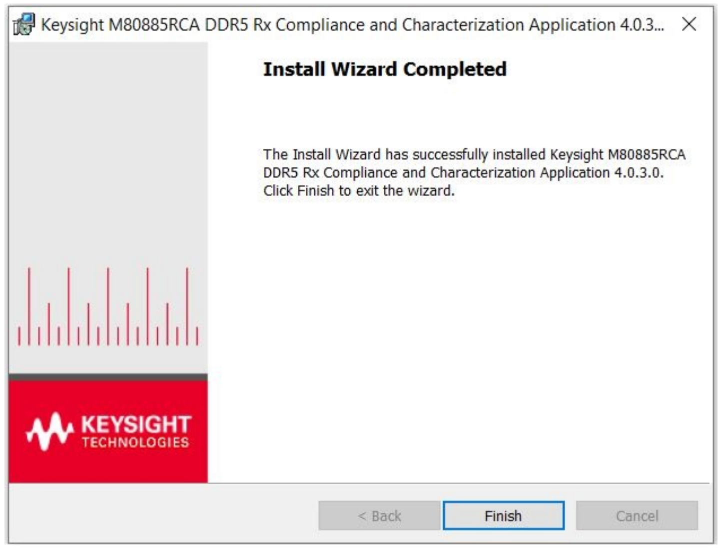


Figure 7 Window indicating end of installation

3 Using the M80885RCA Software

As a prerequisite for using the M80885RCA software, ensure that all the required instruments are defined in the *Keysight Connection Expert* on the PC, where the Keysight M80885RCA DDR5 Receiver Test Application is installed.

Software Concept and Flow of DDR5 Receiver Test

The Keysight M80885RCA DDR5 Receiver Test Application controls the complete hardware required to perform an automated stressed signal calibration and system performance test in accordance with the specification.

The software is based on a generic framework that already supports a wide range of automated compliance test applications for electrical transmission standards, such as, OIF CEI, XAUI, CAUI and many others.

The workflow of a generic compliance test application consists of five basic steps, which are explained in detail in this chapter.

The following table briefly explains each of these steps in the workflow.

Step	Description
Set Up	Select speed option to be tested and specify instrument connection settings, switch matrix setup, scope de-embedding settings, test (DUT and controller) settings, and for loading/saving calibration data
Select Tests	Select calibrations and tests to be run
Configure	Adjust specific test settings (in compliance or debug mode)
Connect	Check the actual hardware connection with the provided reference diagram
Run Test	Run the selected tests (either once or multiple times)

The Keysight M80885RCA DDR5 Receiver Test Application offers different measurement and calibration functions to perform a full DDR5 receiver compliance test in accordance with the specification. The following table lists the calibrations and other tests offered by the application.

<table>
<tr><th>Calibrations</th><th>Measurement Utilities</th><th>Tests</th></tr>
<tr><td>DQS/DQ Calibrations for Sensitivity
- DQS2DQ Skew Calibration
- DQ Amplitude Calibration
- DQ Vref Calibration
- DQS Amplitude Calibration
- DQS (Trig Out) Amplitude Calibration (only available with M8040A setup)
- DQS DCD Calibration
- DQS RJ Calibration

DQS/DQ Stressed-eye Calibrations
- DQ Amplitude at TP1 Calibration
- DQ RJ at TP1 Calibration
- DQ SJ at TP1 Calibration
- DQ Noise at TP1 Calibration (only available with M8040A setup)
- DQ Vref at Device Ball for TP1 Calibration
- DQ Stressed Eye Calibration</td><td>DQS/DQ Measurement Utilities
- DQS2DQ and DQ Vref Optimization</td><td>DQS/DQ Tests
- DQS Voltage Sensitivity Test
- DQS Jitter Sensitivity Test
- DQ Voltage Sensitivity Test
- DQS2DQ Test

Stressed Eye
- Rx Stressed Eye End to End Test (TP1 cal)

DQ/DQS Characterization
- DFE Characterization Tap1
- DFE Characterization Tap2
- DFE Characterization Tap3
- DFE Characterization Tap4</td></tr>
<tr><td>CK/CA Calibrations for Sensitivity
- CK Amplitude Calibration
- CA Amplitude Calibration
- CA Vref Calibration
- CK (Trig Out) Amplitude Calibration (only available with M8040A setup)
- CK DCD Calibration
- CK RJ Calibration

CK/CA Calibrations at TP1
- CA Amplitude at TP1 Calibration
- CA RJ at TP1 Calibration
- CA SJ at TP1 Calibration
- CA Noise at TP1 Calibration (only available with M8040A setup)
- CA Vref at Device Ball for TP1 Calibration
- CA Stressed Eye at Device for TP1 Calibration</td><td>CK/CA Measurement Utilities
- CK to CA and CA Vref Optimization</td><td>CK/CA Tests
- CA Voltage Sensitivity Test
- CK Voltage Sensitivity Test
- CK Jitter Sensitivity Test

Stressed Eye End to End Test
- CA Rx Stressed Eye End to End Test (TP1 cal)</td></tr>
</table>

Starting the M80885RCA DDR5 Receiver Test Application

The M80885RCA DDR5 Receiver Test Application is available to be run as a standalone application on a PC, and either connecting locally or remotely to the hardware setup.

Before you launch the M80885RCA DDR5 Receiver Test Application, make sure that the following software is running and online:

- Keysight M8070B software to connect to M8020A/M8040A High-performance BERT

Ensure that proper connections with the testing instruments are established. Ensure that the measurement instruments are connected on the same LAN as the remote PC, where the M80885RCA DDR5 Receiver Test Application is installed.

To access the M80885RCA DDR5 Receiver Test Application, perform the following steps:

1 From the **Start** menu of the Windows 10 Operating System, select **Keysight M8070B Applications > Launch Keysight M80885RCA**. Alternatively, type **M80885RCA** in the Windows search box to locate the application.

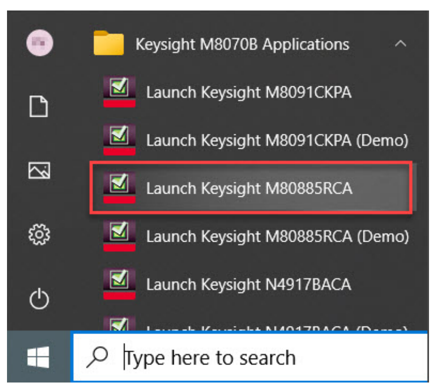


Figure 8 Launching the M80885RCA DDR5 Rx Test Application

NOTE

If you do not see the required entries on the **Start** menu, the M80885RCA DDR5 Receiver Test Application has not yet been installed on the PC.

Refer to "Installing the Software" on page 29 for installation instructions.

- If you are launching the Keysight M80885RCA DDR5 Receiver Test Application for the first time, the End-User License Agreement window appears. Select **Agree** to continue.
- The M80885RCA DDR5 Receiver Test Application banner is displayed.
- If there is a single instance of the M8070B software running locally, the M80885RCA DDR5 Receiver Test Application launches after automatically getting connected to the M8070B software.
- If the M80885RCA DDR5 Receiver Test Application does not detect any instance of the M8070B software running locally, the **Connect to M8070B System Software** window appears.

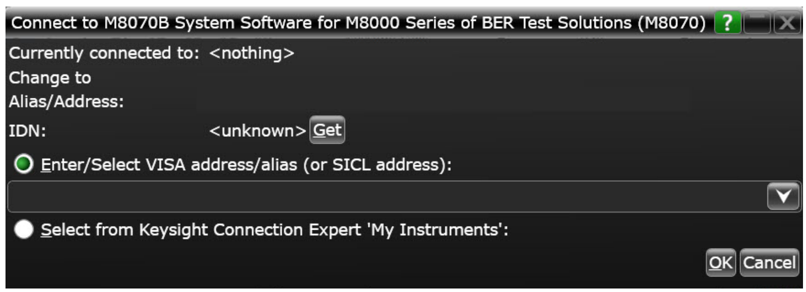


Figure 9 Connecting to M8070B System Software for M8000 Series of BERT Test Solutions (M8070)

2 Perform one of the following actions:

- In the **Enter/Select VISA address/alias (or SICL address):** text field, you can either type or copy the VISA/SICL address directly from the Keysight M8070B software and paste it here. To verify the correct VISA address to connect to M8070B, access the **SCPI Server Information** window by clicking **Utilities > SCPI Server Information...** from the main menu of the Keysight M8070B software.

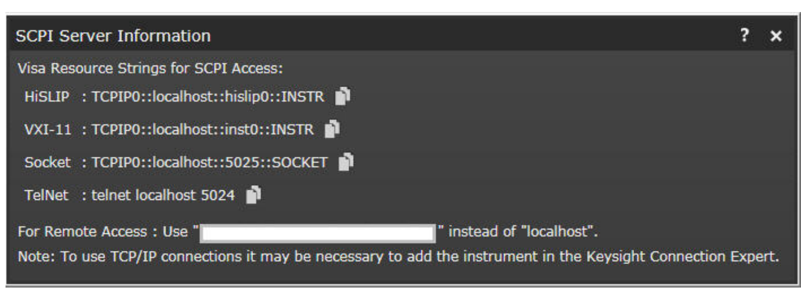


Figure 10 SCPI Server Information window on the M8070B Software

- If the BERT device is online and defined in the *Keysight Connection Expert*, click **Select from Keysight Connection Expert favorites:**. The VISA address list defined in the Keysight Connection Expert software for each online instrument is displayed. After you verify the VISA/SICL address, select the correct VISA Address from the list.

3 Click **Get** on the **Connect to M8070B System Software** window. The **IDN:** field displays the instrument name.

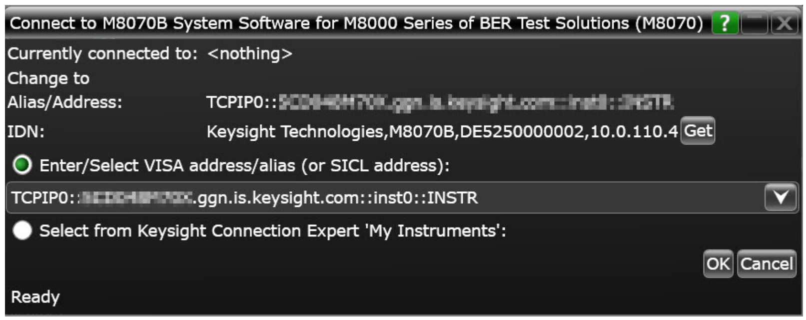
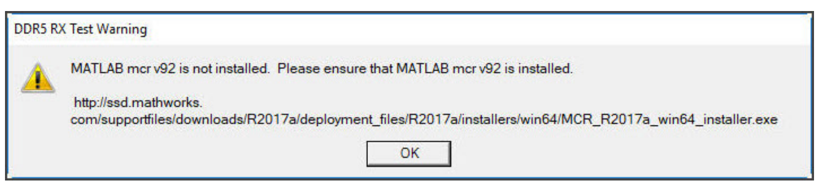


Figure 11 IDN field displaying successful connection to M8070B

4 Click **OK** to establish connection with M8070B and to launch the M80885RCA DDR5 Receiver Test Application. If the connection cannot be established, the application start will be aborted.

5 If a connection is established with M8070B, the M80885RCA DDR5 test application checks for the availability of MATLAB R2017a. If not found, the following message is displayed. The application launch, however, is resumed after clicking the **OK** button.



6 When the application starts successfully it will start with the default layout and will show the **Set Up** tab.

NOTE

The **Message** tab will show info, warning and error messages while running the M80885RCA DDR5 application as well as intermediate results of measurements. Scroll up and down to display relevant messages.

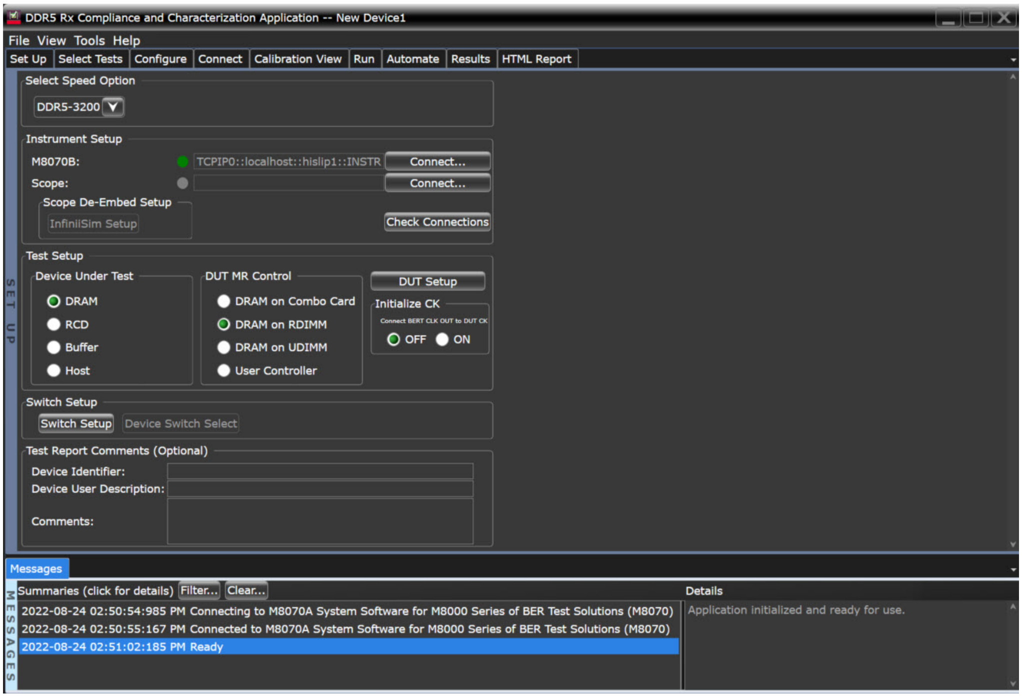


Figure 12 Default view of the M80885RCA DDR5 Receiver Test Application

NOTE

The application framework enables you to use docking and floating windows, so the GUI can be customized to meet your requirements. If you want to reset the GUI to its default layout, select **View > Reset > Tab Layout** in the application menu.

For more information on how to use the various features in the M80885RCA DDR5 Receiver Test Application, refer to the *Keysight M80885RCA DDR5 Receiver Test Application Online Help*.

Set Up tab - Setting up the M80885RCA DDR5 Receiver Test Application

Before you start any calibrations or receiver testing with the M80885RCA DDR5 application, you must set up the application first.

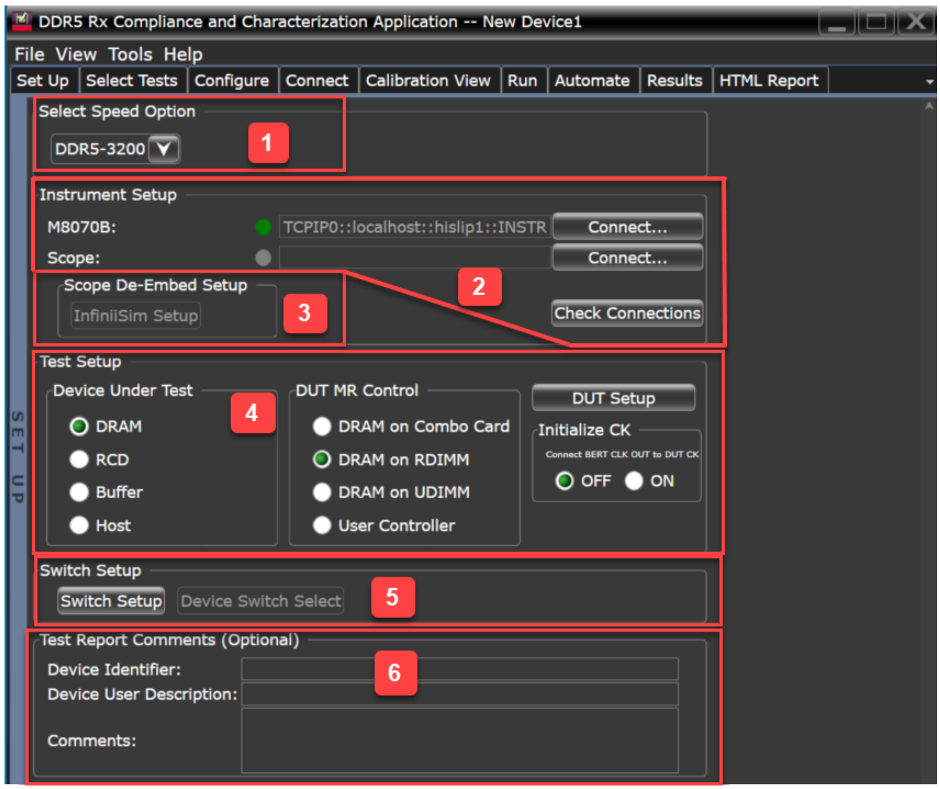


Figure 13 Setting up the M80885RCA DDR5 Receiver Test Application

Under the **Set Up** tab,

1 In the **Speed Option** area, select one out of these options - **DDR5-3200, DDR5-3600, DDR5-4000, DDR5-4400, DDR5-4800, DDR5-5200, DDR5-5600, DDR5-6000, DDR5-6400, DDR5-6800, DDR5-7200, DDR5-7600, DDR5-8000, DDR5-8400, or DDR5-8800** to indicate the speed grade in conformance with the industry standards.

   By default, **DDR5-3200** is selected for M8020A BERT and **DDR5-5200** is selected for M8040A BERT.

2 In the **Instrument Setup** area, specify the VISA/SICL address for the following instruments:

- M8070B
- Oscilloscope

NOTE In the Infiniium software, go to **Utilities > Remote** to retrieve information related to the instrument address.

3 In the **Scope De-Embed Setup** area, specify the InfiniiSim setup details. InfiniiSim enables you to de-embed test fixtures or cables or switch networks that are placed between the Oscilloscope and the device to be measured. For more information about setting up InfiniiSim, refer to the *Keysight M80885RCA DDR5 Receiver Test Application Online Help*.

4 In the **Test Setup** area:

- The **Device Under Test** area enables you to select the type of DUT to be tested. The available options include **DRAM**, **RCD**, **Buffer,** and **Host**. Based on the selection made, the application makes some configurations automatically for the user.

- The **DUT MR Control** area enables you to select the method to be used to control the DUT (DRAM, RCD, and Buffer). Based on the selected DUT, the available controller options include:

Device Under Test	DUT MR Control
DRAM	DRAM on Combo Card DRAM on RDIMM DRAM on UDIMM User Controller
RCD	RCD on MRDIMM (draft) RCD on RCD Test Card RCD on Combo Card RCD on RDIMM User Controller
Buffer	Buffer on MRDIMM (draft) Buffer on Buffer Test Card Buffer on Combo Card User Controller

If the **User Controller** controller option is selected, the user is responsible to control the DUT to perform the tasks, such as reset, initialize, and put into loopback. The other controller options provide automated control.

NOTE

There are two USB connections to control the UDIMM. The first to the CTC2, the second to the controller board. The USB connection to the CTC2 must be at the highest USB address. USB talks to the highest address first. To verify the addresses of the connection, go to the Windows device manager. Under “Universal Serial Bus controllers”, the CTC2 will be listed as a “USB Composite Device”. View the properties and plug the CTC2 connection into the highest port.

NOTE

The Multiplexed Rank Dual Inline Memory Module (MRDIMM) is an emerging form factor being developed in JEDEC. This design leverages design elements from a LRDIMM and RDIMM to achieve high system performance. The test procedure including device initialization, power sequencing, calibration, and test process is still under development.

- The **Host Setup** area: When the **Host** DUT is selected in the **Device Under Test** area, the **Host Setup** area displays. This area enables users to select the Loopback rate. For Host DUT, user must select loopback rate and initialize the device.The available Loopback rate options include:

Device Under Test	Host Setup
Host	Full-Rate Loopback Half-Rate Loopback Quarter-Rate Loopback

- Click the **DUT Setup** button to specify the DUT specific characteristics including DIMM channel, DRAM location, DQ, and CA. The setup information to be provided varies for the various supported DUT/Controller combinations.
- The **Initialize CK** area enables you to connect and enable CLK OUT when DRAM, Buffer, or Channel 2 for RCD DUT is selected. This signal can be used for continuous CLK control from the DUT.

5 In the **Switch Setup** area, click the **Switch Setup** button to set up your switch matrix hardware.

6 The **Test Report Comments (Optional)** area enables you to define an identifier for the DUT and add an associated description and comments. Defining these characteristics is optional. However, it is helpful when running tests on multiple DUTs where you may identify and relate the test results by looking up for the Device Identifier name in the generated HTML test reports.

Configuring Switch Matrix

NOTE In the current version of the M80885RCA test application, the Switch Matrix feature is only supported by the DRAM “Device Under Test”.

Switch Matrix – Overview

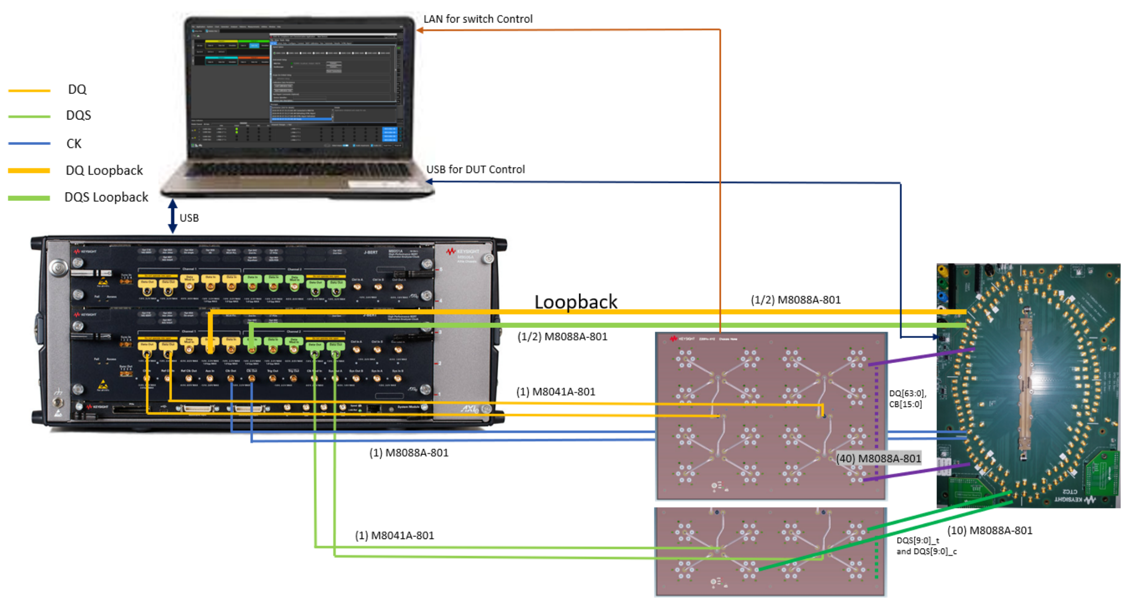
An M8041A and M8045A module have only two channels to run tests. The limited number of channels may, at times, limit the testing of an RDIMM DUT, which has multiple pins. The Switch Matrix feature enables you to overcome this limitation.

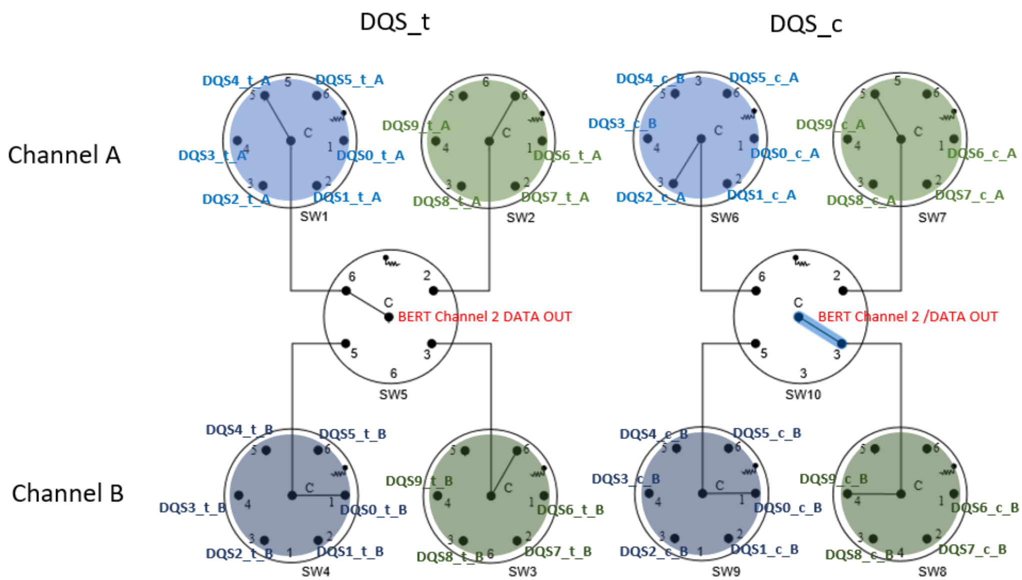
The purpose of the 'Switch Matrix' feature is to ease the testing procedure, make it more feasible and to reduce the overall time. Using this feature, you can connect the four DATA OUTs (two DATA OUTs and two /DATA OUTs) to a switch that can then route the input signals to the appropriate pins of the RDIMM DUT. The switch matrix takes care of obtaining an accurate signal path, whenever required, based on the configurations made in the switch setup dialog.

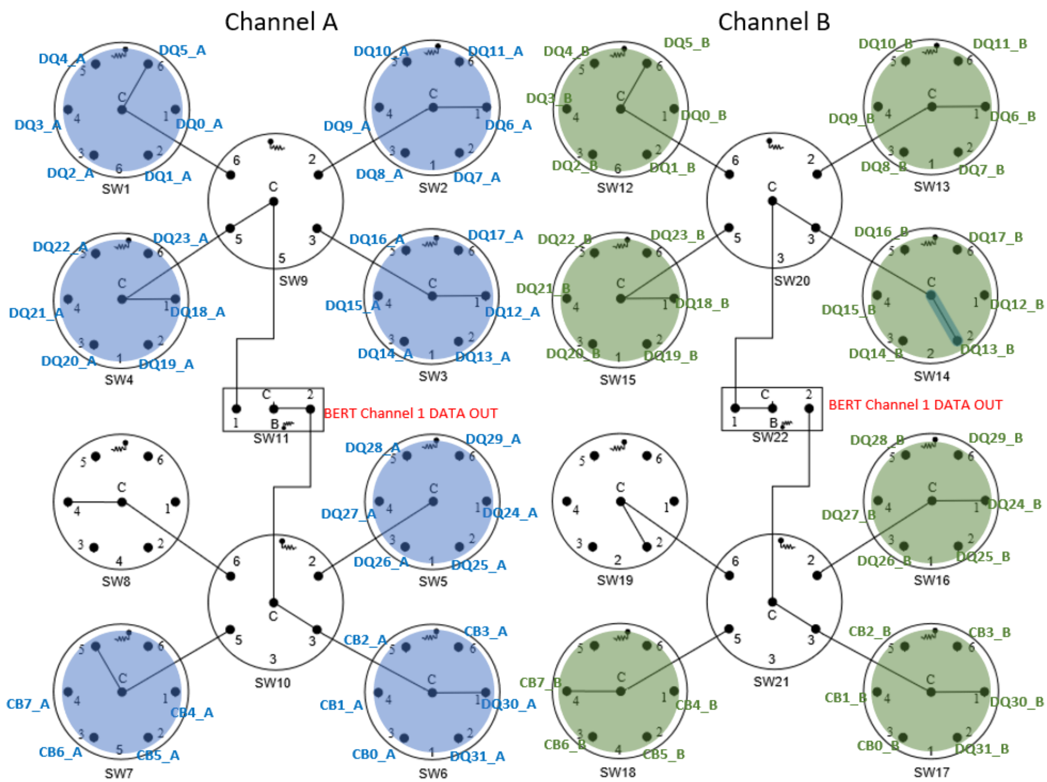
Keysight recommends the following switches to be used with the Test Application:

- Keysight L8990C-00U
- Keysight L8990C-014

The following figures illustrate the physical connections when a switch is used.




DQS_t
DQS_c
Channel A
Channel B
DQS4_t_A
DQS5_t_A
DQS3_t_A
DQS0_t_A
DQS2_t_A
DQS1_t_A
SW1
DQS9_t_A
DQS6_t_A
DQS8_t_A
DQS7_t_A
SW2
DQS4_c_B
DQS5_c_A
DQS3_c_B
DQS0_c_A
DQS2_c_A
DQS1_c_A
SW6
DQS9_c_A
DQS6_c_A
DQS8_c_A
DQS7_c_A
SW7
BERT Channel 2 DATA OUT
SW5
BERT Channel 2 /DATA OUT
SW10
DQS4_t_B
DQS5_t_B
DQS3_t_B
DQS0_t_B
DQS2_t_B
DQS1_t_B
SW4
DQS9_t_B
DQS6_t_B
DQS8_t_B
DQS7_t_B
SW3
DQS4_c_B
DQS5_c_B
DQS3_c_B
DQS0_c_B
DQS2_c_B
DQS1_c_B
SW9
DQS9_c_B
DQS6_c_B
DQS8_c_B
DQS7_c_B
SW8



Initial Switch Setup

Perform the following initial steps to set up the switch.

1 Make a direct connection from one switch to a PC.

2 Turn on the switch.

3 When the LAN LED turns green, go to a web browser and type the default IP address 169.254.44.88 (check with switch user manual to verify the default IP address).

4 Click the **Configure LAN** tab.

5 Click **Edit**.

6 Change all the options to auto settings.

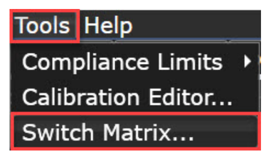
7 Assign a unique hostname.

8 Click **Submit**.
9 Wait for the web page to update and state that it cannot connect to the original IP address.
10 Reboot the switch.
11 In a web browser, type <hostname>/ to verify that the switch did take on the new hostname properly.
12 If the switch does not connect, press the **LAN reset** button and repeat steps 2-11. If it does, continue to the next step.
13 Go to the **Keysight Connection Expert** and add the switch using the hostname that was assigned to the switch.
14 Repeat the above steps for the second switch.

To enable Switch Matrix

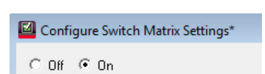
To enable the switch matrix feature:

1 Click **Tools > Switch Matrix...**.



Alternatively, click the **Switch Setup** button under the **Set Up** tab.

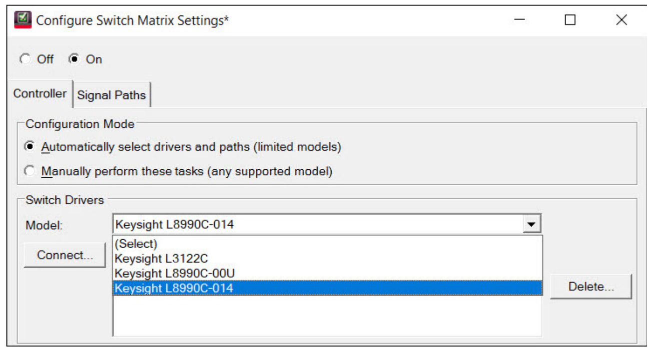
2 In the **Configure Switch Matrix Settings** dialog box, click **On** to enable the Switch Matrix feature. Enabling the Switch Matrix feature enables the automated switch control.



Establishing connection to the Switch Drivers - Automatically

In the **Configure Switch Matrix Settings** dialog, under the **Controller** tab:

1 Navigate to the **Switch Drivers** section and select the switch model.



2 Click the **Connect** button to be able to connect the selected switch driver to a physical switch instrument.

3 A Connect to <switch-model> dialog appears, which enables you to establish a connection to the selected switch models.

Establishing connection to the Switch Drivers - Manually

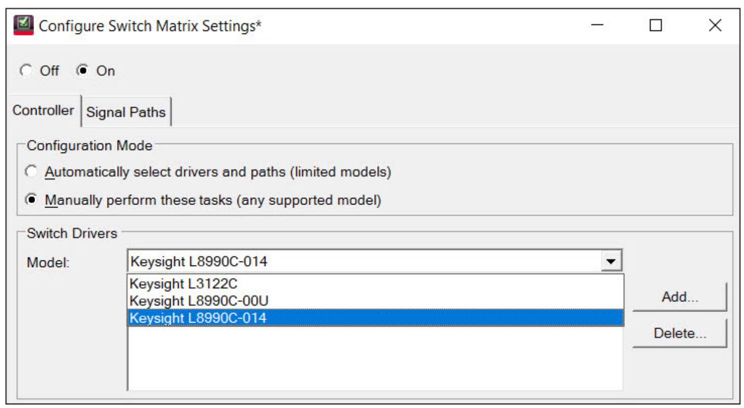
The **Manually perform these tasks (any supported model)** option allows you to decide how many drivers to use and how to route the signal paths.

It enables the use of any supported switch model.

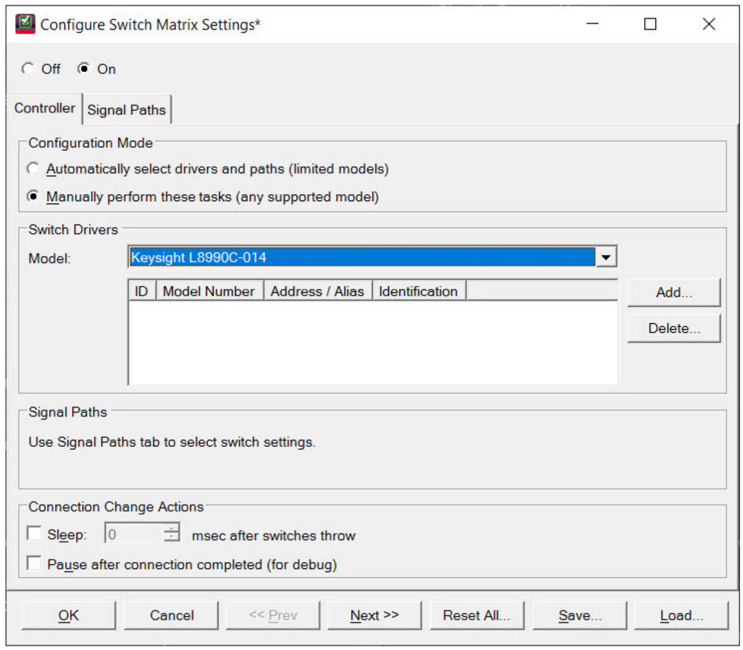
In the **Configure Switch Matrix Settings** dialog, under the **Controller** tab:

1 Select the **Manually perform these tasks (any supported model)** radio button in the **Configuration Mode** section.

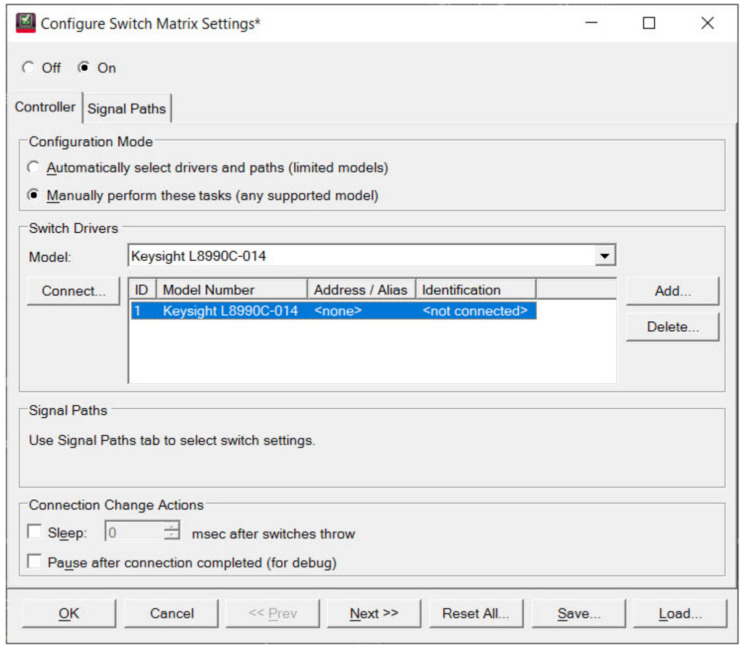
2 In the **Switch Drivers** section, please select the switch model from the **Model:** drop-down options.



3 You may use the **Add** button to append the list of any additional drivers, which require a connection to an instrument. Use the **Delete** button to remove a selected driver from the list. Removing the driver from the list dissociates any signal paths that may have been assigned to it earlier.



4 When you click the **Add...** button, the **Connect...** button appears so that you can establish connectivity to the selected Switch.



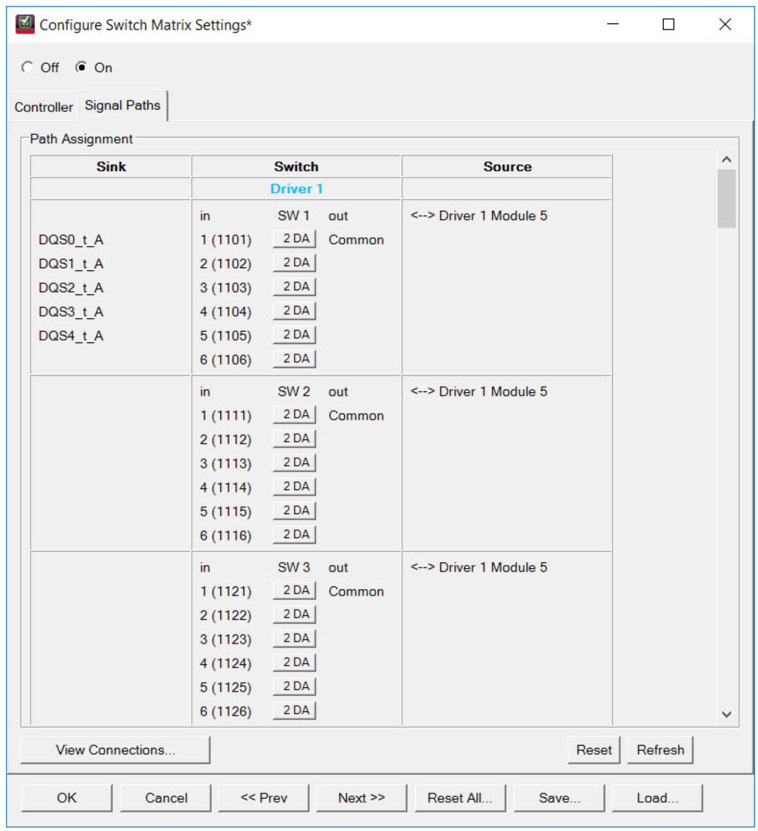
5 The rest of the steps for establishing a connection to the switch models remain the same as described in the previous section. The only difference between automatic and manual modes is that you can add/delete and select switch drivers (any supported model) as per your requirements and preferences in the manual mode.

Configuring Signal Paths - Automatically

Once you have enabled the Switch Matrix feature and set up connections to the switch drivers, you must configure signal paths. Perform the following steps:

1 Ensure that **Configuration Mode** is set to **Automatically** select drivers and paths (limited models).

2 Click the **Signal Paths** tab in the **Configure Switch Matrix Settings** dialog.

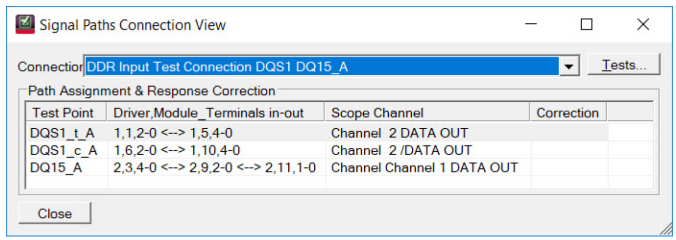


At runtime, when the Switch Matrix module is **On** and when a connection prompt occurs, two events occur:

- The framework suppresses the prompts.

- The Switch Matrix module detects the new connection and then throw switches, as indicated in the **Switch** column, taking into account the current value of the config variable (if any) associated with the connection.

3 Click the **View Connections...** button to view the signal path mapping, to understand how the signal path maps to the connection diagrams being used by the application.



4 Click the **Tests...** button to view information about the tests that use the selected connection to perform automated tests.

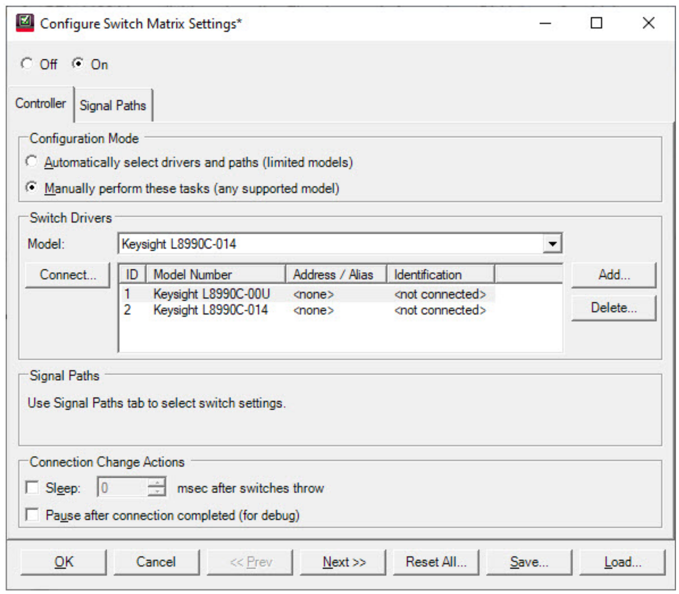
5 Click the **Close** button to exit and return to the **Configure Switch Matrix Settings** dialog to finish the signal path configuration.

6 Once you have finished, click **OK** in the **Configure Switch Matrix Settings** dialog. The application redirects you to the test environment.

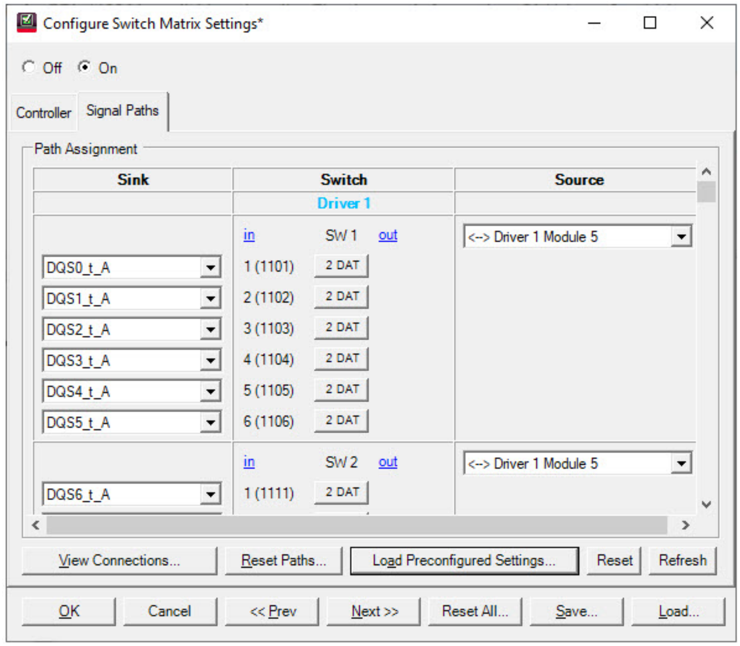
Configuring Signal Paths - Manually

Once you have enabled the Switch Matrix feature, you must configure signal paths. Perform the following steps:

1. Ensure that **Configuration Mode** is set to **Manually select drivers and paths (limited models)**.
2. Connect to the two Switch Matrix Models.



3 Click the **Signal Paths** tab in the **Configure Switch Matrix Settings** dialog box.



4 It is recommended to click **Load Preconfigured Settings...** button and then edit the signal paths.

5 Once you have finished, click **OK** in the **Configure Switch Matrix Settings** dialog box. The application redirects you to the test environment.

Select Tests tab – Select test and measurement task to be performed

The **Select Tests** tab is the main area in the M80885RCA DDR5 where tests can be selected to be performed during the next **Run** command. Each test is part of a test group which can be expanded or collapsed by clicking on the preceding arrow. The info area below the test tree shows additional information about the selected test.

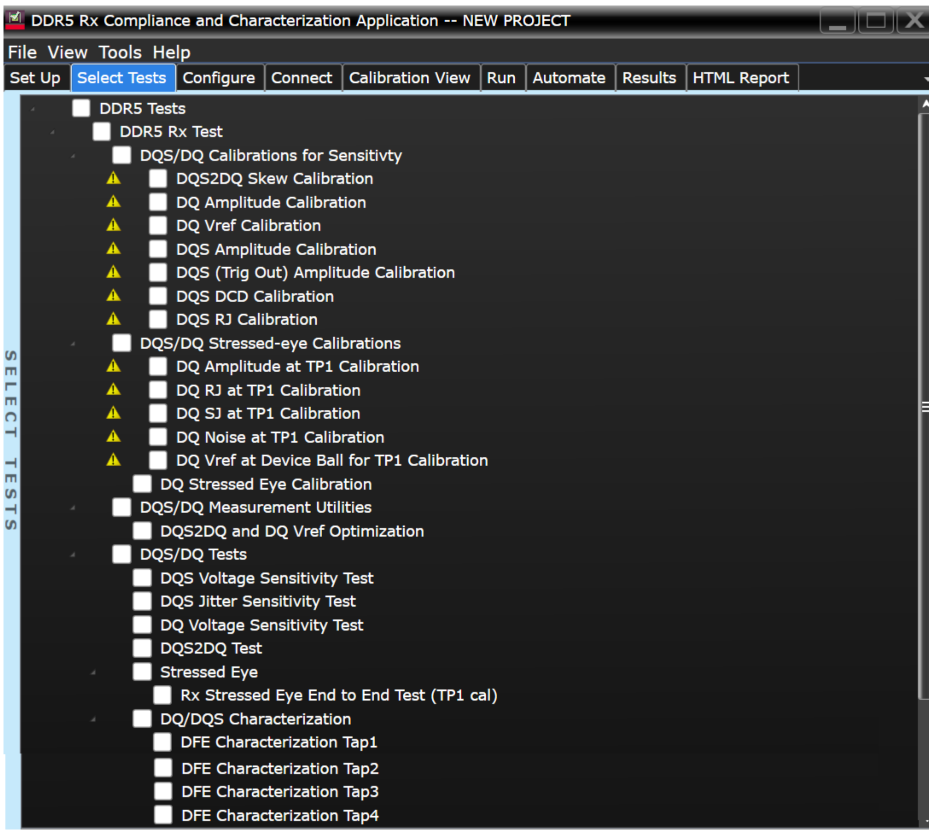


Figure 14 Select Tests tab

NOTE The DQ Noise at TP1 Calibration and CA Noise at TP1 calibration are only available when connected to the M8040A BERT setup.

NOTE

All selected tests will be performed successively (from top to bottom of the list) during the next **Run** command. If a certain test needs to be performed before other tests, please run this test separately with all other tests deactivated.

NOTE

When activating/deactivating a test group, all child tests will be activated/deactivated accordingly.

Configure tab – Configure application and test specific settings

The **Configure** tab lists all user configuration variables available for the selected test parameters. The configuration variables are subdivided into the same groups as the test structure and can likewise be expanded or collapsed by clicking on the small preceding arrow.

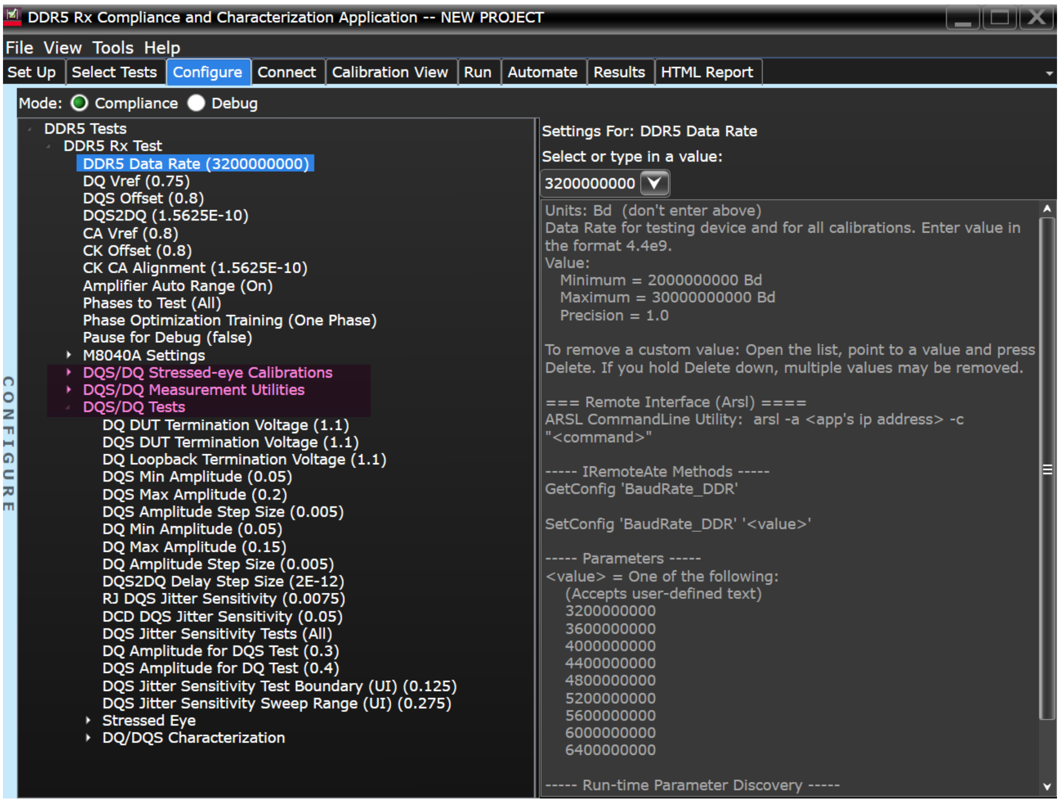


Figure 15 Configure tab

The current value of a variable is shown in parentheses behind the variable name. To change a value, select an existing value from the corresponding drop-down box or type in a new one.

The information text below the drop box shows additional information about the configuration variable, for example, its minimum or maximum value as well as its precision (only applicable for numeric types).

The M80885RCA DDR5 compliance test application offers two configuration modes:

- Compliance mode
- Debug mode

In **Compliance** mode, specific user variables which represent specifications cannot be edited. To allow changing these values (thus deviating from the standard), switch to **Debug** mode.

Connect tab – Display hardware connection diagrams and test specific information

The **Connect** tab displays hardware connection diagrams before the start of a test. This optional step allows the user to check the physical connections between the devices to ensure compliance with the standards.

Calibration View tab – Display calibration results

The **Calibration View** tab displays the results from the calibrations run, in both graphical and tabular format.

Run tab – Run selected tests or measurements

The **Run** tab defines various settings to run tests and starts the selected tests or the automation script created in the **Automate** tab.

Automate tab – Run automated scripts

The **Automate** tab starts any automation scripts created in the Test Application.

Results & HTML Report tabs – Display test results

The **Results** tab and the **HTML Report** tab display the high-level and detailed test and measurement results. In compliance applications, some tests return only a pass/fail value and others return detailed measurement results (such as, scalar values, tables or images captured from equipment with display).

The M80885RCA DDR5 Receiver Test Application also facilitates exporting the measurement results and HTML reports into CSV, PDF files or even to a Web Dataset Repository. For a detailed understanding of the functionality of each tab and various features within the M80885RCA DDR5 Receiver Test Application, refer to the *Keysight M80885RCA DDR5 Receiver Test Application Online Help*.

Technical Support

Check the **Help** menu for various user assistance documents. For technical support, contact Keysight Technical Support (**Help > Technical Support > Contact Technical Support**) or your Keysight representative. When reporting a software crash, go to **Help > Technical Support > Collect Files**. Send the zip file to Keysight.

4 Performing Receiver Compliance Tests with M80885RCA Software

This section describes the calibration and test procedures corresponding to the DDR5 specification in the Keysight M80885RCA DDR5 Receiver Test Application.

Setting Up and Preparing the DDR5 Compliance Test Setup

Before launching the M80885RCA DDR5 Receiver Test Application and performing a DDR5 receiver compliance test, you need to set up the required instruments and test fixtures and make the physical connections as shown in the images below. To ensure stable operation, observe the specified warm up times of the instruments being used. Also, ensure that the BERT M8070B System software is running.

Making Connections for DQS/DQ Calibrations and Tests

Connections for M8020A setup

Making Connections for DQS/DQ Calibrations for Sensitivity

Perform the following steps to make connections for DQS/DQ calibrations for sensitivity:

1 Connect the PC to the BERT via USB.
2 Connect the oscilloscope to LAN or PC via LAN/USB.
3 Open M8070B software.
4 Open M80885RCA software (it will automatically connect to M8070B)
   a Connect M80885RCA to the oscilloscope (on the **Set Up** tab).
5 Connect Generator Data Out 1 _t to DQx on CTC2.
6 Connect Generator Data Out 1 _c to 50 ohm termination.
7 Connect Generator Data Out 2 _t/_c to DQSx_t/DQSx_c on CTC2.
8 Connect DQCal point to Oscilloscope CH1.
9 Connect DQSCal points to Oscilloscope CH2 and CH4.
10 Connect Generator Clk Out 1 _t/_c to CTC2 CLK.

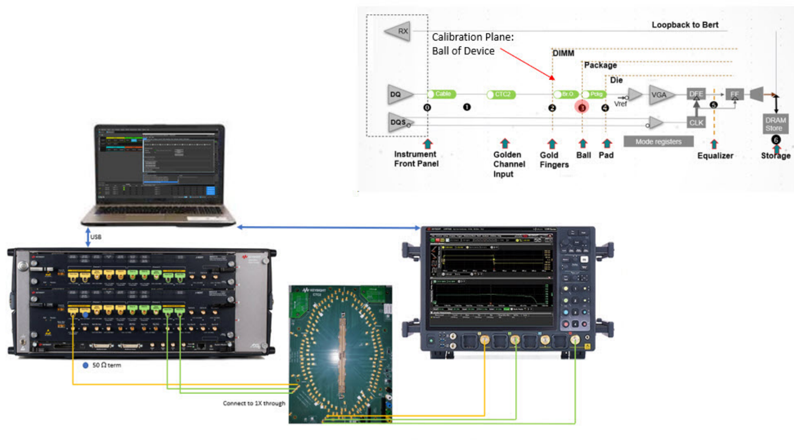


Figure 16 Equipment connections for DQS/DQ calibrations for sensitivity

Note that when **Host** is the selected DUT, the equipment connections for the DQS/DQ Calibrations for Sensitivity will be as shown in Figure 17.

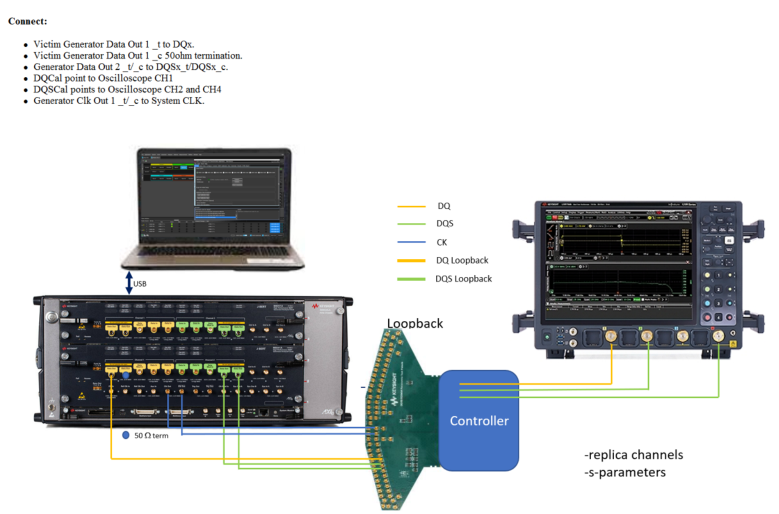


Figure 17 Equipment connections for DQS/DQ calibrations for sensitivity with Host DUT

Making Connections for DQS/DQ Stressed-eye Calibrations - DQ Amplitude at TP1, DQ RJ at TP1, and DQ SJ at TP1

Perform the following steps to make connections for the DQ Amplitude, DQ RJ, and DQ SJ at TP1:

1. Connect the PC to the BERT via USB.
2. Connect the oscilloscope to LAN or PC via LAN/USB.
3. Open M8070B software.
4. Open M80885RCA software (it will automatically connect to M8070B)
   a. Connect M80885RCA to the oscilloscope (on the Setup tab).
5. Connect Generator Data Out 1 _t directly to Oscilloscope CH1 with cable that will be used for test connection to CTC2.
6. Connect Generator Data Out 1 _c to 50 ohm termination.
7. Connect Generator Data Out 2 _t/_c to Oscilloscope CH2 and CH4 with cables that will be used for test connection to CTC2.

NOTE The cables used in steps 5 and 7 will require a SMP-SMA adapter. (Scope = SMA connector, CTC2 = SMP connector)

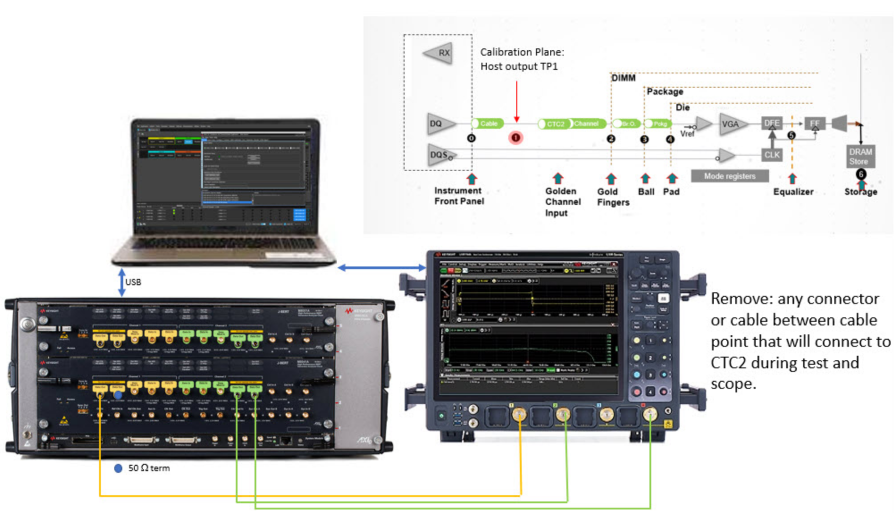


Figure 18 Equipment connections for DQ Amplitude, DQ RJ, and DQ SJ calibrations at TP1

Note that when **Host** is the selected DUT, the equipment connections for DQS/DQ Stressed-eye Calibrations will be as shown in Figure 17.

Making connections for DQ Vref at Device Ball for TP1 Calibration and DQ Stressed Eye Calibration

The DQ Vref at Device Ball for TP1 Calibration and DQ Stressed Eye Calibration require the following calibrations as a prerequisite:

- DQ Amplitude at TP1 Calibration
- DQ RJ at TP1 Calibration
- DQ SJ at TP1 Calibration

Perform the following steps to make connections for DQ Vref at Device Ball for TP1 Calibration and DQ Stressed Eye Calibration:

1. Connect the PC to the BERT via USB.
2. Connect the oscilloscope to LAN or PC via LAN/USB.
3. Open M8070B software.
4. Open M80885RCA software (it will automatically connect to M8070B)
    a. Connect M80885RCA to the oscilloscope (on the **Set Up** tab).
5. Connect Generator Data Out 1 _t to DQx on CTC2.
6. Connect Generator Data Out 1 _c to 50ohm termination.
7. Connect Generator Data Out 2 _t/_c to DQSx_t/DQSx_c on CTC2.
8. Connect DQCal point to Oscilloscope CH1.
9. Connect DQSCal points to Oscilloscope CH2 and CH4.
10. Connect Generator Clk Out 1 _t/_c to CTC2 CLK.

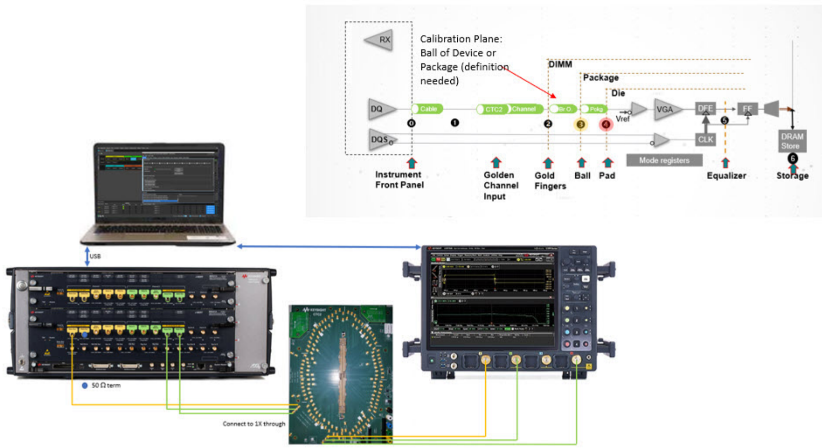


Figure 19 Equipment connections for DQ Vref at Device Ball for TP1 Calibration and DQ Stressed Eye Calibration

Making Connections for DQS/DQ Loopback Tests

Perform the following steps to make connections for Loopback tests:

1 Connect Generator Data Out 1_t to DQx on CTC2.

2 Connect Generator Data Out 1_c to 50 ohm termination.

3 Connect Generator Data Out 2_t/_c to DQSx on CTC2.

4 Connect Generator Clk Out 1 _t/_c to CTC2 CLK.

5 Loopback DQ to Channel 1 Data In.

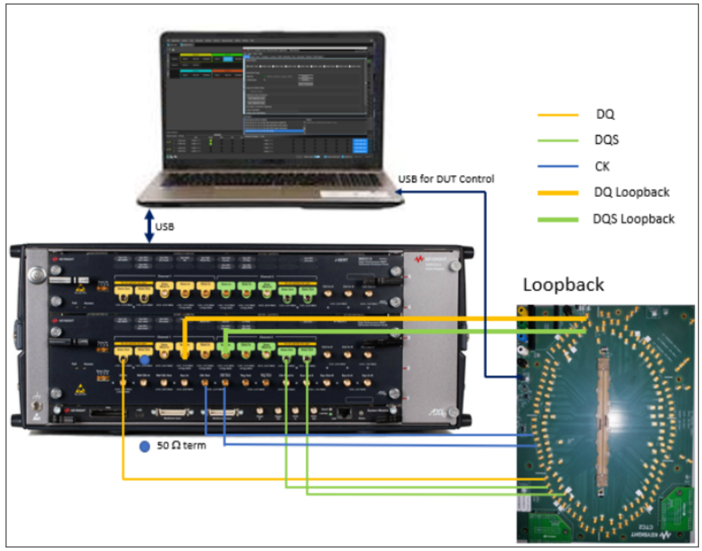


Figure 20 Equipment connections for Loopback tests

Note that when **Host** is the selected DUT, the equipment connections for DQS/DQ Loopback tests will be as shown in Figure 21.

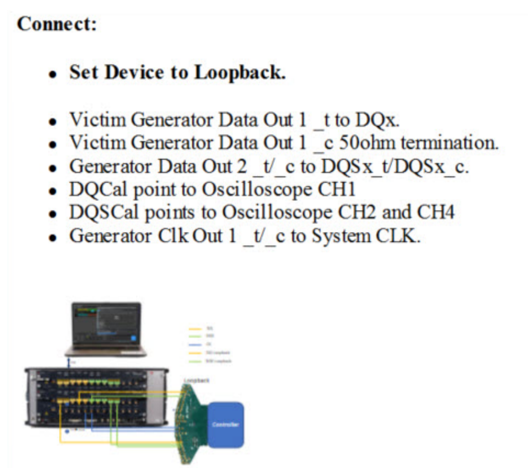


Figure 21 Equipment connections for DQS/DQ Loopback tests with Host DUT

Connections with M8040A setup

Making Connections for DQS/DQ Calibrations for Sensitivity and DQ Vref at Device Ball for TP1 Calibration

Perform the following steps to make connections for DQS/DQ calibrations for sensitivity and DQ Vref at Device Ball for TP1 Calibration:

1 Connect Pickoff Tee to PG CH1 Data Out+
2 Connect AWG CH1 Data Out+ to Pickoff Tee at PG CH1 Data Out+
3 Connect Pickoff Tee at PG CH1 Data Out+ to DQ0_B on CTC2
4 Connect DQ0_B on Replica Card to Oscilloscope CH1
5 Connect PG CH1 Data Out- to 50 Ohm termination
6 Connect PG CH2 Data Out+ to DQS0_B_t on CTC2
7 Connect DQS0_B_t on Replica Card to Oscilloscope CH2
8 Connect PG CH2 Data Out- to DQS0_B_c on CTC2
9 Connect DQS0_B_c on Replica Card to Oscilloscope CH4

NOTE The DQS (Trig Out) Amplitude Calibration uses the TRIG OUT of the BERT instead of PG CH2.

Figure 22 shows the equipment connections for DQS2DQ Skew Calibration, DQ Amplitude Calibration, DQ Vref Calibration, and DQS Amplitude Calibration.

Figure 23 shows the equipment connections for DQS (Trig Out) Amplitude Calibration, DQS DCD Calibration, and DQS RJ Calibration.

Figure 24 shows the equipment connections for DQ Vref at Device Ball for TP1 Calibration.

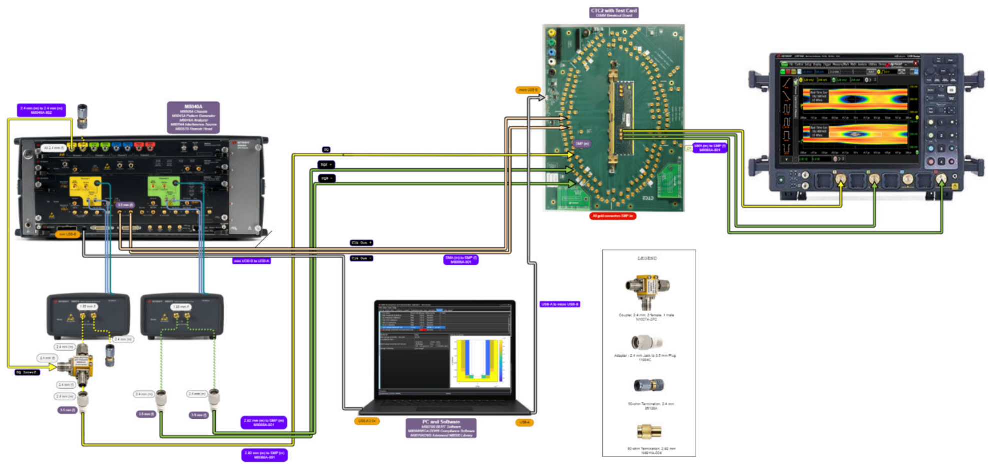


Figure 22 Equipment connections for DQS2DQ Skew Calibration, DQ Amplitude Calibration, DQ Vref Calibration, and DQS Amplitude Calibration

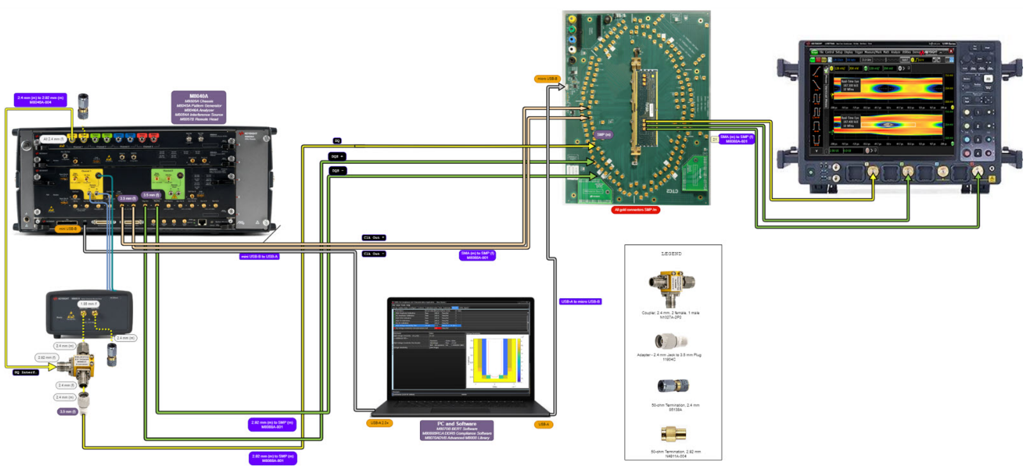


Figure 23 Equipment connections for DQS (Trig Out) Amplitude Calibration, DQS DCD Calibration, and DQS RJ Calibration

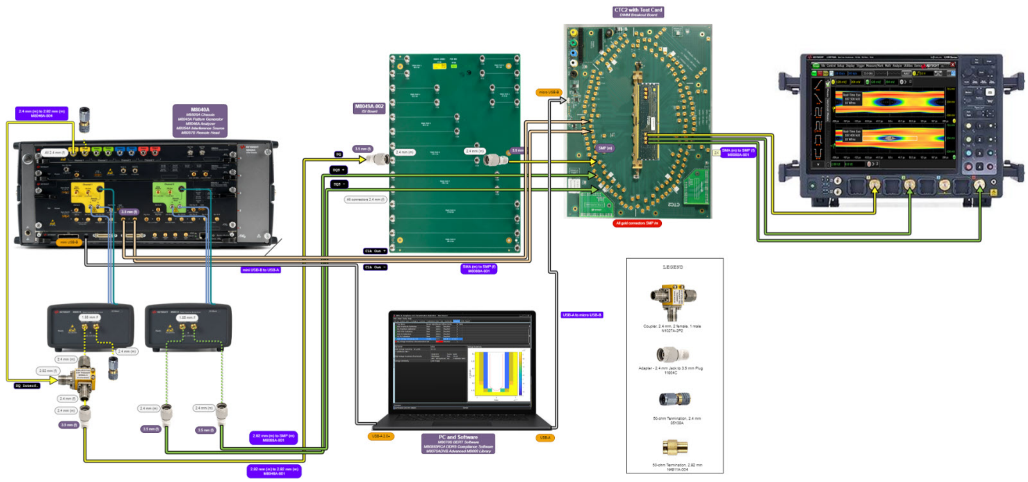


Figure 24 Equipment connections for DQ Vref at Device Ball for TP1 Calibration

Connections for DQS/DQ Stressed-eye Calibrations: DQ Amplitude at TP1, DQ RJ at TP1, DQ SJ at TP1, and DQ Noise at TP1

Perform the following steps to make connections for the DQ Amplitude at TP1, DQ RJ at TP1, DQ SJ at TP1, and DQ Noise at TP1 calibrations at TP1:

1 Connect Pickoff Tee to PG CH1 Data Out+
2 Connect AWG CH1 Data Out+ to Pickoff Tee at PG CH1 Data Out+
3 Connect Pickoff Tee at PG CH1 Data Out+ to Oscilloscope CH1
4 Connect PG CH1 Data Out- to 50 Ohm termination
5 Connect PG CH2 Data Out+ to Oscilloscope CH2
6 Connect PG CH2 Data Out- to Oscilloscope CH4

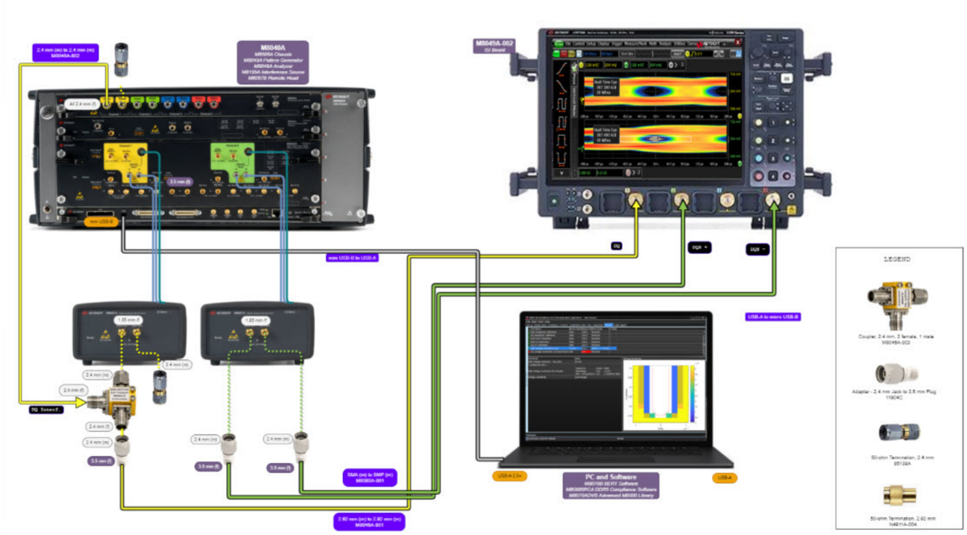


Figure 25 Equipment connections for DQ Amplitude, DQ RJ, DQ SJ, and DQ Noise Calibrations at TP1

Making Connections for DQ Stressed Eye Calibration

Perform the following steps to make connections for DQ Stressed Eye Calibration:

1 Connect Pickoff Tee to PG CH1 Data Out+
2 Connect AWG CH1 Data Out+ to Pickoff Tee at PG CH1 Data Out+
3 Connect Pickoff Tee at PG CH1 Data Out+ to ISI Board Trace
4 Connect from ISI Board Trace to DQ0_B on CTC2
5 Connect DQ0_B on Replica Card to Oscilloscope CH1
6 Connect PG CH1 Data Out- to 50 Ohm termination
7 Connect PG CH2 Data Out+ to DQS0_B_t on CTC2
8 Connect DQS0_B_t on Replica Card to Oscilloscope CH2
9 Connect PG CH2 Data Out- to DQS0_B_c on CTC2
10 Connect DQS0_B_c on Replica Card to Oscilloscope CH4

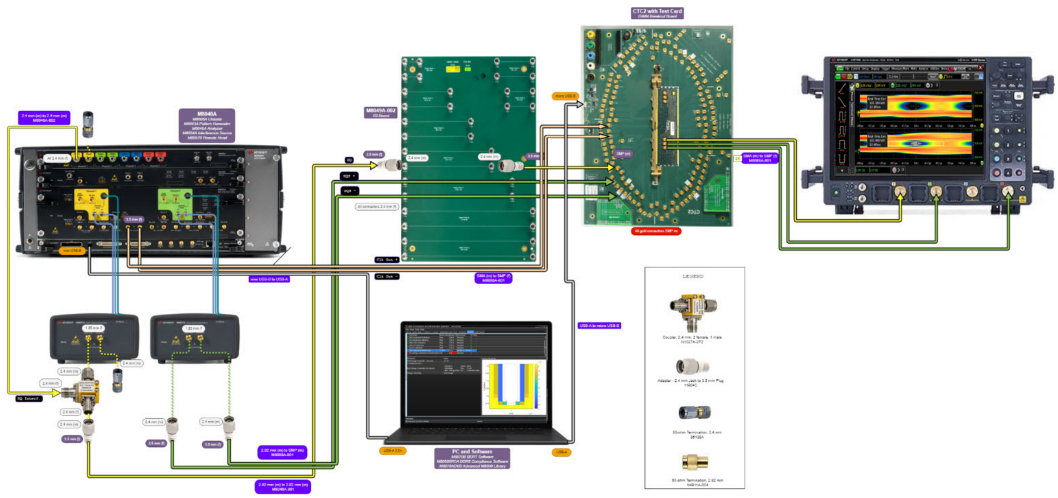


Figure 26 Equipment connections for DQ Stressed Eye Calibration

Note that when **Host** is the selected DUT, the equipment connections for DQS/DQ Calibration for Sensitivity and DQS/DQ Stressed-eye Calibrations will be as shown in Figure 17.

Making Connections for DQS/DQ Loopback Tests

Perform the following steps to make connections for DQS/DQ tests:

1 Connect Pickoff Tee to PG CH1 Data Out+
2 Connect AWG CH1 Data Out+ to Pickoff Tee at PG CH1 Data Out+
3 Connect Pickoff Tee at PG CH1 Data Out+ to DQx on CTC2
4 Connect PG CH1 Data Out- to 50 Ohm termination
5 Connect PG CH2 Data Out+ to DQSx_t on CTC2
6 Connect PG CH2 Data Out- to DQSx_c on CTC2
7 Connect Clock Out _t/_c to CTC2 CLK
8 For “DQS Voltage Sensitivity” test,
   - Connect Loopback DQS to ED Data In
   - Connect PG CH2 Clock Out to ED Clock In
9 For other Loopback tests,
   - Connect Loopback DQ to ED Data In

- Connect PG CH1 Clock Out to ED Clock In

Figure 27 shows equipment connection diagrams for DQS Voltage Sensitivity Test, DQ Voltage Sensitivity Test, DQS2DQ Test, and for DQS/DQ Characterization.

Figure 28 shows equipment connection diagrams for DQS Jitter Sensitivity Test.

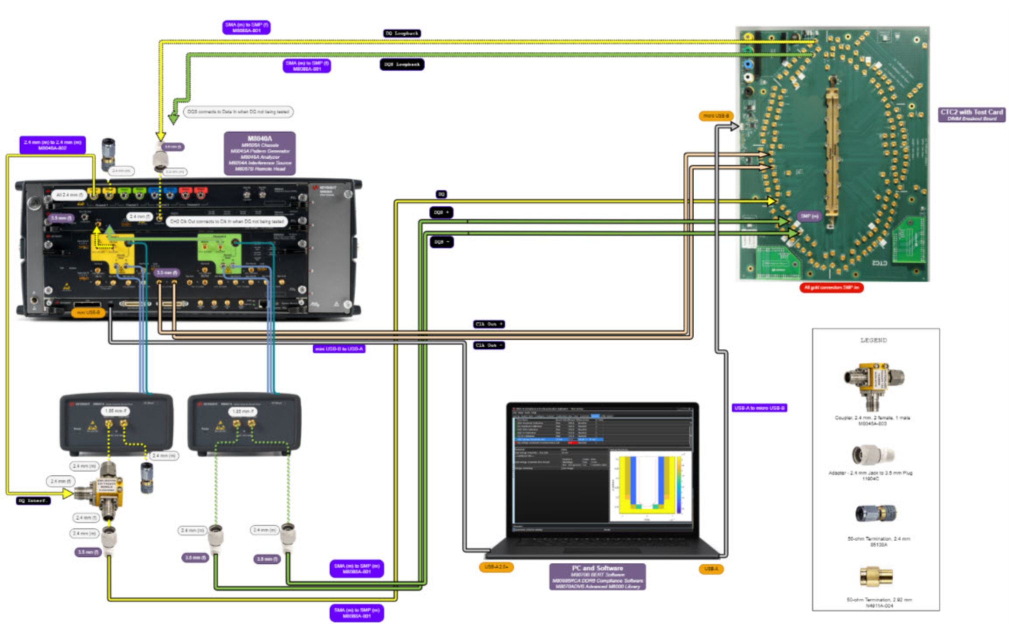


Figure 27 Equipment connections for DQS/DQ Tests

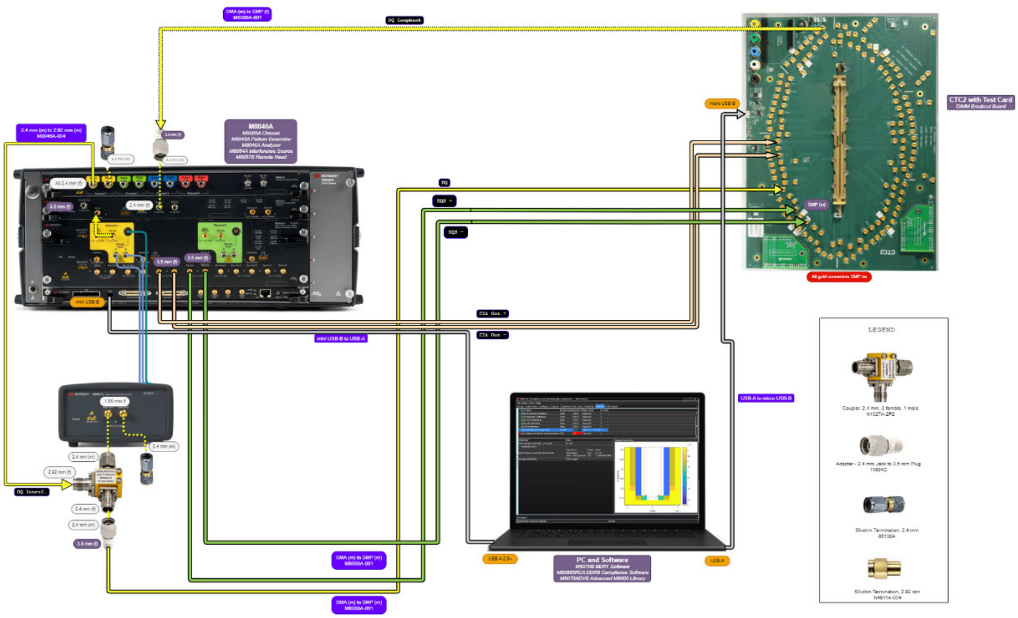


Figure 28 Equipment connections for DQS Jitter Sensitivity Test

Making Connections for Stressed Eye Loopback

Perform the following steps to make connections for Stressed Eye Loopback:

1. Connect Pickoff Tee to PG CH1 Data Out+
2. Connect AWG CH1 Data Out+ to Pickoff Tee at PG CH1 Data Out+
3. Connect Pickoff Tee at PG CH1 Data Out+ to ISI Board trace
4. Connect from ISI Bord trace to DQx on CTC2
5. Connect PG CH1 Data Out- to 50 Ohm termination
6. Connect PG CH2 Data Out+ to DQSx_t on CTC2
7. Connect PG CH2 Data Out- to DQSx_c on CTC2
8. Connect Clock Out _t/_c to CTC2 CLK
9. For “DQS Voltage Sensitivity” test,
   - connect Loopback DQS to ED Data In
   - connect PG CH2 Clock Out to ED Clock In
10. For others Loopback test,

- Connect Loopback DQ to ED Data In
- Connect PG CH1 Clock Out to ED Clock In

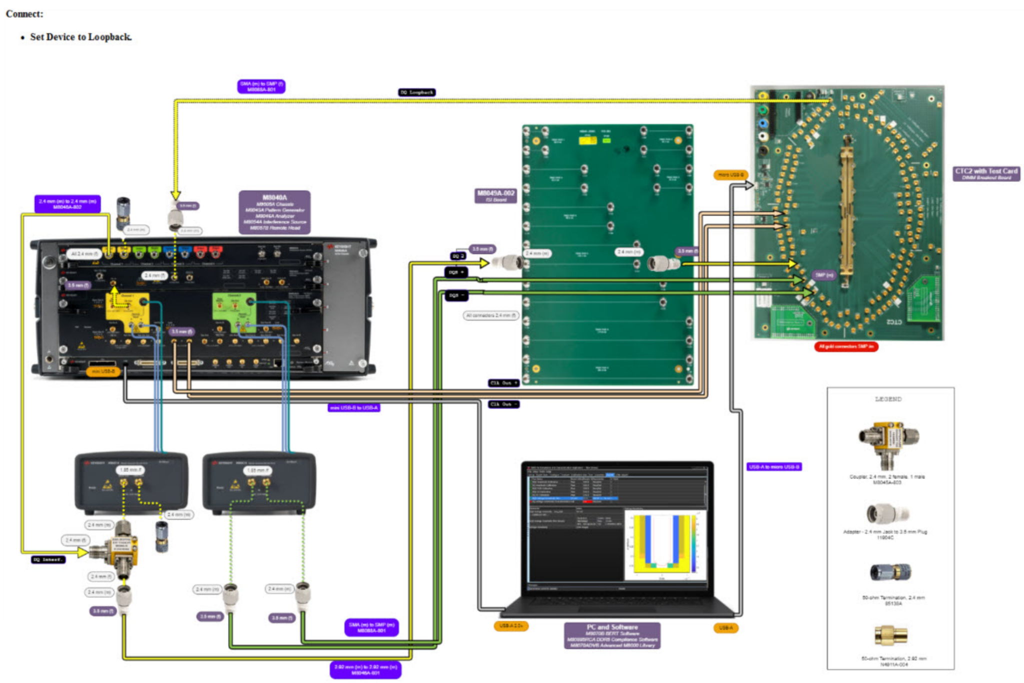


Figure 29 Equipment connections for Stressed Eye Loopback

Note that when **Host** is the selected DUT, the equipment connections for DQS/DQ Tests will be as shown in Figure 21.

Making Connections for CK/CA Calibrations and Tests

NOTE A new configuration has been added to the app to select "Balanced or Unbalanced Termination Model".

NOTE If BERT gives the warnings "Incorrect Termination detected", please make sure that the physical setup has sufficient impedance (by adding external attenuator 3 dB or 6 dB) to meet BERT spec.

Connections for M8020A setup

Making Connections for CK/CA Calibrations for Sensitivity

Perform the following steps to make connections for CK/CA calibrations for sensitivity:

1 Connect the PC to the BERT via USB.
2 Connect the oscilloscope to LAN or PC via LAN/USB.
3 Open M8070B software.
4 Open M80885RCA software (it will automatically connect to M8070B)
   a Connect M80885RCA to the oscilloscope (on the **Set Up** tab).
5 Connect Generator Data Out 1 _t to CAx on CTC2.
6 Connect Generator Data Out 1 _c to 50 ohm termination.
7 Connect Generator Data Out 2 _t/_c to CK_t/CK_c on CTC2.
8 Connect CACal point to Oscilloscope CH1.
9 Connect CKCal points to Oscilloscope CH2 and CH4.

The equipment connections for “CK/CA calibrations for sensitivity” are the same as shown in Figure 16.

Making Connections for CK/CA Calibrations at TP1: CA Amplitude, CA RJ, and CA SJ Calibrations at TP1

Perform the following steps to make connections for the CA Amplitude, CA RJ, and CA SJ Calibrations at TP1:

1 Connect the PC to the BERT via USB.
2 Connect the oscilloscope to LAN or PC via LAN/USB.
3 Open M8070B software.
4 Open M80885RCA software (it will automatically connect to M8070B)
   a Connect M80885RCA to the oscilloscope (on the Setup tab).
5 Connect Generator Data Out 1 _t directly to Oscilloscope CH1 with cable that will be used for test connection to CTC2.
6 Connect Generator Data Out 1 _c to 50 ohm termination.
7 Connect Generator Data Out 2 _t/_c to Oscilloscope CH2 and CH4 with cables that will be used for test connection to CTC2.

NOTE The cables used in steps 5 and 7 will require a SMP-SMA adapter. (Scope = SMA connector, CTC2 = SMP connector)

The equipment connections for “CA Amplitude, CA RJ, and CA SJ calibrations at TP1” are the same as shown in Figure 18.

Making Connections for CA Vref at Device Ball for TP1 Calibration and CA Stressed Eye at Device for TP1 Calibration

The CA Vref at Device Ball for TP1 Calibration and CA Stressed Eye at Device Ball for TP1 Calibration require the following calibrations as a prerequisite:

- CA Amplitude at TP1 Calibration
- CA RJ at TP1 Calibration
- CA SJ at TP1 Calibration

Perform the following steps to make connections for the CA Vref at Device Ball for TP1 Calibration and CA Stressed Eye at Device for TP1 Calibration:

1 Connect the PC to the BERT via USB.
2 Connect the oscilloscope to LAN or PC via LAN/USB.
3 Open M8070B software.

4 Open M80885RCA software (it will automatically connect to M8070B)
   a Connect M80885RCA to the oscilloscope (on the **Set Up** tab).
5 Connect Generator Data Out 1 _t to CAx on CTC2.
6 Connect Generator Data Out 1 _c to 50ohm termination.
7 Connect Generator Data Out 2 _t/_c to CK_t/CK_c on CTC2.
8 Connect CACal point to Oscilloscope CH1.
9 Connect CKCal points to Oscilloscope CH2 and CH4.

The equipment connections for “CA Vref at Device Ball and CA Stressed Eye at Device for TP1 Calibrations” are the same as shown in Figure 19.

Making Connections for CK/CA Loopback Tests

Perform the following steps to make connections for CK/CA Loopback tests:

1 Connect Generator Data Out 1_t to CAx on CTC2.
2 Connect Generator Data Out 1_c to 50 ohm termination.
3 Connect Generator Data Out 2_t/_c to CKx on CTC2.
4 Loopback CA to Channel 1 Data In.

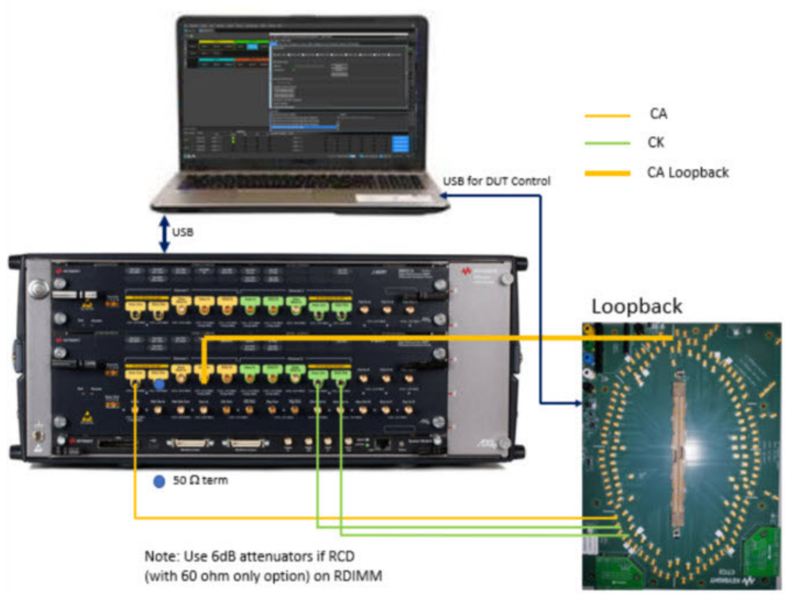


Figure 30 Equipment connections for CK/CA Loopback Tests

Connections for M8040A setup

Making Connections for CK/CA Calibrations for Sensitivity, CA Vref at Device Ball for TP1 Calibration and CA Stressed Eye at Device for TP1 Calibration

Perform the following steps to make connections for CK/CA sensitivity, CA Vref at Device Ball and Stressed Eye Calibrations:

1 Connect Pickoff Tee to PG CH1 Data Out+
2 Connect AWG CH1 Data Out+ to Pickoff Tee at PG CH1 Data Out+
3 Connect Pickoff Tee at PG CH1 Data Out+ to CA1 on CTC2
4 Connect DQ0_B on Replica Card to Oscilloscope CH1
5 Connect PG CH1 Data Out- to 50 Ohm termination
6 Connect PG CH2 Data Out+ to CK_t on CTC2
7 Connect CK_t on Replica Card to Oscilloscope CH2
8 Connect PG CH2 Data Out- to CK_c on CTC2
9 Connect CK_c on Replica Card to Oscilloscope CH4

NOTE The CK (Trig Out) Amplitude Calibration uses the TRIG OUT of the BERT instead of PG CH2.

Figure 31 shows the equipment connection diagram for the following calibrations:

- CK/CA calibrations for sensitivity such as CA Amplitude Calibration, CK Amplitude Calibration, and CA Vref Calibration
- CA Vref at Device Ball for TP1 Calibration

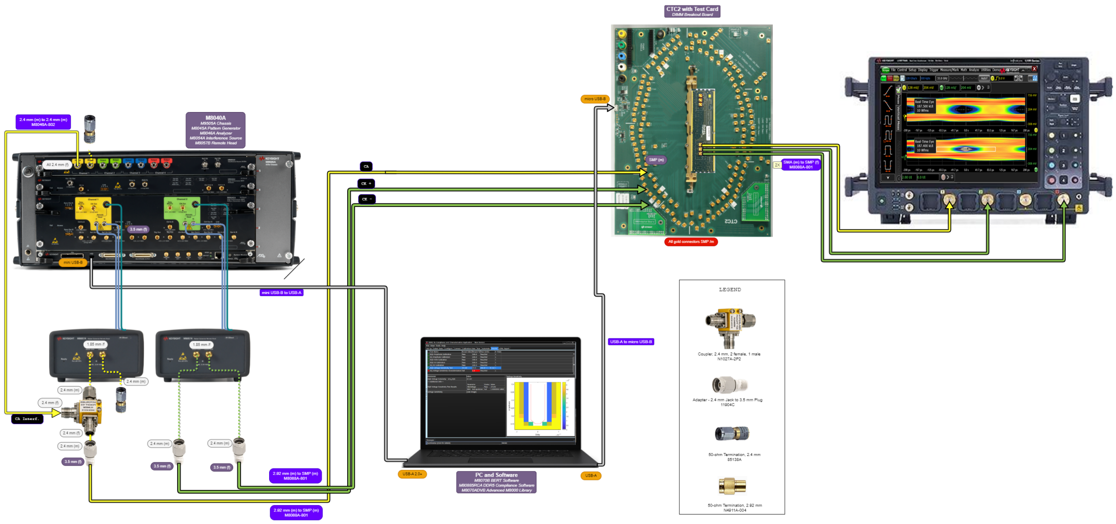


Figure 31 Equipment connection for CK/CA Calibrations for Sensitivity and CA Vref at Device Ball for TP1 Calibration

Figure 32 shows the equipment connection diagram CK (Trig Out) Amplitude Calibration, CK DCD Calibration, and CK RJ Calibration.

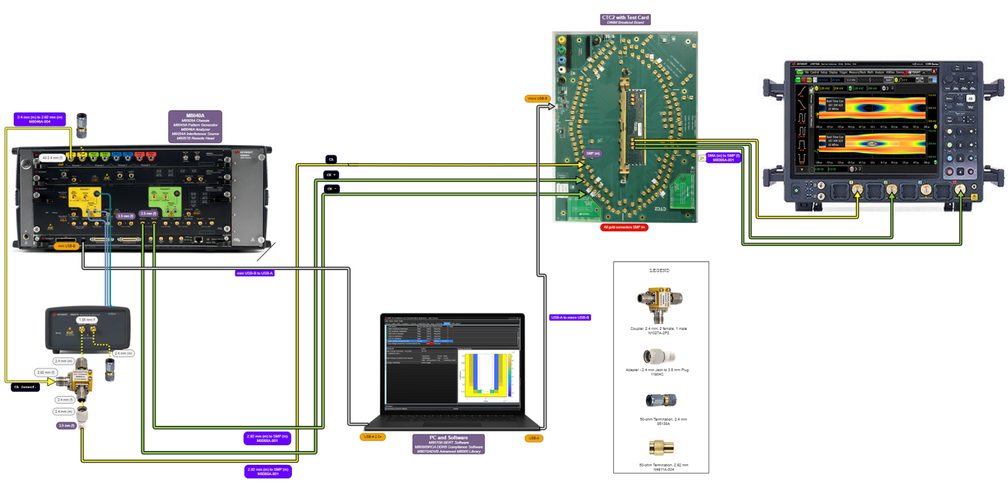


Figure 32 Equipment connections for CK (Trig Out) Amplitude Calibration, CK DCD

Calibration, and CK RJ Calibration

Figure 33 shows the equipment connection diagram for CA Stressed Eye at Device for TP1 Calibration.

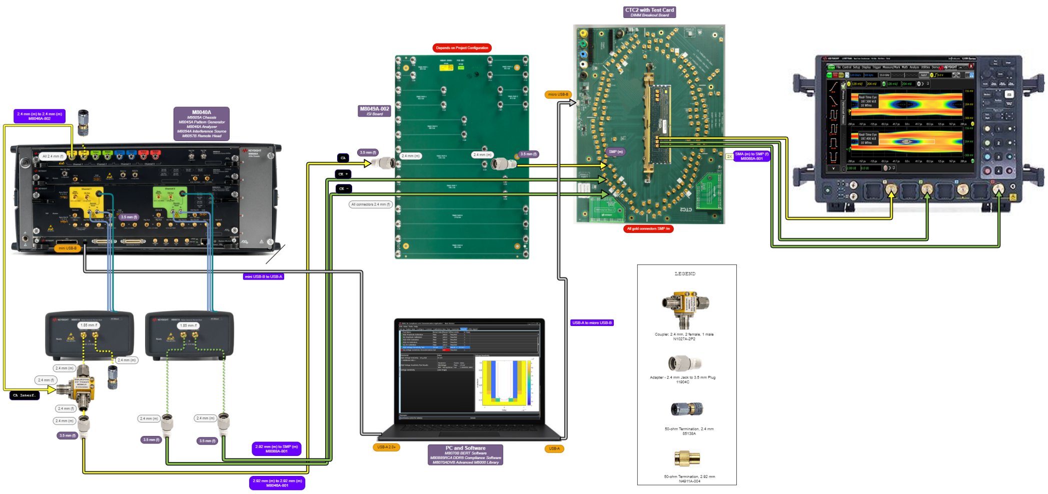


Figure 33 Equipment connections for CA Stressed Eye at Device for TP1 Calibration

Making Connections for CK/CA Calibrations at TP1: CA Amplitude, CA RJ, CA SJ, and CA Noise Calibrations at TP1

Perform the following steps to make connections for the CA Amplitude, CA RJ, CA SJ, and CA Noise Calibrations at TP1:

1 Connect Pickoff Tee to PG CH1 Data Out+
2 Connect AWG CH1 Data Out+ to Pickoff Tee at PG CH1 Data Out+
3 Connect Pickoff Tee at PG CH1 Data Out+ to Oscilloscope CH1
4 Connect PG CH1 Data Out- to 50 Ohm termination
5 Connect PG CH2 Data Out+ to Oscilloscope CH2
6 Connect PG CH2 Data Out- to Oscilloscope CH4

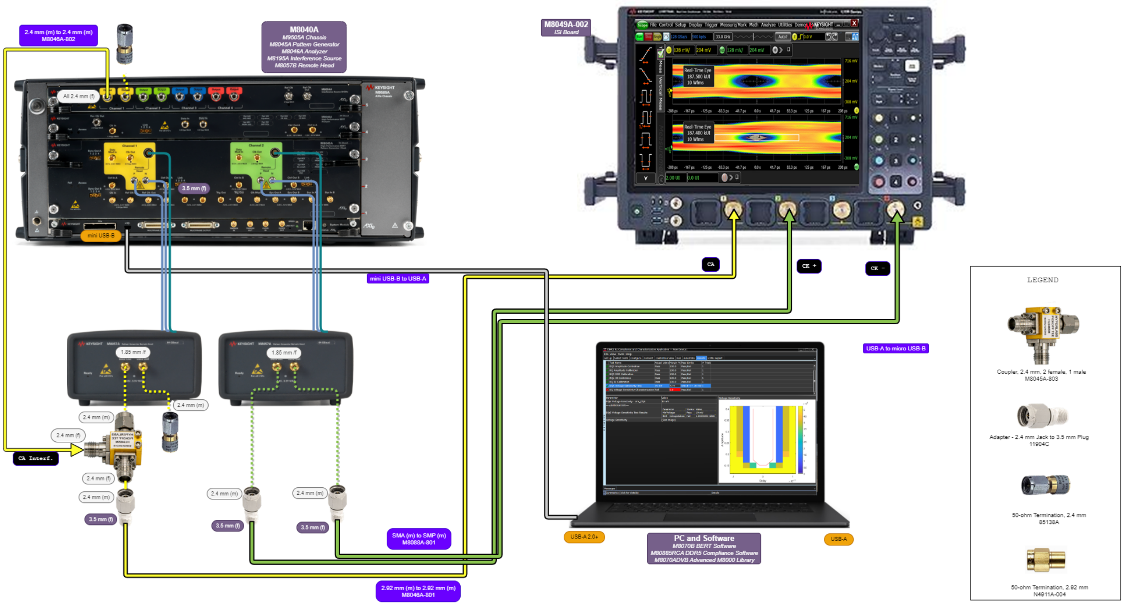


Figure 34 Equipment connections for CA Amplitude, CA RJ, CA SJ, and CA Noise Calibrations at TP1

Making Connections for CK/CA Loopback Tests

Perform the following steps to make connections for CK/CA Loopback tests:

1 Connect Pickoff Tee to PG CH1 Data Out+
2 Connect AWG CH1 Data Out+ to Pickoff Tee at PG CH1 Data Out+
3 Connect Pickoff Tee at PG CH1 Data Out+ to CAx on CTC2
4 Connect PG CH1 Data Out- to 50 Ohm termination
5 Connect PG CH2 Data Out+ to CK_t on CTC2
6 Connect PG CH2 Data Out- to CK_c on CTC2
7 Connect Loopback CA to ED Data In
8 Connect PG CH1 Clock Out to ED Clock In

Figure 35 shows equipment connection diagram for CA Voltage Sensitivity Test and CK Voltage Sensitivity Test.

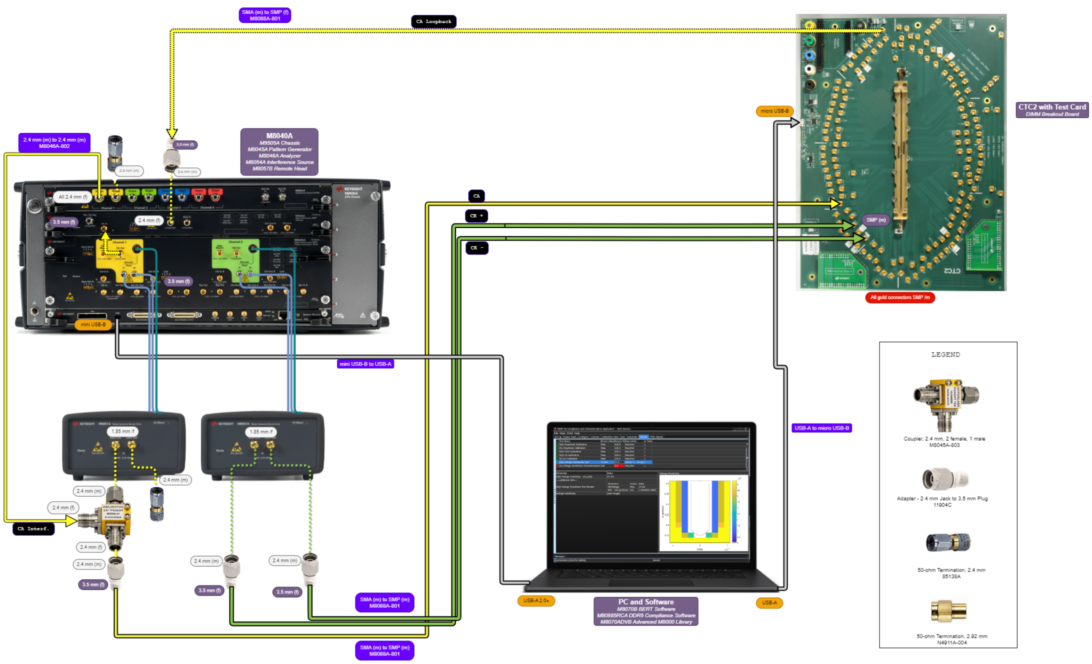


Figure 35 Equipment connections for CA Voltage Sensitivity Test and CK Voltage Sensitivity Test

Figure 36 shows equipment connection diagram for CK Jitter Sensitivity Test.

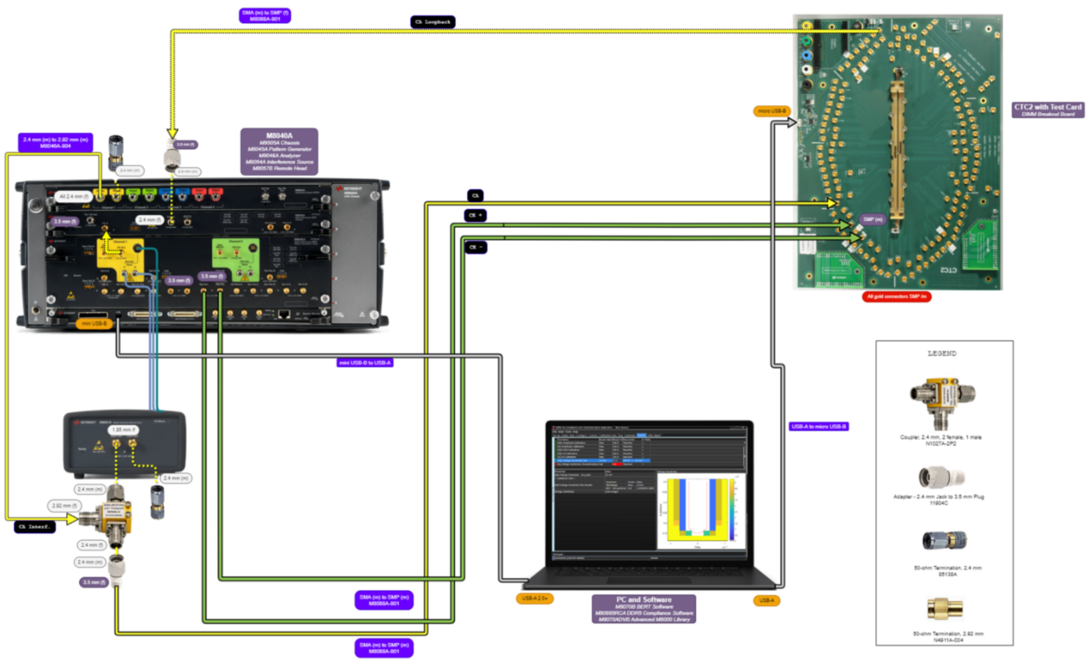


Figure 36 Equipment connections for CK Jitter Sensitivity Test

Figure 37 shows equipment connections for CA Rx Stressed Eye End to End Test (TP1 cal) test.

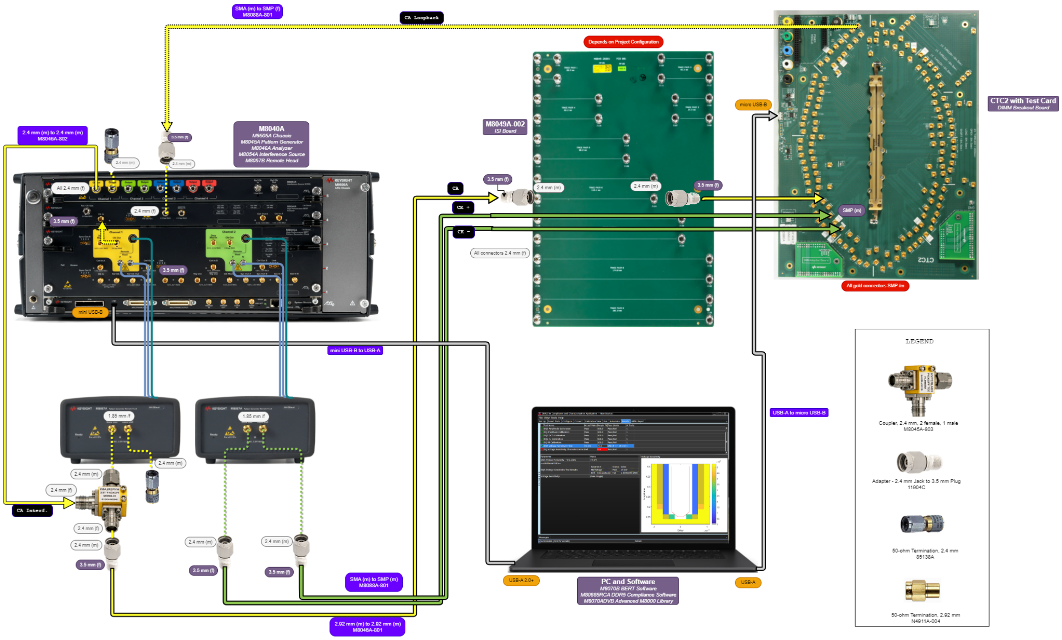


Figure 37 Equipment connections for CA Rx Stressed Eye End to End Test (TP1 cal) test

Configure global test settings

After selecting the speed option in the **Set Up** tab, the M80885RCA software loads the corresponding test limit file (check also: **Tools-> Compliance limits -> Activate/Refresh** limit set) and sets the respective configuration variables in the **Configure** tab. All global test settings, such as the DDR5 Data Rate are listed in the root group (see Figure 38).

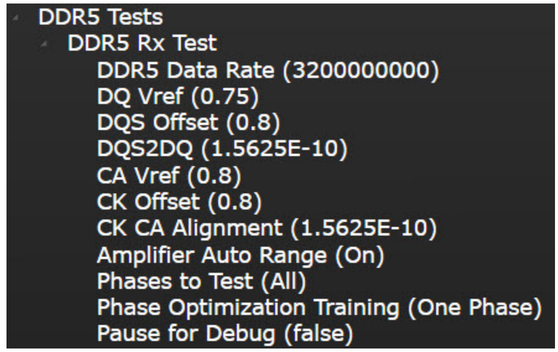


Figure 38 Global configuration variables

Calibrating the stressed receiver conformance test signal

The M80885RCA compliance test solution offers a fully automated calibration procedure to generate this compliance test signal which is then used to perform the stressed receiver sensitivity measurement and determine the receiver compliance.

Configuring calibration specific settings

The calibration specific configuration variables such as the RJ and SJ for DQS, DQ, CK, and CA signals can be found in the DQS/DQ Calibrations and CK/CA Calibrations settings. Figure 39 shows the exemplary calibration settings for the DDR5-3200 speed option.

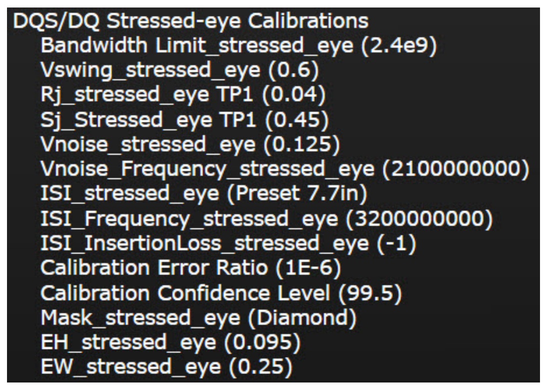


Figure 39 Exemplary calibration configuration variables for DDR5-3200 speed option

Starting the DDR5 test signal calibration

To start the DDR5 test signal calibration, activate the corresponding check box in the test tree and click the **Run** button on the **Run** tab or right-click in the test tree and select **Run checked tests**.

During the calibration, status messages in the message window show the progress of the run and display the currently performed action and intermediate measurement results.

NOTE The automated calibration will reset and reconfigure all used hardware instruments at the beginning of each calibration run. Hence any manual settings will be lost. So, make sure to save these settings prior to starting a calibration run.

NOTE The running calibration process can be aborted by clicking the **Stop** button on the **Run** tab.

After successful completion of the calibration run, the calibration results are reported in the **Calibration View** tab and **Results** tab.

The calibration results under the **Calibration View** tab include the following measurements:

- Set and measured values of the parameters being calibrated in a tabular format
- Set and measured values of the parameters being calibrated in a graphical format

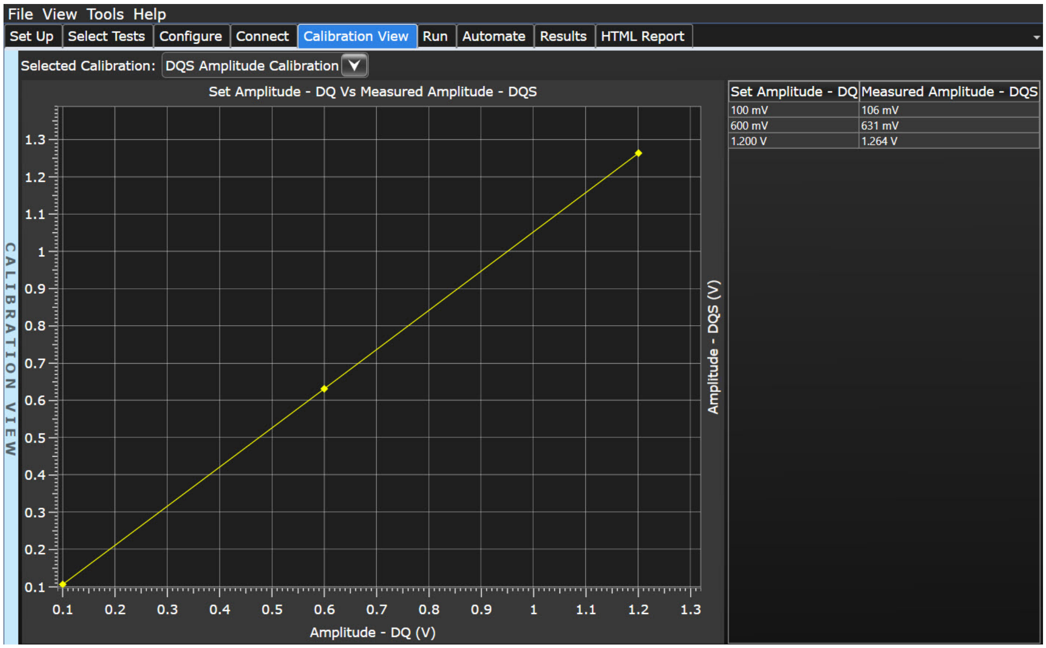


Figure 40 Calibration results

Calibration tasks

DQS/DQ Calibrations

Overview This set of calibrations consists of the following:

Calibration	Test Id	Description
DQS2DQ Skew Calibration	2100	Calibrates DQS to DQ skew
DQS Amplitude Calibration	2101	Calibrates DQS amplitude
DQS (Trig Out) Amplitude Calibration	4101	Calibrates DQS amplitude Note that this calibration is only available for M8040A BERT setup.
DQS DCD Calibration	2102	Calibrates duty cycle distortion (DCD) for DQS signal4
DQS RJ Calibration	2103	Calibrates random jitter for DQS signal

Calibration	Test Id	Description
DQ Amplitude Calibration	2201	Calibrates DQ amplitude
DQ Vref Calibration	2207	Calibrates DQ Vref.
DQ Amplitude at TP1 Calibration	12201	Calibrates DQ amplitude at TP1
DQ RJ at TP1 Calibration	12203	Calibrates random jitter for DQ signal at TP1
DQ SJ at TP1 Calibration	12204	Calibrates sinusoidal jitter for DQ signal at TP1
DQ Noise at TP1 Calibration	12208	Calibrates noise for stressed eye test. Note that this calibration is only available for M8040A BERT setup.
DQ Vref at Device Ball for TP1 Calibration	12207	Calibrates Vref at Device Ball for TP1
DQ Stressed Eye Calibration	12206	Calibrates stressed eye for DQ signal

Connection Diagram

Connect the instruments as shown in "Making Connections for DQS/DQ Calibrations and Tests" on page 64.

Configuration Parameters

You may modify the calibration-specific parameters under the **Configure** tab.

Procedure

NOTE

This section lists the general procedures for calibrations, irrespective of the test points at which these are taken.

DQS2DQ Skew Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 1 (DQ) to 0.4 V amplitude.
3 Set Channel 1 (DQ) Offset to Vref (user set or measured).
4 Set Channel 1 (DQ) to 01 pattern.
5 Set Channel 2 (DQS) to 0.4 V amplitude.
6 Set Channel 2 (DQS) to 01 pattern.
7 Initialize the oscilloscope.
8 Set Channel 1 (DQ) skew to first value in calibration table.
9 Measure DQS to DQ skew on oscilloscope and save the value.

10 Set Channel 1 (DQ) skew to next value in calibration table and repeat step 9 until last calibration table value.
11 Save the calibration table for modeling DQS2DQ skew.

DQS Amplitude Calibration and DQS (Trig Out) Amplitude Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 2 (DQS) to 0.4 V (for oscilloscope initialization).
3 Set Channel 2 (DQS) Offset to DQS offset (user set).
4 Set Channel 2 (DQS) to 01 pattern.
5 Initialize the oscilloscope.
6 Set Channel 2 (DQS) to first value in calibration table.
7 Measure the differential Vamplitude on the oscilloscope and save the value.
8 Set Channel 2 (DQS) to next value in calibration table and repeat step 7 until last calibration table value.
9 Save the calibration table for modeling DQS Amplitude.

NOTE

This calibration is used for DQS Voltage Sensitivity Test.

NOTE

The DQS (Trig Out) Amplitude Calibration uses the TRIG OUT of the BERT instead of PG CH2.

DQ Amplitude Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 1 (DQ) to 0.4 V (for oscilloscope initialization).
3 Set Channel 1 (DQ) Offset to Vref (user set or measured).
4 Set Channel 1 (DQ) to CA3bit pattern.
5 Initialize the oscilloscope.
6 Set Channel 1 (DQ) to first value in calibration table.
7 Measure the Vamplitude on the oscilloscope and save the value.
8 Set Channel 1 (DQ) to next value in calibration table and repeat step 7 until last calibration table value.
9 Save the calibration table for modeling DQ Amplitude.

NOTE

This calibration is used for DQ Voltage Sensitivity Test and DFE Characterization.

DQS DCD Calibration

1 Set the Clk Gen to the selected Data Rate.
2 Set Channel 2 (DQS) to 0.4 V (for oscilloscope initialization).
3 Set Channel 2 (DQS) Offset to DQS offset (user set).
4 Set Channel 2 (DQS) to 01 pattern.
5 Initialize the oscilloscope.
6 Set Channel 2 (DQS) to first value in calibration table.
7 Measure DCD on the oscilloscope and save the value.
8 Set Channel 2 (DQS) to next value in calibration table and repeat step 7 until last calibration table value.
9 Save the calibration table for modeling DQS DCD.

NOTE

This calibration is used for DQS Jitter Sensitivity Test.

NOTE

For DQS DCD Calibration, the M8040A setup will use Trig Out.

DQS RJ Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 2 (DQS) to 0.4 V (for oscilloscope initialization).
3 Set Channel 2 (DQS) Offset to DQS offset (user set).
4 Set Channel 2 (DQS) to 01 pattern.
5 Initialize the oscilloscope.
6 Set Channel 2 (DQS) to first value in calibration table.
7 Measure RJ on the oscilloscope and save the value.
8 Set Channel 2 (DQS) to next value in calibration table and repeat step 7 until last calibration table value.

9 Save the calibration table for modeling DQS RJ.

NOTE

This calibration is used for DQS Jitter Sensitivity Test.

NOTE

For DQS RJ Calibration, the M8040A setup will use Trig Out.

DQ RJ Calibration

1. Set Clk Gen to the selected Data Rate.
2. Set Channel 1 (DQ) to 0.4 V (for oscilloscope initialization).
3. Set Channel 1 (DQ) Offset to DQ offset (user set or measured).
4. Set Channel 1 (DQ) to 01 pattern.
5. Initialize the oscilloscope.
6. Set Channel 2 (DQ) to first value in calibration table.
7. Measure RJ on the oscilloscope and save the value.
8. Set Channel 2 (DQ) to next value in calibration table and repeat step 7 until last calibration table value.
9. Save the calibration table for modeling DQ RJ.

NOTE

This calibration will be used for Rx Stressed Eye End to End Test.

DQ SJ Calibration

1. Set Clk Gen to the selected Data Rate.
2. Set Channel 1 (DQ) to 0.4 V (for oscilloscope initialization).
3. Set Channel 1 (DQ) Offset to DQ offset (user set or measured).
4. Set Channel 1 (DQ) to 01 pattern.
5. Initialize the oscilloscope.
6. Set Channel 2 (DQ) to first value in calibration table.
7. Measure SJ on the oscilloscope and save the value.
8. Set Channel 2 (DQ) to next value in calibration table and repeat step 7 until last calibration table value.

9 Save the calibration table for modeling DQ SJ.

NOTE This calibration will be used for Rx Stressed Eye End to End Test.

DQ Noise Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 1 (DQ) to PRBS 2^15-1.
3 Initialize the oscilloscope
4 Set AWG as “Interference Source”.
5 Apply Voltage Noise based on calibration table.
6 Measure the Vpeak-to-peak of the HIGH State region of the signal.
7 Repeat steps 5 and 6 until the last calibration table value.
8 Save the calibration table for modeling DQ Noise.

NOTE The DQ Noise Calibration is used for Rx Stressed Eye End to End test.

DQ Vref Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 1 (DQ) to 0.1V.
3 Set Channel 1 (DQ) to 000111 pattern.
4 Initialize the oscilloscope.
5 Set Channel 1 (DQ) to first value in calibration table.
6 Measure One mode level and zero mode level. Calculate the center.
7 Set Channel 1(DQ) to next value in calibration table and repeat step 6 until last calibration table value.
8 Save Vref values in cal table.

NOTE The DQ Vref at Device Ball for TP1 Calibration is used for Rx Stressed Eye End to End test.

DQ Stressed Eye Calibration

1 Set BERT to starting eye (Vswing 600mV and ISI).
2 Scale and setup both signals on scope.
3 Set to 2Mpt memory.
4 Save waveforms as .h5.
5 Transfer waveforms to PC running BERT.
6 Process waveforms in Matlab (Matlab will iterate adding noise and jitter until the eye size aligns with EH/EW).
7 Write data to table and configs.

DQS/DQ Measurement Utilities

DQS/DQ Measurement Utilities	Test ID	Description
DQS2DQ and DQ Vref Optimization	2110	DQS to DQ optimal alignment and DQ Vref is measured

DQS2DQ and DQ Vref Optimization

1 Set Vref to ideal setting 0.75V.
2 Set DQ amplitude to 800mV and DQ3bit pattern. This will ensure that Vref will not cause a fail.
3 Set DQS to 400mV amplitude.
4 Use parameter sweep to scan DQS2DQ delay across 4.5UI.
5 Calculate center of DQS2DQ passing region and set Channel 1 delay to this value.
6 Set DQ amplitude to 200mV. A tight amplitude will ensure we find a narrow range for Vref as well as not over drive beyond Vddq.
7 Use parameter sweep to scan Channel 1 (DQ) offset from 500mV to 1.1V.
8 Calculate center of Vref and set Channel 1 (DQ) offset to value.
9 Use parameter sweep to scan DQS2DQ delay one more time to verify that optimal Vref did not affect the exact center. Set Channel 1 (DQ)

Delay to center.

NOTE This optimization is used in all DQS/DQ tests.

Results Pass/Fail

CK/CA Calibrations

Overview This set of calibrations consists of the following calibrations:

Calibration	Test Id	Description
CK Amplitude Calibration	3101	Calibrates CK amplitude
CA Amplitude Calibration	3201	Calibrates CA amplitude
CK DCD Calibration	3102	Calibrates duty cycle distortion (DCD) for CK signal
CK RJ Calibration	3103	Calibrates random jitter for CK signal
CA Vref Calibration	3207	Calibrates Vref for CA signal.
CK (Trig Out) Amplitude Calibration	5101	Calibrates CK amplitude Note that this calibration is only available for M8040A BERT setup.
CA Amplitude at TP1 Calibration	13201	Calibrates CA amplitude at TP1
CA RJ at TP1 Calibration	13203	Calibrates random jitter for CA signal at TP1
CA SJ at TP1 Calibration	13204	Calibrates sinusoidal jitter for CA signal at TP1
CA Noise at TP1 Calibration	13208	Calibrates noise for stressed eye tests Note that this calibration is only available for M8040A BERT setup.
CA Vref at Device Ball for TP1 Calibration	13207	Calibrates Vref at Device Ball for TP1
CA Stressed Eye at TP1 Calibration	13206	Calibrates stressed eye at TP1

Connection Diagram Connect the instruments as shown in “Making Connections for CK/CA Calibrations and Tests” on page 78.

Configuration Parameters

You may modify the calibration-specific parameters listed under the **Configure** tab.

Procedure

NOTE

This section lists the general procedures for calibrations, irrespective of the test points at which these are taken.

CK Amplitude Calibration and CK (Trig Out) Amplitude Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 2 (CK) to 0.4 V (for oscilloscope initialization).
3 Set Channel 2 (CK) Offset to CK offset (user set).
4 Set Channel 2 (CK) to 01 pattern.
5 Initialize the oscilloscope.
6 Set Channel 2 (CK) to first value in calibration table.
7 Measure differential Vamplitude on the oscilloscope and save the value.
8 Set Channel 2 (CK) to next value in calibration table and repeat step 7 until last calibration table value.
9 Save the calibration table for modeling CK Amplitude.

NOTE

This calibration is used for CK Voltage Sensitivity Test.

NOTE

The CK (Trig Out) Amplitude Calibration uses the TRIG OUT of the BERT instead of PG CH2.

CA Amplitude Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 1 (CA) to 0.4 V (for oscilloscope initialization).
3 Set Channel 1 (CA) Offset to Vref (user set or measured).
4 Set Channel 1 (CA) to CA3bit pattern.
5 Initialize the oscilloscope.

6 Set Channel 1 (CA) to first value in calibration table.
7 Measure the Vamplitude on the oscilloscope and save the value.
8 Set Channel 1 (CA) to next value in calibration table and repeat step 7 until last calibration table value.
9 Save the calibration table for modeling CA Amplitude.

NOTE This calibration is used for CA voltage Sensitivity Test.

CK DCD Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 2 (CK) to 0.4 V (for oscilloscope initialization).
3 Set Channel 2 (CK) Offset to CK offset (user set).
4 Set Channel 2 (CK) to 01 pattern.
5 Initialize the oscilloscope.
6 Set Channel 2 (CK) to first value in calibration table.
7 Measure DCD on the oscilloscope and save the value.
8 Set Channel 2 (CK) to next value in calibration table and repeat step 7 until last calibration table value.
9 Save the calibration table for modeling CK DCD.

NOTE This calibration is used for CK Jitter Sensitivity Test.

NOTE For CK DCD Calibration, the M8040A setup will use Trig Out.

CK/CA RJ Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 2 (CK) to 0.4 V (for oscilloscope initialization).
3 Set Channel 2 (CK) Offset to CK offset (user set).
4 Set Channel 2 (CK) to 01 pattern.
5 Initialize the oscilloscope.

6 Set Channel 2 (CK) to first value in calibration table.
7 Measure RJ on the oscilloscope and save the value.
8 Set Channel 2 (CK) to next value in calibration table and repeat step 7 until last calibration table value.
9 Save the calibration table for modeling CK/CA RJ.

NOTE This calibration is used for CK Jitter Sensitivity Test.

NOTE For CK RJ Calibration, the M8040A setup will use Trig Out.

CA SJ Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 1 (CA) to 0.4 V (for oscilloscope initialization).
3 Set Channel 1 (CA) Offset to CA offset (user set or measured).
4 Set Channel 1 (CA) to 01 pattern.
5 Initialize the oscilloscope.
6 Set Channel 2 (CA) to first value in calibration table.
7 Measure SJ on the oscilloscope and save the value.
8 Set Channel 2 (CA) to next value in calibration table and repeat step 7 until last calibration table value.
9 Save calibration table for modeling CA SJ.

NOTE This calibration will be used for CA Stressed Eye End to End Test.

CA Noise Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 1 (DQ) to PRBS 2^15-1.
3 Initialize the oscilloscope
4 Set AWG as “Interference Source”.
5 Apply Voltage Noise based on calibration table.

6 Measure the Vpeak-to-peak of the HIGH State region of the signal.
7 Repeat steps 5 and 6 until the last calibration table value.
8 Save the calibration table for modeling DQ Noise.

NOTE This calibration will be used for CA Rx Stressed Eye End to End Test.

CA Vref Calibration

1 Set Clk Gen to the selected Data Rate.
2 Set Channel 1 (CA) to 0.1V.
3 Set Channel 1 (CA) to 000111 pattern.
4 Initialize the oscilloscope.
5 Set Channel 1 (CA) to first value in calibration table.
6 Measure One mode level and zero mode level. Calculate the center.
7 Set Channel 1(CA) to next value in calibration table and repeat step 6 until last calibration table value.
8 Save Vref values in cal table.

NOTE The CA Vref at Device Ball for TP1 calibration is used for CA Rx Stressed Eye End to End test.

CA Stressed Eye Calibration

1 Set BERT to starting eye (Vswing 600mV and ISI).
2 Scale and setup both signals on scope.
3 Set to 2Mpt memory.
4 Save waveforms as .h5.
5 Transfer waveforms to PC running BERT.
6 Process waveforms in Matlab (Matlab will iterate adding noise and jitter until the eye size aligns with EH/EW).
7 Write data to table and configs.

CK/CA Measurement Utilities

CK/CA Measurement Utilities	Test ID	Description
CK to CA and CA Vref Optimization	3110	CK to CA optimal alignment and CA Vref is measured.

CK to CA and CA Vref Optimization

1 Set Vref to ideal setting 0.8V.
2 Set CA amplitude to 800mV and CA3bit pattern. This will ensure that Vref will not cause a fail.
3 Set CK to 400mV amplitude.
4 Use parameter sweep to scan CK to CA delay across 7.5UI.
5 Calculate center of CK to CA passing region and set Channel 1 delay to this value.
6 Set CA amplitude to 200mV. A tight amplitude will ensure we find a narrow range for Vref as well as not over drive beyond Vdd.
7 Use parameter sweep to scan Channel 1 (CA) offset from 500mV to 1.1V.
8 Calculate center of Vref and set Channel 1 (CA) offset to value.
9 Use parameter sweep to scan CK to CA delay one more time to verify that optimal Vref did not affect the exact center. Set Channel 1 (CA) Delay to center.

NOTE This optimization is used in all CK/CA tests.

Results Pass/Fail

Testing the stressed DUT receiver compliance

The M80885RCA software offers several automated receiver test procedures divided into two groups - DQS/DQ Tests and CK/CA Tests.

Configuring receiver tests settings

Depending on the tests being performed, specific settings must be made prior to starting a receiver test. The receiver test related configuration variables have been divided in two test-specific sub-groups, DQS/DQ Tests and CK/CA Tests. Figure 41 shows the DQS/DQ Tests configuration variables.

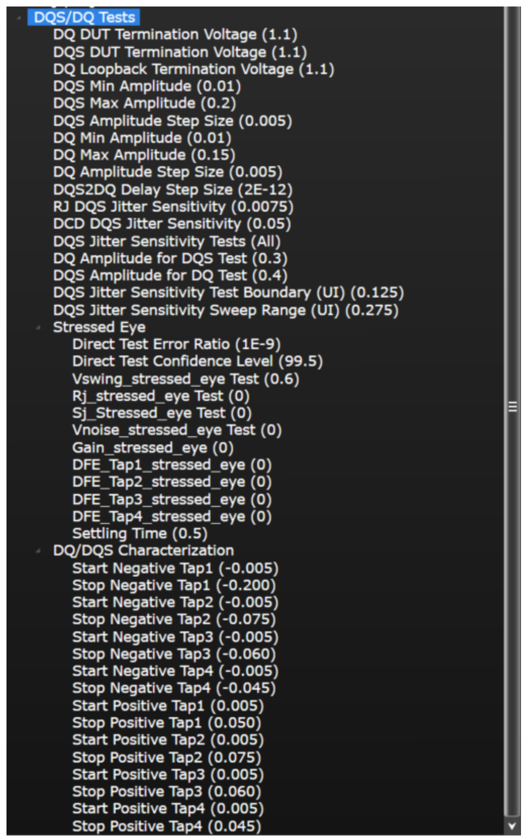


Figure 41 Configuration variables for receiver testing

Receiver tests

DQS/DQ Tests

Overview This set of tests consists of the following:

Test	Test Id	Description
DQS Voltage Sensitivity Test	6100	Tests the voltage sensitivity of the DQS signal
DQ Voltage Sensitivity Test	6101	Tests the voltage sensitivity of the DQ signal
DQS Jitter Sensitivity Test	6102	Tests the jitter sensitivity of the DQS signal
DQS2DQ Test	6104	DQS2DQ Test
Rx Stressed Eye End to End Test (TP1 cal)	16103	Rx Stressed Eye Test using the TP1 calibration
DFE Characterization Tap1	6105	DFE Characterization for Tap1
DFE Characterization Tap2	6106	DFE Characterization for Tap2
DFE Characterization Tap3	6107	DFE Characterization for Tap3
DFE Characterization Tap4	6108	DFE Characterization for Tap4

Connection Diagram Connect the instruments as shown in "Making Connections for DQS/DQ Loopback Tests" on page 68.

Configuration Parameters You may modify the test-specific parameters listed under the **DQS/DQ Tests** section under the **Configure** tab.

Procedure

DQS Voltage Sensitivity

Pattern: 1010

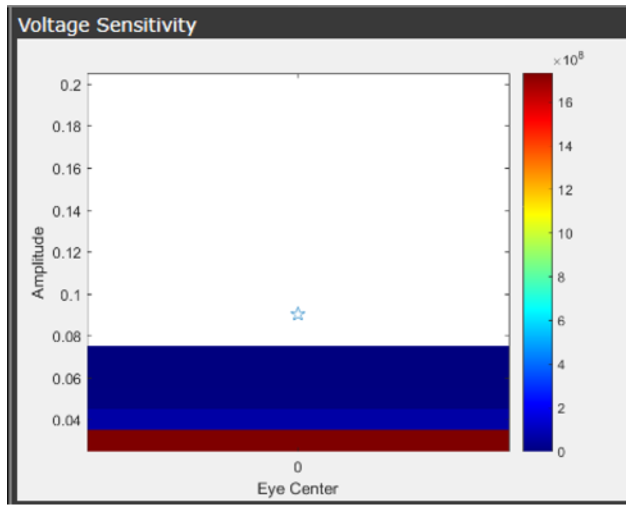
Impairments: No jitter or noise. No parallel signaling; this minimizes crosstalk.

Calibrations: Calibrate voltage settings to receiver input

Procedure:

1 Set DQS to DQ skew to optimum (always passing).
2 Set DQ voltage to always passing.
3 Set DQS voltage to always passing.
4 Decrease DQS amplitude in voltage step size defined by user.
5 Record error.

6 Continue steps 4 and 5 until large number of errors are recorded.
7 Plot voltage BER curve.



DQ Voltage Sensitivity

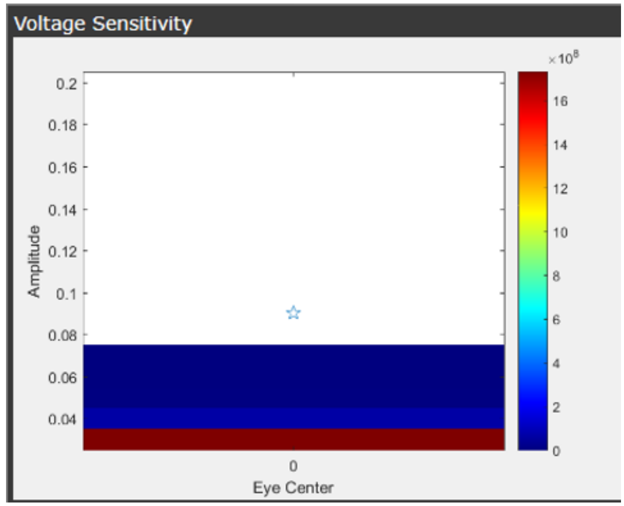
Pattern: PRBS and 1010

Impairments: No jitter or noise. No parallel signaling; this minimizes crosstalk.

Calibration: Calibrate voltage settings to receiver input

Procedure:

1 Write train and/or set best Vref.
2 Set DQS to DQ skew to optimum (always passing).
3 Set DQ voltage to always passing – centered around Vref.
4 Set DQS voltage to always passing.
5 Decrease DQ amplitude around Vref in voltage step size defined by user via DQS2DQ Delay Step Size.
6 Record error.
7 Continue steps 4 and 5 until large number of errors are recorded.
8 Plot voltage versus delay BER curve – eye defined by cross section at desired BER.



DQS Jitter Sensitivity

NOTE Run this test only after passing DQS and DQ voltage sensitivity tests.

Pattern: 1010

Impairments: All other lanes “set up to create a system-like noise condition on the power grid”; DQ is jitter and noise free (except correlated jitter).

1 No injected Rj, only duty cycle distortion (UI DCD) of tRx_DQS_DCD_DQS.
2 No duty cycle distortion, only injected Rj between 0UI to tRx_DQS_Rj_DQS.
3 Duty cycle distortion (UI-DCD) and injected Rj applied simultaneously, as specified in the parameter tRx_DQS_DCD_Rj_DQS.

Calibration: Calibrate voltage settings to receiver input. Calibrate jitter settings to receiver input.

Procedure:

1 Write train and/or set best Vref.
2 Set DQS to DQ skew to optimum (always passing). CLK must be aligned with DQS.
3 Set DQS voltage to always passing.
4 Set DQS to no jitter.
5 Skew DQS2DQ across DQ eye and measure DQ error.
6 Record error – tRx_DQ_tMargin.
7 Reset DQS skew to always passing.
8 Inject tRx_DQS_DCD_DQS.
9 Skew DQS2DQ across DQ eye and measure DQ error.
10 Record ΔtRx_DQ_tMargin_DCD_DQS <-results compared to tRx_DQ_tMargin.
11 Reset DQS skew to always passing.
12 Remove DCD stress, inject tRx_DQS_Rj_DQS.
13 Skew DQS2DQ across DQ eye and measure DQ error.
14 Record ΔtRx_DQ_tMargin_rj_DQS <- results compared to tRx_DQ_tMargin.
15 Reset DQS skew to always passing.
16 Add tRx_DQS_DCD_DQS.
17 Skew DQS2DQ across DQ eye and measure DQ error.
18 Record ΔtRx_DQ_tMargin_DCD_Rj_DQS.
19 Repeat steps 3 to 18 for user-defined steps of DQS/DQ skew. (according to the specification, this step is optional)
20 Four BER results are created and compared. Plot is similar to DQ Voltage Sensitivity, but four graphs only in the X direction.

DQS2DQ Test

Pattern: 1010

Impairments: No jitter or noise, DC to surrounding pins to minimize crosstalk

Calibrations: Calibrate DQS DQ timing relationship to receiver input

Procedure:

1 Set DQS to DQ skew to optimum (always passing).
2 Set DQ voltage to always passing.

3 Set DQS voltage to always passing.
4 Sweep DQS to DQ timing from -1UI of DQS2DQ start to +1UI after DQS2DQ end.
5 Record error.

Rx Stressed Eye End to End Test

Pattern: 1010

Impairments: Physical channel, noise/jitter as defined (JESD79-5C_v1.30 section 8.10.1 Parameters for DDR5 Rx Stressed Eye Tests).

Calibrations: RJ, SJ, SI and Eye at DUT

Procedure:

1 Initialize device (dll speed, ODT 48 ohms, pda etc).
2 Set DFE to values found in calibration.
3 Set loopback.
4 Set all stresses and signals as from cal.
5 Scan DQS2DQ across UI to user defined Vref step size. First scan is 5.3e6 to get eye.
6 Scan widest portion of eye and highest portion of eye to full BER.
7 Eye needs to pass EH and EW spec.

DFE Characterization

Procedure:

1 Set device to no DFE.
2 Set BERT to a single bit transition pattern for DQ.
3 Scan for optimal DQS and DQ alignment.
4 Once aligned, scan offset of DQ (channel 1).
5 Set device DFE to next step.
6 Scan offset of DQ.
7 Continue through the rest of the DFE steps.
8 Calculate DFE steps by finding the difference in offset of each step.

CK/CA Tests

Overview This set of tests consists of the following tests:

Calibration	Test Id	Description
CK Voltage Sensitivity Test	7100	Tests the voltage sensitivity of the CK signal
CA Voltage Sensitivity Test	7101	Tests the voltage sensitivity of the CA signal
CK Jitter Sensitivity Test	7102	Tests the jitter sensitivity of the CK signal
CA Rx Stressed Eye End to End Test (TP1 cal)	17103	CA Rx Stressed Eye End to End Test (TP1 cal)

Connection Diagram Connect the instruments as shown in "Making Connections for CK/CA Loopback Tests" on page 80.

Configuration Parameters You may modify the calibration-specific parameters listed under the **CK/CA Tests** section under the **Configure** tab.

Procedure

NOTE For these tests, there is a requirement for CK to be set up to run continuously. The Initialize CK utility sets up CK on Channel 2 for continuous operation.

CK Voltage Sensitivity

Pattern: 1010

Impairments: No jitter or noise. No parallel signaling; this minimizes crosstalk.

Calibrations: Calibrate voltage settings to receiver input

Procedure:

1 Set CK to CA skew to optimum (always passing).
2 Set CA voltage to always passing.
3 Set CK voltage to always passing.
4 Decrease CK amplitude in voltage step size defined by user.
5 Record error.
6 Continue steps 4 and 5 until large number of errors are recorded.
7 Plot voltage BER curve.

CA Voltage Sensitivity

Pattern: PRBS and 1010

Impairments: No jitter or noise. No parallel signaling; this minimizes crosstalk

Calibration: Calibrate voltage settings to receiver input

Procedure:

1 Write train and/or set best Vref.
2 Set CK to CA skew to optimum (always passing).
3 Set CA voltage to always passing – centered around Vref.
4 Set CK voltage to always passing.
5 Decrease CA amplitude around Vref in voltage step size defined by user via CK CA Delay Step Size.
6 Record error.
7 Continue steps 4 and 5 until large number of errors are recorded.
8 Plot voltage versus delay BER curve – eye defined by cross section at desired BER.

CK Jitter Sensitivity

NOTE Run this test only after passing CK and CA voltage sensitivity tests.

Pattern: 1010

Impairments: All other lanes “set up to create a system-like noise condition on the power grid”; CA is jitter and noise free (except correlated jitter).

1 No injected Rj, only duty cycle distortion (UI DCD) of tRx_DQS_DCD_DQS.
2 No duty cycle distortion, only injected Rj between 0UI to tRx_DQS_Rj_DQS.
3 Duty cycle distortion (UI-DCD) and injected Rj applied simultaneously, as specified in the parameter tRx_DQS_DCD_Rj_DQS.

Calibration: Calibrate voltage settings to receiver input. Calibrate jitter settings to receiver input.

Procedure:

1 Write train and/or set best Vref.
2 Set CK to CA skew to optimum (always passing). CLK must be aligned with CK.
3 Set CK voltage to always passing.
4 Set CK to no jitter.
5 Skew CK2CA across CA eye and measure CA error.
6 Record error – tRx_DQ_tMargin.
7 Reset CK skew to always passing.
8 Inject tRx_DQS_DCD_DQS.
9 Skew CK2CA across CA eye and measure CA error.
10 Record ΔtRx_DQ_tMargin_DCD_DQS <-results compared to tRx_DQ_tMargin.
11 Reset CK skew to always passing.
12 Remove DCD stress, inject tRx_DQS_Rj_DQS.
13 Skew CK2CA across CA eye and measure DQ error.
14 Record ΔtRx_DQ_tMargin_rj_DQS <- results compared to tRx_DQ_tMargin.
15 Reset CK skew to always passing.
16 Add tRx_DQS_DCD_DQS.
17 Skew CK2CA across CA eye and measure CA error.
18 Record ΔtRx_DQ_tMargin_DCD_Rj_DQS.
19 Repeat steps 3 to 18 for user-defined steps of CK/CA skew. (according to the specification, this step is optional)
20 Four BER results are created and compared. Plot is similar to CA Voltage Sensitivity, but four graphs only in the X direction.

CA Rx Stressed Eye End to End Test

Pattern: 1010

Impairments: Physical channel, noise/jitter as defined (JESD79-5C_v1.30 section 8.10.1 Parameters for DDR5 Rx Stressed Eye Tests).

Calibrations: RJ, SJ, SI and Eye at DUT

Procedure:

1 Initialize device (dll speed, ODT 48 ohms, pda etc).
2 Set DFE to values found in calibration.

3 Set loopback.
4 Set all stresses and signals as from cal.
5 Scan CK2CA across UI to user-defined Vref step size. First scan is 5.3e6 to get eye.
6 Scan widest portion of eye and highest portion of eye to full BER.
7 Eye needs to pass EH and EW spec.

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