D9042DPPC/D9342DPPC DisplayPort UHBR Compliance Test Application

KEYSIGHT

METHODS OF IMPLEMENTATION

Notices

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DisplayPort Automated Testing—At A Glance

NOTE The tests performed by the DisplayPort UHBR Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

You may refer to the following specification documents for compliance testing measurements. For more information, see the VESA web site at www.vesa.org.

Reference Documents
VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)
VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)

The Keysight D9042DPPC DisplayPort UHBR Compliance Test Application helps to verify compliance of the DisplayPort 2.1 devices with DisplayPort specifications for UHBR only using Keysight Infiniium Digital Storage Oscilloscopes with bandwidths of 21 GHz or higher. The DisplayPort UHBR Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.
- Allows to analyze saved waveforms or simulated waveforms in offline mode

Required Equipment and Software

In order to run the DisplayPort UHBR automated tests, you need the following equipment and software:

- Use one of the following oscilloscope models:
  - For D9042DPPC DisplayPort UHBR Test Application:
    - Z Series Oscilloscopes
    - V Series Oscilloscopes
    - UXR-B Series Oscilloscopes
  - For D9342DPPC DisplayPort UHBR Test Application:
    - XR8 Series Oscilloscopes
    - UXR-B Series Oscilloscopes
- The minimum version of Infiniium Oscilloscope Software (see the D9042DPPC/D9342DPPC DisplayPort UHBR Compliance Test Application Release Notes)
- D9042DPPC/D9342DPPC DisplayPort UHBR Compliance Test Application
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope)
- D9042DPPC/D9342DPPC DisplayPort UHBR Compliance Test Application license

In order to run the automated tests on DisplayPort DUTs, you need the following fixtures and accessories:

- DisplayPort Test Point Adapter:

For DUT Type	Required Fixtures/Accessories (Recommended)	Quantity
Source	For USB Type-C Connector ▪ N7015A Type-C High-Speed Test Fixture For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P*	1 (each)

* All Wilder Technologies Test Point Adapters require the Wilder Technologies DP-TPA-A Aux Control Board.

Required Fixtures/Accessories	Quantity
Low insertion loss phase matched cables @ 40 GHz **	2 pair

**Low insertion loss phase matched cables accessories (recommended)

- Controller (Optional)

Testing Type	Supported Fixtures/Accessories (Optional)	Quantity
For Alt Mode Control	Keysight N7018A Type-C Test Controller	1

- Supported Probes

  DisplayPort UHBR apps currently supports the following probes:
  - MX0025A InfiniiMax Ultra Probe Amplifier, 25 GHz
  - N2802A InfiniiMax III Series Probe Amplifier, 25 GHz
  - N2803A InfiniiMax III Series Probe Amplifier, 30 GHz

In This Book

This manual describes the tests that are performed by the DisplayPort UHBR Compliance Test Application in more detail; it contains information from (and refers to) various DisplayPort specifications and it describes how the tests are performed.

- Chapter 1, “Installing the DisplayPort UHBR Compliance Test Application” shows how to install and license the automated test application (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” shows how to start the DisplayPort UHBR Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, “DisplayPort UHBR Source Tests” describes the normative and informative tests for compliance verification of DisplayPort UHBR source devices.

See Also

- The DisplayPort UHBR Compliance Test Application's Online Help, which describes:
  - Keysight DisplayPort UHBR Automated Testing—At a Glance
  - Starting the Keysight DisplayPort UHBR Test Application
  - Creating or Opening a Test Project
  - Setting Up the Test Environment
  - Selecting Tests
  - Configuring Tests
  - Verifying Physical Connections
  - Running Tests
  - Configuring Automation in the Test Application
  - Viewing Results
  - Viewing HTML Test Report
  - Exiting the Test Application
  - Additional Settings in the Test App

Contents

1 Installing the DisplayPort UHBR Compliance Test Application

If you have purchased the D9042DPPC/D9342DPPC DisplayPort UHBR Compliance Test Application separate from your oscilloscope you must install the software and the license key.

Installing the Test Application

1. Make sure that you have the minimum required version of the Infiniium oscilloscope software (see the D9042DPPC/D9342DPPC test application release notes for the related info). In order to check the version of the Infiniium oscilloscope software installed on your system, please open the software and select **Help > About Infiniium...** from the main menu.
2. To download the DisplayPort UHBR Compliance Test Application, please visit the Keysight website:
   - http://www.keysight.com/find/D9042DPPC
   - http://www.keysight.com/find/D9342DPPC
3. On the web page, please navigate to **Trials and Licenses** tab> click **Details & Download** button. In the **Current Version** tab, click the **Download** button to begin the download. You may be required to enter your details like, Email Address, Last Name, and First Name for the download to start.
4. Once the file is downloaded, open the file location, double click the executable file, and follow the general installation instructions.
5. When the installation process is completed, please restart the Infiniium oscilloscope software and the test application name should be visible in the **Analyze menu > Automated Test Apps** list. If license is not installed, the application will appear under the **Unlicensed Apps** option in the **Analyze** menu.

Installing the License Key

To procure a license, you require the Ethernet Address information that is displayed in the Keysight Software Manager Utility installed on the same machine where you wish to install the license.

Using Keysight Software Manager Utility

To view and copy the Ethernet Address from Keysight Software Manager Utility:

1. Launch **Keysight Software Manager Utility** on the machine where you wish to run the Test Application and its features.
2. Copy the **Ethernet Address**, which is a set of alphanumeric values (as highlighted in Figure 1) that appears in the **Add License** tab of the application.

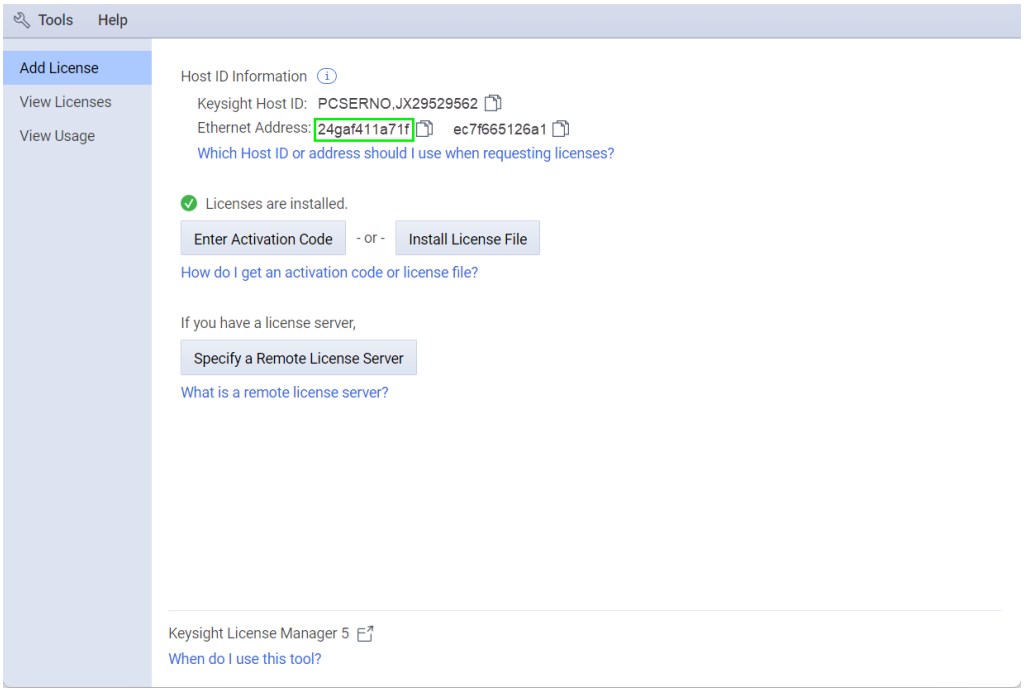


Figure 1 Viewing the Ethernet Address

To install one of the procured licenses using the Keysight Software Manager Utility application:

1 Save the license files on the machine where you wish to run the Test Application and its features.

2 Launch Keysight Software Manager Utility.

3 In the **Add License** tab (Figure 2), use one of the options to install the license file.

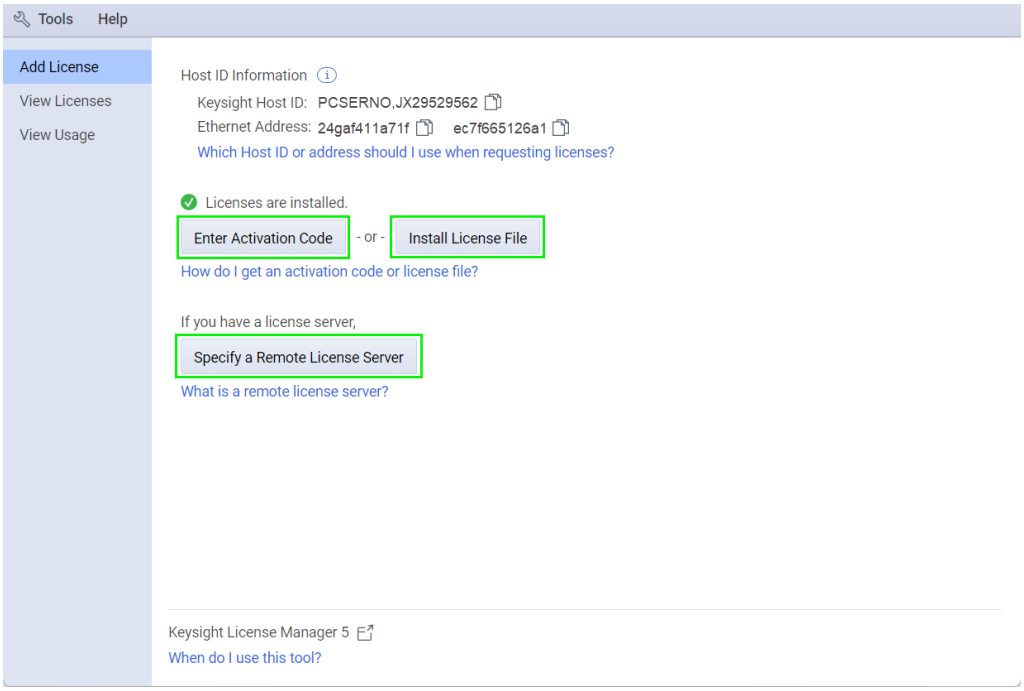


Figure 2 License installation options

For more information regarding installation of procured licenses in Keysight Software Manager Utility, refer to **Supporting Documentation** section on the Keysight Software Manager Utility web page.

2 Preparing to Take Measurements

Before running the automated tests, you must acquire the appropriate test fixtures, and you should calibrate the oscilloscope and probe. After the oscilloscope and probe have been calibrated, you are ready to start the DisplayPort UHBR Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

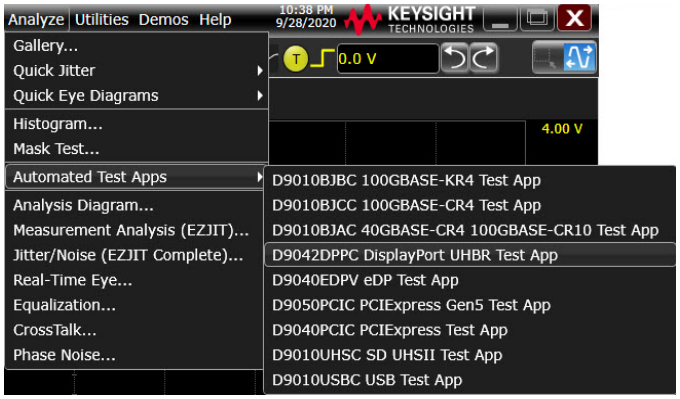
If you haven't already calibrated the oscilloscope and probe, please refer to the documentation for the Infiniium Oscilloscope being used for testing, to know more about Calibration procedures. This step is not applicable to offline mode of DisplayPort UHBR Compliance Test Application.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DisplayPort UHBR Compliance Test Application

1 From the Infiniium oscilloscope's main menu, choose **Analyze > Automated Test Apps > D9042DPPC/D9342DPPC DisplayPort UHBR Test App**.



2 From the Infiniium 2026 Oscilloscope's main menu, click **Tools > Apps > Automated Test Apps > D9342DPPC DisplayPort UHBR Test App.**

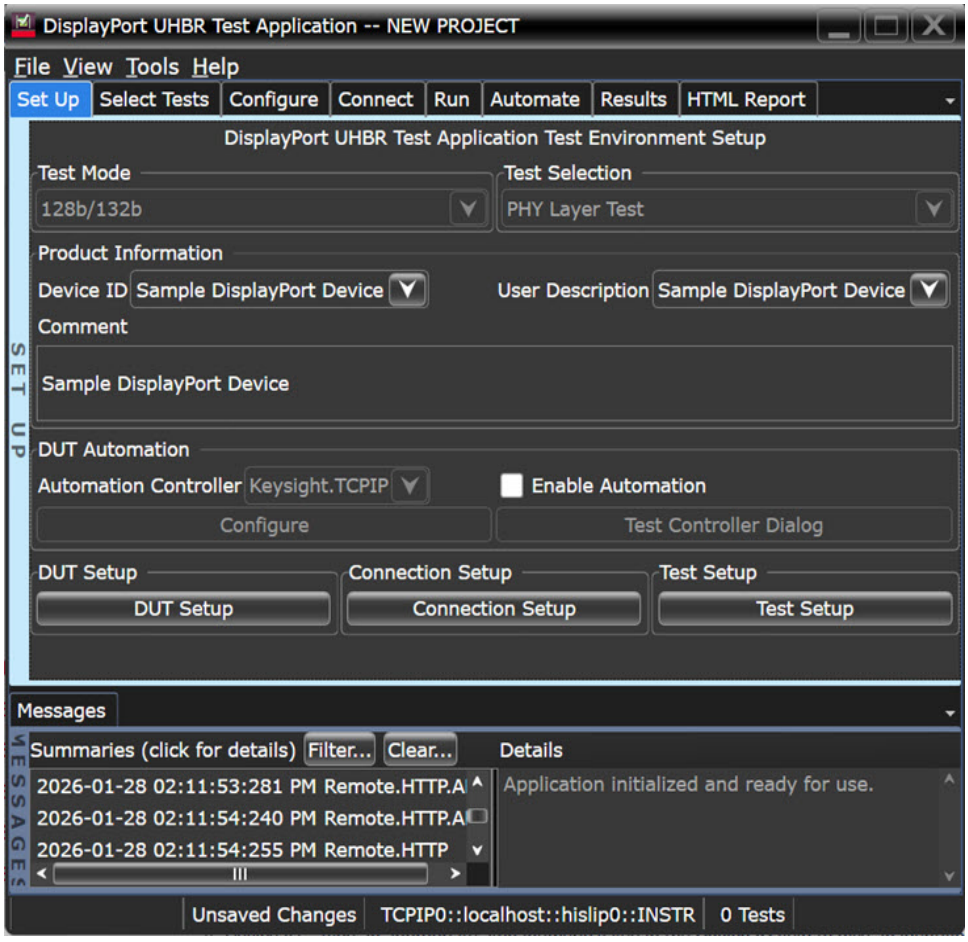


Figure 3 Default View of the DisplayPort UHBR Compliance Test Application

NOTE If DisplayPort Test does not appear in the Automated Test Apps menu, the DisplayPort UHBR Compliance Test Application has not been installed (see Chapter 1, "Installing the DisplayPort UHBR Compliance Test Application).

NOTE To understand the functionality of the various features in the user interface of the test application, please refer to the Keysight D9042DPPC/D9342DPPC DisplayPort UHBR Compliance Test Application Online Help available in the **Help** menu. You may also visit the **Document Library** section of the product page to download the document:

http://www/keysight.com/find/D9042DPPC

http://www/keysight.com/find/D9342DPPC

Figure 3 shows the DisplayPort UHBR Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests.

Table 1 DisplayPort UHBR Application Tabs and their Description

Tab	Description
Set Up	Lets you identify and set up the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically, so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (for example, channels used in test, voltage levels, etc.).
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Lets you construct scripts using commands that drive execution of the application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE In the **Configure** tab, the values for all such Configuration parameters that are Oscilloscope-dependent, will correspond to the Oscilloscope Model (DSOs or UXRs), with which you are running the test application.

3 DisplayPort UHBR Source Tests

This chapter describes the DisplayPort UHBR source tests.

Overview

This section describes the normative and informative main link physical layer tests for compliance verification of DisplayPort UHBR source devices.

Test Point Definition for DisplayPort UHBR Tests

Five different test points are identified for the physical layer measurement. See Figure 4

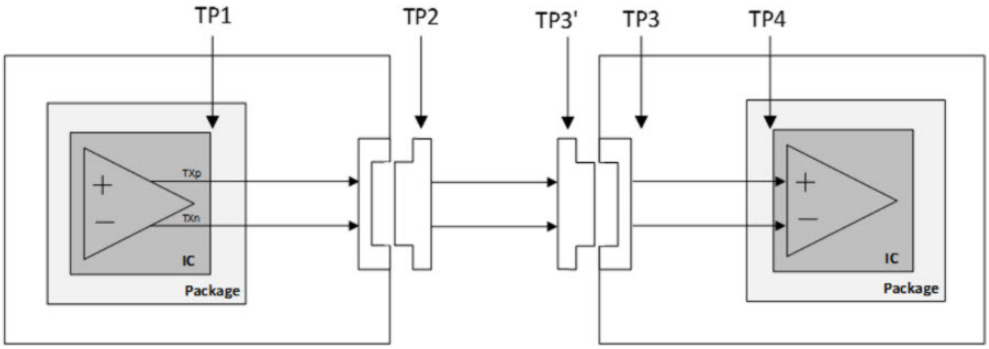


Figure 4 Test Points in a DisplayPort InterConnect System

Table 2 defines the Test Points used for various DisplayPort Tests.

Table 2 Test Points for DisplayPort Tests

Test Point	Description
TP1	Located at the transmitter device's pins
TP2	Located at the test interface on a Test Point Access fixture, as close as possible to the DP-mated connection to a DP Source device
TP2_CTLE	RX Jitter Tolerance calibration and testing interface point of DUT with plug
TP3	Located at the test interface on a Test Point Access fixture, as close as possible to the DP-mated connection to a DP Sink device
TP3'	Used for signal injection point to a DP Sink device (receptacle DUT)
TP3_EQ	TP3 using a defined cable model with an equalizer applied. There are two defined cable models: ▪ Worst-case cable model ▪ Zero-length, zero-loss cable
TP3_CTLE	TP3 using a defined cable model with CTLE applied
TP3_DFE	TP3 using a defined cable model with CTLE and DFE applied.
TP4	Located at the receiver's package pins.
TPRX	Located at the receiver IC's pads.
TPRX_CTLE	TPRX using a defined cable model and a defined DPRX device model with CTLE applied.
TPRX_DFE	TPRX using a defined cable model and a defined DPRX device model with CTLE and DFE applied.

UHBR Connectivity

The UHBR10 PHY Electrical Specification is defined so that UHBR10-capable devices inter-operate when connected using a detachable DP8K cable or USB Super Speed Gen 1-only Type-C cable (see Figure 5), as well as a DPRX with a tethered USB Type-C plug cable (see Figure 6). UHBR10-capable devices may use DP, mDP, or USB Type-C connectors. UHBR13.5- and UHBR20-capable devices are currently specified to use only a DPRX with a tethered USB Type-C plug cable (see Figure 6).

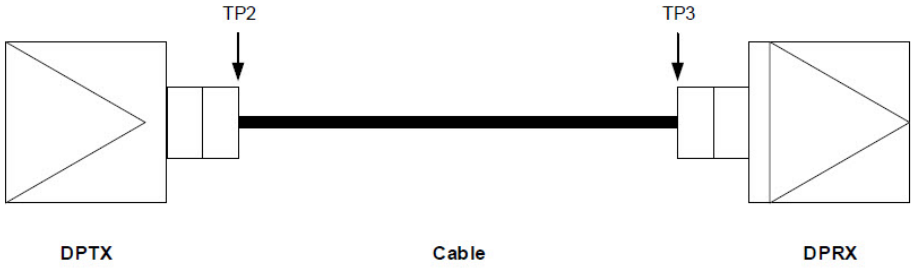


Figure 5 DPTX and DPRX Connected by way of a Detachable Cable

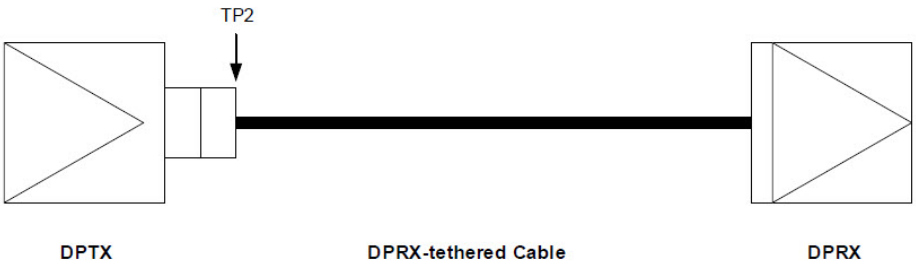


Figure 6 DPRX with a Tethered USB Type-C Plug Cable

Transmitter Equalization and Presets

A UHBR-capable DPTX shall implement a 3-tap equalization. The DPTX applies transmitter coefficients, as illustrated in Figure 7. Individual coefficients may be positive or negative values. C0 may be 0 < C0 < 1. C-1 and C+1 shall be 0 or a negative value.

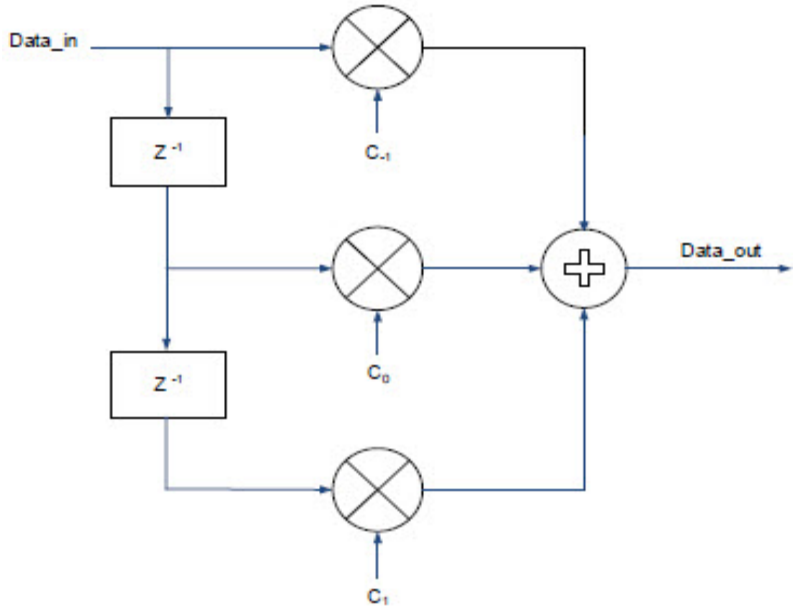


Figure 7 3-tap FFE Example

where:

- Z^{-1} = Delay element, 1-unit interval
- C_i = Transmitter FFE (FIR) equalization coefficients; index i is the location relative to the main cursor (preshoot, cursor, or post cursor)

$$Preshoot = 20 \times log_{10} \times \frac{-C_{-1} + C_0 + C_1}{C_{-1} + C_0 + C_1}$$

$$De\text{-}emphasis = 20 \times log_{10} \times \frac{C_{-1} + C_0 + C_1}{C_{-1} + C_0 - C_1}$$

Figure 8 FFE Coefficients

Table 3 Preset FFE Coefficients [a] [b]

Preset	Pre-shoot (dB)	De-emphasis (dB)	Informative Filter Coefficients		
			C_{-1}	C_0	C_{+1}
0	0	0	0	1	0
1	0	-1.9	0	0.90	-0.10
2	0	-3.6	0	0.83	-0.17
3	0	-5.0	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8.0	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.6	0	0.17	0.83	0
15	1.7	-1.7	-0.05	0.55	-0.05

a The coefficients are normalized such that $|C_{-1}| + C_0 + |C_1|$ corresponds to full output swing that is 800 mV_diff_pp nominal. Preset configuration 15 represents operation mode that has a lower transmitter swing.

b See Figure 8, to know how preshoot and de-emphasis are calculated.

Reference Receiver Clock Data Recovery

All measurement are performed after the effects of a Reference Receiver CDR will require the clock recovery technique of the Reference Receiver CDR in Section 3.5.5.4 of the VESA DisplayPort (DP) Standard Version 2.1 (October 22, 2022).

The CDR can be modeled by a 2nd order PLL response that derives the following jitter transfer function, described in the Laplace domain as follows:

$$H_{jitter}(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

where:

- s = Frequency in the Laplace domain
- ζ = Damping factor, 0.94
- ω_n = System's natural frequency, 2.2E7rad/sec

The observed jitter transfer function (OJTF) shall be as illustrated in Figure 9.

NOTE In contrast to the OJTF for UHBRx Reference Receiver CDRs, which is a high-pass filter, the Reference Receiver CDRs for bit rates up to HBR3 are defined as jitter tracking function (JTF), which is a low-pass filter.

Bit Rate	Bandwidth	Damping Factor
UHBR10	5 MHz	0.94
UHBR13.5	5 MHz	0.94
UHBR20	5 MHz	0.94

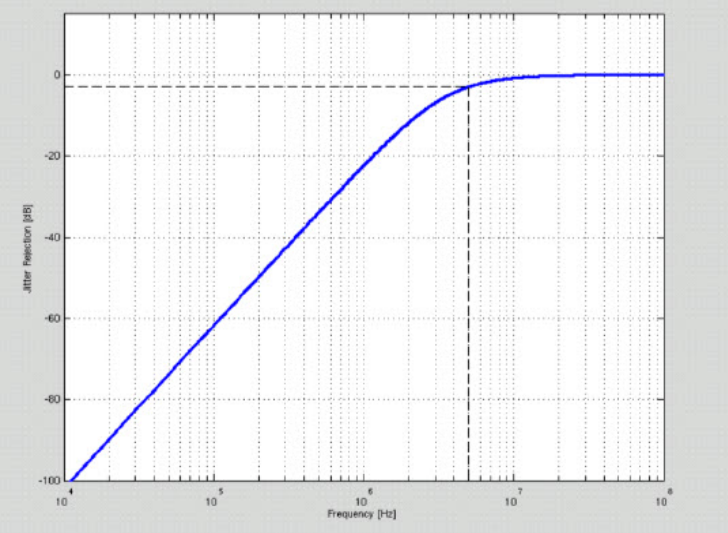


Figure 9 UHBRx Reference Receiver CDR OJTF

Reference Receiver Equalization

All the measurements done at the TP3_EQ, should be referenced to a reference receiver equalization function, that is, all measurements shall be performed after applying appropriate equalization on the measured signals. The reference receiver applied at TP3_EQ comprises of parametric Continuous-Time-Linear-Equalizer (CTLE) and Decision-Feedback-Equalizer (DFE), as described below.

For UHBR10

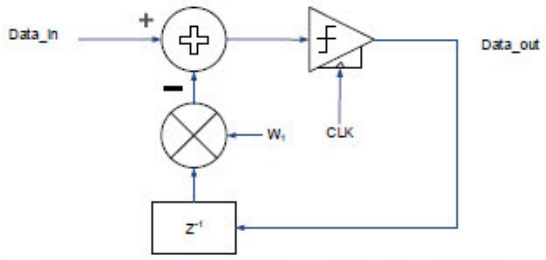
The Reference Receiver CTLE for UHBR10 is defined by the following equation.

$$H(s) = 1.496 \times \omega_{p2} \times \frac{\left(s + \frac{A_{DC}}{1.496} \times \omega_{p1}\right)}{(s + \omega_{p1}) \times (s + \omega_{p2})}$$

where:

- $A_{AC} = 3.5\text{dB}$
- $A_{DC} = \left\{10^{\frac{-x}{20}}: x = 0, 1, 2, , , 9[dB]\right\}$
- $\omega_{p1} = 2\pi \times 1E9 \frac{rad}{sec}$
- $\omega_{p2} = 2\pi \times 8E9 \frac{rad}{sec}$

For UHBR10, a Reference Receiver DFE is necessary to equalize channel loss. For UHBR10, a 1-tap Reference Receiver DFE, such as the one illustrated in following figure, is mandatory.



where:

- Z^{-1} = Delay element, 1-unit interval.
- W = Tap weight or coefficient applied to the feedback sum relative to the delay. Up to 50mV for a 1-tap DFE.

For UHBR13.5

The informative Reference Receiver CTLE for UHBR13.5 is defined by the following equation.

$$H(s) \triangleq 1.41 \times \omega_{p2} \times \frac{\left(s + \frac{A_{DC}}{1.41} \times \omega_{p1}\right)}{(s + \omega_{p1}) \times (s + \omega_{p2})}$$

where:

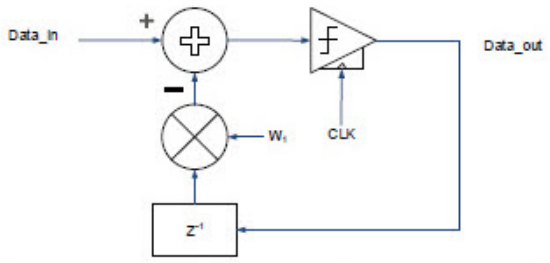
- $A_{AC} = 3.0\text{dB}$

  $A_{DC} = \left\{10^{\frac{-x}{20}} : x = 0, 1, 2, , , 9[dB]\right\}$

- $\omega_{p1} = 2\pi \times 5E9 \frac{rad}{sec}$

- $\omega_{p2} = 2\pi \times 10E9 \frac{rad}{sec}$

For UHBR13.5, a Reference Receiver DFE is necessary to equalize channel loss. For UHBR13.5, a 1-tap Reference Receiver DFE, such as the one illustrated in following figure can be used.



where:

- Z^{-1} = Delay element, 1-unit interval.
- W = Tap weight or coefficient applied to the feedback sum relative to the delay. Up to 50mV for a 1-tap DFE.

The informative Reference Receiver CTLE for UHBR20 is defined by the following equation.

For UHBR20

The Reference Receiver CTLE for UHBR20 is defined by the following equation.

$$H(s) = 1.41 \times \omega_{p2} \times \frac{(s + \frac{A_{DC}}{1.41} \times \omega_{p1})}{(s + \omega_{p1}) \times (s + \omega_{p2})}$$

where:

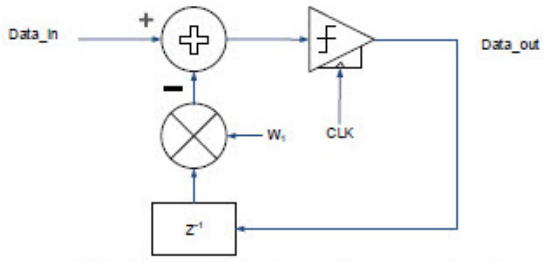
- $A_{AC} = 3.0\text{dB}$

  $A_{DC} = \{10^{\frac{-x}{20}}: x = 0, 1, 2, , , 9[dB]\}$

- $\omega_{p1} = 2\pi \times 5E9 \frac{rad}{sec}$

- $\omega_{p2} = 2\pi \times 10E9 \frac{rad}{sec}$

For UHBR20, a Reference Receiver DFE is necessary to equalize channel loss. For UHBR20, a 1-tap Reference Receiver DFE, such as the one illustrated in following figure can be used.



where:

- Z^{-1} = Delay element, 1-unit interval.
- W = Tap weight or coefficient applied to the feedback sum relative to the delay. Up to 50mV for a 1-tap DFE.

Bandwidth Limit

The oscilloscope bandwidth will be limited to following bandwidth for different UHBR bit rate:

Table 4 Oscilloscope bandwidth limit

Bit Rate	Bandwidth
UHBR10	16 GHz
UHBR13.5	21 GHz
UHBR20	21 GHz

Setting Up the Compliance Test Application for DisplayPort UHBR Source Tests:

Before you run the compliance tests on the Device Under Test (DUT):

1 Connect the appropriate test fixture to the DUT.

2 Start the automated testing application as described in "Starting the DisplayPort UHBR Compliance Test Application" on page 23.

3 The **Set Up** tab on the DisplayPort UHBR Compliance Test Application is displayed by default (see Figure 3).

4 To test for compliance with DisplayPort Standard Version 2.1, the option **Source** appears by default in the **Device Type** drop-down options.

5 Select the **Connector Type** as **USB Type-C**, **Enhanced FsDP**, or **Enhanced mDP**, as required.

6 Select the **DUT Lane Count** as **1 Lane, 2 Lanes,** or **4 Lanes.**

7 Select the **Bit Rate** as **10 Gbps**, **13.5 Gbps**, or **20 Gbps**.

8 If required, in the **Automation Controller** setup section, select the appropriate **Automation Controller** from the drop-down options and click **Enable Automation** to activate the button required to connect and configure the selected DisplayPort Controller instrument.

9 Click the **Connection Setup** button in the **Connection Setup** section and define the connection settings required to run the tests.

10 Click the **Test Setup** button in the **Test Setup** section and define the DUT parameters and test settings required to run the tests.

11 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the options defined in the **Set Up** tab.

12 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

13 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

14 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Please refer to the Keysight D9042DPPC/D9342DPPC DisplayPort UHBR Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort UHBR Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort UHBR Compliance Test Application, please refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort UHBR Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

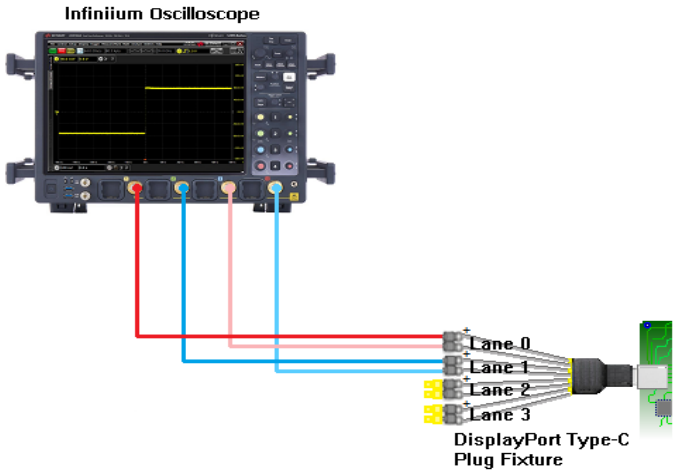


Figure 10 Sample Connection Diagram for DisplayPort UHBR Source Tests

Configuration for Connection Setup and Test Setup

Following steps describe the common settings that must be done on the **Connection Setup** and **Test Setup** windows for the Source tests to appear under the **Select Tests** tab.

Configuring the Connection Setup Window

1 In the **Connection Setup** area, please click the **Connection Setup** button. The **Connection Setup** window appears.

2 In the **Connection Setup** window,

a Select **Connection Type** as either **Single Ended**, **Differential**, or **Common Mode** depending on whether you are using differential, common, or single ended probes. To use **Switch Matrix** mode, please navigate to **Tools > Switch Matrix...** instead.

b The **No. of Channels** will be set to **4 Channels** by default.

c In the **Lane Selection** area, select the lanes that you want to test. For **Single Ended** connection, you may select up to two lanes. For other connection types, you may select up to four lanes.

d In the **Channel Selection** area, please assign appropriate channels to lanes.

NOTE

To know more about the **Connection Setup** window tabs, please see the following section in the Online Help:

Online Help > Setting Up the Test Environment > Connection Setup

3 Click **OK** to return to the **Set Up** tab.

Configuring the Test Setup Window

1 In the **Test Setup** area, please click the **Test Setup** button. The **Test Setup** window appears.

2 In the **Test Setup** window,

a Use **TP2 Test** or **TP3 Test 1** tab to define the preset numbers for TP2 and TP3_EQ tests, respectively.

b Use the **TP3 Test 2** tab to define the CTLE DC gain values for all the TP3_EQ tests**.**

c Use the **Fixture and Cable De-Embed** tab to define whether to de-embed fixture or cable or both for all the tests.

d Use the **Power Profile** tab to select the power profiles for a DUT with Type-C implementation.

NOTE

To know more about the **Test Setup** window tabs, please see the following section in the Online Help:

Online Help > Setting Up the Test Environment > Test Setup

3 Click **OK** to return to the **Set Up** tab.

NOTE

After configuring the **Test Setup** and **Connection Setup** to run a specific type of source tests, please click the **Select Tests** tab to view and select the tests, which appear on the basis of the DisplayPort settings defined in the **Test Setup** and **Connection Setup** windows.

Please see "Setting Up the Compliance Test Application for DisplayPort UHBR Source Tests:" on page 35 to complete the task flow for DUT setup along with configuring the Compliance Application to run each test.

Preset Best_TP2

Test ID

11001, 11002, 11003, 11004 – Preset Best_TP2 (UHBR10)

12001, 12002, 12003, 12004 – Preset Best_TP2 (UHBR13.5)

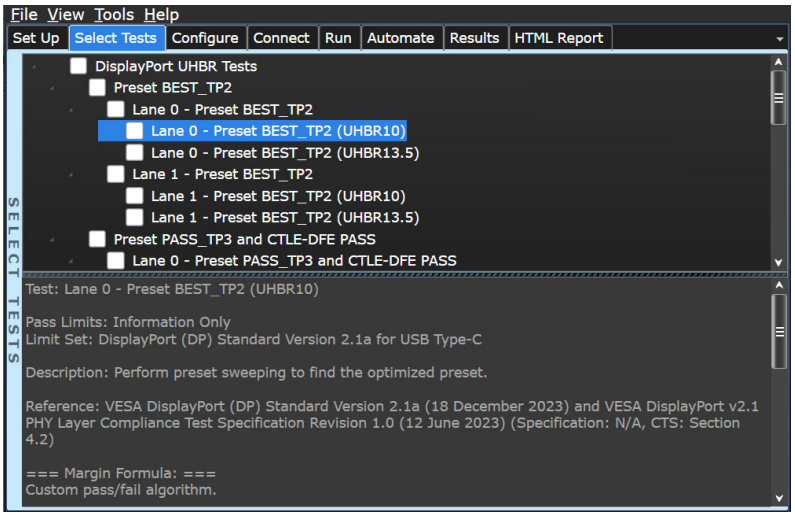
13001, 13002, 13003, 13004 – Preset Best_TP2 (UHBR20)

Test Overview

The objective of this test is to perform preset sweeping to find the optimized preset at TP2.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for Preset 0.
2 Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
3 Capture the waveform, and process it with the oscilloscope:
   a Sampling Rate ≥ 80 GSa/s
   b Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sampling rates, use memory depth in the same ratio.
   c Adjust vertical scale to fit signal into oscilloscope screen.
   d Perform jitter separation with:
      - Pattern length: Periodic
      - RJ Method: Spectral Only
      - BER Level: 1E-9
4 Capture Data Deterministic Jitter (DDJ).
5 Register DDJ value.
6 Repeat the test for all remaining presets (till preset 15 as shown in Table 3).
7 Repeat the test for all the remaining lanes.
8 For each lane, choose the preset that provides minimum DDJ.

PASS Condition

For each lane, the preset that provides the minimum DDJ is the optimized preset at TP2 for the given bit rate.

Test References

Please see:

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023), (Specification: N/A, CTS: Section 4.2)*

Expected/Observable Results

The optimized preset meets the criteria as mentioned in the “PASS Condition” section for this test.

Preset PASS_TP3 and CTLE-DFE PASS_TP3

Test ID

11501, 11502, 11503, 11504 – Preset PASS_TP3 and CTLE-DFE PASS_TP3 (UHBR10)

12501, 12502, 12503, 12504 – Preset PASS_TP3 and CTLE-DFE PASS_TP3 (UHBR13.5)

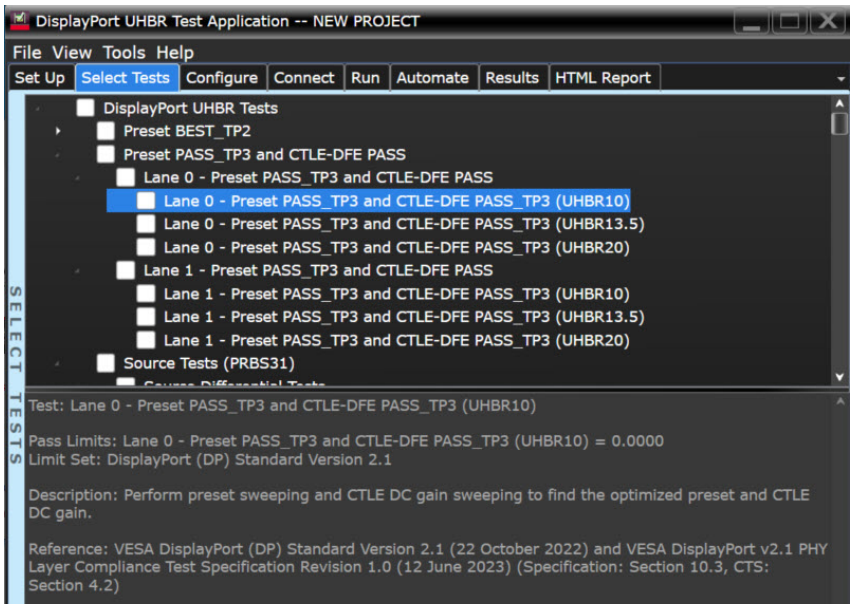
13501, 13502, 13503, 13504 – Preset PASS_TP3 and CTLE-DFE PASS_TP3 (UHBR20)

Test Overview

The objective of the this test is to perform preset sweeping and CTLE DC gain sweeping to find the optimized preset and CTLE DC gain.

Test Conditions

Test Parameter	Condition
Test Point	TP3
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP3
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled for Preset 0.
2 Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; interpolation shall be applied for obtaining effective sample rate of 1280 GSa/s (e.g., X16 interpolation for 80 GSa/s hardware sampling rate), no average to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
3 Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Accumulate at 1E6 UI.
4 Capture eye height and eye width.
5 Register mean eye height and mean eye width values.
6 Calculate the Eye Area = Eye Height x Eye Width.
7 Repeat the test for all CTLE DC gain.
8 Repeat the test for all remaining presets (till preset 15 as shown in Table 3).
9 Repeat the test for all the remaining lanes.
10 For each lane, choose the preset that provides maximum eye area.

PASS Condition

For each lane, the preset and CTLE DC gain that provides the maximum eye area is the optimized preset and CTLE DC gain, respectively, at TP3 for the given bit rate.

Test References

Please see:

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: N/A, CTS: Section 4.2)*

Expected/Observable Results

The optimized preset and CTLE DC gain meet the criteria as mentioned in the “PASS Condition” section for this test.

Bit Rate

Test ID

11091, 11092, 11093, 11094 – Bit Rate, Min (UHBR10)

12091, 12092, 12093, 12094 – Bit Rate, Min (UHBR13.5)

13091, 13092, 13093, 13094 – Bit Rate, Min (UHBR20)

11101, 11102, 11103, 11104 – Bit Rate, Max (UHBR10)

12101, 12102, 12103, 12104 – Bit Rate, Max (UHBR13.5)

13101, 13102, 13103, 13104 – Bit Rate, Max (UHBR20)

11041, 11042, 11043, 11044 – Average Minimum Bit Rate (UHBR10)

12041, 12042, 12043, 12044 – Average Minimum Bit Rate (UHBR13.5)

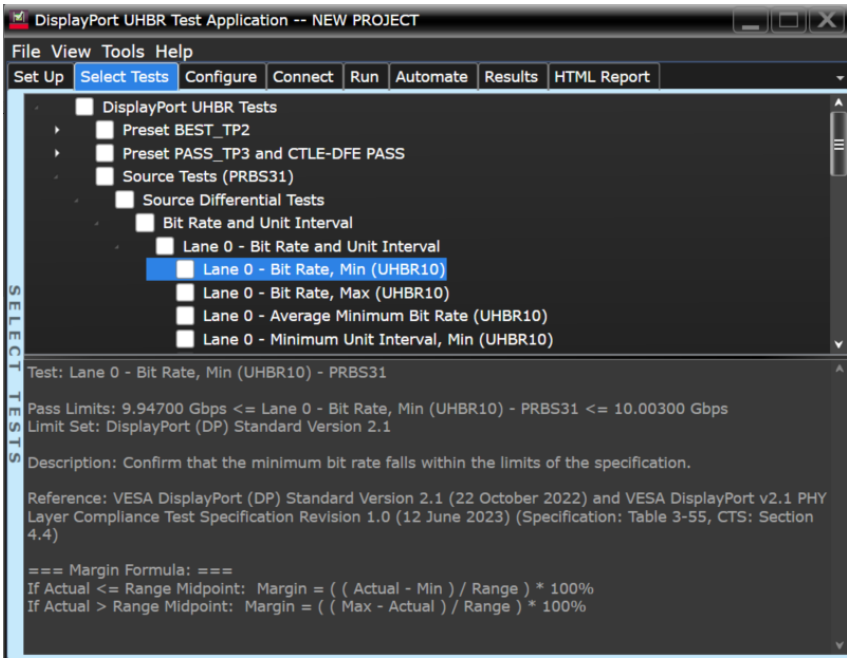
13041, 13042, 13043, 13044 – Average Minimum Bit Rate (UHBR20)

Test Overview

The objective of this test is to confirm that the maximum, minimum, and average bit rates fall within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled for optimum preset number. Please see "Preset Calibration TP2" on page 39.

2 Capture the waveform and process it with the oscilloscope:

a Sampling Rate = 80 GSa/s.

b Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rate, use memory depth in the same ratio.

c No CDR, no average and no interpolation to be used.

d Adjust vertical scale to fit signal into oscilloscope screen.

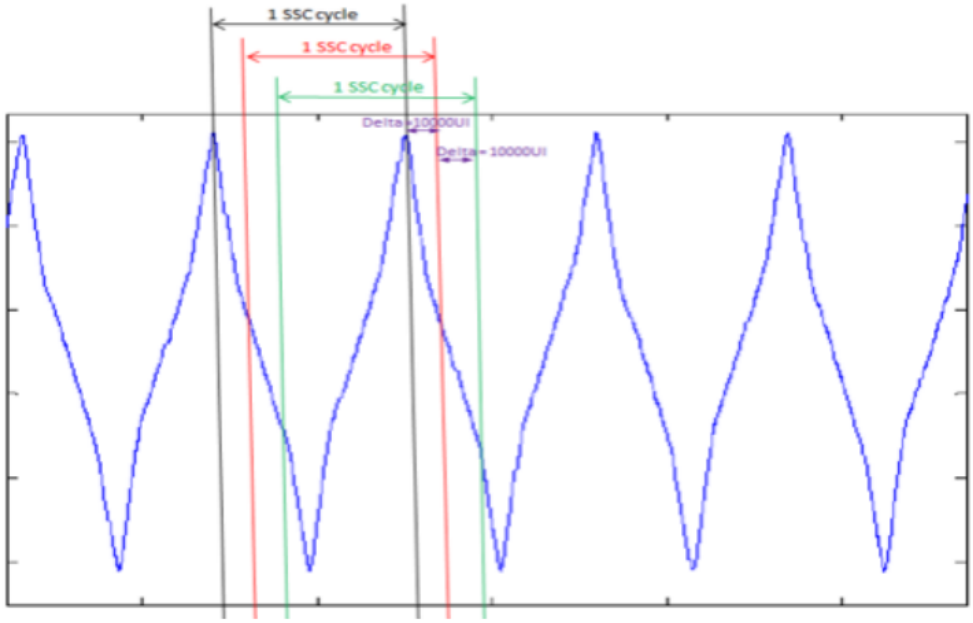
e Oscilloscope bandwidth should be as specified in Table 4.

3 Calculate UI dynamically using a uniform moving average filter procedure with following window size.

Bit Rate	Window Size Symbol
UHBR10	3000
UHBR13.5	4000
UHBR20	6000

4 Measure and calculate the values of both $BitRate_{MIN}$ and $BitRate_{MAX}$.

5 Use mathematical analysis to measure the average unit Interval over a window at the size of one SSC cycle, determined by the SSC_Down_Spread_Rate.



6 Measure Average Unit Interval over different windows that uniformly cover the scope capture over more than 10 SSC cycles with 10000 UI window jump.

7 Measure and calculate the value for $BitRate_{AVERAGE\_MIN}$.

8 Repeat the test for all remaining lanes.

PASS Condition

For Bit Rate Min:

- BitRate_MIN <= BitRateMIN <= BitRate_MAX

For Bit Rate Max:

- BitRate_MIN <= BitRateMAX <= BitRate_MAX

For Bit Rate Average:

- BitRate_AVERAGE <= BitRateAVERAGE_MIN

Table 5 Bit Rate - Pass Limits

Bit Rate	Min (BitRate_MIN)	Max (BitRate_MAX)	Average (BItRate_Average)
UHBR10	9.94700E+9	10.00300E+9	9.97200E+9
UHBR13.5	13.42845E+9	13.50405E+9	13.46220E+9
UHBR20	19.89400E+9	20.00600E+9	19.94400E+9

Test References

Please see:

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-55, CTS: Section 4.4)*

Expected/Observable Results

The measured maximum, minimum, and average bit rates for test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

Minimum Unit Interval, Min/Max (Information Only Test)

Test ID

11021, 11022, 11023, 11024 – Minimum Unit Interval, Min (UHBR10)

12021, 12022, 12023, 12024 – Minimum Unit Interval, Min (UHBR13.5)

13021, 13022, 13023, 13024 – Minimum Unit Interval, Min (UHBR20)

11031, 11032, 11033, 11034 – Minimum Unit Interval, Max (UHBR10)

12031, 12032, 12033, 12034 – Minimum Unit Interval, Max (UHBR13.5)

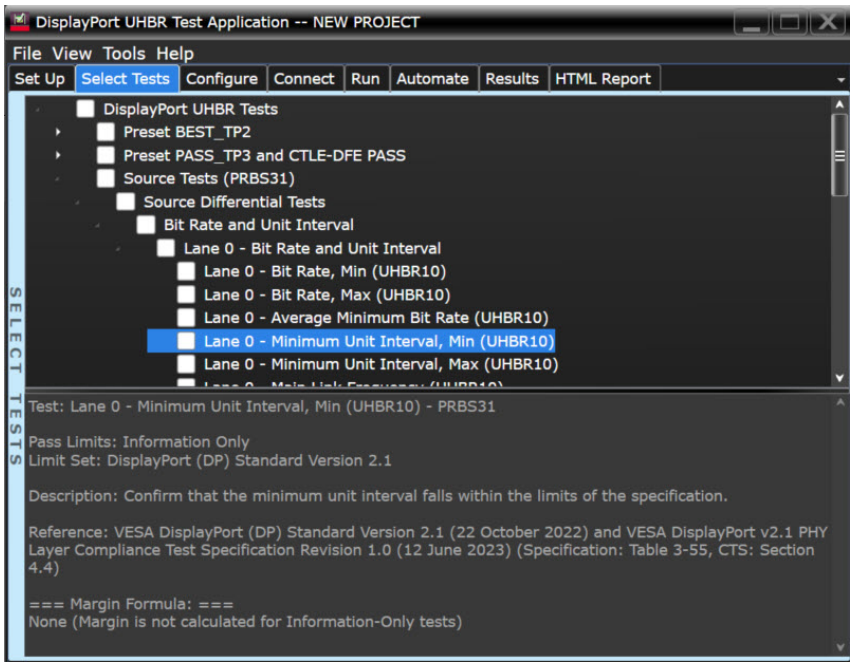
13031, 13032, 13033, 13034 – Minimum Unit Interval, Max (UHBR20)

Test Overview

The objective of this test is to confirm that the minimum unit interval falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.

2 Capture the waveform and process it with the oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rate, use memory depth in the same ratio.
- No CDR, no average and no interpolation to be used.
- Adjust vertical scale to fit signal into oscilloscope screen.
- Oscilloscope bandwidth should be as specified in Table 4.

3 Calculate UI dynamically using a uniform moving average filter procedure with following window size.

Bit Rate	Window Size Symbols
UHBR10	3000
UHBR13.5	4000
UHBR20	6000

4 Measure and calculate the values of both UI_{MIN} and UI_{MAX}.

5 Repeat the test for all remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-55, CTS: Section 4.4)*

Expected/Observable Results

The measured maximum or minimum unit interval for test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

Main Link Frequency (Information Only Test)

Test ID

11061, 11062, 11063, 11064 – Main Link Frequency (UHBR10)

12061, 12062, 12063, 12064 – Main Link Frequency (UHBR13.5)

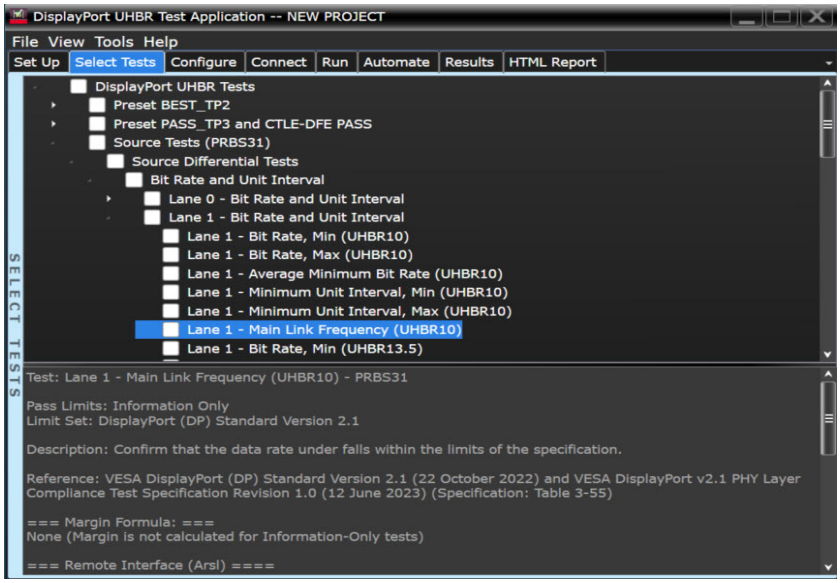
13061, 13062, 13063, 13064 – Main Link Frequency (UHBR20)

Test Overview

The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as mentioned in the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Run the “Unit Interval” Test as a prerequisite to obtain UI_{Mean}.

2 Use the obtained value of UI_{Mean} to calculate the value of main link frequency:
Main Link Frequency = {[Nominal Bit Rate - $(1/UI_{Mean})$]/Nominal Bit Rate} * 1.0E6

3 Repeat the test for all remaining lanes.

PASS Condition

This test is information only.

Test References

Please see:

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-55)*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

SSC Down Spread Range

Test ID

11071, 11072, 11073, 11074 – SSC Down Spread Range (UHBR10)

12071, 12072, 12073, 12074 – SSC Down Spread Range (UHBR13.5)

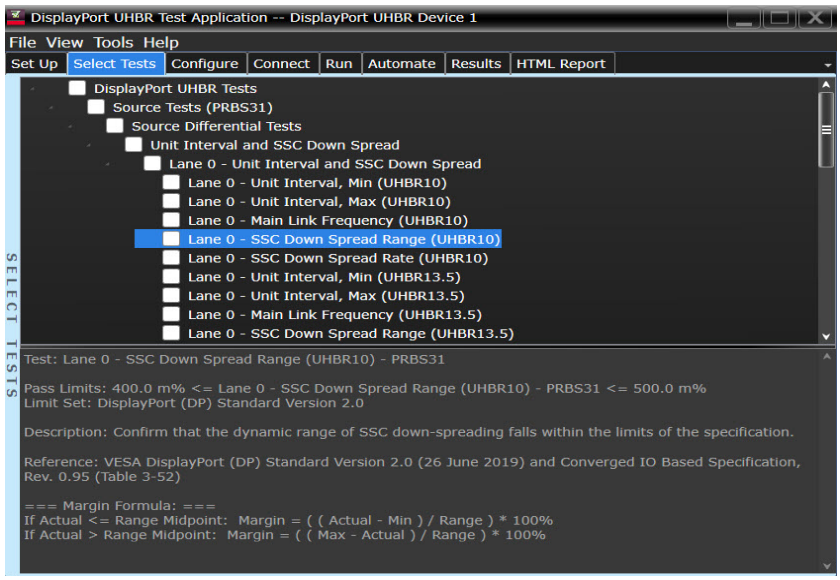
13071, 13072, 13073, 13074 – SSC Down Spread Range (UHBR20)

Test Overview

The objective of the test is to confirm that the dynamic range of SSC down-spreading is within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1. Run the “Unit Interval” Test as a prerequisite to obtain UI_{MAX} and UI_{MIN}.
2. Use the obtained value of UI_{MAX} and UI_{MIN} to calculate the range percentage:
   Maximum Deviation = 100*{[Nominal Data Rate - (1 / UI_{MAX})] / Nominal Data Rate}
   Minimum Deviation = 100*{[Nominal Data Rate - (1 / UI_{MIN})] / Nominal Data Rate}
3. Calculate SSC Down Spread Range using the equation:
   SSC Down Spread Range = Maximum Deviation - Minimum Deviation
4. Repeat the test for all remaining lanes.

PASS Condition

SSC Down Spread Range ≤ 0.5%

Table 6 Common DP Main-Link UHBR Electrical System Parameters

Symbol	Bit Rate	Max	Unit	Comments
SSC_Down_Spread_Range	UHBR10	0.5	%	SSC_DOWN_SPREAD_RANGE specifies the mandated SSC modulation depth, represented by the difference of the minimum and maximum modulated frequencies, referenced to the link speed.
	UHBR13.5	0.5	%	
	UHBR20	0.5	%	

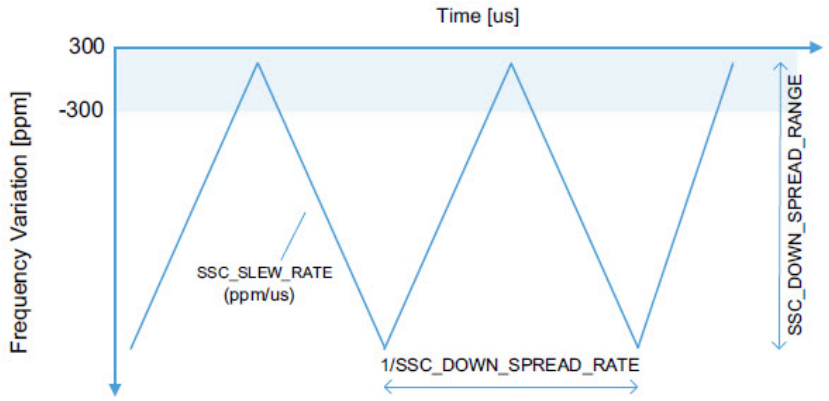


Figure 11 UHBR SSC Parameters (Figure 3-68 of the specification)

Test References

Please see:

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-55, CTS: Section 4.5)*

Expected/Observable Results

The measured SSC down spread range for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

SSC Down Spread Rate

Test ID

11081, 11082, 11083, 11084 – SSC Down Spread Rate (UHBR10)

12081, 12082, 12083, 12084 – SSC Down Spread Rate (UHBR13.5)

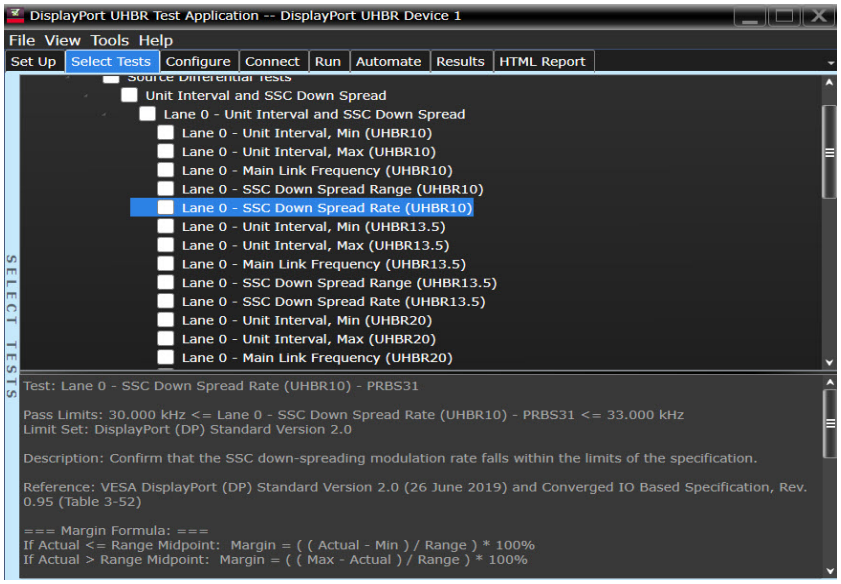
13081, 13082, 13083, 13084 – SSC Down Spread Rate (UHBR20)

Test Overview

The objective of the test is to confirm that the SSC down-spreading modulation rate falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1. Configure DUT transmitter to output PRBS31 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.
2. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rate use memory depth in the same ratio.
   - No CDR, no average and no interpolation to be used
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Oscilloscope bandwidth should be as specified in Table 4.
3. Measure and calculate the frequency of the SSC profile.
4. Repeat the test for all remaining lanes.

PASS Condition

30.00 kHz ≤ SSC Down Spread Rate ≤ 33.00 KHz

Table 7 Common DP Main-Link UHBR Electrical System Parameters

Symbol	Bit Rate	Min	Max	Unit	Comments
SSC_Down_Spread_Rate	UHBR10	30.00	33.00	kHz	N/A
	UHBR13.5	30.00	33.00	kHz	
	UHBR20	30.00	33.00	kHz	

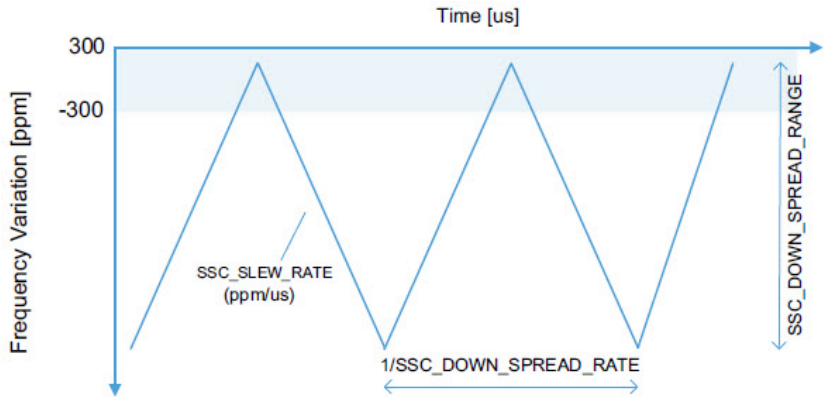


Figure 12 UHBR SSC Parameters (Figure 3-68 of the specification)

Test References

Please see:

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-55, CTS: Section 4.5)*

Expected/Observable Results

The measured SSC down spread rate for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

SSC Slew Rate

Test ID

11151, 11152, 11153, 11154 – SSC Slew Rate (UHBR10)

12151, 12152, 12153, 12154 – SSC Slew Rate (UHBR13.5)

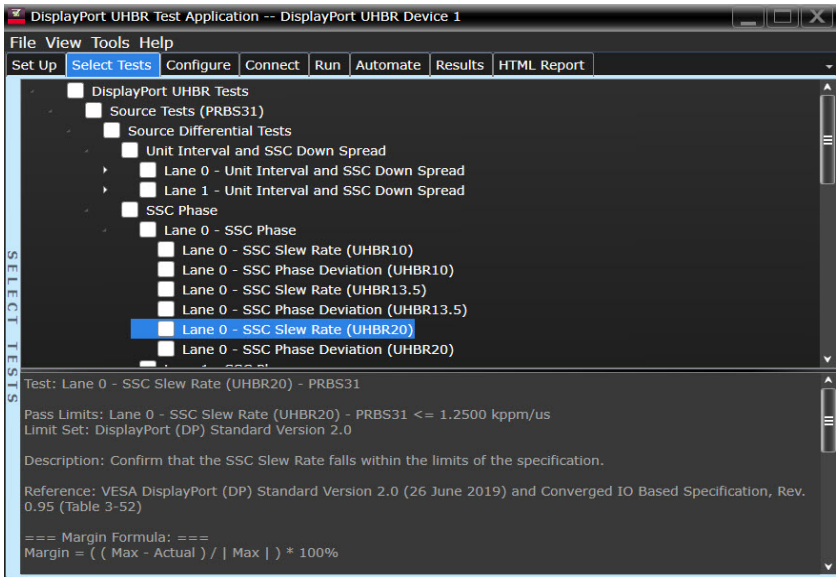
13151, 13152, 13153, 13154 – SSC Slew Rate (UHBR20)

Test Overview

The objective of the test is to confirm that the SSC slew rate falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.

2 Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - No CDR, no average and no interpolation to be used
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Oscilloscope bandwidth should be as specified in Table 4.

3 Extract SSC slew rate from the transmitted signal over measurement intervals of 0.5 µs.

4 Extract SSC slew rate from the phase information after applying a 2nd order Low-Pass-Filter with 3 dB cut-off at 5 MHz.

5 Repeat the test for the remaining lanes.

PASS Condition

SSC Slew Rate ≤ 1.2500 kppm/µs

Table 8 Common DP Main-Link UHBR Electrical System Parameters

Symbol	Bit Rate	Max	Unit	Comments
SSC_SLEW_RATE	**UHBR10**	1.2500	kppm/**µs**	The SSC slew rate shall be extracted from the transmitted signal over measurement intervals of 0.5 us. The SSC slew rate shall be extracted from the signal phase after applying a 2nd order low-pass filter with 3 dB point at 5 MHz.
	UHBR13.5	1.2500	kppm/**µs**	
	UHBR20	1.2500	kppm/**µs**	

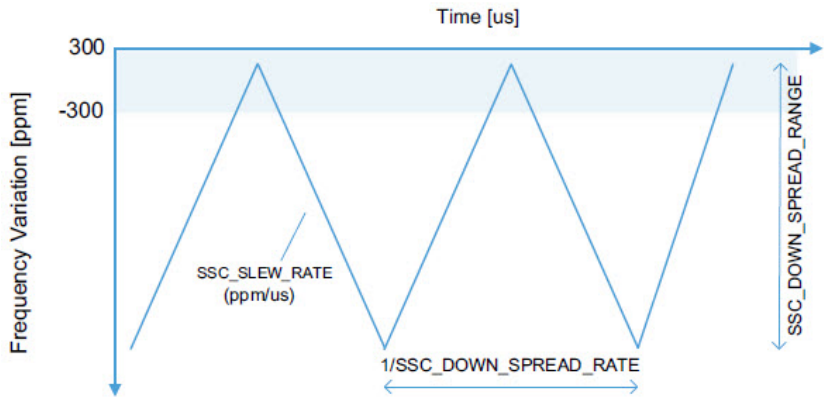


Figure 13 UHBR SSC Parameters (Figure 3-68 of the specification)

Test References

Please see:

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-55, CTS: Section 4.5)*

Expected/Observable Results

The measured SSC slew rate for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

SSC Phase Deviation

Test ID

11111, 11112, 11113, 11114 – SSC Phase Deviation (UHBR10)

12111, 12112, 12113, 12114 – SSC Phase Deviation (UHBR13.5)

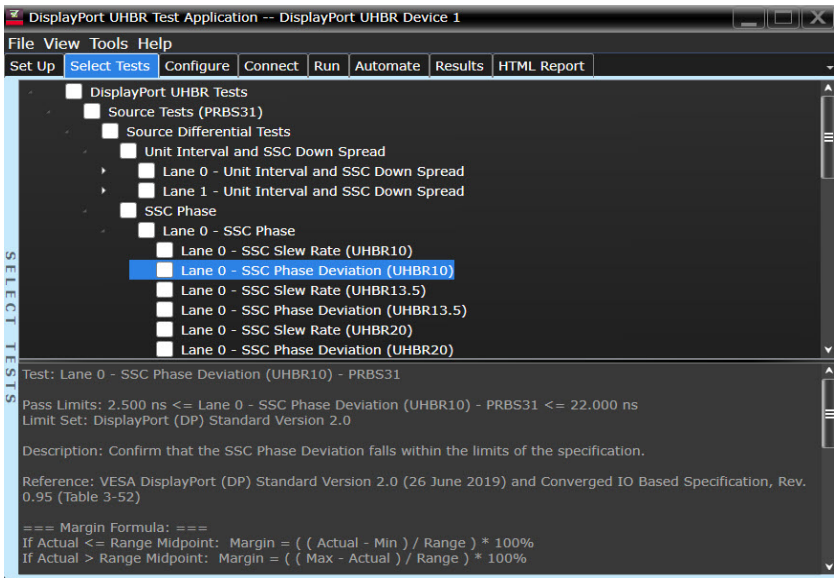
13111, 13112, 13113, 13114 – SSC Phase Deviation (UHBR20)

Test Overview

The objective of the test is to confirm that the SSC phase deviation falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- DisplayPort UHBR Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort UHBR Tests
Source Tests (PRBS31)
Source Differential Tests
Unit Interval and SSC Down Spread
Lane 0 - Unit Interval and SSC Down Spread
Lane 1 - Unit Interval and SSC Down Spread
SSC Phase
Lane 0 - SSC Phase
Lane 0 - SSC Slew Rate (UHBR10)
Lane 0 - SSC Phase Deviation (UHBR10)
Lane 0 - SSC Slew Rate (UHBR13.5)
Lane 0 - SSC Phase Deviation (UHBR13.5)
Lane 0 - SSC Slew Rate (UHBR20)
Lane 0 - SSC Phase Deviation (UHBR20)
Test: Lane 0 - SSC Phase Deviation (UHBR10) - PRBS31
Pass Limits: 2.500 ns <= Lane 0 - SSC Phase Deviation (UHBR10) - PRBS31 <= 22.000 ns
Limit Set: DisplayPort (DP) Standard Version 2.0
Description: Confirm that the SSC Phase Deviation falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.0 (26 June 2019) and Converged IO Based Specification, Rev. 0.95 (Table 3-52)
=== Margin Formula: ===
If Actual <= Range Midpoint: Margin = ((Actual - Min) / Range) * 100%
If Actual > Range Midpoint: Margin = ((Max - Actual) / Range) * 100%

Measurement Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.

2 Capture the waveform and process it with the oscilloscope:
- Sampling Rate ≥ 80 GSa/s
- Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
- No CDR, no average and no interpolation to be used
- Adjust vertical scale to fit signal into oscilloscope screen.
- Oscilloscope bandwidth should be as specified in Table 4.

3 Extract the SSC Phase Deviation from the transmitted signal.

4 Extract the SSC Phase Deviation from the phase jitter after applying a 2nd order low-pass filter with 3 dB point at 5 MHz.

5 Repeat the test for the remaining lanes.

PASS Condition

SSC Phase Deviation ≤ 22.00 ns

Table 9 Common DP Main-Link UHBR Electrical System Parameters

Symbol	Bit Rate	Max	Unit	Comments
SSC_PHASE_DEVIATION	**UHBR10**	22.00	ns	SSC phase deviation shall be extracted from the transmitted signal. During this test, the transmitter shall be configured to send the PRBS31 pattern. The SSC phase deviation shall be measured after applying a 2nd order low-pass filter with 3-dB point at 5 MHz.
	UHBR13.5	22.00	ns	
	UHBR20	22.00	ns	

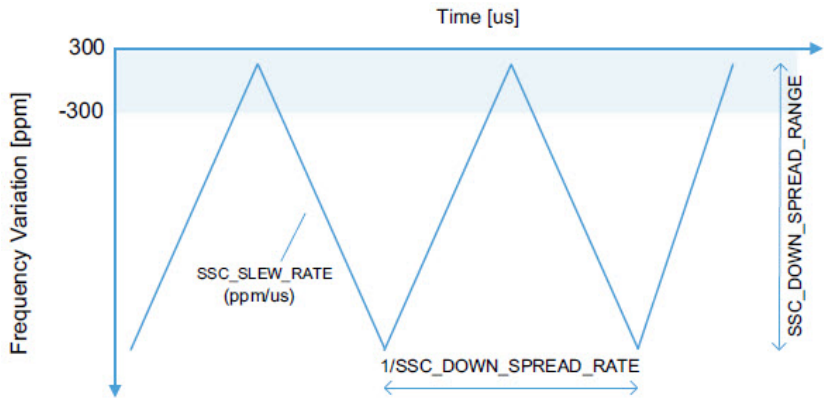


Figure 14 UHBR SSC Parameters (Figure 3-68 of the specification)

Test References

Please see:

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-55, CTS: Section 4.5)*

Expected/Observable Results

The measured SSC phase deviation for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

Peak To Peak Voltage (Information Only Test)

Test ID

11231, 11232, 11233, 11234 – Peak to Peak Voltage (UHBR10)

12231, 12232, 12233, 12234 – Peak to Peak Voltage (UHBR13.5)

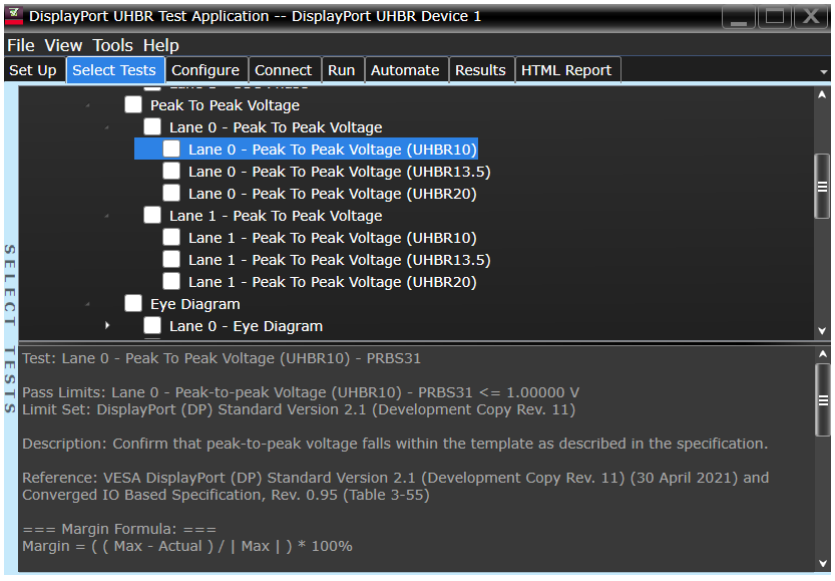
13231, 13232, 13233, 13234 – Peak to Peak Voltage (UHBR20)

Test Overview

The objective of the test is to confirm that the peak-to-peak voltage falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.

2 Perform measurements with:

   a Reference CDR based on the "Reference Receiver Clock Data Recovery" in page XX, no average and no interpolation to be used.

   b Oscilloscope bandwidth should be as specified in Table 4.

3 Capture the waveform and process it with the oscilloscope:

   - Sampling Rate ≥ 80 GSa/s
   - Adjust vertical scale to fit signal into oscilloscope screen.

4 Capture the Vmax and Vmin results.

5 Calculate Vpp = Vmax - Vmin.

6 Repeat the test for all remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-59)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-64)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-69)*

Expected/Observable Results

The measured peak-to-peak voltage for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the "PASS Condition" section of the test.

TP2 Eye Diagram

Test ID

11221, 11222, 11223, 11224 – TP2 Eye Diagram (UHBR10)

12221, 12222, 12223, 12224 – TP2 Eye Diagram (UHBR13.5)

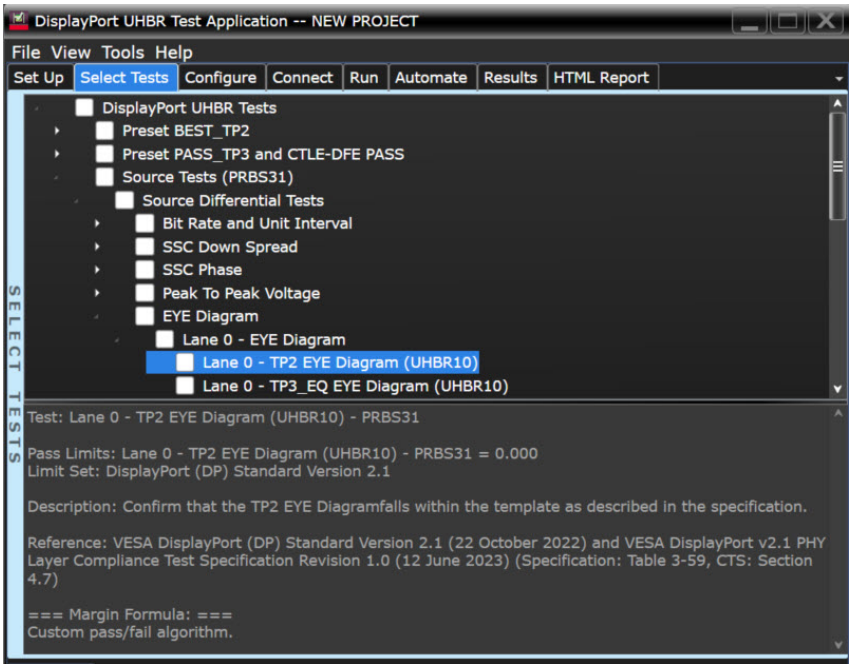
13221, 13222, 13223, 13224 – TP2 Eye Diagram (UHBR20)

Test Overview

The objective of the test is to confirm that the eye diagram falls within the template as described in the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.

2 Perform measurements with:

- Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; interpolation shall be applied for obtaining effective sample rate of 1280 GSa/s (e.g., X16 interpolation for 80 GSa/s hardware sampling rate), no average to be used.
- Oscilloscope bandwidth should be as specified in Table 4.

3 Capture the waveform and process it with the oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Adjust vertical scale to fit signal into oscilloscope screen.
- Accumulate at 1E6 UI

4 Measure eye height at (50±10)% UI.

5 Compare the data eye to the standard eye diagram mask. Check for conditions described in the section “Pass Condition”.

6 If the eye is within the standard eye mask, the test is declared as pass, otherwise proceed with step 7.

7 In case the eye mask test fails:

a Modify the eye mask, set the mask center at the measured eye height.

b Compare the modified eye mask to the standard.

c Report the comparison results.

8 Repeat the test for all the remaining lanes.

PASS Condition

If any part of the waveform hits the mask, the status of the test is FAIL.

Table 10 UHBR10 DPTX TP2 Metrics System Parameters (Normative)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$X1_{UHBR10}$	**EYE Mask Horizontal Deviation**			200.00	mUI	Measured at $1E^{-6}$ BER.[e f]
$Y1_{UHBR10}$	**EYE Mask Inner Height**[g]	121.00			mV	Measured at $1E^{-6}$ BER.[e f]

e Measured without RJ/DJ decomposition, using 1-M UI capture
f See the heading UHBR Eye Mask
g One-sided voltage opening of the differential signal

Table 11 UHBR13.5 DPTX TP2 Metrics System Parameters (Normative)[a]

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$X1_{UHBR13.5}$	**EYE Mask Horizontal Deviation**			220.00	mUI	Measured at $1E^{-6}$ BER.[c d]
$Y1_{UHBR13.5}$	**EYE Mask Inner Height**[e]	100.00			mV	Measured at $1E^{-6}$ BER.[c d]

a All parameters are measured at the cable input (TP2') without Reference Receiver CTLE + Reference Receiver DFE applied, but with the optimal FFE preset value.
c Measured without RJ/DJ decomposition, using 1-M UI capture
d See the heading UHBR Eye Mask
e One-sided voltage opening of the differential signal

Table 12 UHBR20 DPTX TP2 Metrics System Parameters (Normative)[a b]

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$X1_{UHBR20}$	**EYE Mask Horizontal Deviation (EhnDP DP80LL)**			235.00	mUI	Measured at $1E^{-6}$ BER.[c d]
$X1_{UHBR20}$	**EYE Mask Horizontal Deviation (EhnDP DP80)**			230.00	mUI	Measured at $1E^{-6}$ BER.[c d]
$X1_{UHBR20}$	**EYE Mask Horizontal Deviation (USB-C)**			230.00	mUI	Measured at $1E^{-6}$ BER.[c d]
$Y1_{UHBR20}$	**EYE Mask Inner Height (EhnDP DP80LL)**		85.00		mV	Measured at $1E^{-6}$ BER.[c d]
$Y1_{UHBR20}$	**EYE Mask Inner Height (EhnDP DP80)**		120.00		mV	Measured at $1E^{-6}$ BER.[c d]
$Y1_{UHBR20}$	**EYE Mask Inner Height (USB-C)**		120.00		mV	Measured at $1E^{-6}$ BER.[c d]
$Y2_{UHBR20}$	**EYE Mask Outer Height**			650.00	mV	Measured at $1E^{-6}$ BER.[c d]

a All parameters are measured at the DPTX receptacle, with CDR applied, and without CTLE and DFE applied.
b FFE preset optimized for measurement point.
c Measured without RJ/DJ decomposition, using 1-M UI capture.
d See the heading UHBR Eye Mask
e One-sided voltage opening of the differential signal. s

UHBRx EYE Mask

The EYE mask shape is unchanged from HBR3 and HBR2; however, the metric that defines the EYE has evolved. As illustrated in the following figure, the inner EYE mask diamond vertices are now defined differently, as follows:

- EYE mask height is defined by the maximum and minimum deviation from the 0-differential voltage (+Y1 and -Y1). Y1 is the minimum differential peak voltage measurement (in mV).
- Horizontal EYE mask opening has vertices that are defined by the excursion from the outside

of the UI (X1 and 1-X1). X1 is the maximum limit (in percentage of UI), and measured at the 0-V differential crossing point. Due to the 128b/132b channel encoding used in UHBRx systems, it is not practical to perform RJ/DJ separation. The Data EYE is created by an oscilloscope capture that approximates a $1E^{-6}$ BER. The data EYE mask is then directly compared against this measurement without the need for extrapolation.

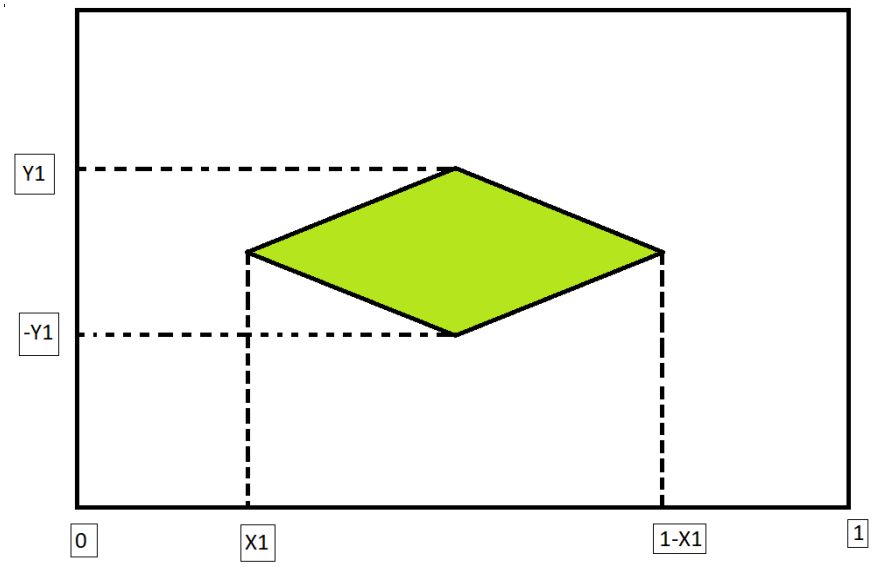


Figure 15 UHBRx EYE Opening Definitions (Figure O-2 of the specification)

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-59, CTS: Section 4.7)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-64, CTS: Section 4.7)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

TP3_EQ EYE Diagram

Test ID

11521, 11522, 11523, 11524 – TP3_EQ EYE Diagram (UHBR10)

12521, 12522, 12523, 12524 – TP3_EQ EYE Diagram (UHBR13.5)

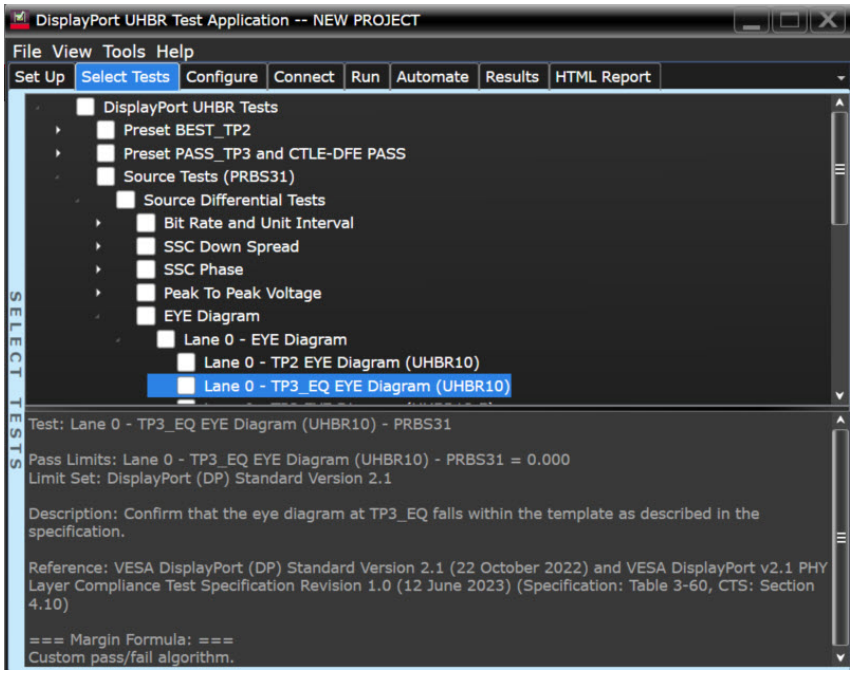
13521, 13522, 13523, 13524 – TP3_EQ EYE Diagram (UHBR20)

Test Overview

The objective of the test is to confirm that the eye diagram at TP3_EQ falls within the template as described in the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP3_EQ
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled for optimum preset number. Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
2 Embed the cable model based on connector type.
3 Ensure that measurements are done with optimum reference receiver equalizer (CTLE and DFE). Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
4 Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; interpolation shall be applied for obtaining effective sample rate of 1280 GSa/s (e.g., X16 interpolation for 80 GSa/s hardware sampling rate), no average to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
5 Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Accumulate at 1E6 UI
6 Compare the data eye to the TP3_EQ eye diagram mask. Check for conditions described in the section “Pass Condition”.
7 If the eye is within the standard eye mask, the test is declared as pass, otherwise proceed with step 8.
8 In case the eye mask test fails:
   a Modify the eye mask, set the mask center at the measured eye height.
   b Compare the modified eye mask to the standard.
9 Report the comparison results.
10 Repeat the test for the remaining lanes.

PASS Condition

If any part of the waveform hits the mask, the status of the test is FAIL.

Table 13 UHBR10 DPTX TP3_EQ Metrics System Parameters (Normative)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$X1_{UHBR10}$	**EYE Mask Horizontal Deviation**			237.00	mUI	Measured at $1E^{-6}$ BER.[e f]
$Y1_{UHBR10}$	**EYE Mask Inner Height**[g]	47.00			mV	Measured at $1E^{-6}$ BER.[e f]

e Measured without RJ/DJ decomposition, using 1-M UI capture
f See the heading UHBR Eye Mask
g One-sided voltage opening of the differential signal

Table 14 UHBR13.5 DPTX TP3_EQ Metrics System Parameters (Normative)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$X1_{UHBR13.5}$	**EYE Mask Horizontal Deviation**			240.00	mUI	Measured at $1E^{-6}$ BER.[c d]
$Y1_{UHBR13.5}$	**EYE Mask Inner Height**[e]	40.00			mV	Measured at $1E^{-6}$ BER.[c d]

c Measured without RJ/DJ decomposition, using 1-M UI capture
d See the heading UHBR Eye Mask
e One-sided voltage opening of the differential signal

Table 15 UHBR20 DPTX TP3_EQ Metrics System Parameters (Normative)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$X1_{UHBR20}$	**EYE Mask Horizontal Deviation (EhnDP DP80LL)**			220.00	mUI	Measured at $1E^{-6}$ BER.[d e]
$X1_{UHBR20}$	**EYE Mask Horizontal Deviation (EhnDP DP80)**			220.00	mUI	Measured at $1E^{-6}$ BER.[d e]
$X1_{UHBR20}$	**EYE Mask Horizontal Deviation (USB-C)**			220.00	mUI	Measured at $1E^{-6}$ BER.[d e]
$Y1_{UHBR20}$	**EYE Mask Inner Height (EhnDP DP80LL)**	50.00			mV	Measured at $1E^{-6}$ BER.[d e]
$Y1_{UHBR20}$	**EYE Mask Inner Height (EhnDP DP80)**	50.00			mV	Measured at $1E^{-6}$ BER.[d e]
$Y1_{UHBR20}$	**EYE Mask Inner Height (USB-C)**	50.00			mV	Measured at $1E^{-6}$ BER.[d e]
$Y2_{UHBR20}$	**EYE Mask Outer Height**			650.00	mV	Measured at $1E^{-6}$ BER.[d e]

d Measured without RJ/DJ decomposition, using 1-M UI capture.
e See the heading UHBR Eye Mask
f One-sided voltage opening of the differential signal.

UHBRx EYE Mask

The EYE mask shape is unchanged from HBR3 and HBR2; however, the metric that defines the EYE has evolved. As illustrated in the following figure, the inner EYE mask diamond vertices are now defined differently, as follows:

- EYE mask height is defined by the maximum and minimum deviation from the 0-differential voltage (+Y1 and -Y1). Y1 is the minimum differential peak voltage measurement (in mV).
- Horizontal EYE mask opening has vertices that are defined by the excursion from the outside

of the UI (X1 and 1-X1). X1 is the maximum limit (in percentage of UI), and measured at the 0-V differential crossing point. Due to the 128b/132b channel encoding used in UHBRx systems, it is not practical to perform RJ/DJ separation. The Data EYE is created by an oscilloscope capture that approximates a $1E^{-6}$ BER. The data EYE mask is then directly compared against this measurement without the need for extrapolation.

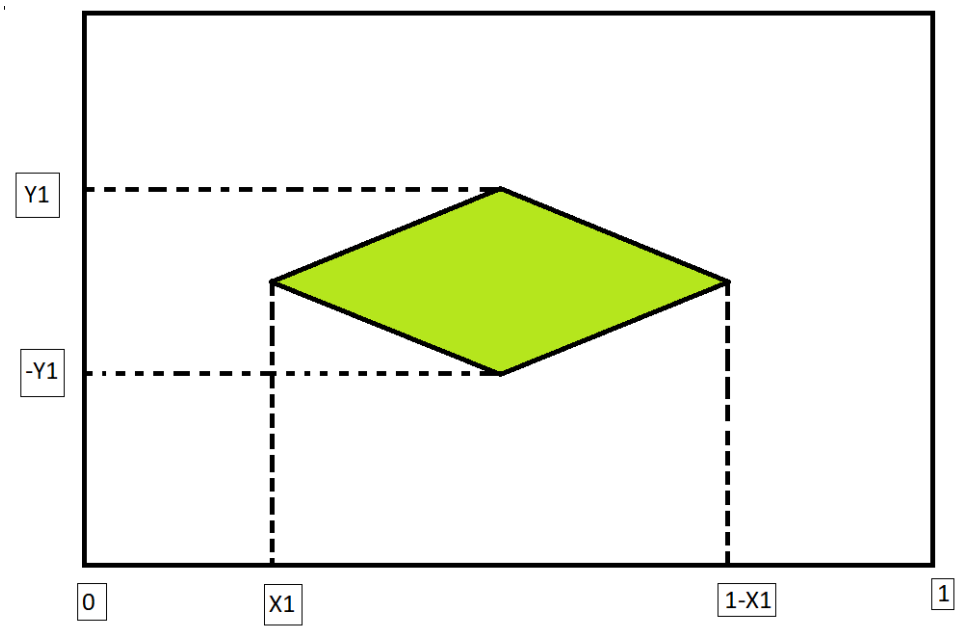


Figure 16 UHBRx EYE Opening Definitions (Figure O-2 of the specification)

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-60, CTS: Section 4.10)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-65, CTS: Section 4.10)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AC Common Mode Voltage (Information Only Test)

Test ID

11211, 11212, 11213, 11214 – AC Common Mode Voltage (UHBR10)

12211, 12212, 12213, 12214 – AC Common Mode Voltage (UHBR13.5)

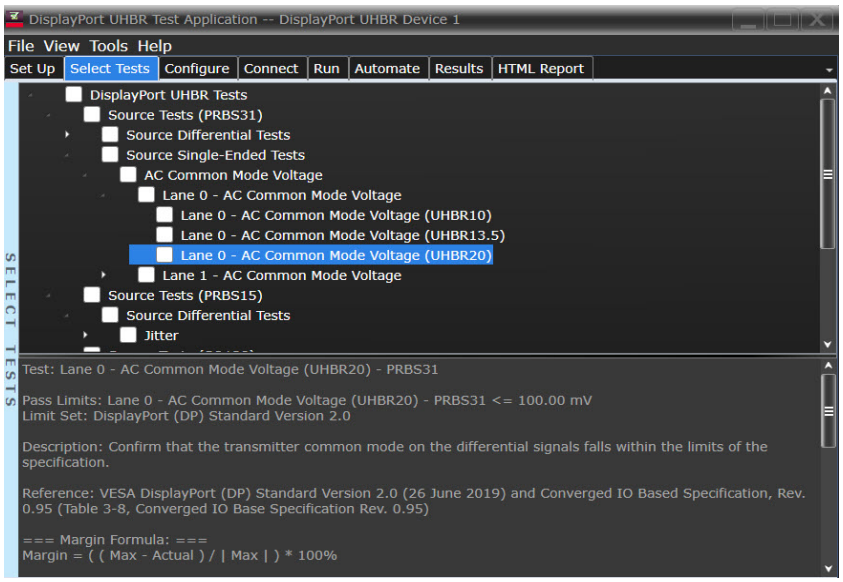
13211, 13212, 13213, 13214 – AC Common Mode Voltage (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter common mode on the differential signals is within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Common Mode, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- DisplayPort UHBR Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort UHBR Tests
Source Tests (PRBS31)
Source Differential Tests
Source Single-Ended Tests
AC Common Mode Voltage
Lane 0 - AC Common Mode Voltage
Lane 0 - AC Common Mode Voltage (UHBR10)
Lane 0 - AC Common Mode Voltage (UHBR13.5)
Lane 0 - AC Common Mode Voltage (UHBR20)
Lane 1 - AC Common Mode Voltage
Source Tests (PRBS15)
Source Differential Tests
Jitter
Test: Lane 0 - AC Common Mode Voltage (UHBR20) - PRBS31
Pass Limits: Lane 0 - AC Common Mode Voltage (UHBR20) - PRBS31 <= 100.00 mV
Limit Set: DisplayPort (DP) Standard Version 2.0
Description: Confirm that the transmitter common mode on the differential signals falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.0 (26 June 2019) and Converged IO Based Specification, Rev. 0.95 (Table 3-8, Converged IO Base Specification Rev. 0.95)
=== Margin Formula: ===
Margin = ((Max - Actual) / | Max |) * 100%

Measurement Procedure

1 Configure the DUT transmitter to output PRBS31 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.

2 Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 27 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - No CDR, no average and no interpolation to be used
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Oscilloscope bandwidth should be as specified in Table 4.

3 Calculate the AC Common Mode Voltage (V_{AC-CM}) using the equation:
   $V_{AC-CM} = (V_{TX-P} + V_{TX-N}) / 2$

4 Repeat the test for all the remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- For UHBR10
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: N/A, CTS: Section 4.9)*
- For UHBR13.5 and UHBR20
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: N/A, CTS: Section 4.9)*

Expected/Observable Results

The measured AC common mode voltage for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP2 Total Jitter

Test ID

11421, 11422, 11423, 11424 – TP2 Total Jitter (UHBR10)

12421, 12422, 12423, 12424 – TP2 Total Jitter (UHBR13.5)

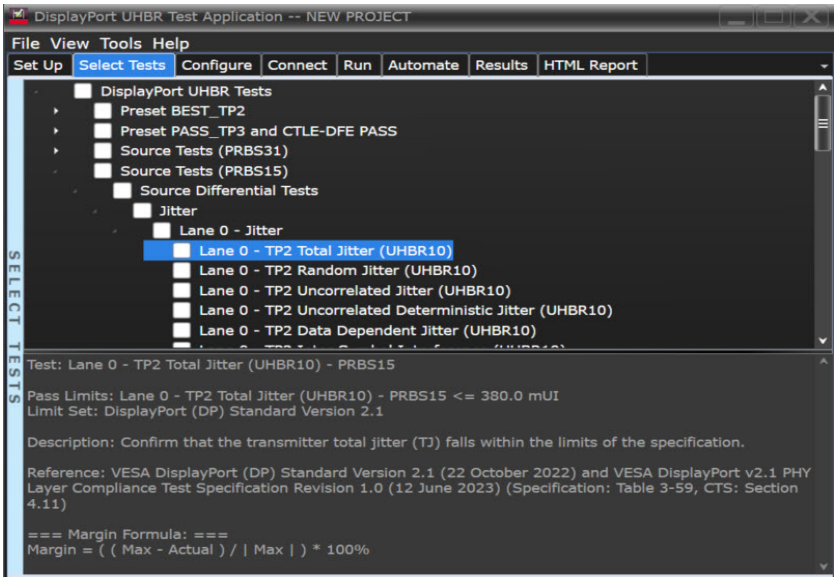
13421, 13422, 13423, 13424 – TP2 Total Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter total jitter (TJ) falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- NEW PROJECT
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort UHBR Tests
Preset BEST_TP2
Preset PASS_TP3 and CTLE-DFE PASS
Source Tests (PRBS31)
Source Tests (PRBS15)
Source Differential Tests
Jitter
Lane 0 - Jitter
Lane 0 - TP2 Total Jitter (UHBR10)
Lane 0 - TP2 Random Jitter (UHBR10)
Lane 0 - TP2 Uncorrelated Jitter (UHBR10)
Lane 0 - TP2 Uncorrelated Deterministic Jitter (UHBR10)
Lane 0 - TP2 Data Dependent Jitter (UHBR10)
Test: Lane 0 - TP2 Total Jitter (UHBR10) - PRBS15
Pass Limits: Lane 0 - TP2 Total Jitter (UHBR10) - PRBS15 <= 380.0 mUI
Limit Set: DisplayPort (DP) Standard Version 2.1
Description: Confirm that the transmitter total jitter (TJ) falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.1 (22 October 2022) and VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (12 June 2023) (Specification: Table 3-59, CTS: Section 4.11)
=== Margin Formula: ===
Margin = ((Max - Actual) / | Max |) * 100%

Measurement Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.
2 Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
3 Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
4 Capture the Total Jitter (TJ) result.
5 Repeat the test for all the remaining lanes.

PASS Condition

TJ <= TJ_MAX

Table 16 UHBR DPTX TP2 Metrics System Parameters (Normative)

Symbol	Bit Rate	Max (TJ_MAX)	Unit	Comments
TJ	**UHBR10**	380	mUI	Peak-to-peak at $1E^{-9}$ BER [a]
	UHBR13.5	370	mUI	Peak-to-peak at $1E^{-9}$ BER
	UHBR20 (EhnDP DP80LL)	495	mUI	Peak-to-peak at $1E^{-9}$ BER
	UHBR20 (EhnDP DP80)	480	mUI	Peak-to-peak at $1E^{-9}$ BER
	UHBR20 (USB-C)	480	mUI	Peak-to-peak at $1E^{-9}$ BER

a. Crest factor of 12.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-59, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-64, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP2 Random Jitter (Information Only Test)

Test ID

11431, 11432, 11433, 11434 – TP2 Random Jitter (UHBR10)

12431, 12432, 12433, 12434 – TP2 Random Jitter (UHBR13.5)

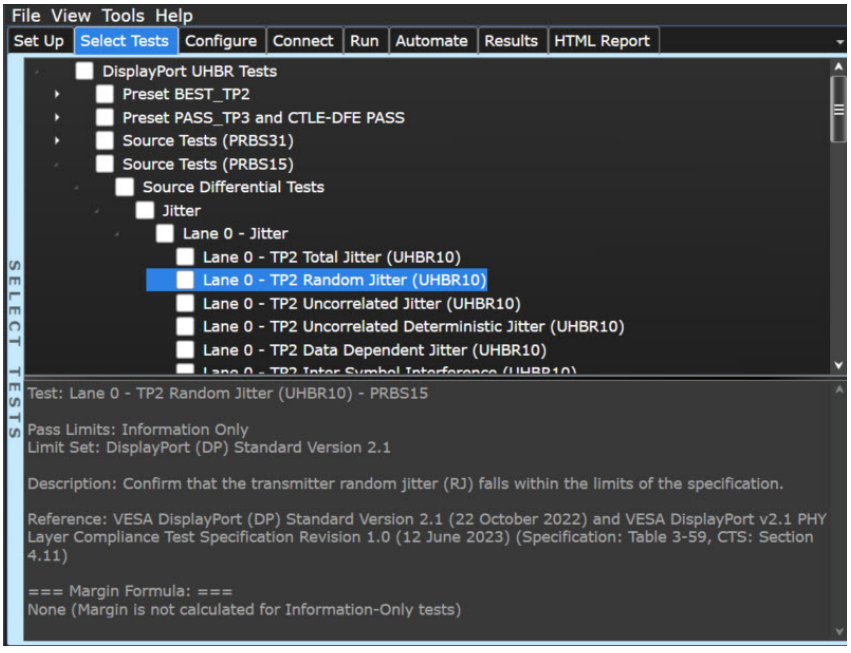
13431, 13432, 13433, 13434 – TP2 Random Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter random jitter (RJ) falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.
2. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
3. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
4. Capture the Random Jitter (RJ) result.
5. Repeat the test for all the remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-59, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-64, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured random jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP2 Uncorrelated Jitter

Test ID

11441, 11442, 11443, 11444 – TP2 Uncorrelated Jitter (UHBR10)

12441, 12442, 12443, 12444 – TP2 Uncorrelated Jitter (UHBR13.5)

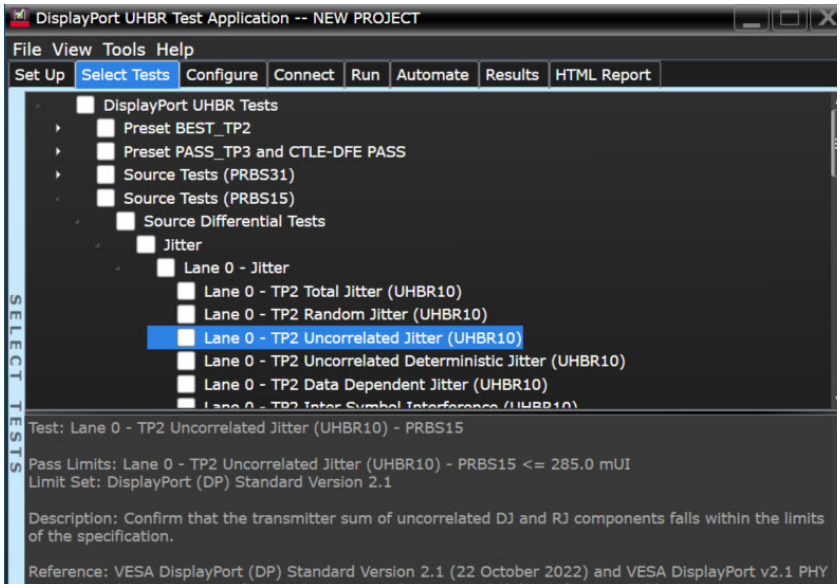
13441, 13442, 13443, 13444 – TP2 Uncorrelated Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter sum of uncorrelated DJ and RJ components falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.
2 Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
3 Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
4 Capture TJ and DDJ (EZJIT) results.
5 Calculate UJ=TJ-DDJ.
6 Repeat the test for all remaining lanes.

PASS Condition

UJ <= UJ_MAX

Table 17 UHBR DPTX TP2 Metrics System Parameters (Normative)

Symbol	Bit Rate	Max (UJ_MAX)	Unit	Comments
UJ	**UHBR10**	285	mUI	Peak-to-peak at $1E^{-9}$ BER [a]
	UHBR13.5	285	mUI	Peak-to-peak at $1E^{-9}$ BER [b]
	UHBR20	285	mUI	Peak-to-peak at $1E^{-9}$ BER [b]

a. Crest factor of 12
b. Extended from UHBR10

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-59, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-64, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured uncorrelated jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP2 Uncorrelated Deterministic Jitter

Test ID

11451, 11452, 11453, 11454 – TP2 Uncorrelated Deterministic Jitter (UHBR10)

12451, 12452, 12453, 12454 – TP2 Uncorrelated Deterministic Jitter (UHBR13.5)

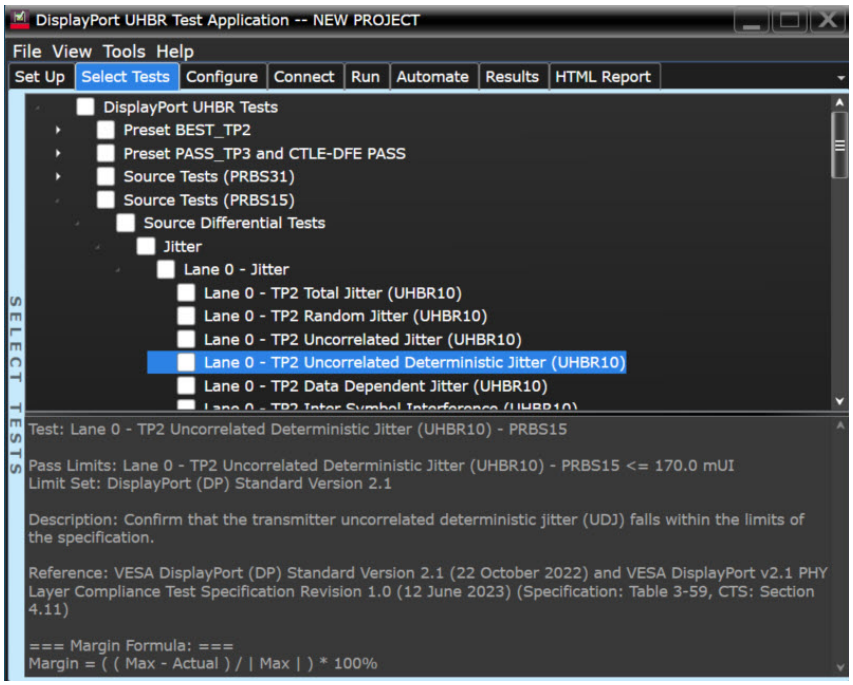
13451, 13452, 13453, 13454 – TP2 Uncorrelated Deterministic Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter uncorrelated deterministic jitter (UDJ) falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- NEW PROJECT
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort UHBR Tests
Preset BEST_TP2
Preset PASS_TP3 and CTLE-DFE PASS
Source Tests (PRBS31)
Source Tests (PRBS15)
Source Differential Tests
Jitter
Lane 0 - Jitter
Lane 0 - TP2 Total Jitter (UHBR10)
Lane 0 - TP2 Random Jitter (UHBR10)
Lane 0 - TP2 Uncorrelated Jitter (UHBR10)
Lane 0 - TP2 Uncorrelated Deterministic Jitter (UHBR10)
Lane 0 - TP2 Data Dependent Jitter (UHBR10)
Test: Lane 0 - TP2 Uncorrelated Deterministic Jitter (UHBR10) - PRBS15
Pass Limits: Lane 0 - TP2 Uncorrelated Deterministic Jitter (UHBR10) - PRBS15 <= 170.0 mUI
Limit Set: DisplayPort (DP) Standard Version 2.1
Description: Confirm that the transmitter uncorrelated deterministic jitter (UDJ) falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.1 (22 October 2022) and VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (12 June 2023) (Specification: Table 3-59, CTS: Section 4.11)
=== Margin Formula: ===
Margin = ((Max - Actual) / | Max |) * 100%

Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.
2. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
3. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
4. Capture the UDJ result (same as BUJ over the oscilloscope).
5. Repeat the test for all remaining lanes.

PASS Condition

UDJ <= UDJ_MAX

Table 18 UHBR DPTX TP2 Metrics System Parameters (Normative)

Symbol	Bit Rate	Max (UDJ_MAX)	Unit	Comments
UDJ	**UHBR10**	170	mUI	N/A
	UHBR13.5	170	mUI	N/A
	UHBR20	170	mUI	N/A

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-59, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-64, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured uncorrelated deterministic jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP2 Data Dependent Jitter (Information Only Test)

Test ID

11491, 11492, 11493, 11494 - TP2 Data Dependent Jitter (UHBR10)

12491, 12492, 12493, 12494 - TP2 Data Dependent Jitter (UHBR13.5)

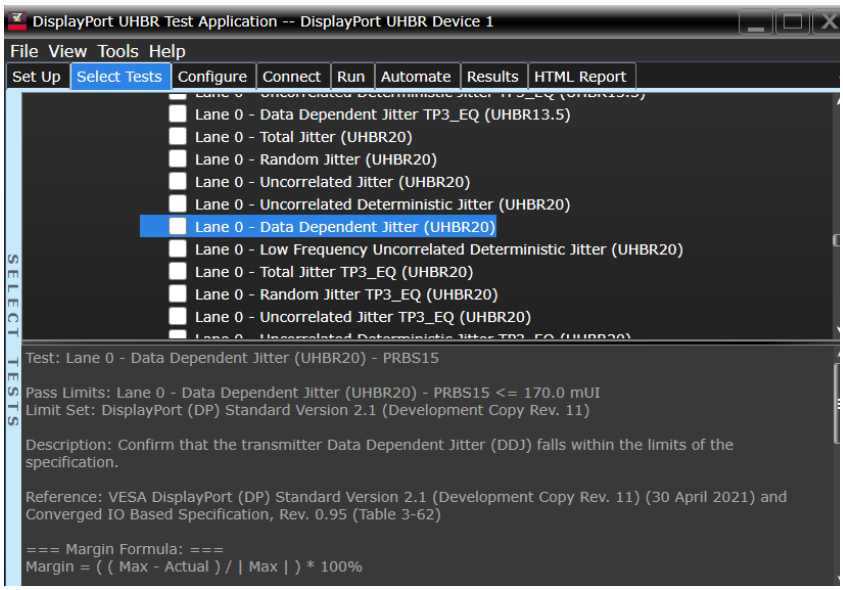
13491, 13492, 13493, 13494 - TP2 Data Dependent Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter data dependent jitter (DDJ) falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- DisplayPort UHBR Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
Lane 0 - Data Dependent Jitter TP3_EQ (UHBR13.5)
Lane 0 - Total Jitter (UHBR20)
Lane 0 - Random Jitter (UHBR20)
Lane 0 - Uncorrelated Jitter (UHBR20)
Lane 0 - Uncorrelated Deterministic Jitter (UHBR20)
Lane 0 - Data Dependent Jitter (UHBR20)
Lane 0 - Low Frequency Uncorrelated Deterministic Jitter (UHBR20)
Lane 0 - Total Jitter TP3_EQ (UHBR20)
Lane 0 - Random Jitter TP3_EQ (UHBR20)
Lane 0 - Uncorrelated Jitter TP3_EQ (UHBR20)
SELECT TESTS
Test: Lane 0 - Data Dependent Jitter (UHBR20) - PRBS15
Pass Limits: Lane 0 - Data Dependent Jitter (UHBR20) - PRBS15 <= 170.0 mUI
Limit Set: DisplayPort (DP) Standard Version 2.1 (Development Copy Rev. 11)
Description: Confirm that the transmitter Data Dependent Jitter (DDJ) falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.1 (Development Copy Rev. 11) (30 April 2021) and Converged IO Based Specification, Rev. 0.95 (Table 3-62)
=== Margin Formula: ===
Margin = ((Max - Actual) / | Max |) * 100%

Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.
2. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
3. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
4. Capture the Data Deterministic Jitter (DDJ) result.
5. Repeat the test for all remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-59, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-64, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured data deterministic jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the "PASS Condition" section of this test.

TP2 Inter Symbol Interference (Information Only Test)

Test ID

11461, 11462, 11463, 11464 – TP2 Inter Symbol Interference (UHBR10)

12461, 12462, 12463, 12464 – TP2 Inter Symbol Interference (UHBR13.5)

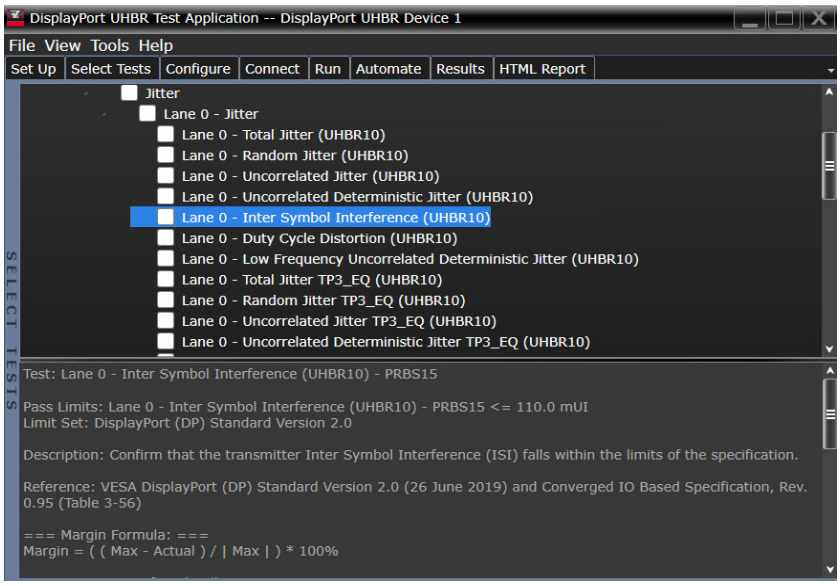
13461, 13462, 13463, 13464 – TP2 Inter Symbol Interference (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter Inter Symbol Interference (ISI) falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- DisplayPort UHBR Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Jitter
Lane 0 - Jitter
Lane 0 - Total Jitter (UHBR10)
Lane 0 - Random Jitter (UHBR10)
Lane 0 - Uncorrelated Jitter (UHBR10)
Lane 0 - Uncorrelated Deterministic Jitter (UHBR10)
Lane 0 - Inter Symbol Interference (UHBR10)
Lane 0 - Duty Cycle Distortion (UHBR10)
Lane 0 - Low Frequency Uncorrelated Deterministic Jitter (UHBR10)
Lane 0 - Total Jitter TP3_EQ (UHBR10)
Lane 0 - Random Jitter TP3_EQ (UHBR10)
Lane 0 - Uncorrelated Jitter TP3_EQ (UHBR10)
Lane 0 - Uncorrelated Deterministic Jitter TP3_EQ (UHBR10)
Test: Lane 0 - Inter Symbol Interference (UHBR10) - PRBS15
Pass Limits: Lane 0 - Inter Symbol Interference (UHBR10) - PRBS15 <= 110.0 mUI
Limit Set: DisplayPort (DP) Standard Version 2.0
Description: Confirm that the transmitter Inter Symbol Interference (ISI) falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.0 (26 June 2019) and Converged IO Based Specification, Rev. 0.95 (Table 3-56)
=== Margin Formula: ===
Margin = ((Max - Actual) / | Max |) * 100%

Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.
2. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
3. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
4. Capture the Inter Symbol Interference (ISI) result.
5. Repeat the test for all remaining lanes.

PASS Condition

Informative test.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured inter symbol interference for the test signal shall be a valid result.

TP2 Duty Cycle Distortion (Information Only Test)

Test ID

11471, 11472, 11473, 11474 – TP2 Duty Cycle Distortion (UHBR10)

12471, 12472, 12473, 12474 – TP2 Duty Cycle Distortion (UHBR13.5)

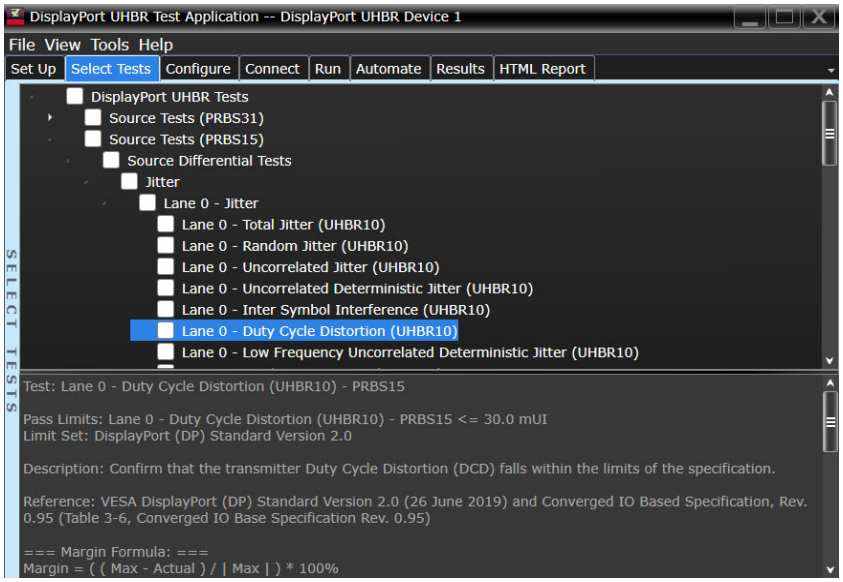
13471, 13472, 13473, 13474 – TP2 Duty Cycle Distortion (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter Duty Cycle Distortion falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- DisplayPort UHBR Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort UHBR Tests
Source Tests (PRBS31)
Source Tests (PRBS15)
Source Differential Tests
Jitter
Lane 0 - Jitter
Lane 0 - Total Jitter (UHBR10)
Lane 0 - Random Jitter (UHBR10)
Lane 0 - Uncorrelated Jitter (UHBR10)
Lane 0 - Uncorrelated Deterministic Jitter (UHBR10)
Lane 0 - Inter Symbol Interference (UHBR10)
Lane 0 - Duty Cycle Distortion (UHBR10)
Lane 0 - Low Frequency Uncorrelated Deterministic Jitter (UHBR10)
Test: Lane 0 - Duty Cycle Distortion (UHBR10) - PRBS15
Pass Limits: Lane 0 - Duty Cycle Distortion (UHBR10) - PRBS15 <= 30.0 mUI
Limit Set: DisplayPort (DP) Standard Version 2.0
Description: Confirm that the transmitter Duty Cycle Distortion (DCD) falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.0 (26 June 2019) and Converged IO Based Specification, Rev. 0.95 (Table 3-6, Converged IO Base Specification Rev. 0.95)
=== Margin Formula: ===
Margin = ((Max - Actual) / | Max |) * 100%

Measurement Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.

2 Perform measurements with:

- Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
- Oscilloscope bandwidth should be as specified in Table 4.

3 Capture the waveform and process it with the oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
- Adjust vertical scale to fit signal into oscilloscope screen.
- Perform jitter separation with:
  - Pattern length: Periodic
  - RJ Method: Spectral Only
  - BER Level: 1E-9

4 Capture the Duty Cycle Distortion (DCD) result.

5 Repeat the test for all the remaining lanes.

PASS Condition

DCD <= DCD_MAX

Table 19 Transmitter Parameters at TP2

Symbol	Bit Rate	Max (DCD_MAX)	Unit	Comments
UDJ	**UHBR10**	30	mUI	N/A
	UHBR13.5[a]	30	mUI	N/A
	UHBR20	30	mUI	N/A

a. Extended from UHBR20

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1 (October 22, 2022)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1 (October 22, 2022)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured duty cycle distortion for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP2 Low Frequency Uncorrelated Deterministic Jitter

Test ID

11481, 11482, 11483, 11484 – TP2 Low Frequency UDJ (UHBR10)

12481, 12482, 12483, 12484 – TP2 Low Frequency UDJ (UHBR13.5)

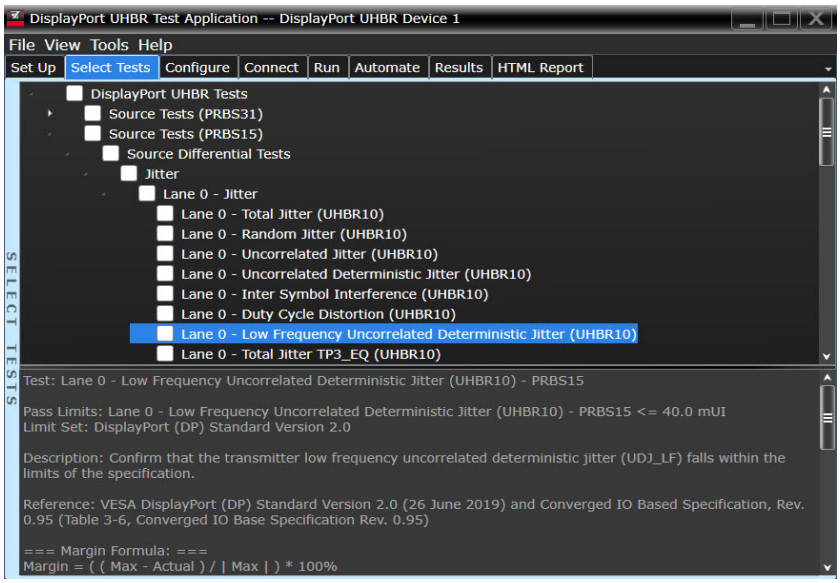
13481, 13482, 13483, 13484 – TP2 Low Frequency UDJ (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter low frequency uncorrelated deterministic jitter falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2 (UHBR10)
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- DisplayPort UHBR Device 1
File View Tools Help
Set Up
Select Tests
Configure
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort UHBR Tests
Source Tests (PRBS31)
Source Tests (PRBS15)
Source Differential Tests
Jitter
Lane 0 - Jitter
Lane 0 - Total Jitter (UHBR10)
Lane 0 - Random Jitter (UHBR10)
Lane 0 - Uncorrelated Jitter (UHBR10)
Lane 0 - Uncorrelated Deterministic Jitter (UHBR10)
Lane 0 - Inter Symbol Interference (UHBR10)
Lane 0 - Duty Cycle Distortion (UHBR10)
Lane 0 - Low Frequency Uncorrelated Deterministic Jitter (UHBR10)
Lane 0 - Total Jitter TP3_EQ (UHBR10)
Test: Lane 0 - Low Frequency Uncorrelated Deterministic Jitter (UHBR10) - PRBS15
Pass Limits: Lane 0 - Low Frequency Uncorrelated Deterministic Jitter (UHBR10) - PRBS15 <= 40.0 mUI
Limit Set: DisplayPort (DP) Standard Version 2.0
Description: Confirm that the transmitter low frequency uncorrelated deterministic jitter (UDJ_LF) falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.0 (26 June 2019) and Converged IO Based Specification, Rev. 0.95 (Table 3-6, Converged IO Base Specification Rev. 0.95)
=== Margin Formula: ===
Margin = ((Max - Actual) / | Max |) * 100%

Measurement Procedure

1 Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset Best_TP2" on page 38.

2 Perform measurements with:
- Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
- Oscilloscope bandwidth should be as specified in Table 4.

3 Capture the waveform and process it with the oscilloscope:
- Sampling Rate ≥ 80 GSa/s
- Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
- Adjust vertical scale to fit signal into oscilloscope screen.
- Perform jitter separation with:
  - Pattern length: Periodic
  - RJ Method: Spectral Only
  - BER Level: 1E-9

4 Apply 2^{nd} order Low-Pass-Filter (LPF) with 3 dB cut-off at 0.5 MHz on Time Interval Error (TIE).

5 Capture the UDJ_LF result (same as BUJ over the oscilloscope after apply LPF).

6 Repeat the test for all remaining lanes.

PASS Condition

UDJ_LF <= UDJ_LF_MAX

Table 20 Transmitter Parameters at TP2

Symbol	Bit Rate	Max (UDJ_LF_MAX)	Unit	Comments
UDJ	**UHBR10**	58	mUI	N/A
	UHBR13.5[a]	70	mUI	N/A
	UHBR20	75	mUI	N/A

a. Extended from UHBR20

Test References

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-59, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-64, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured low frequency uncorrelated deterministic jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP3_CTLE Total Jitter (Information Only Test)

Test ID

11621, 11622, 11623, 11624 – TP3_CTLE Total Jitter (UHBR10)

12621, 12622, 12623, 12624 – TP3_CTLE Total Jitter (UHBR13.5)

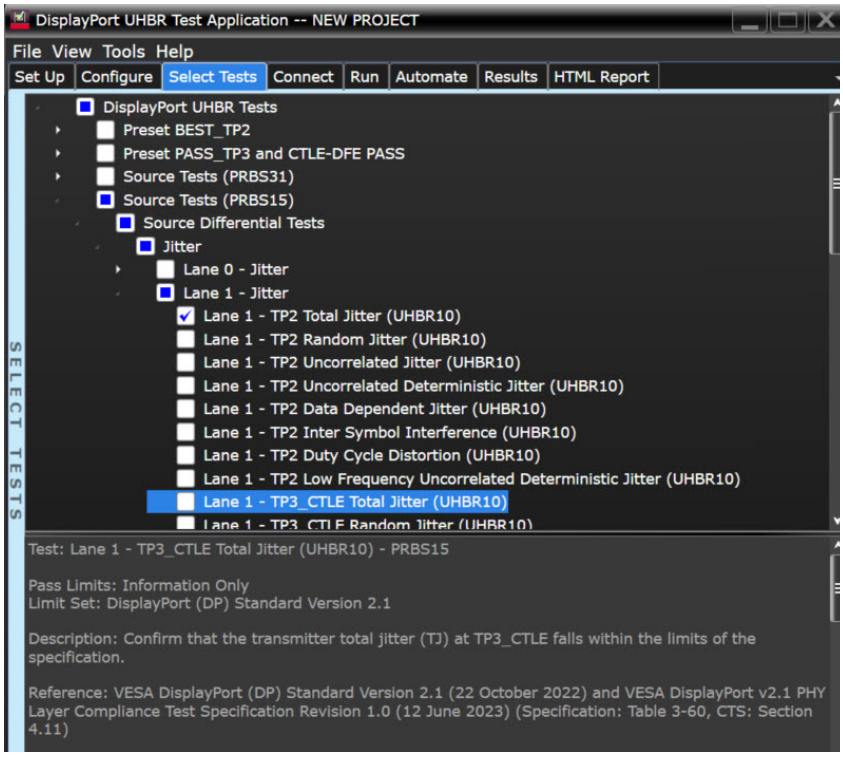
13621, 13622, 13623, 13624 – TP3_CTLE Total Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter total jitter (TJ) at TP3_CTLE falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP3_CTLE
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP3_CTLE
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- NEW PROJECT
File View Tools Help
Set Up
Configure
Select Tests
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort UHBR Tests
Preset BEST_TP2
Preset PASS_TP3 and CTLE-DFE PASS
Source Tests (PRBS31)
Source Tests (PRBS15)
Source Differential Tests
Jitter
Lane 0 - Jitter
Lane 1 - Jitter
Lane 1 - TP2 Total Jitter (UHBR10)
Lane 1 - TP2 Random Jitter (UHBR10)
Lane 1 - TP2 Uncorrelated Jitter (UHBR10)
Lane 1 - TP2 Uncorrelated Deterministic Jitter (UHBR10)
Lane 1 - TP2 Data Dependent Jitter (UHBR10)
Lane 1 - TP2 Inter Symbol Interference (UHBR10)
Lane 1 - TP2 Duty Cycle Distortion (UHBR10)
Lane 1 - TP2 Low Frequency Uncorrelated Deterministic Jitter (UHBR10)
Lane 1 - TP3_CTLE Total Jitter (UHBR10)
Lane 1 - TP3_CTLE Random Jitter (UHBR10)
Test: Lane 1 - TP3_CTLE Total Jitter (UHBR10) - PRBS15
Pass Limits: Information Only
Limit Set: DisplayPort (DP) Standard Version 2.1
Description: Confirm that the transmitter total jitter (TJ) at TP3_CTLE falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.1 (22 October 2022) and VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (12 June 2023) (Specification: Table 3-60, CTS: Section 4.11)

Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number.
2. Embed the cable model based on connector type.
3. Ensure that measurements are done with optimum reference receiver equalizer (CTLE and DFE).
4. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
5. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
6. Capture the Total Jitter (TJ) result.
7. Repeat the test for all the remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-60, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-65, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP3_CTLE Random Jitter (Information Only Test)

Test ID

11631, 11632, 11633, 11634 – TP3_CTLE Random Jitter (UHBR10)

12631, 12632, 12633, 12634 – TP3_CTLE Random Jitter (UHBR13.5)

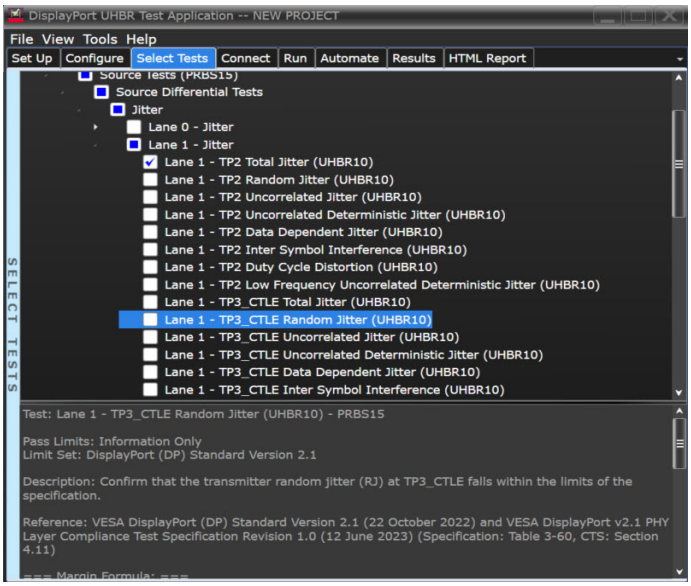
13631, 13632, 13633, 13634 – TP3_CTLE Random Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter random jitter (RJ) at TP3_CTLE falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP3_CTLE
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP3_CTLE
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- NEW PROJECT
File View Tools Help
Set Up
Configure
Select Tests
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Source Tests (PRBS15)
Source Differential Tests
Jitter
Lane 0 - Jitter
Lane 1 - Jitter
Lane 1 - TP2 Total Jitter (UHBR10)
Lane 1 - TP2 Random Jitter (UHBR10)
Lane 1 - TP2 Uncorrelated Jitter (UHBR10)
Lane 1 - TP2 Uncorrelated Deterministic Jitter (UHBR10)
Lane 1 - TP2 Data Dependent Jitter (UHBR10)
Lane 1 - TP2 Inter Symbol Interference (UHBR10)
Lane 1 - TP2 Duty Cycle Distortion (UHBR10)
Lane 1 - TP2 Low Frequency Uncorrelated Deterministic Jitter (UHBR10)
Lane 1 - TP3_CTLE Total Jitter (UHBR10)
Lane 1 - TP3_CTLE Random Jitter (UHBR10)
Lane 1 - TP3_CTLE Uncorrelated Jitter (UHBR10)
Lane 1 - TP3_CTLE Uncorrelated Deterministic Jitter (UHBR10)
Lane 1 - TP3_CTLE Data Dependent Jitter (UHBR10)
Lane 1 - TP3_CTLE Inter Symbol Interference (UHBR10)
Test: Lane 1 - TP3_CTLE Random Jitter (UHBR10) - PRBS15
Pass Limits: Information Only
Limit Set: DisplayPort (DP) Standard Version 2.1
Description: Confirm that the transmitter random jitter (RJ) at TP3_CTLE falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.1 (22 October 2022) and VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (12 June 2023) (Specification: Table 3-60, CTS: Section 4.11)
=== Margin Formula: ===

Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
2. Embed the cable model based on connector type.
3. Ensure that measurements are done with optimum reference receiver equalizer (CTLE and DFE). Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
4. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
5. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
6. Capture the Random Jitter (RJ) result.
7. Repeat the test for all the remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-60, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-65, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured random jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP3_CTLE Uncorrelated Jitter (Information Only Test)

Test ID

11641, 11642, 11643, 11644 – TP3_CTLE Uncorrelated Jitter (UHBR10)

12641, 12642, 12643, 12644 – TP3_CTLE Uncorrelated Jitter (UHBR13.5)

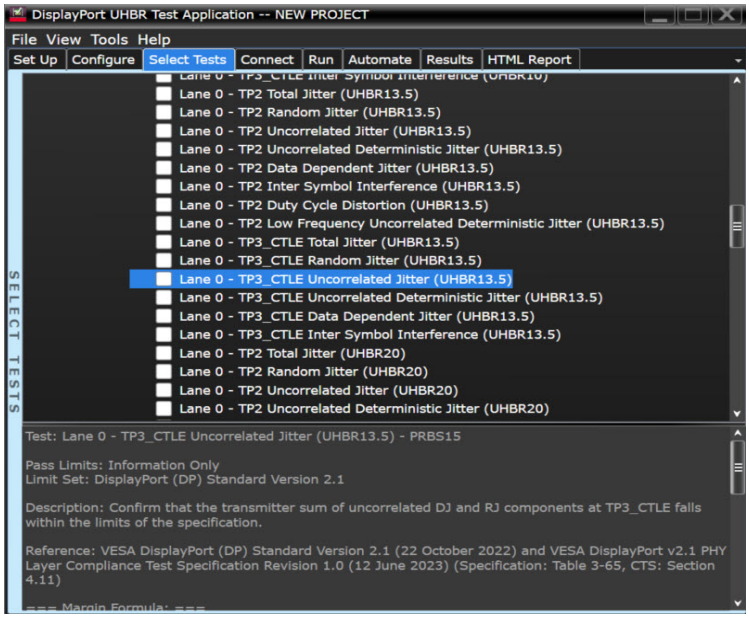
13641, 13642, 13643, 13644 – TP3_CTLE Uncorrelated Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter sum of uncorrelated DJ and RJ components at TP3_CTLE falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP3_CTLE
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP3_CTLE
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent


DisplayPort UHBR Test Application -- NEW PROJECT
File View Tools Help
Set Up
Configure
Select Tests
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
Lane 0 - TP2 Total Jitter (UHBR13.5)
Lane 0 - TP2 Random Jitter (UHBR13.5)
Lane 0 - TP2 Uncorrelated Jitter (UHBR13.5)
Lane 0 - TP2 Uncorrelated Deterministic Jitter (UHBR13.5)
Lane 0 - TP2 Data Dependent Jitter (UHBR13.5)
Lane 0 - TP2 Inter Symbol Interference (UHBR13.5)
Lane 0 - TP2 Duty Cycle Distortion (UHBR13.5)
Lane 0 - TP2 Low Frequency Uncorrelated Deterministic Jitter (UHBR13.5)
Lane 0 - TP3_CTLE Total Jitter (UHBR13.5)
Lane 0 - TP3_CTLE Random Jitter (UHBR13.5)
Lane 0 - TP3_CTLE Uncorrelated Jitter (UHBR13.5)
Lane 0 - TP3_CTLE Uncorrelated Deterministic Jitter (UHBR13.5)
Lane 0 - TP3_CTLE Data Dependent Jitter (UHBR13.5)
Lane 0 - TP3_CTLE Inter Symbol Interference (UHBR13.5)
Lane 0 - TP2 Total Jitter (UHBR20)
Lane 0 - TP2 Random Jitter (UHBR20)
Lane 0 - TP2 Uncorrelated Jitter (UHBR20)
Lane 0 - TP2 Uncorrelated Deterministic Jitter (UHBR20)
Test: Lane 0 - TP3_CTLE Uncorrelated Jitter (UHBR13.5) - PRBS15
Pass Limits: Information Only
Limit Set: DisplayPort (DP) Standard Version 2.1
Description: Confirm that the transmitter sum of uncorrelated DJ and RJ components at TP3_CTLE falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.1 (22 October 2022) and VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (12 June 2023) (Specification: Table 3-65, CTS: Section 4.11)

Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
2. Embed the cable model based on connector type.
3. Ensure that measurements are done with optimum reference receiver equalizer (CTLE and DFE). Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
4. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
5. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
6. Capture TJ and DDJ (EZJIT) results.
7. Calculate UJ=TJ-DDJ.
8. Repeat the test for all remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-60, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-65, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured uncorrelated jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP3_CTLE Uncorrelated Deterministic Jitter (Information Only Test)

Test ID

11651, 11652, 11653, 11654 – TP3_CTLE Uncorrelated Deterministic Jitter (UHBR10)

12651, 12652, 12653, 12654 – TP3_CTLE Uncorrelated Deterministic Jitter (UHBR13.5)

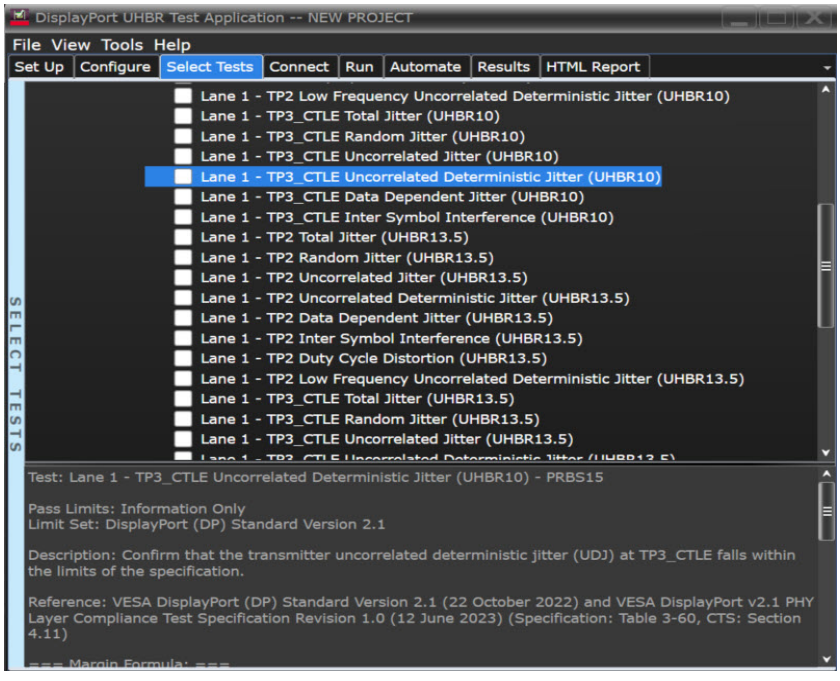
13651, 13652, 13653, 13654 – TP3_CTLE Uncorrelated Deterministic Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter uncorrelated deterministic jitter (UDJ) at TP3_CTLE falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP3_CTLE
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP3_CTLE
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
2. Embed the cable model based on connector type.
3. Ensure that measurements are done with optimum reference receiver equalizer (CTLE and DFE). Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
4. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
5. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
6. Capture the UDJ result (same as BUJ over the oscilloscope).
7. Repeat the test for all remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-60, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-65, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured uncorrelated deterministic jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

TP3_CTLE Data Dependent Jitter (Information Only Test)

Test ID

11691, 11692, 11693, 11694 - TP3_CTLE Data Dependent Jitter (UHBR10)

12691, 12692, 12693, 12694 - TP3_CTLE Data Dependent Jitter (UHBR13.5)

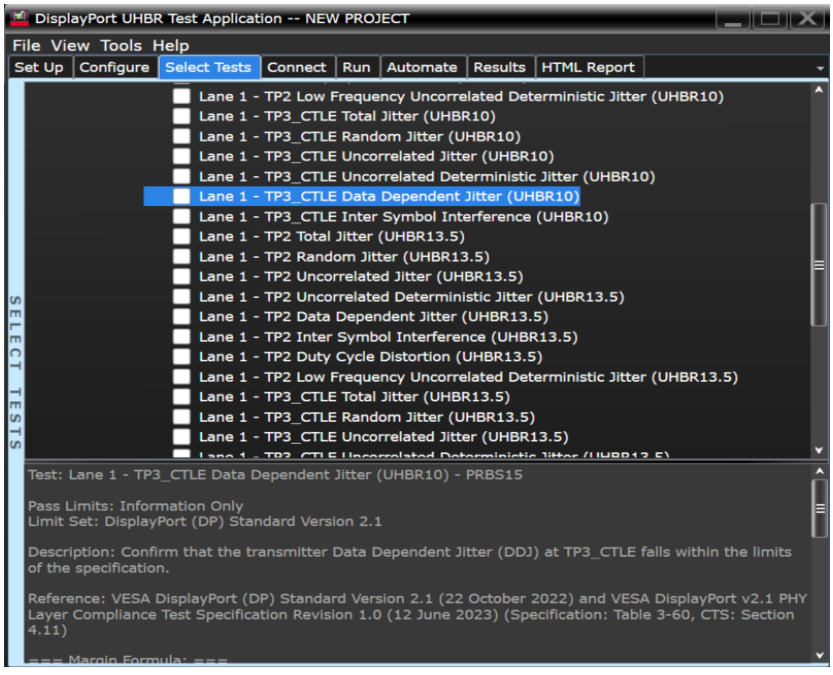
13691, 13692, 13693, 13694 - TP3_CTLE Data Dependent Jitter (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter data dependent jitter (DDJ) falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP3_CTLE
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP3_CTLE
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
2. Embed the cable model based on connector type.
3. Ensure that measurements are done with optimum reference receiver equalizer (CTLE and DFE). Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
4. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
5. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
6. Capture the Data Deterministic Jitter (DDJ) result.
7. Repeat the test for all remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-60, CTS: Section 4.11)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-65, CTS: Section 4.11)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured data deterministic jitter for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the "PASS Condition" section of this test.

TP3_CTLE Inter Symbol Interference (Information Only Test)

Test ID

11661, 11662, 11663, 11664 – TP3_CTLE Inter Symbol Interference (UHBR10)

12661, 12662, 12663, 12664 – TP3_CTLE Inter Symbol Interference (UHBR13.5)

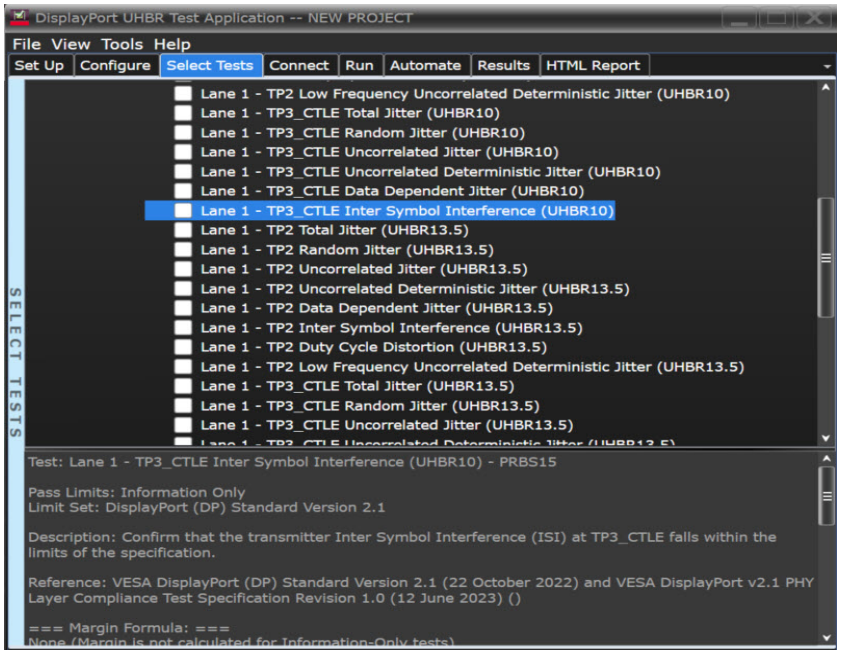
13661, 13662, 13663, 13664 – TP3_CTLE Inter Symbol Interference (UHBR20)

Test Overview

The objective of the test is to confirm that the transmitter Inter Symbol Interference (ISI) at TP3_CTLE falls within the limits of the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP3_CTLE
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP3_CTLE
Test Pattern	PRBS15
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent



Measurement Procedure

1. Configure the DUT transmitter to output PRBS15 on all lanes with SSC enabled for optimum preset number. Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
2. Embed the cable model based on connector type.
3. Ensure that measurements are done with optimum reference receiver equalizer (CTLE and DFE). Please see "Preset PASS_TP3 and CTLE-DFE PASS_TP3" on page 41.
4. Perform measurements with:
   - Reference CDR based on the "Reference Receiver Clock Data Recovery" on page 30; no average and no interpolation to be used.
   - Oscilloscope bandwidth should be as specified in Table 4.
5. Capture the waveform and process it with the oscilloscope:
   - Sampling Rate ≥ 80 GSa/s
   - Evaluate 40 Mpts per channel when using 80 GSa/s. For higher sample rates, use memory depth in the same ratio.
   - Adjust vertical scale to fit signal into oscilloscope screen.
   - Perform jitter separation with:
     - Pattern length: Periodic
     - RJ Method: Spectral Only
     - BER Level: 1E-9
6. Capture the Inter Symbol Interference (ISI) result.
7. Repeat the test for all remaining lanes.

PASS Condition

This test is for information only.

Test References

Please see:

- *For UHBR10*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
- *For UHBR13.5*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
- *For UHBR20*
  - *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
  - *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023)*
  - *SCR to Released DP2.1a on UHBR20 PHY Spec Update for Leveraging DP80LL Cable Loss Budget (Adopted) (December 12, 2024)*

Expected/Observable Results

The measured inter symbol interference for the test signal shall be a valid result.

Embedded Re-timer Frequency Variation

Test ID

11051, 11052, 11053, 11054 - Embedded Re-timer Frequency Variation (UHBR10)

12051, 12052, 12053, 12054 - Embedded Re-timer Frequency Variation (UHBR13.5)

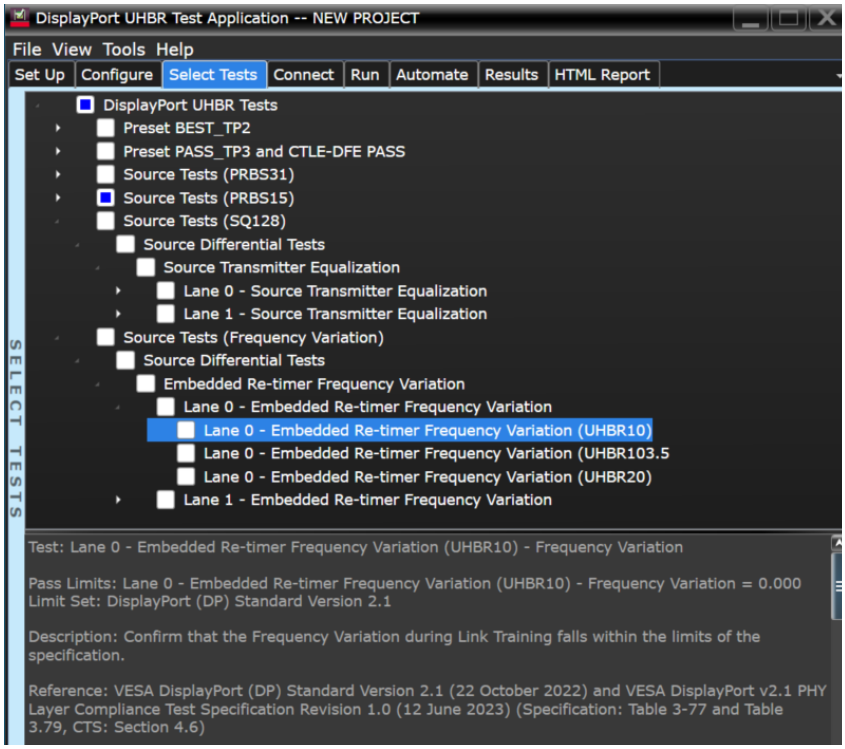
13051, 13052, 13053, 13054 - Embedded Re-timer Frequency Variation (UHBR20)

Test Overview

The objective of the test is to confirm that the frequency variation during source re-timer or LTTPR Clock Switch on any DP UHBR source device port does not exceed minimum or maximum values as mentioned in the specification.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	SQ2, PRBS31
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present


DisplayPort UHBR Test Application -- NEW PROJECT
File View Tools Help
Set Up
Configure
Select Tests
Connect
Run
Automate
Results
HTML Report
SELECT TESTS
DisplayPort UHBR Tests
Preset BEST_TP2
Preset PASS_TP3 and CTLE-DFE PASS
Source Tests (PRBS31)
Source Tests (PRBS15)
Source Tests (SQ128)
Source Differential Tests
Source Transmitter Equalization
Lane 0 - Source Transmitter Equalization
Lane 1 - Source Transmitter Equalization
Source Tests (Frequency Variation)
Source Differential Tests
Embedded Re-timer Frequency Variation
Lane 0 - Embedded Re-timer Frequency Variation
Lane 0 - Embedded Re-timer Frequency Variation (UHBR10)
Lane 0 - Embedded Re-timer Frequency Variation (UHBR103.5
Lane 0 - Embedded Re-timer Frequency Variation (UHBR20)
Lane 1 - Embedded Re-timer Frequency Variation
Test: Lane 0 - Embedded Re-timer Frequency Variation (UHBR10) - Frequency Variation
Pass Limits: Lane 0 - Embedded Re-timer Frequency Variation (UHBR10) - Frequency Variation = 0.000
Limit Set: DisplayPort (DP) Standard Version 2.1
Description: Confirm that the Frequency Variation during Link Training falls within the limits of the specification.
Reference: VESA DisplayPort (DP) Standard Version 2.1 (22 October 2022) and VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (12 June 2023) (Specification: Table 3-77 and Table 3.79, CTS: Section 4.6)

Measurement Procedure

1 Capture the clock switch during 3 stages: pre-clock switch, clock switch and post-clock switch in a single waveform and post process it as following:

   a The signal phase shall be extracted after applying a 2nd order Low-Pass-Filter (LPF) with 3 dB point at 5 MHz.

   b Calculate the initial non-modulated transmit frequency aka INIT_FREQ_VARIATION. Note: Initial frequency corresponds to the transmitter average frequency offset from the Link baseline rate, without including low frequency jitter variations, which shall be filtered out by averaging the extracted frequency variation waveform over a window of at least 30 us.

   c Calculate the frequency variations during the clock switch over 200 ns measurement windows aka DELTA_FREQ_200ns.

   d Calculate the frequency variation during the clock switch over 1000 ns measurement windows aka DELTA_FREQ_1000ns.

2 Repeat this procedure 20 times and report the worst case captured waveform.

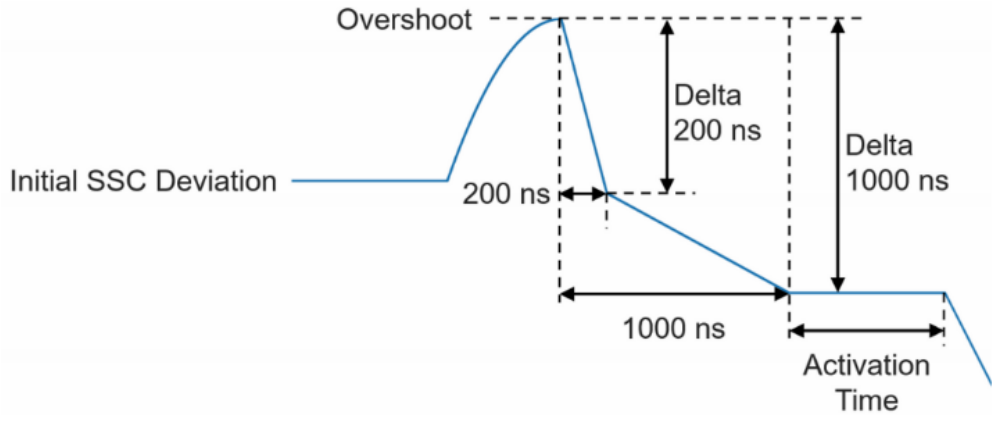


Figure 17 Measurement Parameters on the SSC Profile

PASS Condition

Table 21 UHBR DPTX TP2 Metrics System Parameters (Normative)

Symbol	Min	Max	Unit	Comments
INIT_FREQ_VARIATION	-300	300	ppm	
Overshoot		1400	ppm	
DELTA_FREQ_200ns		1400	ppm	
DELTA_FREQ_1000ns		2200	ppm	

Test References

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Table 3-77 and Table 3.79, CTS: Section 4.6)

Expected/Observable Results

The measured frequency variation training measurements for the test signal shall be within the conformance limits as specified in the specification and also mentioned under the “PASS Condition” section of this test.

Equalization

Test ID

119001, 119002, 119003, 119004 - Equalization Test Preset 0 (UHBR10)
129001, 129002, 129003, 129004 - Equalization Test Preset 0 (UHBR13.5)
139001, 139002, 139003, 139004 - Equalization Test Preset 0 (UHBR20)

119011, 119012, 119013, 119014 - Equalization Test Preset 1 (UHBR10)
129011, 129012, 129013, 129014 - Equalization Test Preset 1 (UHBR13.5)
139011, 139012, 139013, 139014 - Equalization Test Preset 1 (UHBR20)

119021, 119022, 119023, 119024 - Equalization Test Preset 2 (UHBR10)
129021, 129022, 129023, 129024 - Equalization Test Preset 2 (UHBR13.5)
139021, 139022, 139023, 139024 - Equalization Test Preset 2 (UHBR20)

119031, 119032, 119033, 119034 - Equalization Test Preset 3 (UHBR10)
129031, 129032, 129033, 129034 - Equalization Test Preset 3 (UHBR13.5)
139031, 139032, 139033, 139034 - Equalization Test Preset 3 (UHBR20)

119041, 119042, 119043, 119044 - Equalization Test Preset 4 (UHBR10)
129041, 129042, 129043, 129044 - Equalization Test Preset 4 (UHBR13.5)
139041, 139042, 139043, 139044 - Equalization Test Preset 4 (UHBR20)

119051, 119052, 119053, 119054 - Equalization Test Preset 5 (UHBR10)
129051, 129052, 129053, 129054 - Equalization Test Preset 5 (UHBR13.5)
139051, 139052, 139053, 139054 - Equalization Test Preset 5 (UHBR20)

119061, 119062, 119063, 119064 - Equalization Test Preset 6 (UHBR10)
129061, 129062, 129063, 129064 - Equalization Test Preset 6 (UHBR13.5)
139061, 139062, 139063, 139064 - Equalization Test Preset 6 (UHBR20)

119071, 119072, 119073, 119074 - Equalization Test Preset 7 (UHBR10)
129071, 129072, 129073, 129074 - Equalization Test Preset 7 (UHBR13.5)
139071, 139072, 139073, 139074 - Equalization Test Preset 7 (UHBR20)

119081, 119082, 119083, 119084 - Equalization Test Preset 8 (UHBR10)
129081, 129082, 129083, 129084 - Equalization Test Preset 8 (UHBR13.5)
139081, 139082, 139083, 139084 - Equalization Test Preset 8 (UHBR20)

119091, 119092, 119093, 119094 - Equalization Test Preset 9 (UHBR10)
129091, 129092, 129093, 129094 - Equalization Test Preset 9 (UHBR13.5)
139091, 139092, 139093, 139094 - Equalization Test Preset 9 (UHBR20)

119101, 119102, 119103, 119104 - Equalization Test Preset 10 (UHBR10)
129101, 129102, 129103, 129104 - Equalization Test Preset 10 (UHBR13.5)
139101, 139102, 139103, 139104 - Equalization Test Preset 10 (UHBR20)

119111, 119112, 119113, 119114 - Equalization Test Preset 11 (UHBR10)
129111, 129112, 129113, 129114 - Equalization Test Preset 11 (UHBR13.5)
139111, 139112, 139113, 139114 - Equalization Test Preset 11 (UHBR20)

119121, 119122, 119123, 119124 - Equalization Test Preset 12 (UHBR10)
129121, 129122, 129123, 129124 - Equalization Test Preset 12(UHBR13.5)
139121, 139122, 139123, 139124 - Equalization Test Preset 12 (UHBR20)

119131, 119132, 119133, 119134 - Equalization Test Preset 13 (UHBR10)
129131, 129132, 129133, 129134 - Equalization Test Preset 13 (UHBR13.5)
139131, 139132, 139133, 139134 - Equalization Test Preset 13 (UHBR20)

119141, 119142, 119143, 119144 - Equalization Test Preset 14 (UHBR10)
129141, 129142, 129143, 129144 - Equalization Test Preset 14 (UHBR13.5)
139141, 139142, 139143, 139144 - Equalization Test Preset 14 (UHBR20)

119151, 119152, 119153, 119154 - Equalization Test Preset 15 (UHBR10)
129151, 129152, 129153, 129154 - Equalization Test Preset 15 (UHBR13.5)
139151, 139152, 139153, 139154 - Equalization Test Preset 15 (UHBR20)

11951, 11951, 11953, 11954 - Transmitter Swing Preset 15 (UHBR10)
12951, 12951, 12953, 12954 - Transmitter Swing Preset 15 (UHBR13.5)
13951, 13951, 13953, 13954 - Transmitter Swing Preset 15 (UHBR20)

Test Overview

The objective of the equalization tests is to confirm that the transmitter equalization is within the limits of the specification. There are 3 criteria being measured in this test:

- "Equalization Pre-shoot (Preset 0 ~ Preset 15)
- "Equalization De-emphasis (Preset 0 ~ Preset 15)
- "Transmitter Swing Preset 15

Test Conditions

Test Parameter	Condition
Test Point	TP2 (UHBR10)
Bit Rate	UHBR10, UHBR13.5, or UHBR20
Spread Spectrum Clocking	SSC Enabled or SSC Disabled
Preset Number	Any preset number optimized for TP2
Test Pattern	SQ128
Lane Setting	All test lanes are supported
Connection Type	Single Ended, Differential, and Switch Matrix
Re-timer	Re-timer Present or Re-timer Absent

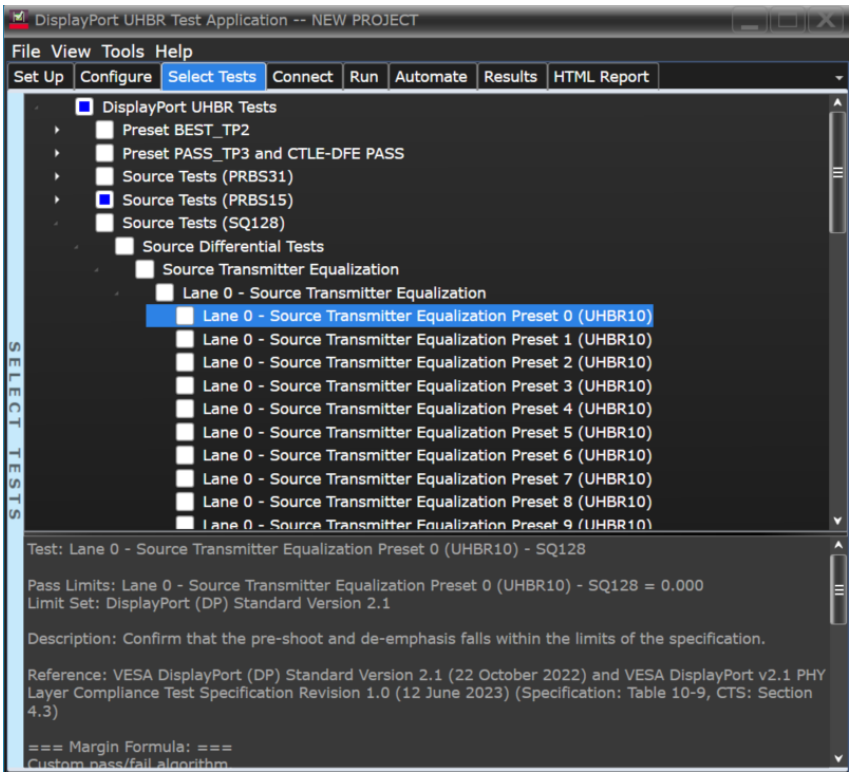


Table 22 Transmitter Equalization Preset Table

Preset	Pre-shoot	De-emphasis
0	0	0
1	0	-1.9
2	0	-3.6
3	0	-5.0
4	0	-8.4
5	0.9	0
6	1.1	-1.9
7	1.4	-3.8
8	1.7	-5.8
9	2.1	-8.0
10	1.7	0
11	2.2	-2.2
12	2.5	-3.6
13	3.4	-6.7
14	3.6	0
15	1.7	-1.7

Two Methods for Calculating Pre-Shoot and De-Emphasis

Method 1

- Configuration 1: $V_1 = (C_{-1} + C_0 + C_1) * V_{swing}$
- Configuration 2: $V_2 = (-C_{-1} + C_0 + C_1) * V_{swing}$
- Configuration 3: $V_3 = (C_{-1} + C_0 - C_1) * V_{swing}$

- Preshoot = $20*\log_{10}[(-C_{-1} + C_0 + C_1) / (C_{-1} + C_0 + C_1)] = 20*\log_{10}(V_2/V_1)$

- Deemphasis = $20*\log_{10}[(C_{-1} + C_0 + C_1) / (C_{-1} + C_0 - C_1)] = 20*\log_{10}(V_1/V_3)$

Method 2

- Configuration 1: $V'_2 = (C_0 + C_1) * Vswing$
- Configuration 2: $V'_3 = (C_{-1} + C_0) * Vswing$
- Configuration 3: $V'_4 = C_0 * Vswing$

- Preshoot = $20*\log_{10}[(-C_{-1} + C_0 + C_1) / (C_{-1} + C_0 + C_1)] = 20*\log_{10}[(V'_2 - V'_3 + V'_4) / (V'_2 + V'_3 - V'_4)]$

- Deemphasis = $20*\log_{10}[(C_{-1} + C_0 + C_1) / (C_{-1} + C_0 - C_1)] = 20*\log_{10}[(V'_2 + V'_3 - V'_4) / (-V'_2 + V'_3 + V'_4)]$

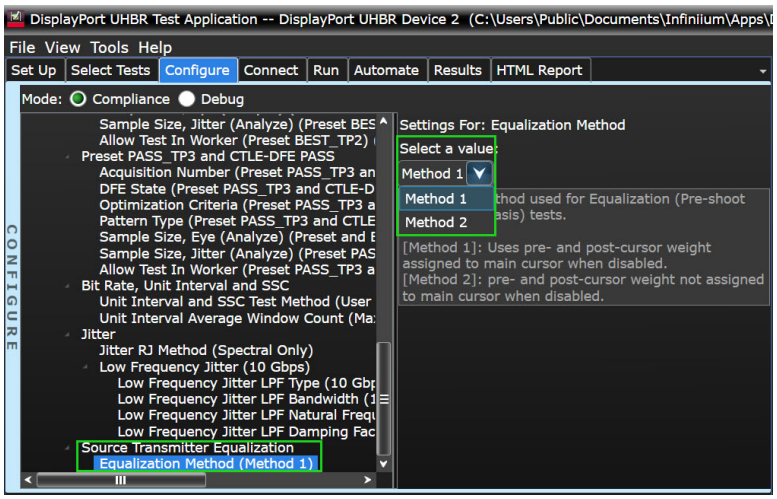
NOTE

The difference in configuration and calculation between Method 1 and Method 2:

Configuration (1) – Normal FFE: Preshoot Enabled, De-emphasis Enabled
Configuration (2) – De-emphasis only: Preshoot Disabled, De-emphasis Enabled
Configuration (3) – Preshoot only: Preshoot Enabled, De-emphasis Disabled
Configuration (4) – No FFE: Preshoot Disabled, De-emphasis Disabled

Steps to Select Method 1 or Method 2

1 Navigate to **Configure** tab > **Source Transmitter Equalization** > **Equalization Method**



2 Now, select either **Method 1** or **Method 2**, as required.

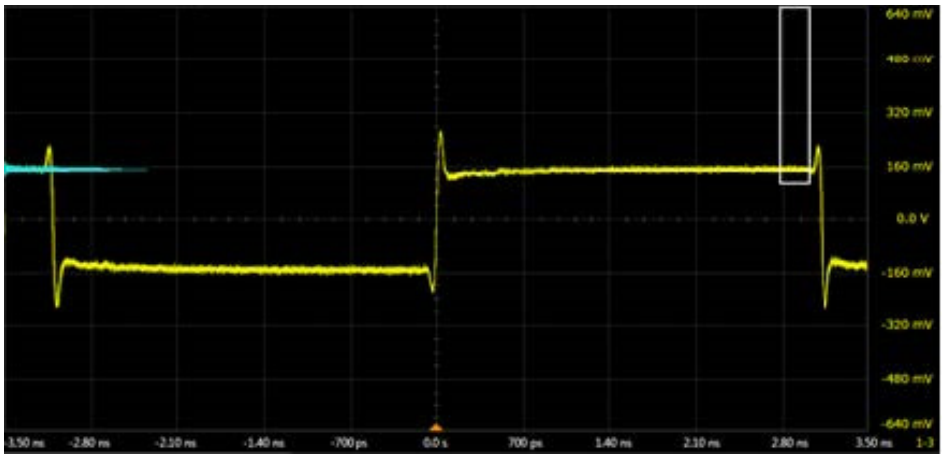
Measurement Procedure

For Equalization Pre-shoot and Equalization De-emphasis:

1 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled for Preset 0 along with both pre-shoot and de-emphasis enabled.

2 Capture the waveform and process it with the oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Evaluate 100 kpts per channel when using 80 GSa/s. For higher sample rate, use memory depth in the same ratio.
- Average one cycle using 150 cycles, no CDR and no interpolation to be used
- Adjust vertical scale to fit signal into oscilloscope screen.
- Oscilloscope bandwidth should be as specified in Table 4.



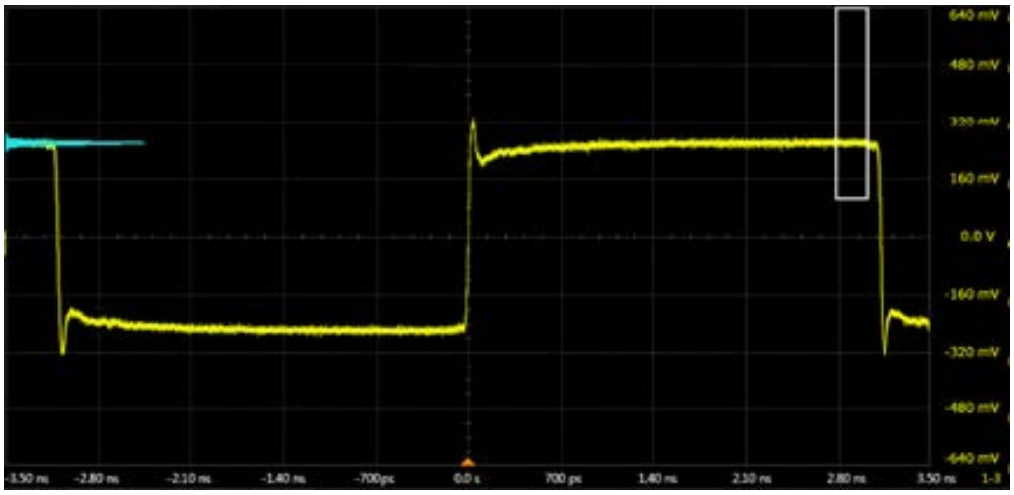
3 Measure differential amplitude voltage (V_1) for bits 57 to 62 using the equation:
$V1 = [|V_{bits(57-62)}$ (64 bits of 1's) - $V_{bits(57-62)}$ (64 bits of 0's)|]

4 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled for Preset 0 along with de-emphasis enabled but no pre-shoot.

5 Capture the waveform and process it with the oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Evaluate 100 kpts per channel when using 80 GSa/s. For higher sample rate, use memory depth in the same ratio.
- Average one cycle using 150 cycles, no CDR and no interpolation to be used
- Adjust vertical scale to fit signal into oscilloscope screen.

- Oscilloscope bandwidth should be as specified in Table 4.

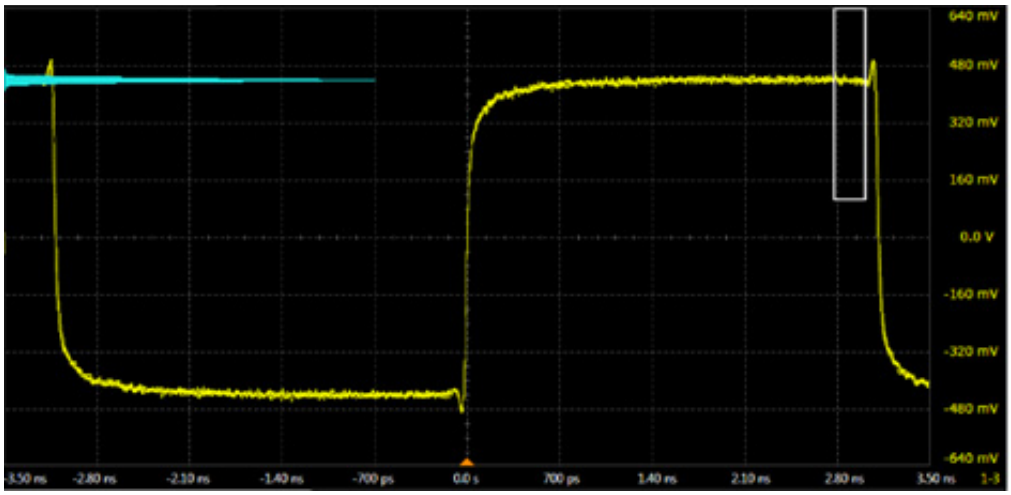


6 Measure differential amplitude voltage (V_2 or V'_2) for bits 57 to 62 using the equation:
V_2 or V'_2= [|$V_{bits(57-62)}$ (64 bits of 1's) - $V_{bits(57-62)}$ (64 bits of 0's)|]

7 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled for Preset 0 along with pre-shoot enabled but no de-emphasis.

8 Capture the waveform and process it with the oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Evaluate 100 kpts per channel when using 80 GSa/s. For higher sample rate, use memory depth in the same ratio.
- Average one cycle using 150 cycles, no CDR and no interpolation to be used
- Adjust vertical scale to fit signal into oscilloscope screen.
- Oscilloscope bandwidth should be as specified in Table 4.

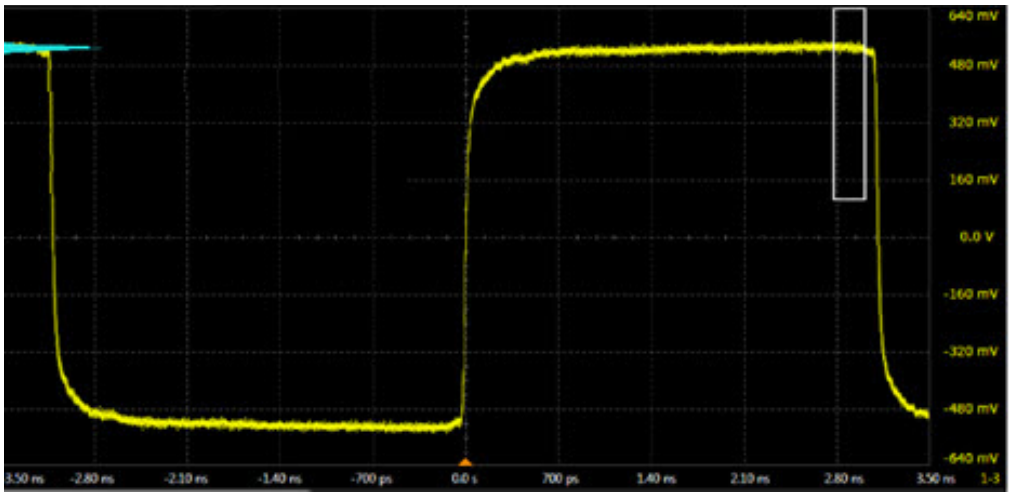


9 Measure differential amplitude voltage (V_3 or V'_3) for bits 57 to 62 using the equation:
V_3 or V'_3 = [|$V_{bits(57-62)}$ (64 bits of 1's) - $V_{bits(57-62)}$ (64 bits of 0's)|]

10 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled for Preset 0 along with de-emphasis enabled but no pre-shoot.

11 Capture the waveform and process it with the oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Evaluate 100 kpts per channel when using 80 GSa/s. For higher sample rate, use memory depth in the same ratio.
- Average one cycle using 150 cycles, no CDR and no interpolation to be used
- Adjust vertical scale to fit signal into oscilloscope screen.
- Oscilloscope bandwidth should be as specified in Table 4.



12 Measure differential amplitude voltage (V'_4) for bits 57 to 62 using the equation:
$V'_4 = [|V_{bits(57-62)}\ (64\ bits\ of\ 1's) - V_{bits(57-62)}\ (64\ bits\ of\ 0's)|]$

13 Calculate the Pre-shoot and De-emphasis values as per formulas mentioned in "Two Methods for Calculating Pre-Shoot and De-Emphasis" on page 140.

14 Repeat steps 2 to 10 for all Presets defined in Table 22.

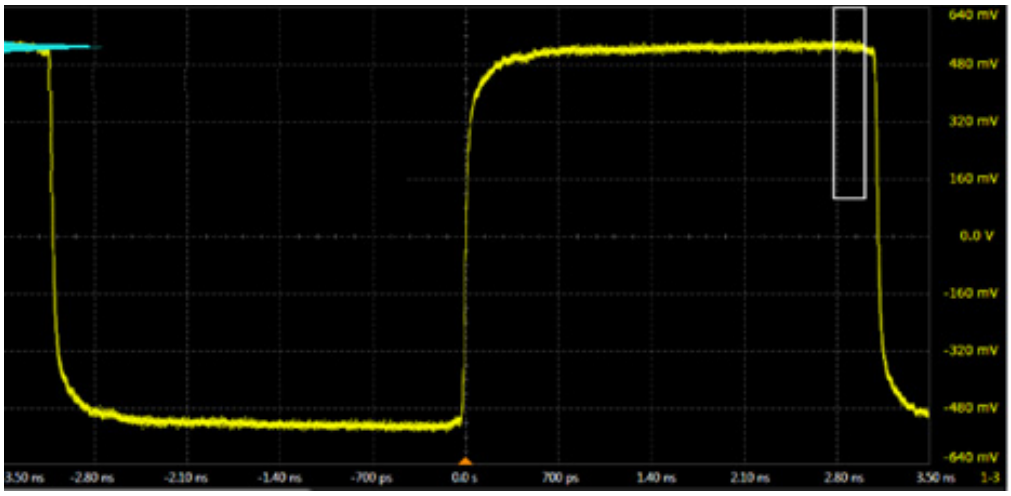
15 Check for PASS/FAIL conditions for both Pre-shoot and De-emphasis.

For Transmitter Swing Preset 15:

1 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled for Preset 0 but with both pre-shoot and de-emphasis disabled.

2 Capture the waveform and process it with the oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Evaluate 100 kpts per channel when using 80 GSa/s. For higher sample rate, use memory depth in the same ratio.
- Average one cycle using 150 cycles, no CDR and no interpolation to be used
- Adjust vertical scale to fit signal into oscilloscope screen.
- Oscilloscope bandwidth should be as specified in Table 4.

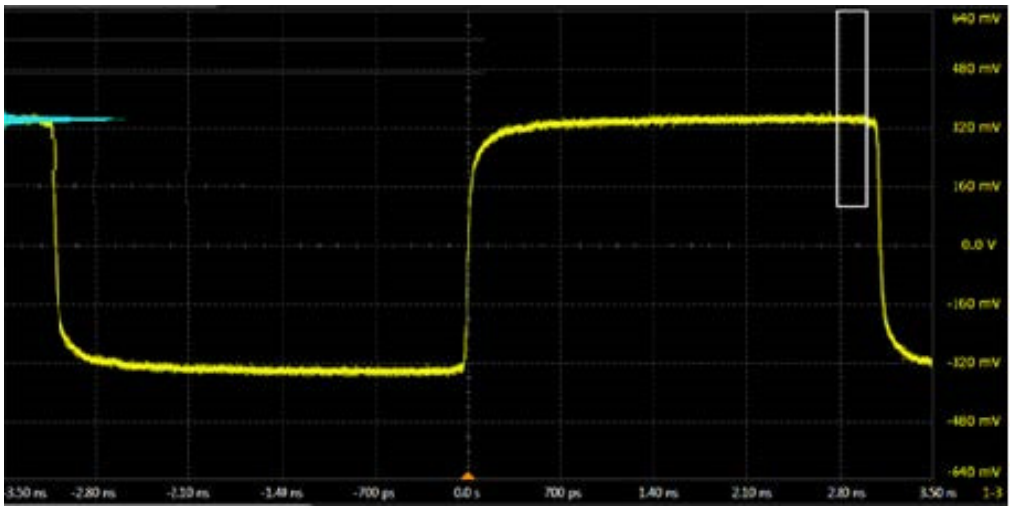


3 Measure differential amplitude voltage (V_0) for bits 57 to 62 using the equation:
$V_0 = [|V_{bits(57-62)}$ (64 bits of 1's) - $V_{bits(57-62)}$ (64 bits of 0's)$|]$

4 Configure the DUT transmitter to output alternating square pattern of 64 0's and 64 1's on all lanes with SSC enabled for Preset 15 but with both pre-shoot and de-emphasis disabled.

5 Capture the waveform and process it with the oscilloscope:

- Sampling Rate ≥ 80 GSa/s
- Evaluate 100 kpts per channel when using 80 GSa/s. For higher sample rate, use memory depth in the same ratio.
- Average one cycle using 150 cycles, no CDR and no interpolation to be used
- Adjust vertical scale to fit signal into oscilloscope screen.
- Oscilloscope bandwidth should be as specified in Table 4.



6 Measure differential amplitude voltage (V_{15}) for bits 57 to 62 using the equation:
V_{15} = [|$V_{bits(57-62)}$ (64 bits of 1's) - $V_{bits(57-62)}$ (64 bits of 0's)|]
Calculate Transmitter Swing Preset 15 to be 20 * $\log_{10}[V_0/V_{15}]$

7 Repeat the test for all the remaining lanes.

PASS Condition

For Equalization Pre-shoot

- If the Pre-Shoot for a particular Preset number is not within ± 1dB of the matching value in Table 30, the status of test is FAIL.

For Equalization De-emphasis

- If the De-Emphasis for a particular Preset number is not within ± 1dB of the matching value in Table 30, the status of test is FAIL.

For Transmitter Swing Preset 15

- 2.5 dB <= Transmitter Swing Preset 15 <= 4.5 dB

Test References

- *VESA DisplayPort (DP) Standard Version 2.1a (December 18, 2023)*
- *VESA DisplayPort v2.1 PHY Layer Compliance Test Specification Revision 1.0 (June 12, 2023) (Specification: Section 3.5.5.3, Table 3-57, CTS: Section 4.3)*

Expected/Observable Results

The measured transmitter equalization shall be within the conformance limits as specified in the specification and also mentioned under the "PASS Condition" section of this test.

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