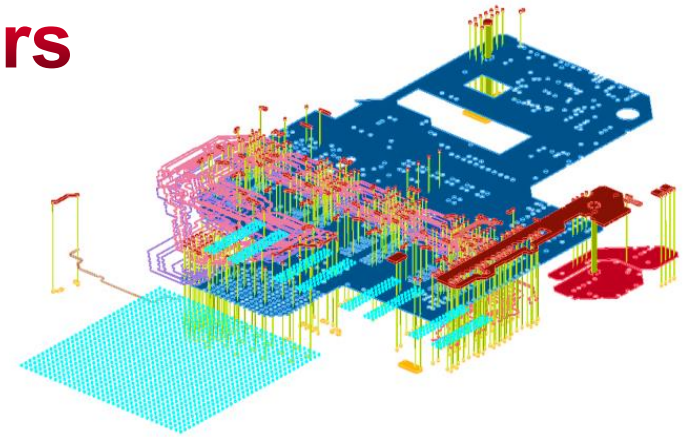
Power Integrity Boot Camp for Designers



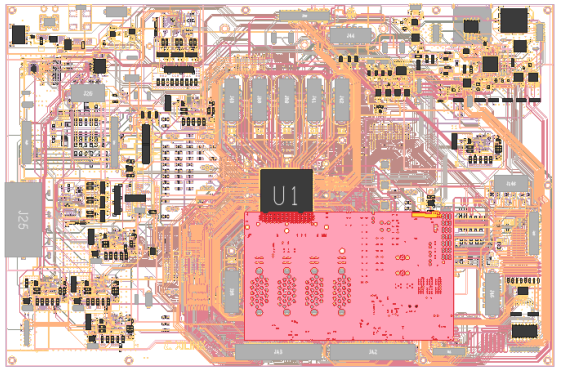
Section 4
Decoupling Capacitor Optimization and the Power Integrity Ecosystem

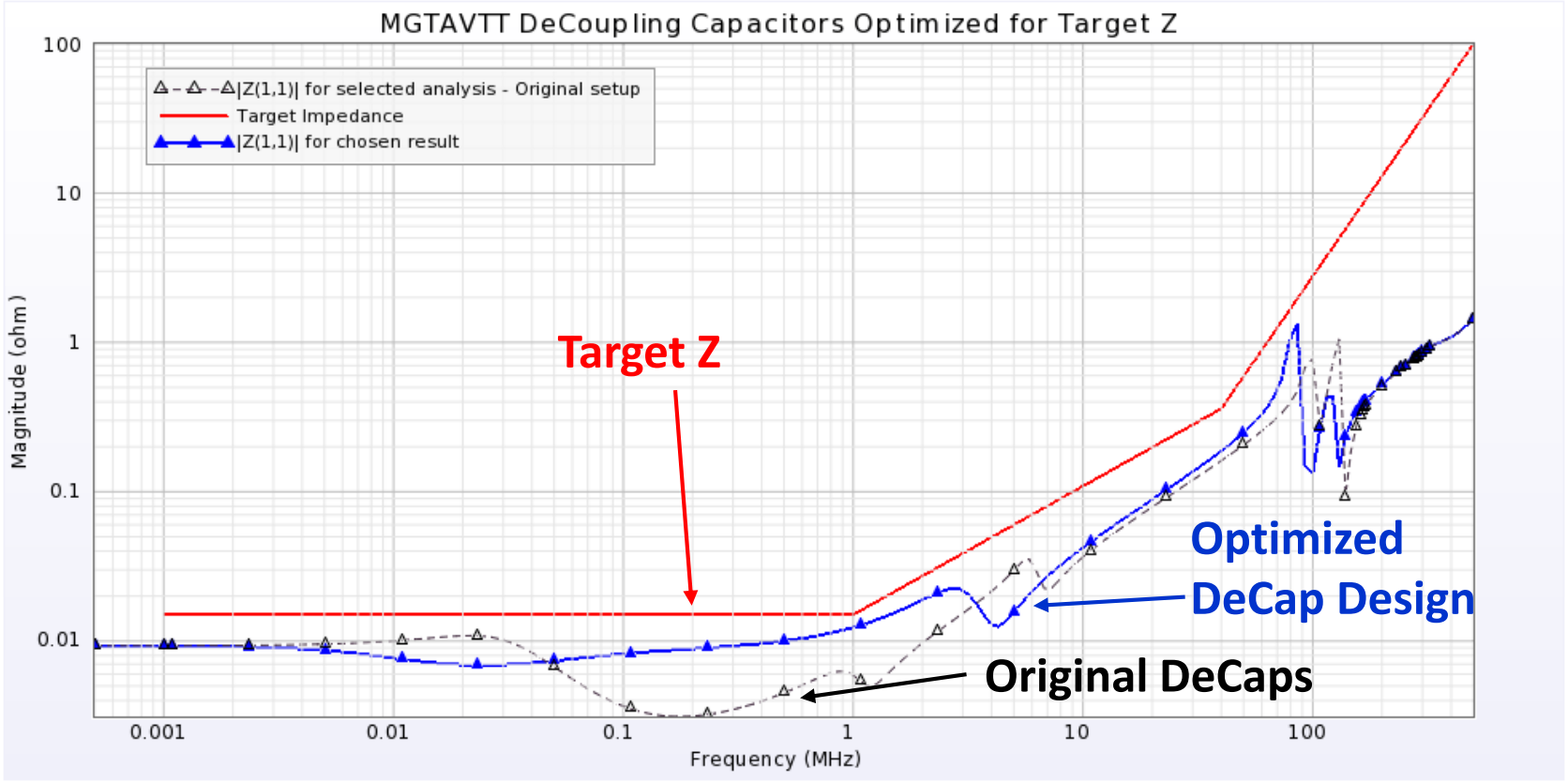
KEYSIGHT TECHNOLOGIES

with solutions partner

PICOTEST

PCB Decoupling Capacitor Optimization





Decoupling Capacitors

Yes	C190	330 uF
Yes	C215	330 uF
Yes	C216	330 uF
Yes	C218	330 uF
Yes	C303	220 nF
Yes	C305	220 nF
Yes	C750	220 nF
Yes	C753	220 nF
Yes	C757	220 nF
No	C217	100 uF
No	C225	100 uF
No	C315	4.7 uF
No	C316	4.7 uF
No	C778	4.7 uF
No	C779	4.7 uF
No	C780	4.7 uF

40% Fewer Components

Fewer solder joints higher reliability

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Design Methodology for DeCap Optimization

3 STEP PROCESS

1. Calculate 1st order approximations

$$C_{bulk} = \frac{L_{supply}}{Z_{Target}^2} \qquad C_{decap} = \frac{ESL_{Cbulk}}{Z_{Target}^2} \qquad \text{Max } L_{PDN} = C_{pkg} * Z_{Target}^2$$

2. Use Target Z to optimize the decoupling capacitor selection using high fidelity EM models (ADS PIPro)

3. Validate with full Power Integrity Eco-System simulation in ADS

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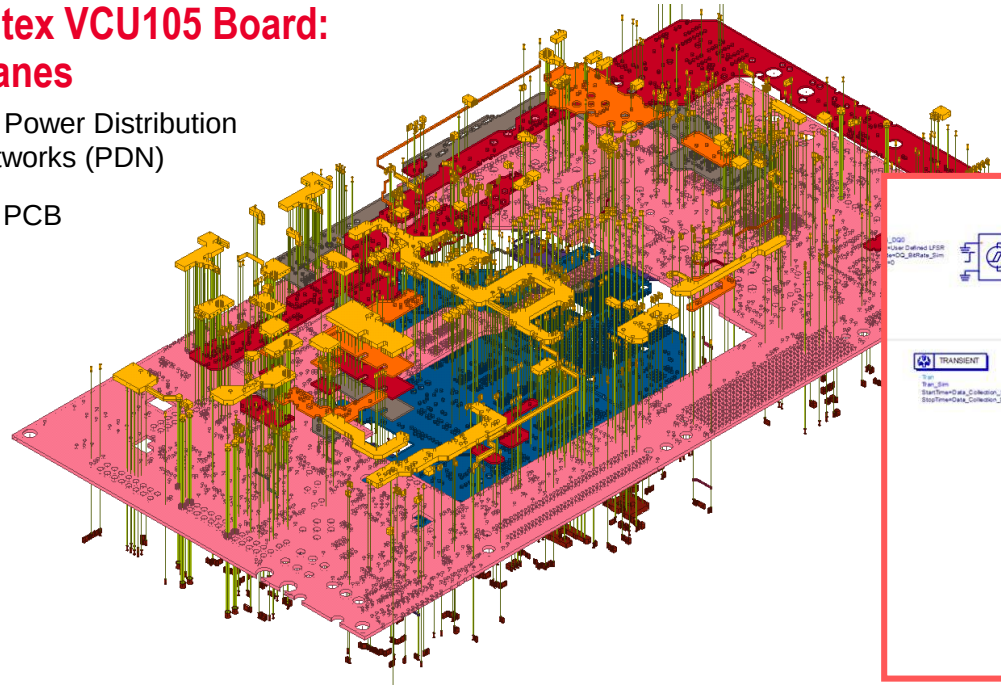
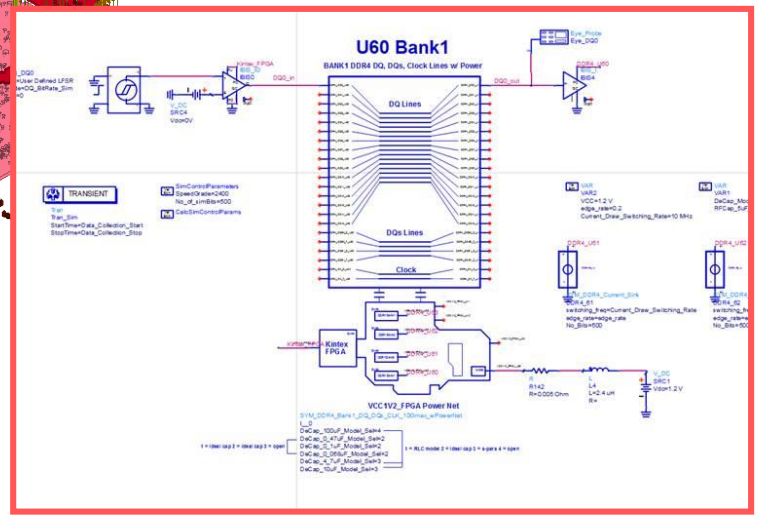
Modern Applications with Multiple PDNs

Xilinx Kintex VCU105 Board: Power Planes

15 Major Power Distribution Networks (PDN)

16 Layer PCB





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ADS PIPro EM Simulation of the PCB PDN

1) IMPORT THE PCB

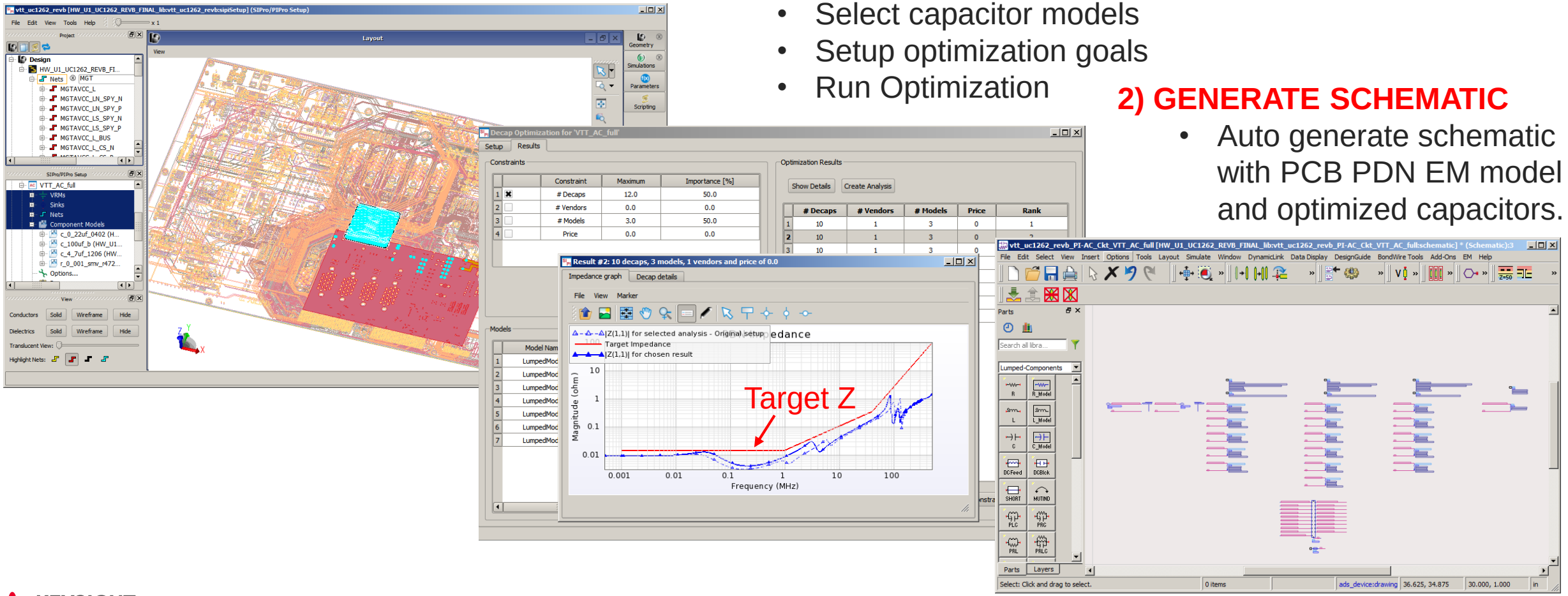
- Select VRM, Sink, Nets, Components
- Run EM AC Frequency Sweep

2) OPTIMIZE DECOUPLING

- Select capacitor models
- Setup optimization goals
- Run Optimization

2) GENERATE SCHEMATIC

- Auto generate schematic with PCB PDN EM model and optimized capacitors.



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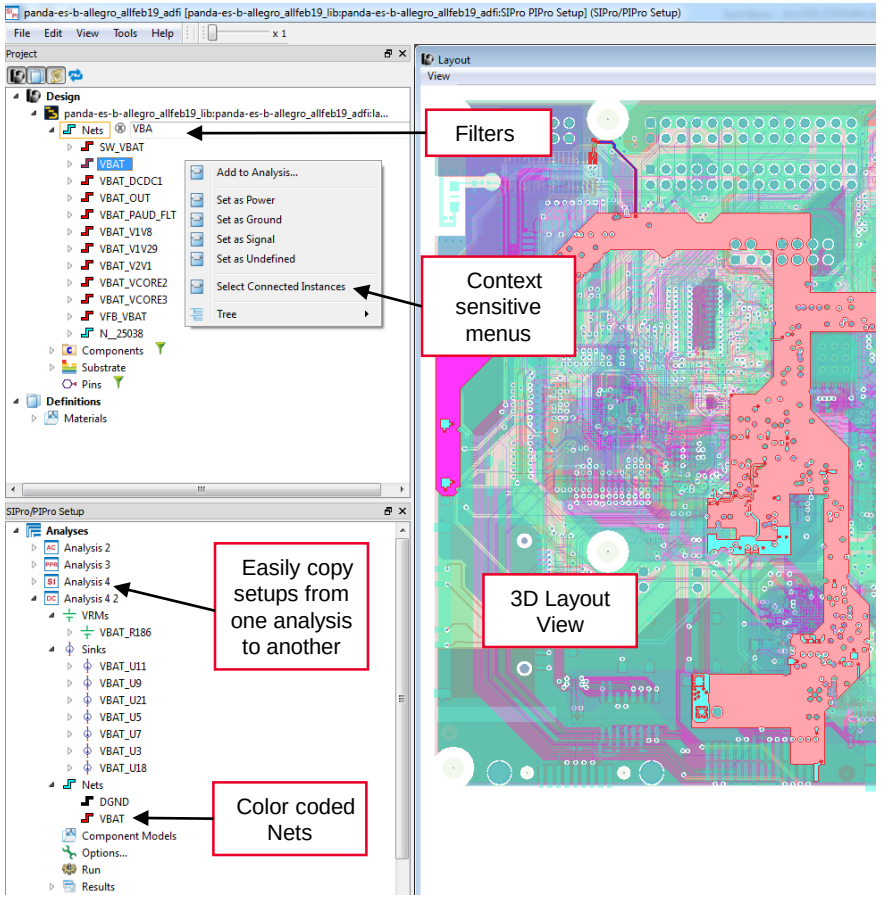
PIPro: PI-specific use-model and flow

Designed for Usability

- Filter by Net
- Filter by Component
- Right-click to add-to-analysis
- Drag & Drop
- Hierarchical search for complex selections
- Context sensitive menus e.g. *'Select instances connected to ONLY the selected nets'*



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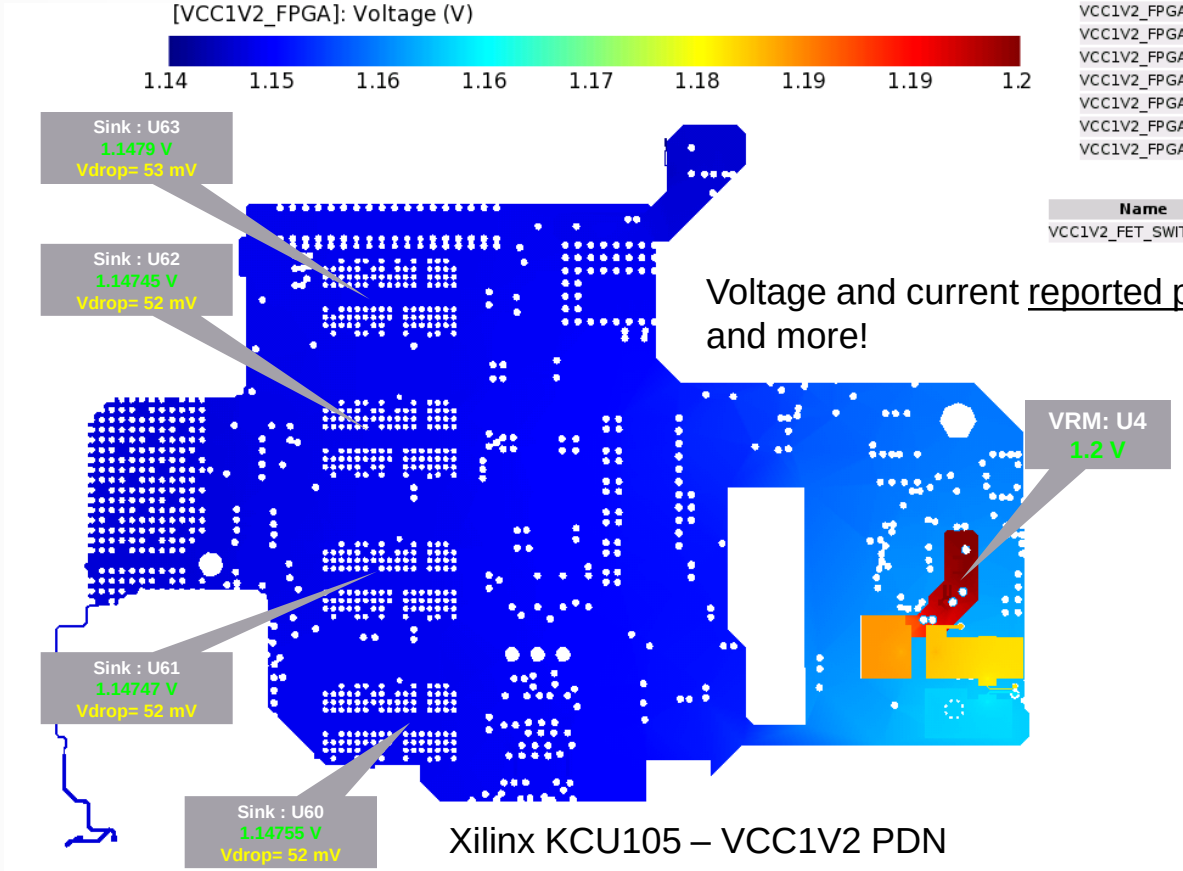
PIPro – DC IR Drop



Xilinx KCU105 – VCC1V2 PDN

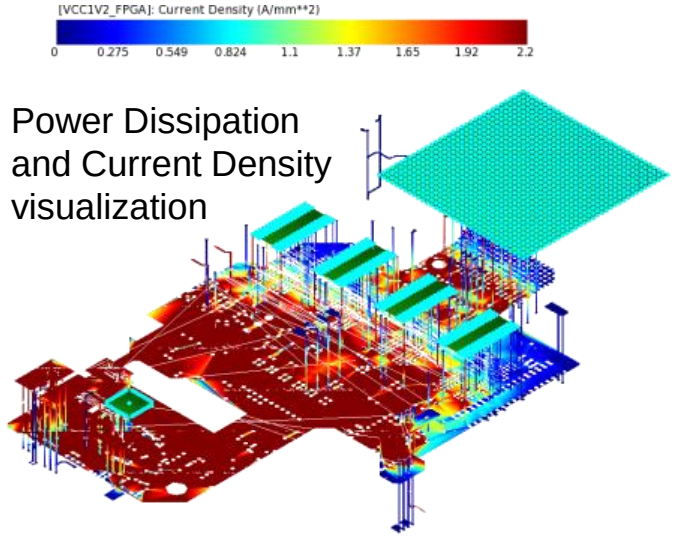
SINKs

Name	Source Current	VRM Voltage	Input Voltage	Tolerance	Margin	Pass/Fail
VCC1V2_FPGA_U60	0.3 A	1.2 V	1.14755 V	5 %	0.00755 V	pass
VCC1V2_FPGA_U61	0.3 A	1.2 V	1.14749 V	5 %	0.00749 V	pass
VCC1V2_FPGA_U62	0.3 A	1.2 V	1.14745 V	5 %	0.00745 V	pass
VCC1V2_FPGA_U63	0.3 A	1.2 V	1.14747 V	5 %	0.00747 V	pass
VCC1V2_FPGA_U1	0.8 A	1.2 V	1.1463 V	5 %	0.0063 V	pass
VCC1V2_FPGA_U24	0.4 A	1.2 V	1.14094 V	5 %	0.00094 V	pass
VCC1V2_FPGA_U41	0.3 A	1.2 V	1.14687 V	5 %	0.00687 V	pass
VCC1V2_FPGA_U42	0.3 A	1.2 V	1.14715 V	5 %	0.00715 V	pass

VRMs

Name	Source Voltage	Output Voltage	Output Current	Tolerance	Margin	Pass/Fail
VCC1V2_FET_SWITCH_U4	1.2 V	1.2 V	-2.99999 A	5 %	0.06 V	pass

Voltage and current reported per Via, Sink, VRM and more!



Power Dissipation and Current Density visualization

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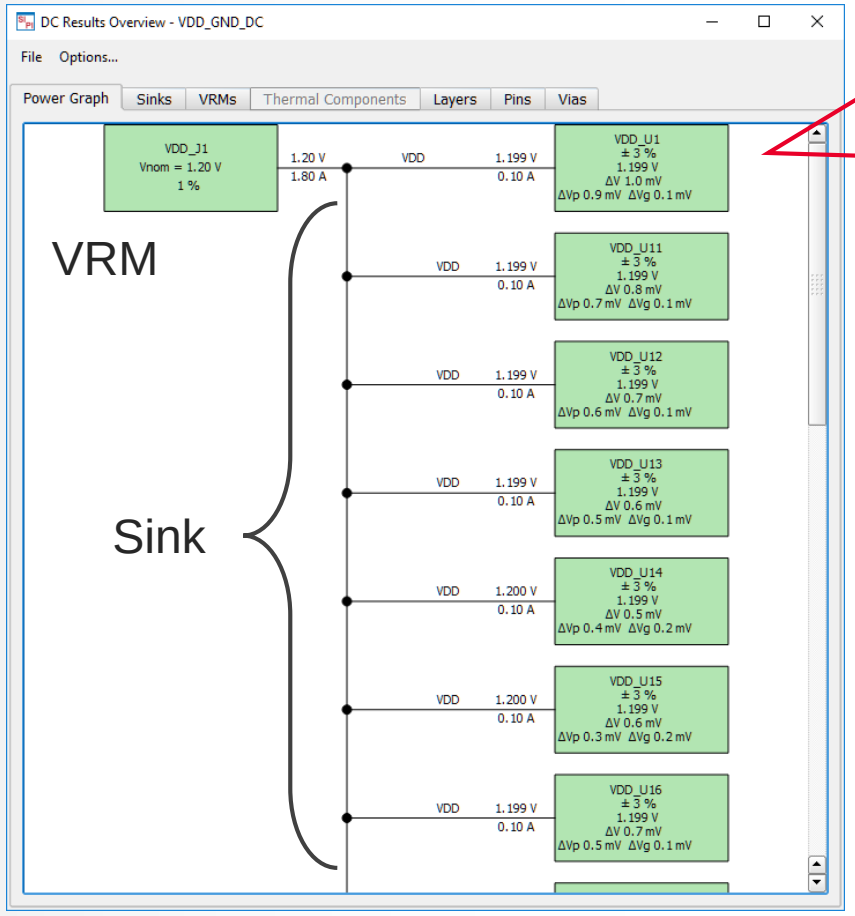
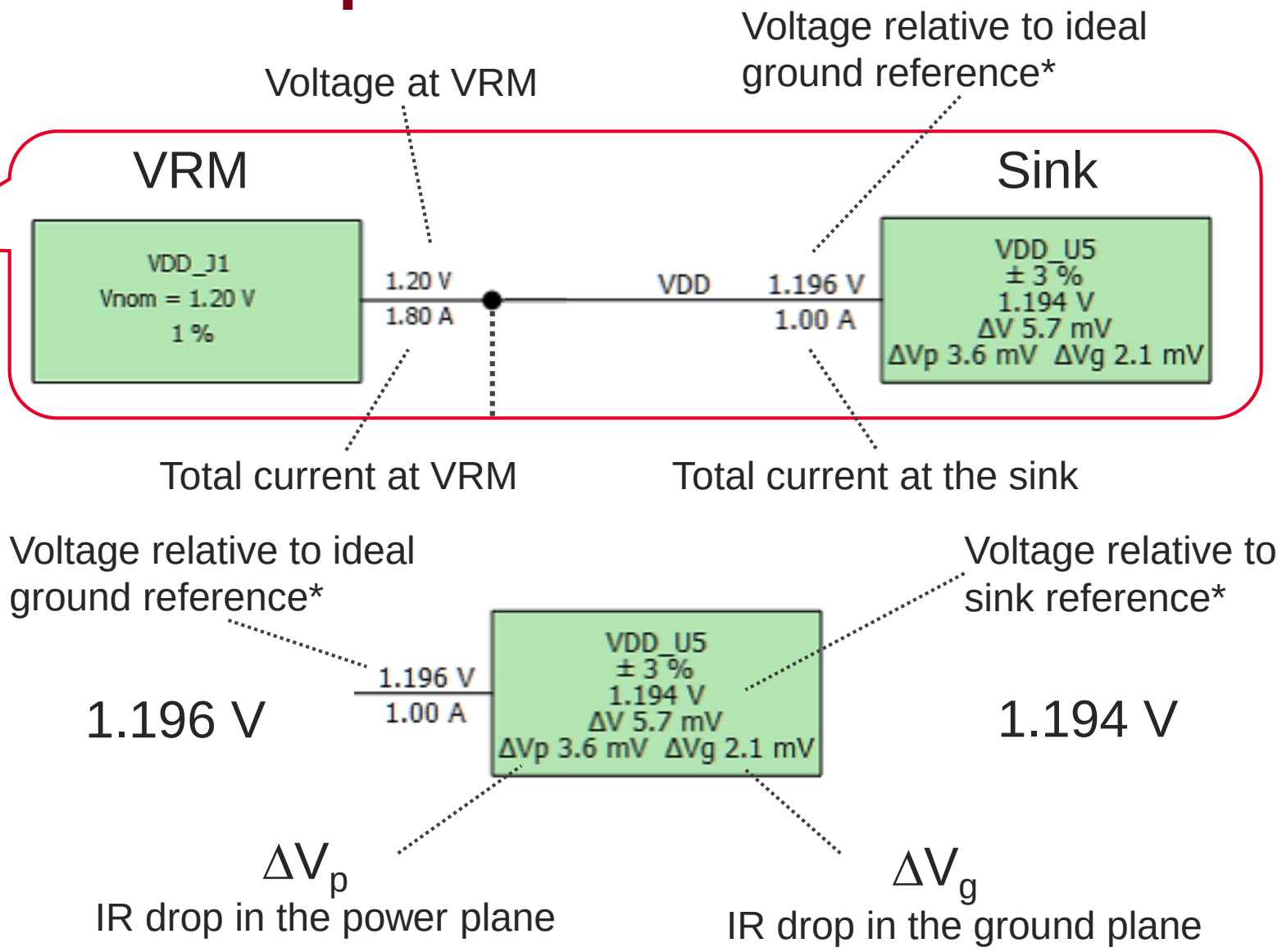
How to Interpret the Power Graph?

Power graph





*Try turning ideal ground on and off and see how power graph changes

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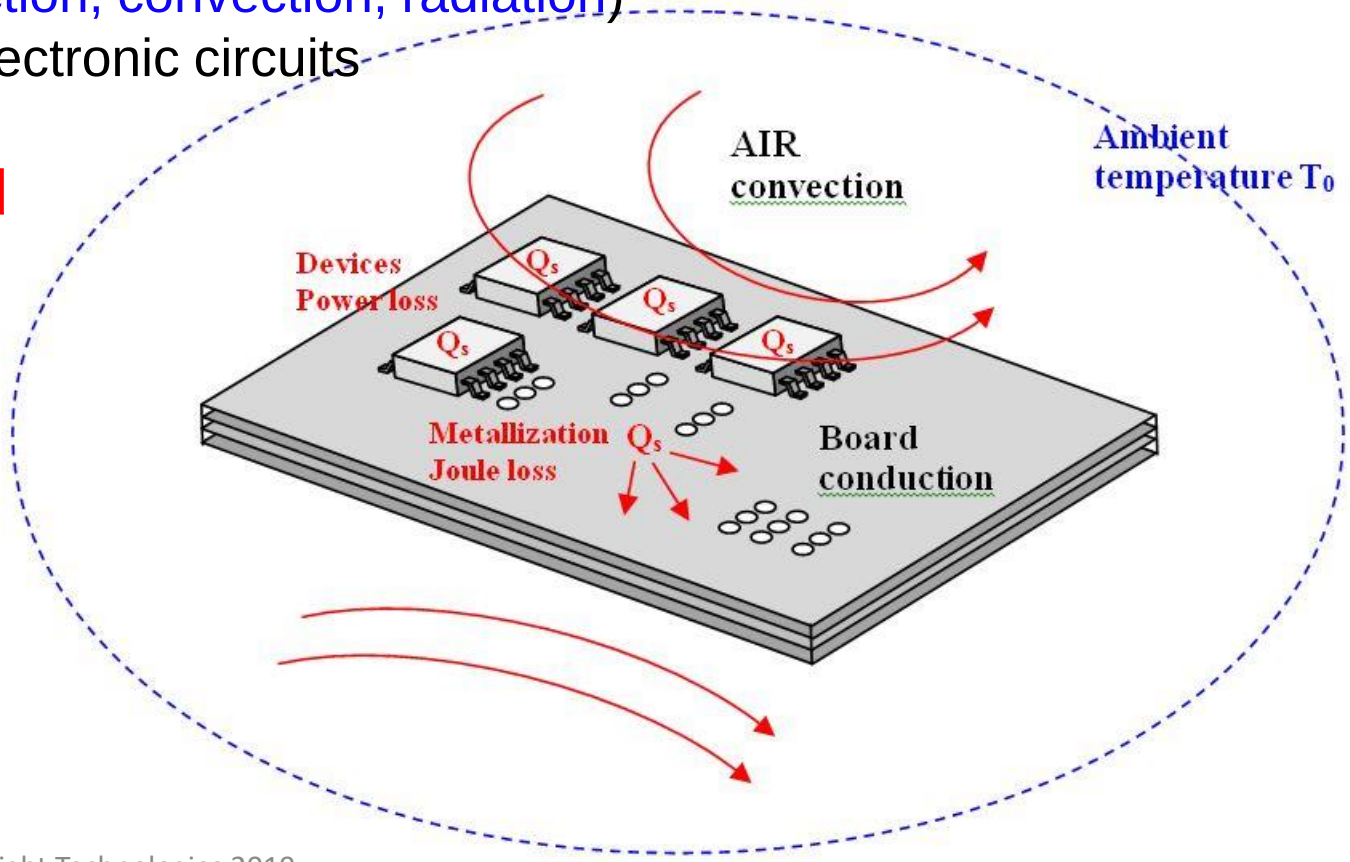
DC Electro - Thermal Design Challenge

WATCH OUT FOR HIGH CURRENT DENSITIES IN THE GROUND RETURN PATH

- Electronic devices produce **HEAT**
- Joule losses in metallization produce **HEAT**
- Heat is transferred to the ambient (conduction, convection, radiation)
- Heat causes a **Temperature rise** in the electronic circuits

Thermal validation is needed to avoid

- Component overheating
- Thermal stress
- Electronic malfunctioning



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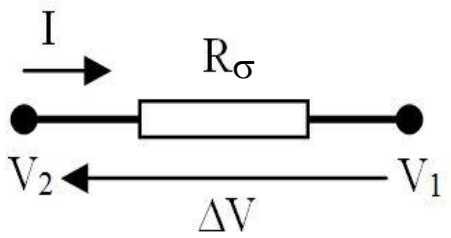
#1 – Thermal Run Away

WATCH OUT FOR CURRENT CONSTRICTION POINTS

Coupled Electro-Thermal Equations

Electric resistance R_σ [V/A]

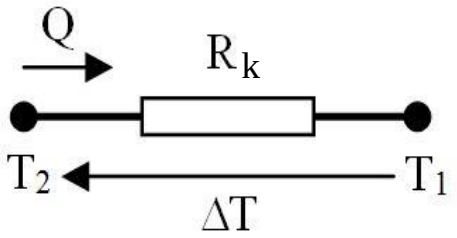
$$V_2 - V_1 = R_\sigma \cdot I$$



…Where electric resistance R_σ changes with temperature T

Thermal resistance R_k [K/W]

$$T_2 - T_1 = R_k \cdot Q$$



…Where the injected heat flux Q changes with voltage V

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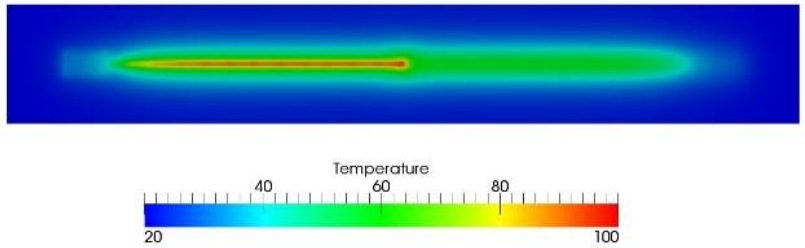
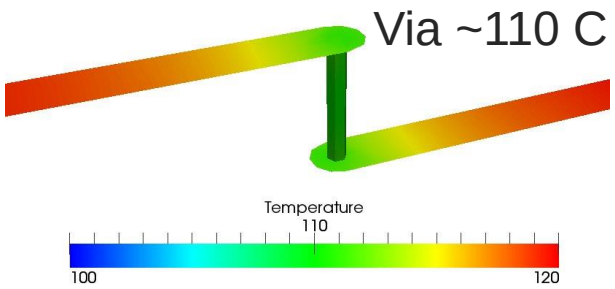
Thermal is Non-Intuitive: IPC Got it Wrong

HIGH CURRENT DENSITY IN A SINGLE POINT GROUND RETURN CONNECTION

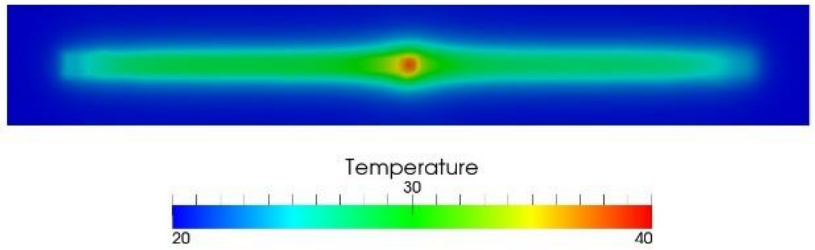
27 mil trace ≅ Via Cross Section

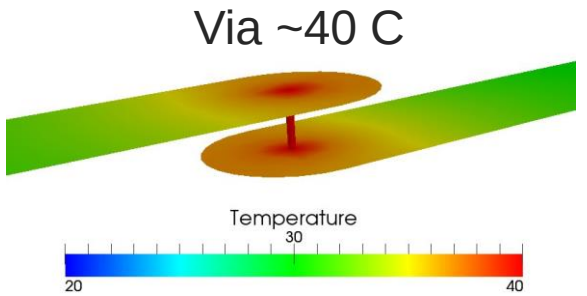




Equivalent cross section via has more conductive cooling than the trace.

200 mil trace >> Via Cross Section





ADS PIPro Simulation

Wide trace provides conductive cooling for the via.

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ADS PIPro EM Simulation of the PCB PDN

1) IMPORT THE PCB

- Select VRM, Sink, Nets, Components
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2) OPTIMIZE DECOUPLING

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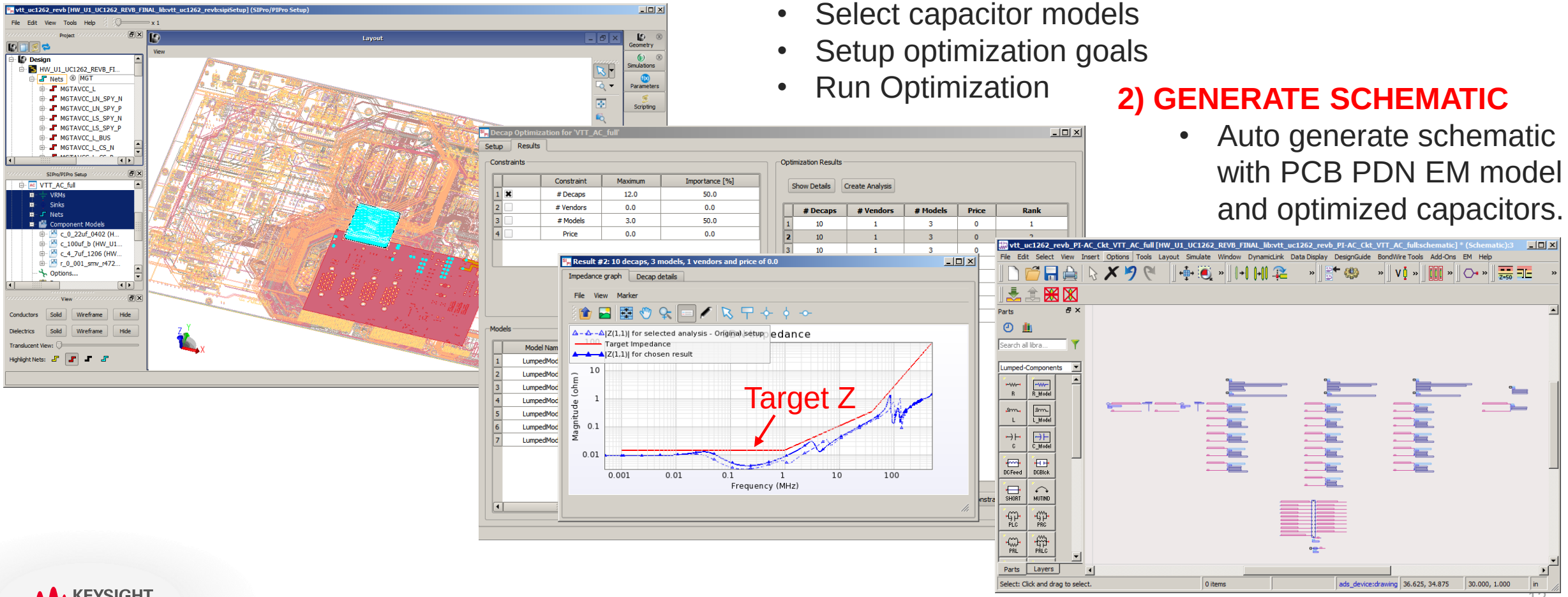

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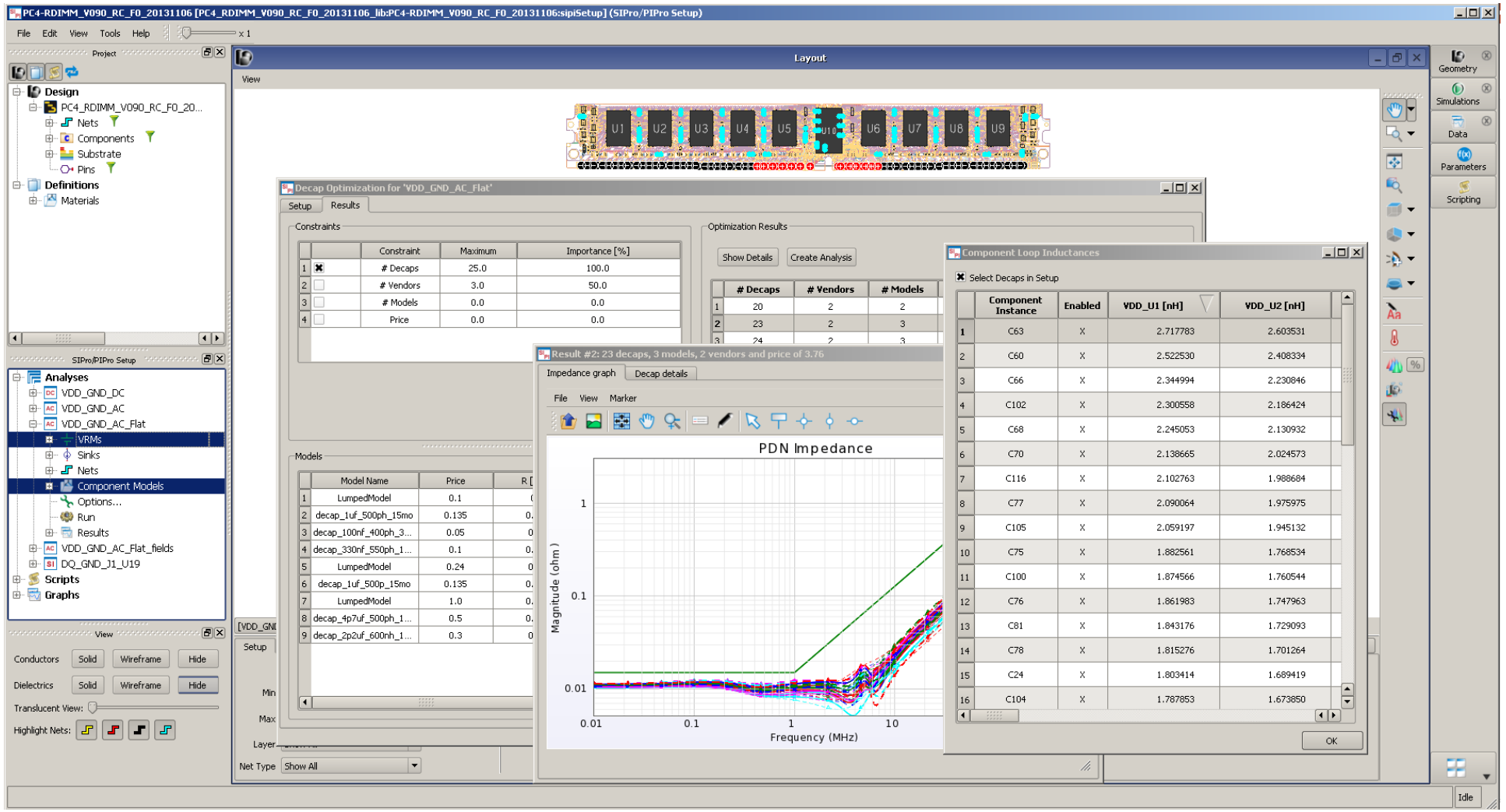
DDR4 DIMM Example – Ships with ADS

DECOUPLING CAPACITOR OPTIMIZATION FOR FLAT Z



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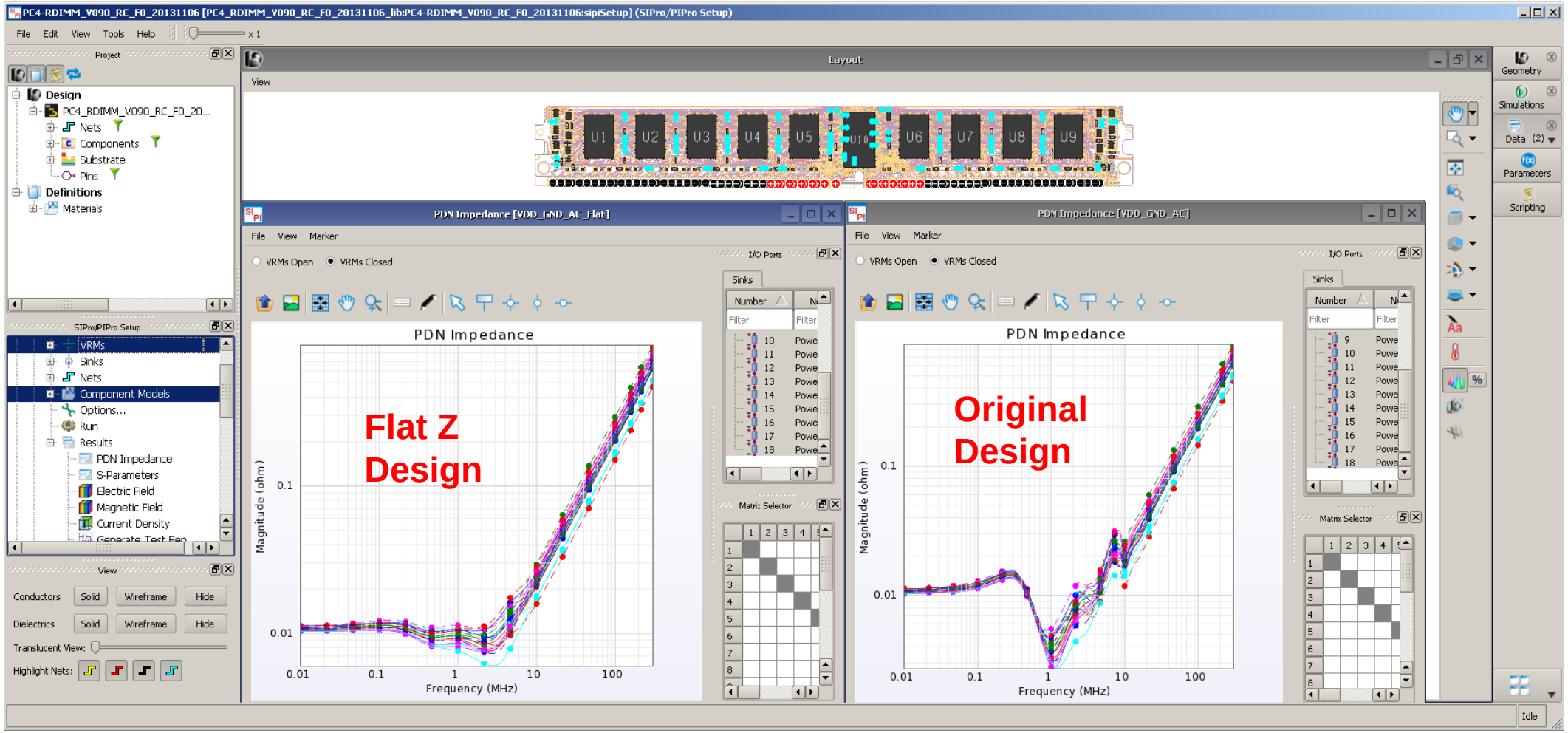
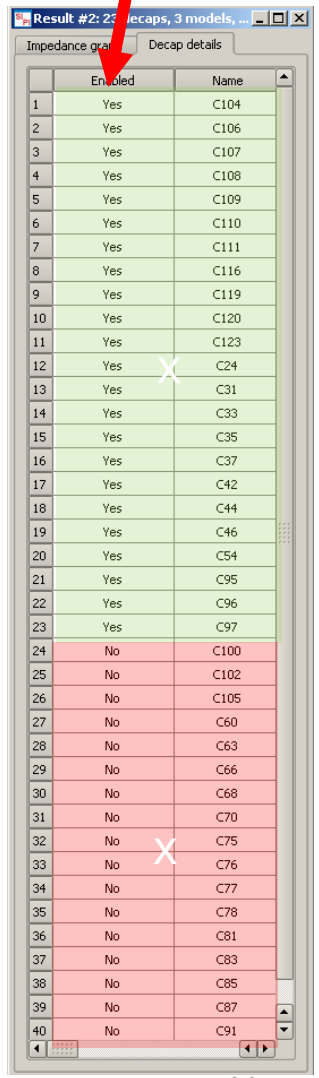
PCB Decoupling Capacitor Optimization

FLAT IMPEDANCE VS FREQUENCY FOR BEST PERFORMANCE

Flat Z with 40% fewer capacitors





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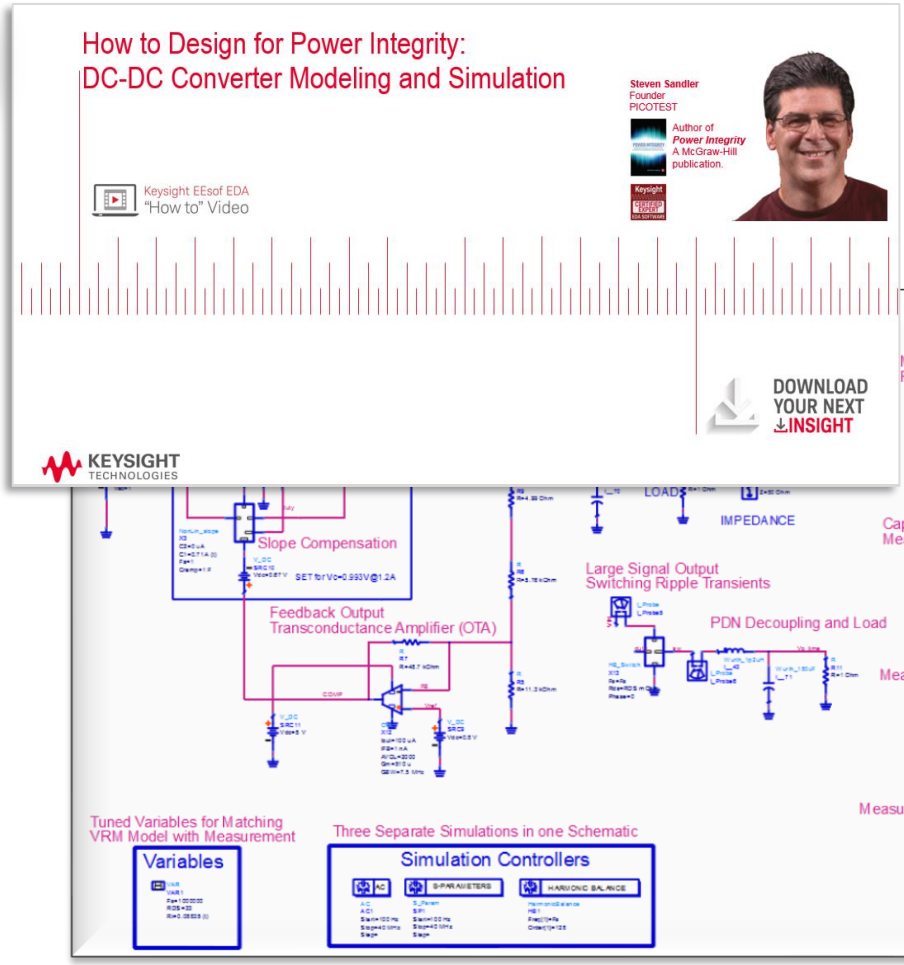
Voltage Regulator State Spaced Averaged Models

Measurement Based VRM Modeling

Steve Sandler – PICOTEST

PICOTEST

4



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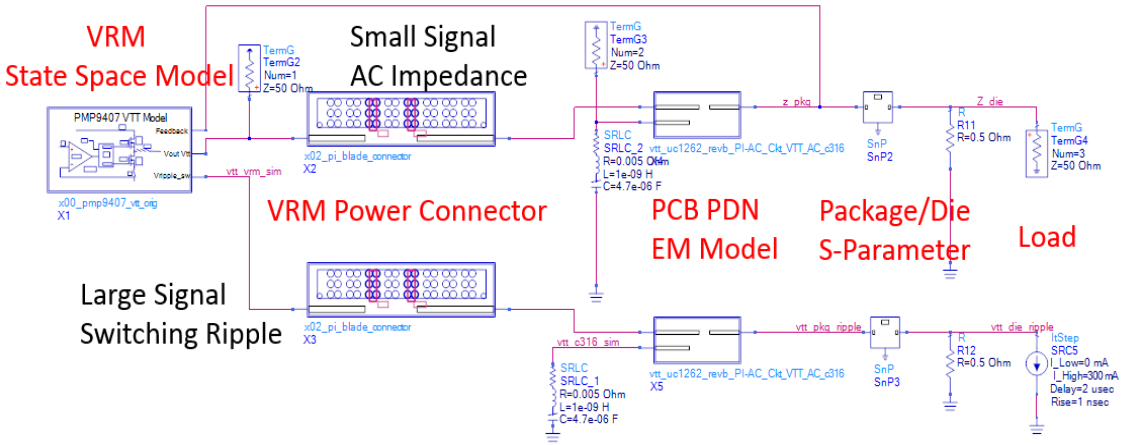
Modeling the Power Integrity Ecosystem

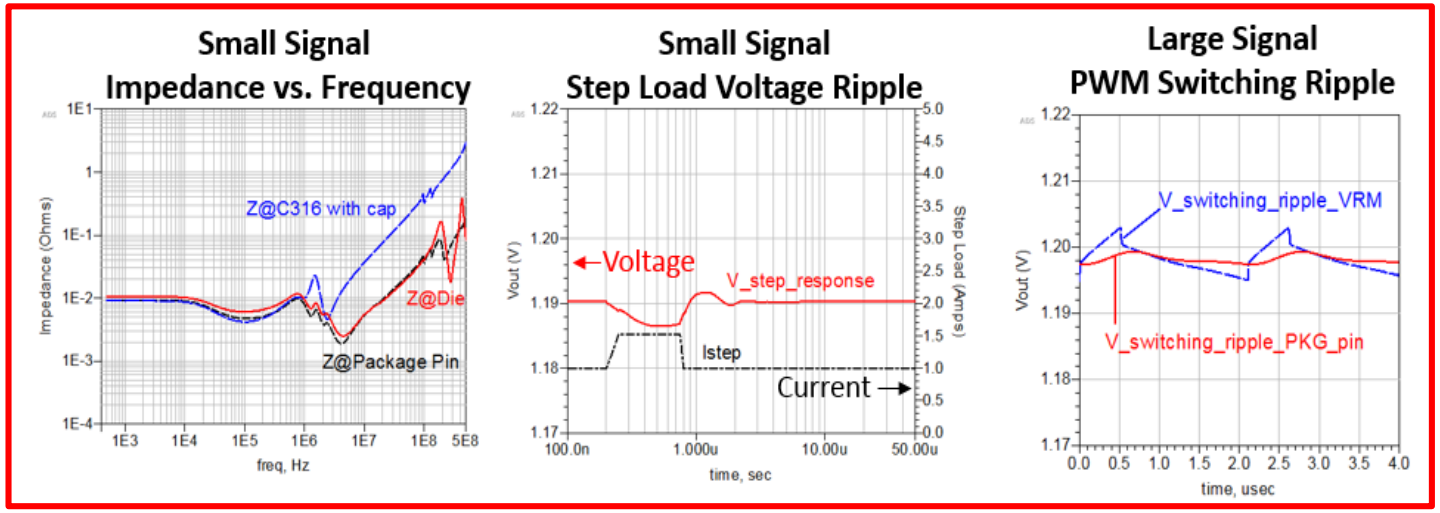
VRM + PDN + Load = PI Ecosystem

Three Separate Simulations in one Schematic

Simulation Controllers

AC	S-PARAMETERS	HARMONIC BALANCE
AC	S_Param	HarmonicBalance
AC1	SP1	HB1
Start=100 Hz	Start=100 Hz	Freq[1]=Fs
Stop=40 MHz	Stop=40 MHz	Order[1]=256
Step=	Step=	





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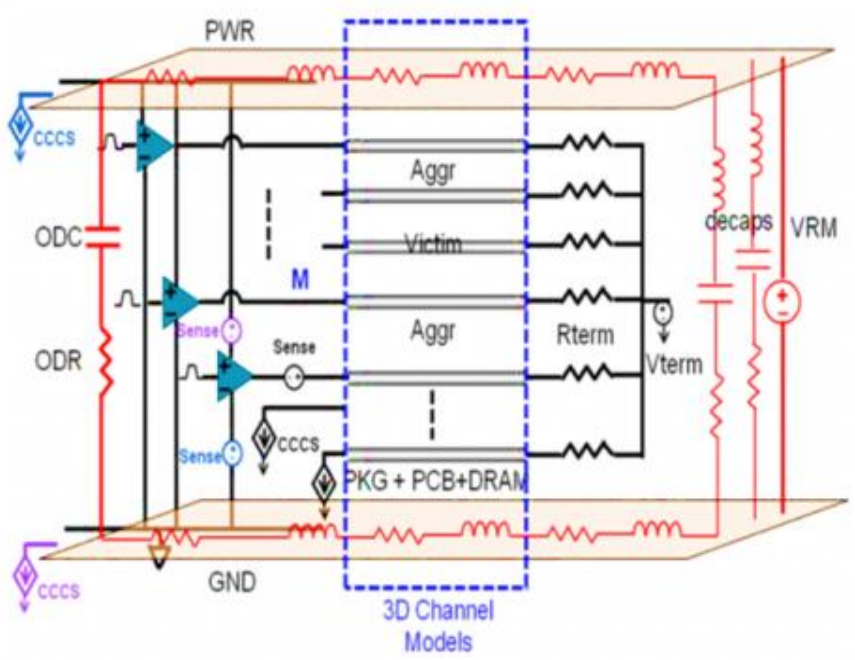
SI and PI Co-EM Simulation



Power and Signal Nets in the same EM simulation

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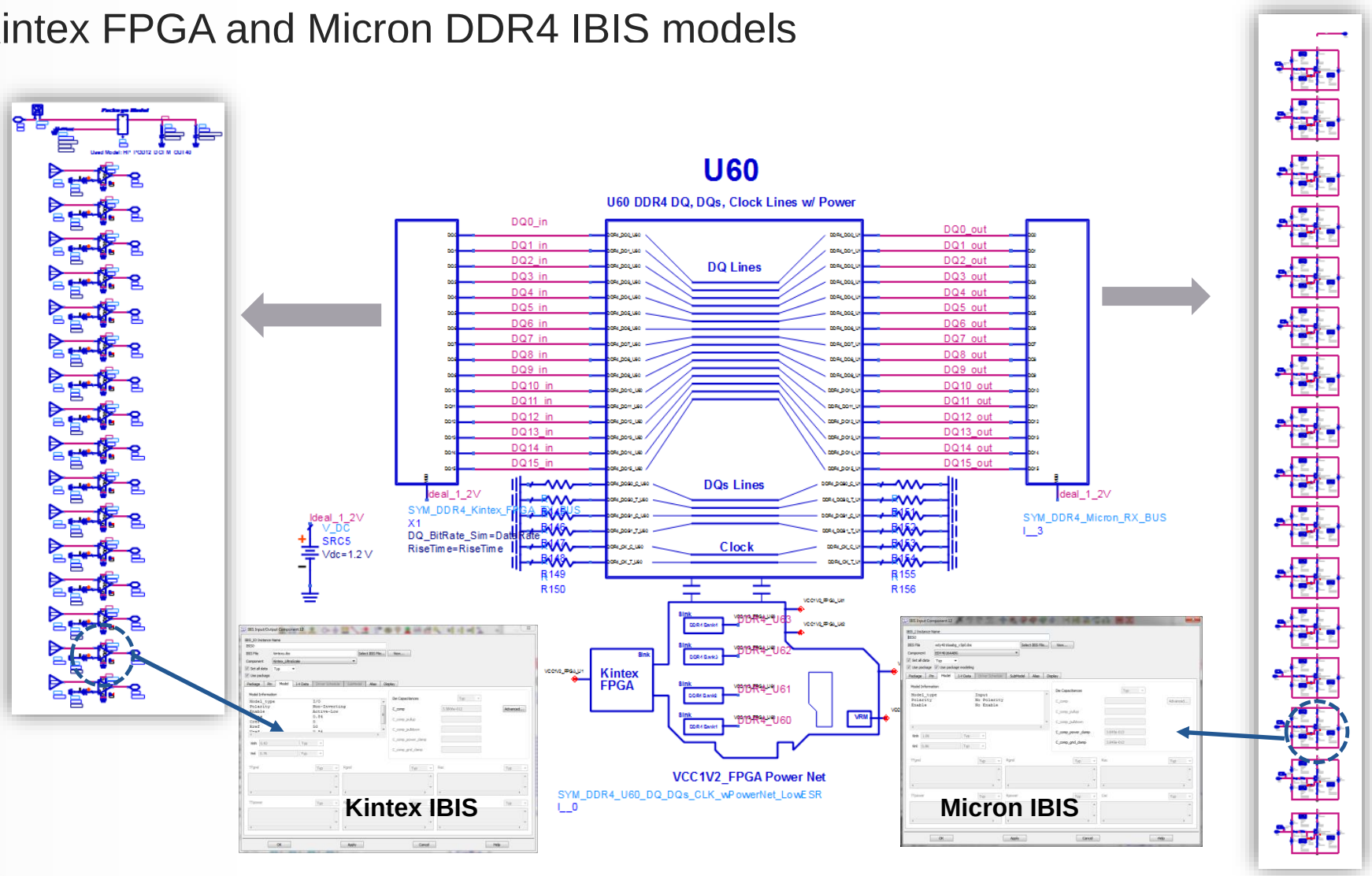
Vendor Specific IBIS Models to Improve Accuracy

- Xilinx Kintex FPGA and Micron DDR4 IBIS models



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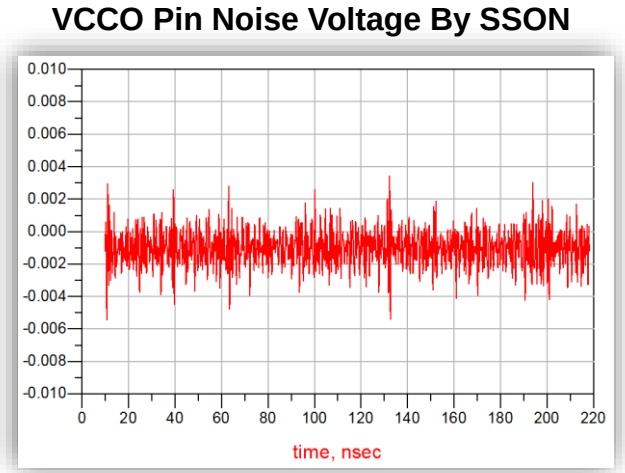
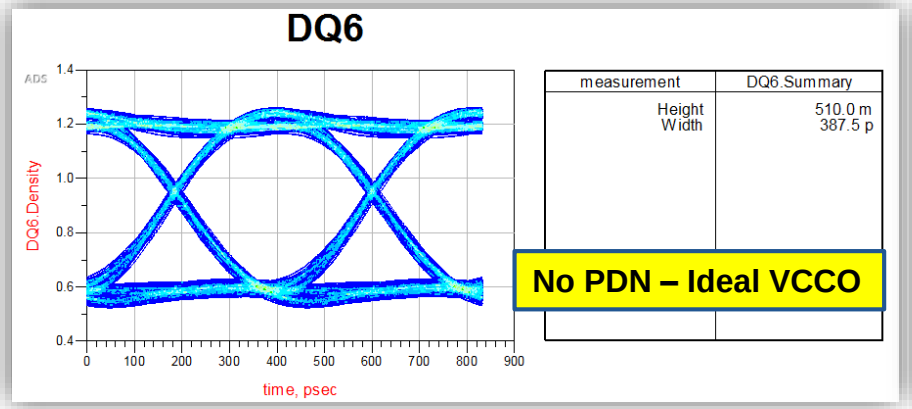
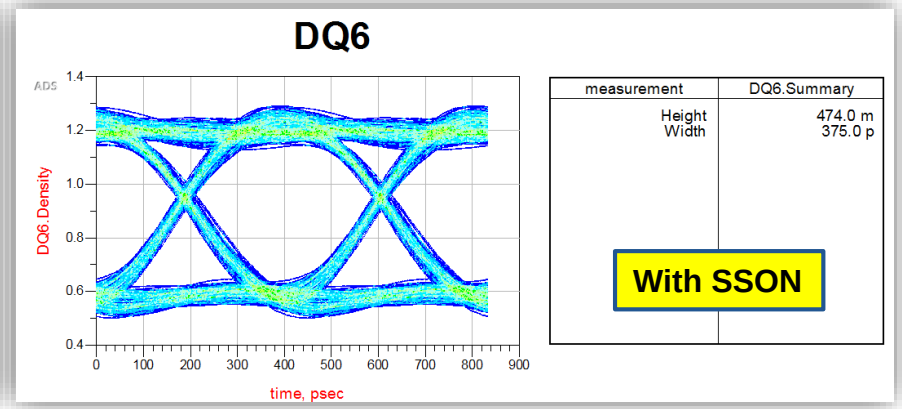
Simultaneous Switching Noise (SSN)

- Shows SSN noise voltage at VCCO pin, which is similar to the measured data
  - Both eye width and height are reduced by SSO noise, as expected.
  - 387.5p → 375p, **510mV → 474mV** respectively







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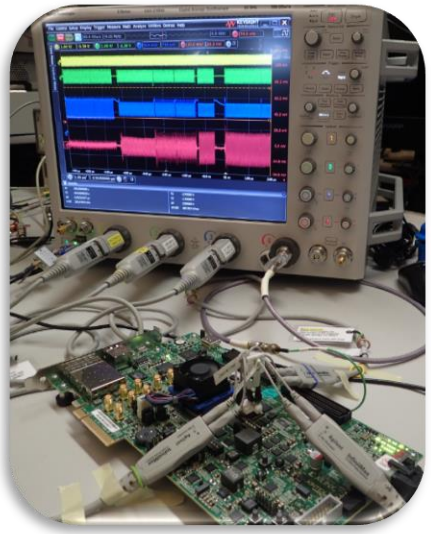
SSO Noise Measured Example

- Simultaneous Switching Output Noise (SSON)



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Summary

- How parallel resonances lead to significant voltage ringing on the power rail
- How to calculate decoupling C for a flat target Z
- The impact of Capacitor PCB mounting parasitics
- ADS with PIPro DeCap Optimization for reduced part count and full PI Ecosystem simulation

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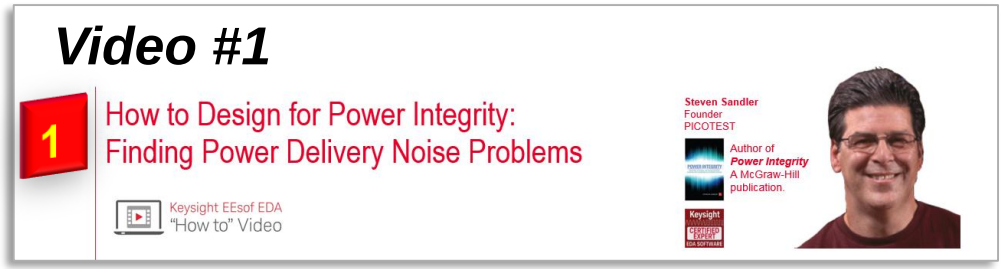
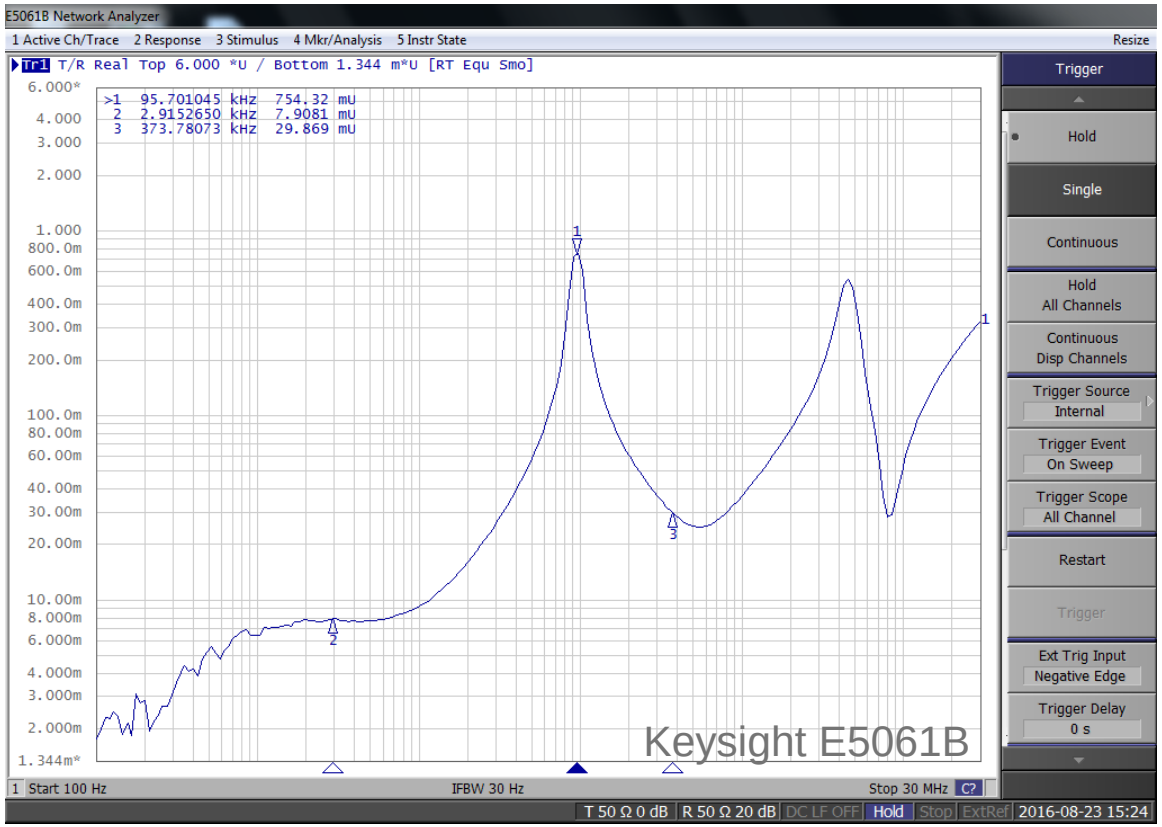
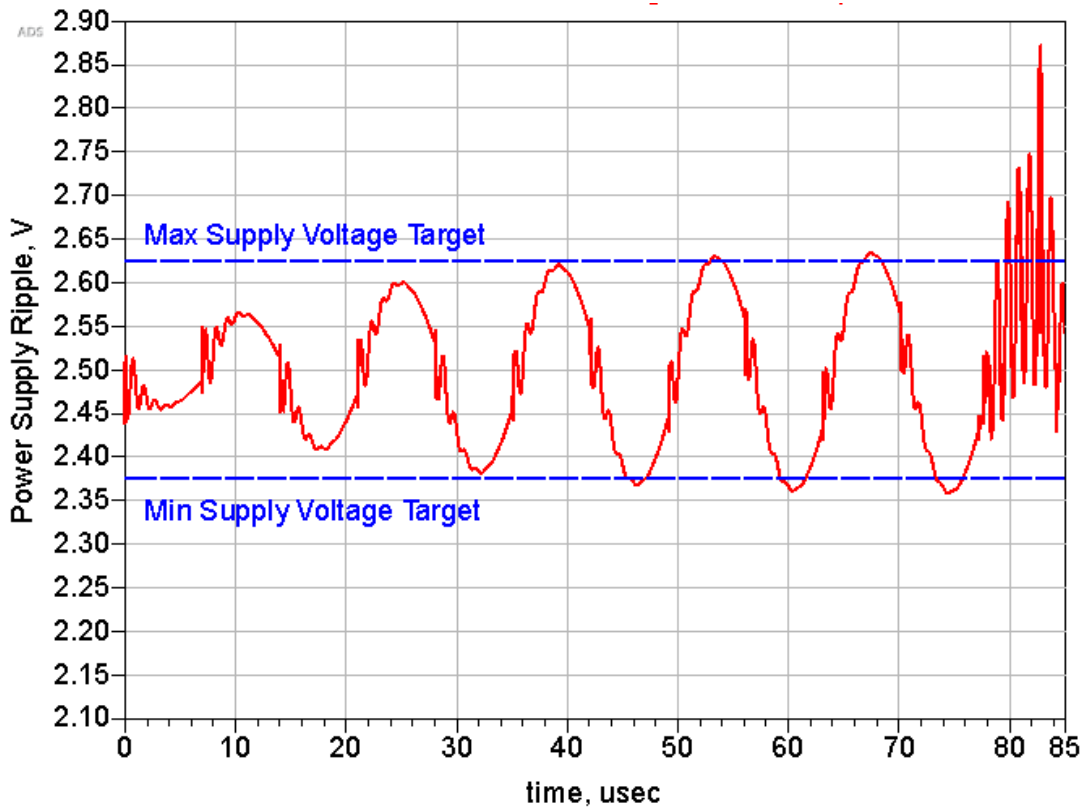
PDN Disasters Do Exist – Always Look at the PDN Impedance!



Frequency Domain Shows Resonances



Time Domain Excitation – Rogue Wave Failure



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Big Screen Simulation and Measurement Demo

- E5061B Network Analyzer Impedance Parallel Capacitors
- ADS PIPro Demo of DeCap Optimization

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Hands-On Lab: 190219_ADS_PI_Lab4_DeCap_Optimize_v2_wrk.7zads

Basics – Instructor Led Demo

Flat Z Capacitor Selection

Explore –

Parallel Capacitor SPICE vs. EM Models

Advanced –

PIPro Decoupling Capacitor Optimization

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