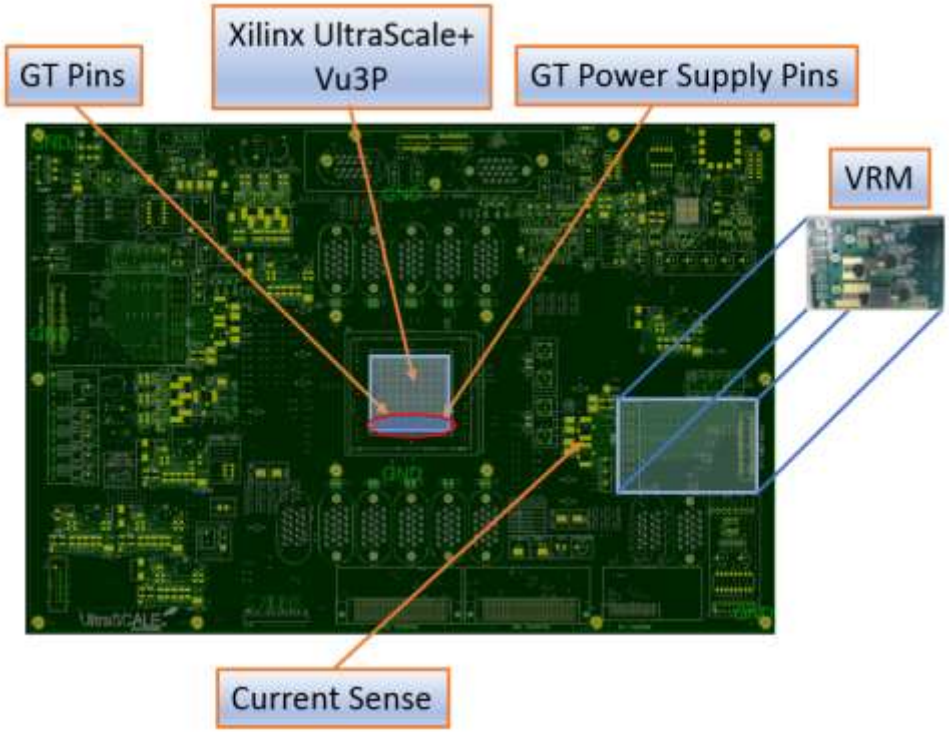
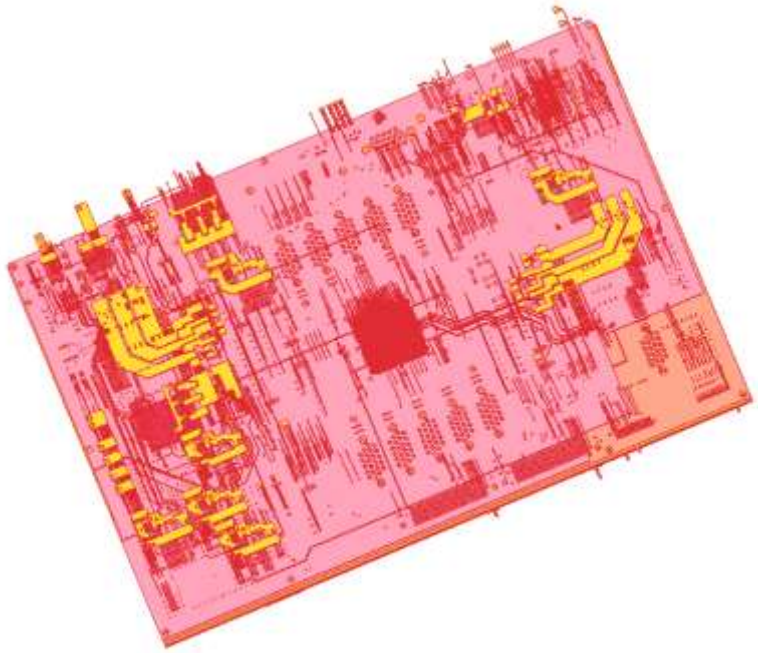
# Decoupling Capacitor Optimization for Power Integrity


| Keysight Technologies | 2018.03.29 |
| --- | --- |
| Heidi Barnes | |

## 22-Layer High Density FPGA Printed Circuit Board




## Complex Integration of Multiple Power Distribution Networks



*Is the decoupling capacitor reference design optimized for my application?*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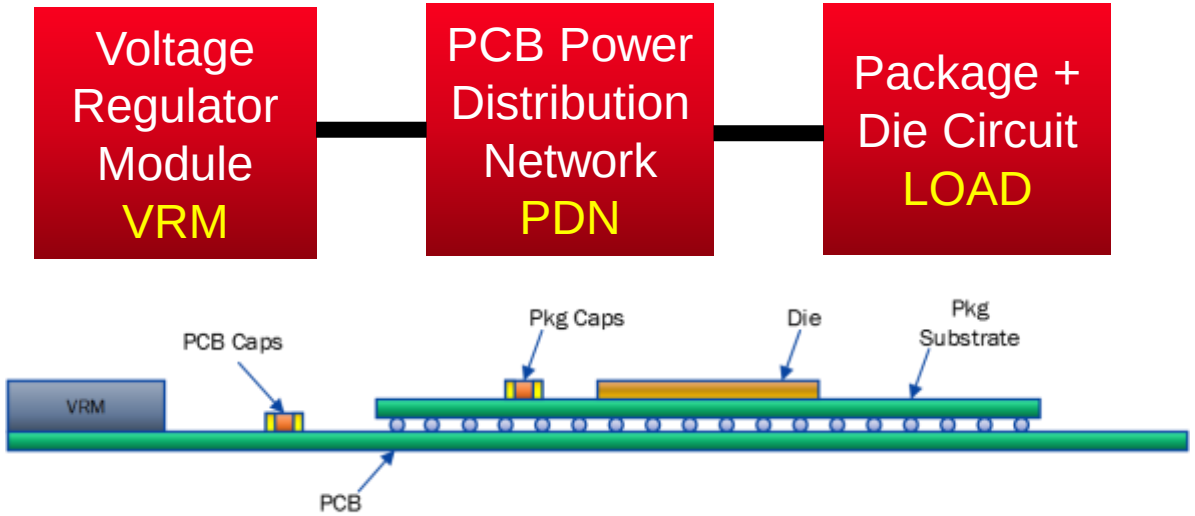
# The Supply of Power from the Decoupling Capacitors

POWER INTEGRITY




**Target Impedance Calculation**

$$Z_{\text{Target}} = \frac{\Delta V_{\text{Max Ripple}}}{\Delta I_{\text{Max Transient Load}}}$$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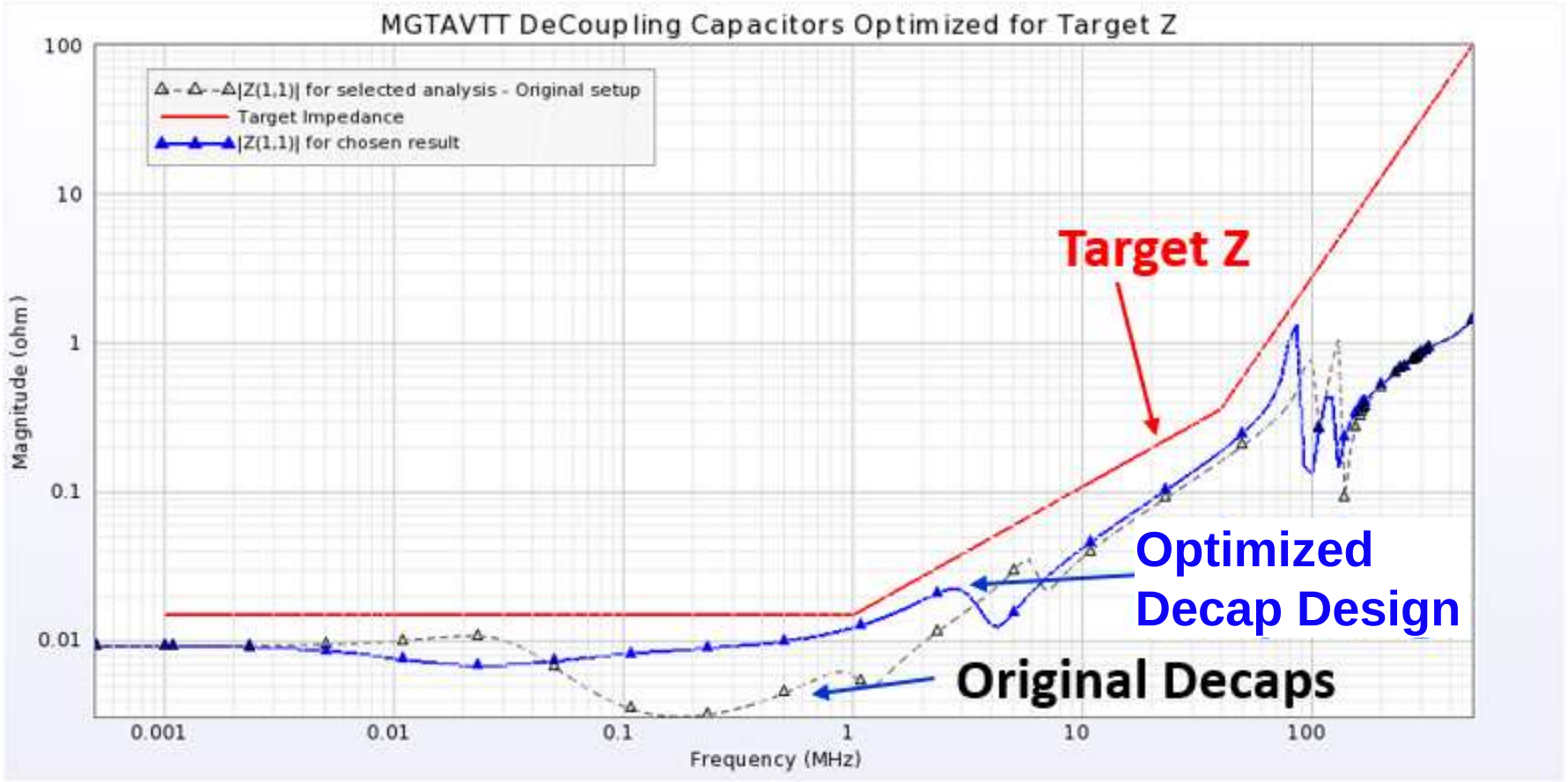
# Optimize Decoupling to Maximize Performance/Cost Ratio

## TARGET Z DECOUPLING CAPACITOR OPTIMIZATION




**40% Reduction in Part Count**

Capacitors

| | | |
|---|---|---|
| Yes | C190 | 330 uF |
| Yes | C215 | 330 uF |
| Yes | C216 | 330 uF |
| Yes | C218 | 330 uF |
| Yes | C303 | 220 nF |
| Yes | C305 | 220 nF |
| Yes | C750 | 220 nF |
| Yes | C753 | 220 nF |
| Yes | C757 | 220 nF |
| No | C217 | 100 uF |
| No | C225 | 100 uF |
| No | C315 | 4.7 uF |
| No | C316 | 4.7 uF |
| No | C778 | 4.7 uF |
| No | C779 | 4.7 uF |
| No | C780 | 4.7 uF |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# 3 Step Decoupling Capacitor Optimization

## DESIGN METHODOLOGY FOR DECAP OPTIMIZATION

1. Calculate 1st order approximations using simple resistor, inductor, capacitor R-L-C models

2. Use Target Z to optimize the decoupling capacitor selection using high fidelity EM models (ADS PIPro)

3. Validate with full Power Integrity Eco-System simulation in ADS


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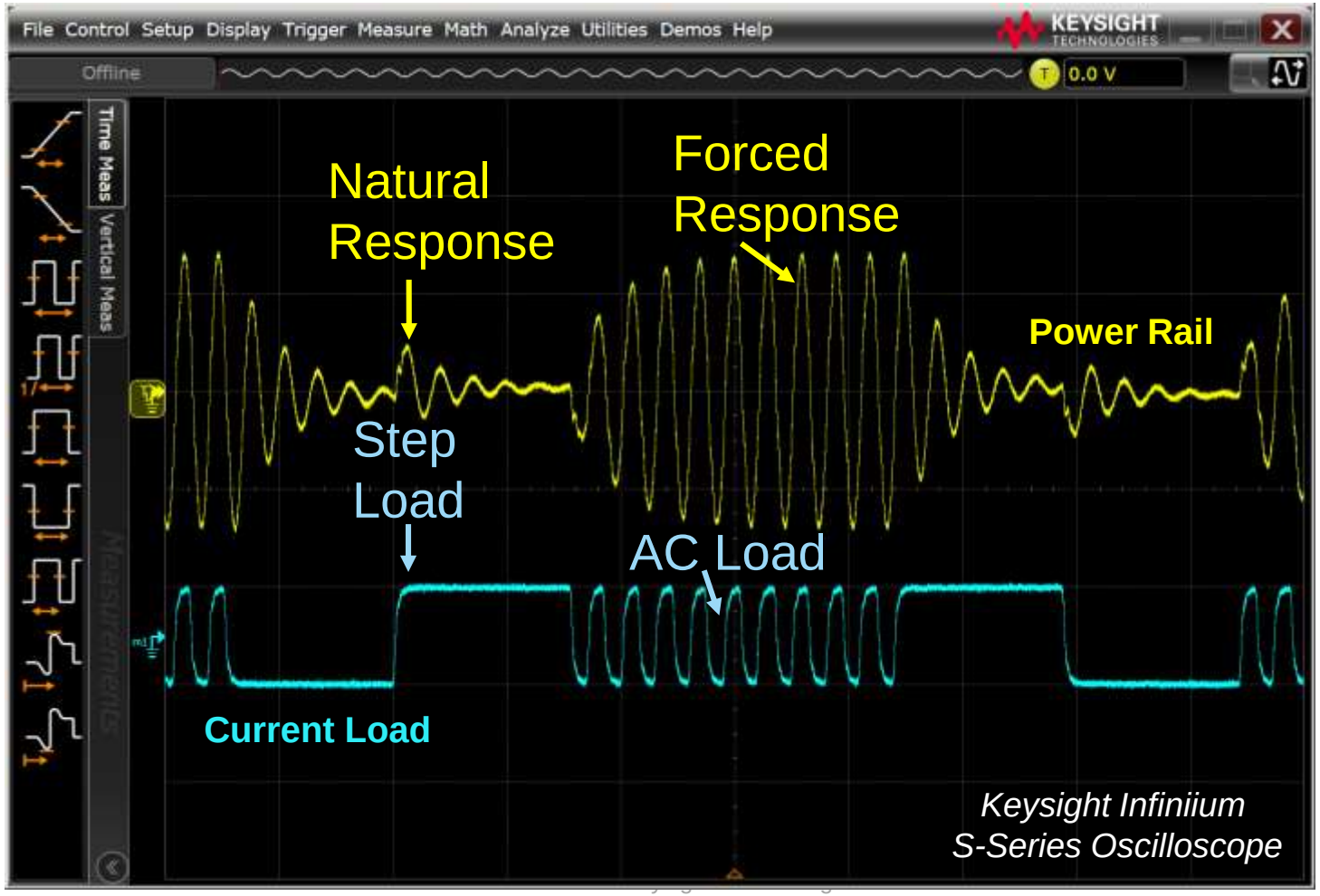
# Decoupling Capacitors Can Reduce Voltage Ripple

## TIME DOMAIN NATURAL AND FORCED BEHAVIOR

### Power Supply Rail Measurements




**Volts**

**Amps**

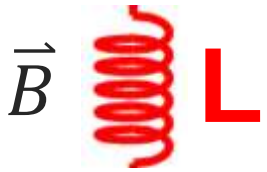
# Where does the ringing come from?

## ENERGY SWINGS BETWEEN THE L AND THE C

***Energy stored in the Magnetic Field***

$$V(t) = L\frac{di}{dt}$$

$$Z = j\omega L$$

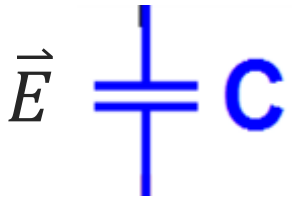



***Phase V Leads I***

***Energy stored in the Electric Field***

$$I = \int C\frac{dV}{dt}$$

$$Z = \frac{-1}{j\omega C}$$




***Phase V Lags I***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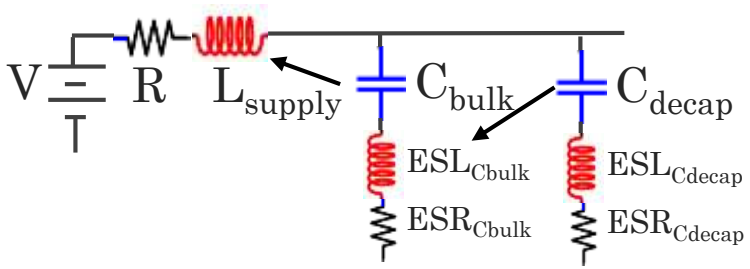
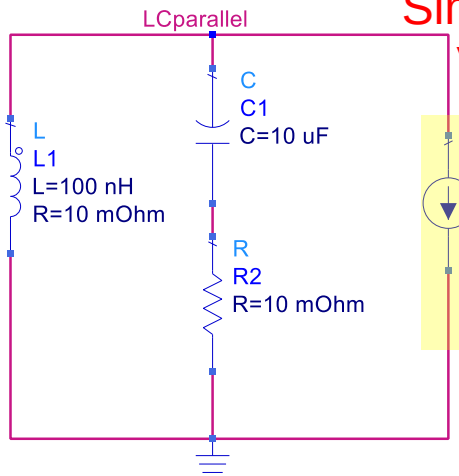
# L C Parallel Resonance Problem in the PDN Design

## IMPEDANCE PEAKS CAUSE HIGHER VOLTAGE RIPPLE

Parallel L-C in the PDN




Simulation Trick

V=Z*1=Z

1 Amp

AC Sweep

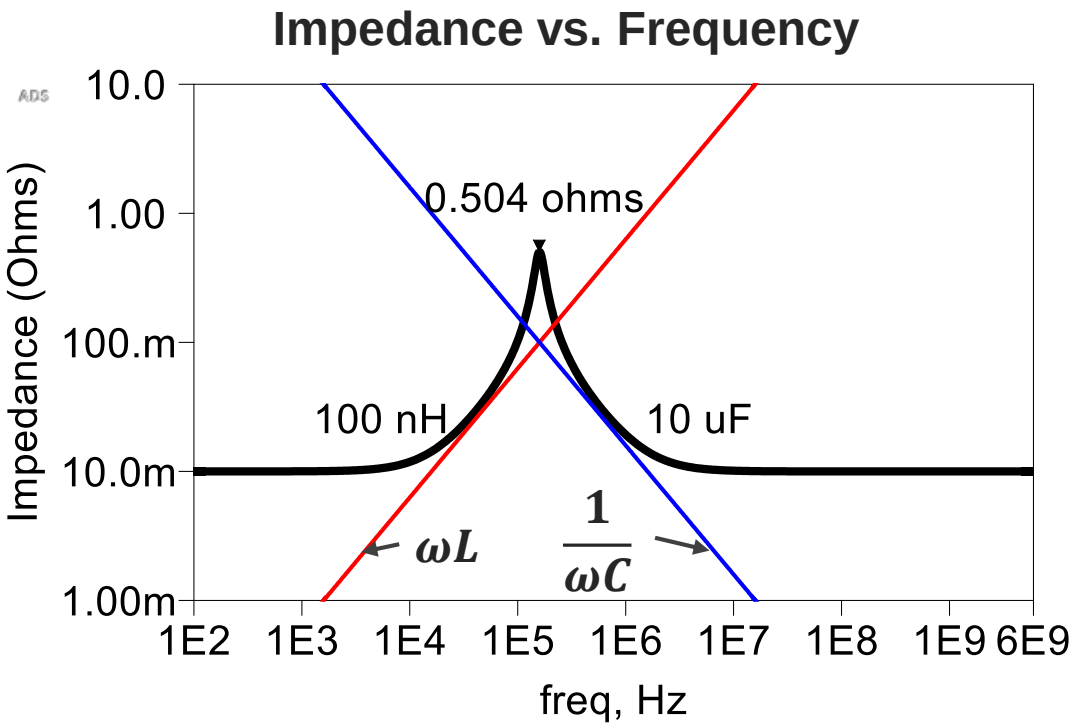
$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

$$\Delta V = \Delta I \cdot Z_{peak}$$

$$\boldsymbol{Z_{peak} = Z_0 \cdot Q}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$Q = \frac{Z_0}{R_{total}}$$




Zpeak=500 mOhms

Zo=100 mOhms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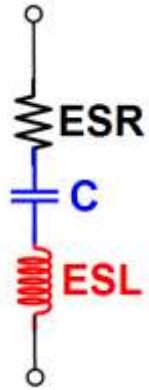
# L C Series Resonance Challenge with Capacitors

## A CAPACITOR IS AN INDUCTOR AT HIGH FREQUENCIES

### Capacitor Model



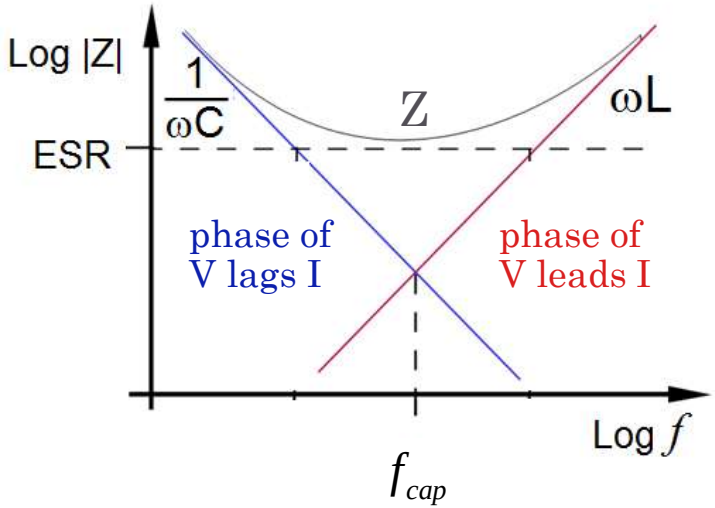

### Impedance Equation

$$Z = ESR_{cap} + \left( j\omega \times ESL_{cap} - j\frac{1}{\omega \times C} \right)$$

$$f_{cap} = \frac{1}{2\pi\sqrt{ESL_{cap} \times C}}$$

Voltage and current are in phase at $f_{cap}$

### Series RLC Impedance vs. Frequency





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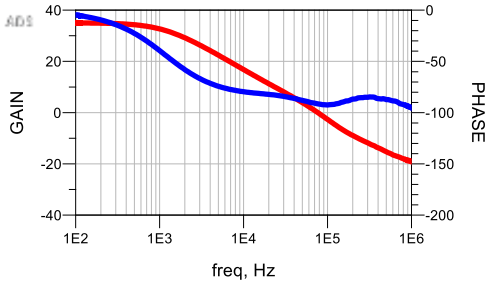
# Bandwidth of the Power Supply Control Loop $f_{supply}$

## IMPEDANCE PLOTS INSTEAD OF BODE PLOTS

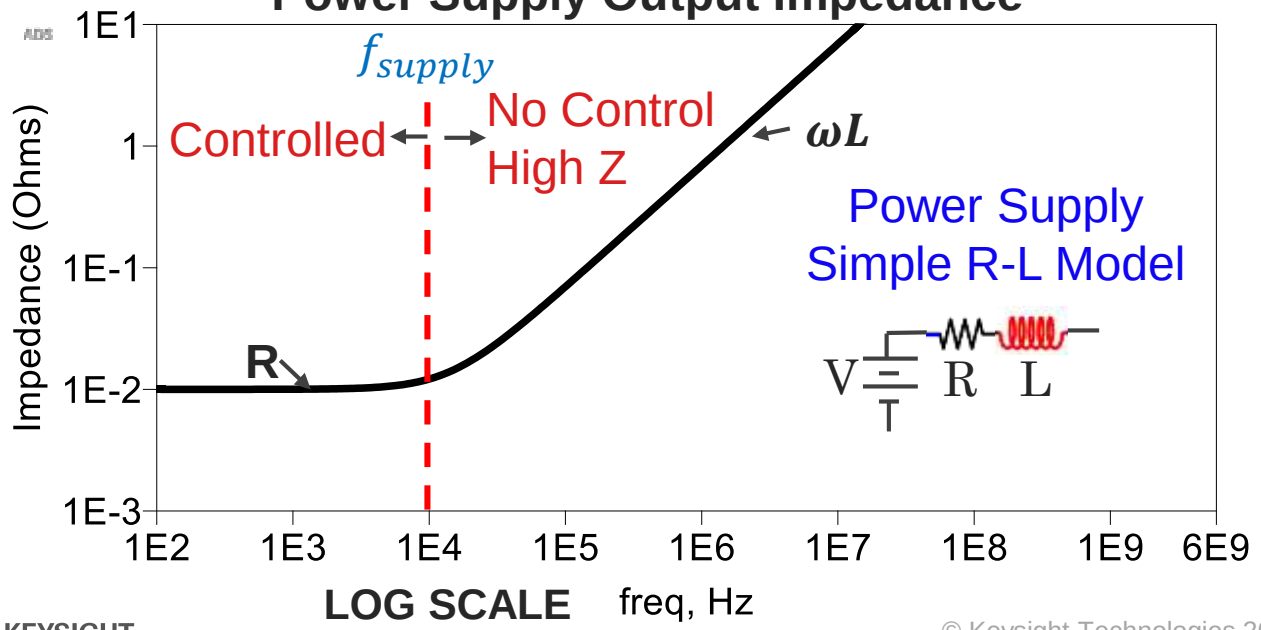
**PROBLEM**
The Load can make the Power Supply Control Loop go unstable

**1st Order SOLUTION**
Design for Flat Impedance at the output to keep V and I in phase and the feedback stable.

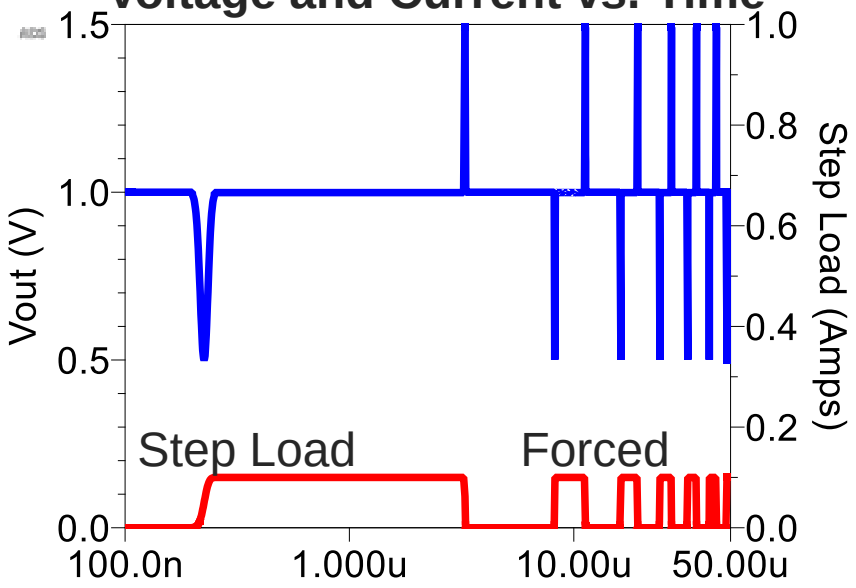
Bode Gain Phase Stability




**Frequency Domain**
**Power Supply Output Impedance**




**Time Domain**
**Voltage and Current vs. Time**

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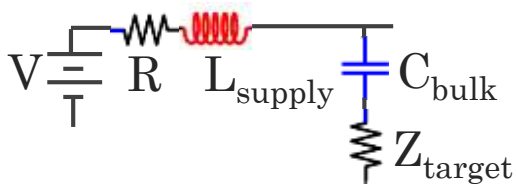
# Transition from Power Supply to Bulk Capacitor

## DESIGNING FOR FLAT IMPEDANCE

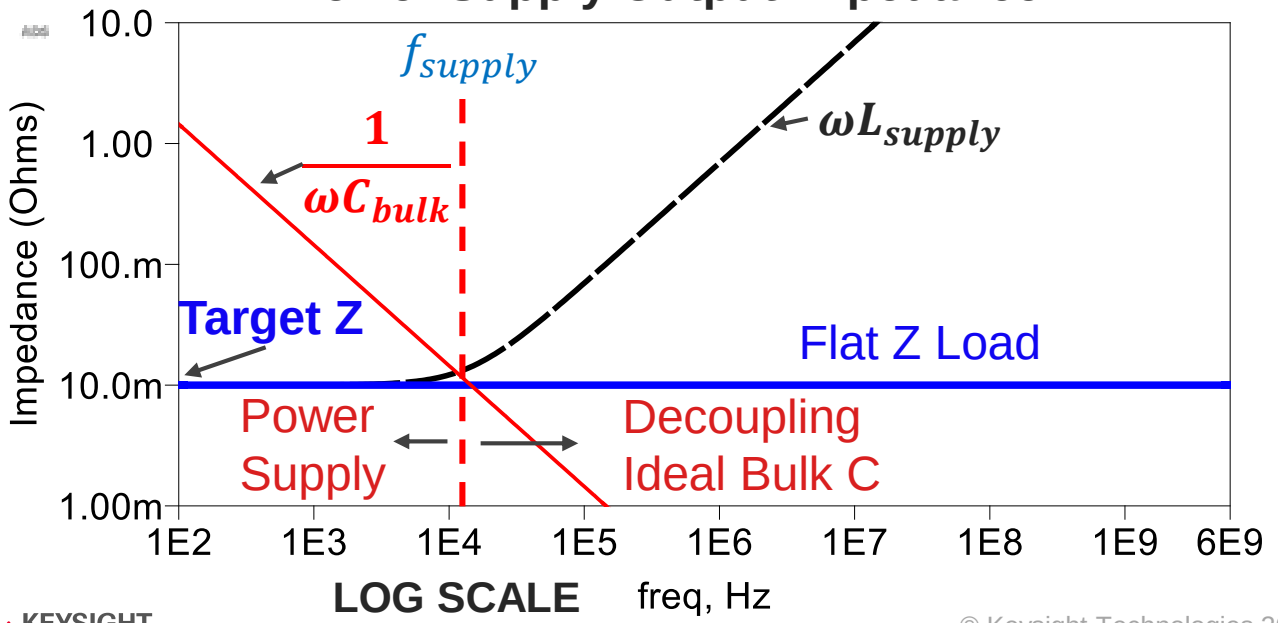



**PROBLEM**
Find the decoupling capacitor that will maintain a Flat Z Load for the Power Supply

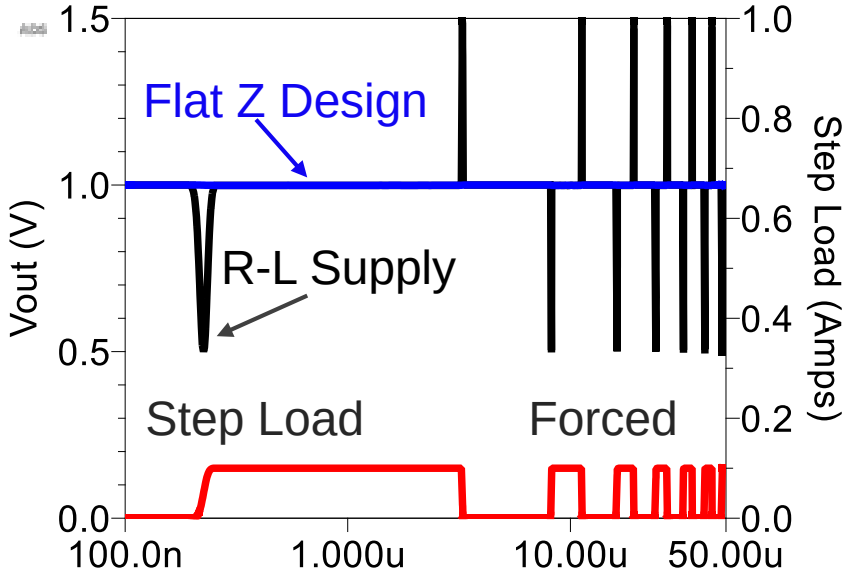
**1st Order SOLUTION**
Add Bulk Capacitor to maintain flat impedance

$$C_{bulk} = \frac{L_{supply}}{Z^2_{Target}}$$

**Frequency Domain**
**Power Supply Output Impedance**




**Time Domain**
**Voltage and Current vs. Time**





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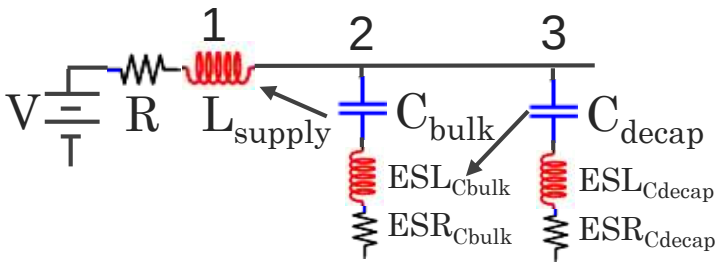
# Adding Decoupling Capacitors

**FLAT Z = MAXIMUM STABILITY AND MINIMUM RIPPLE**

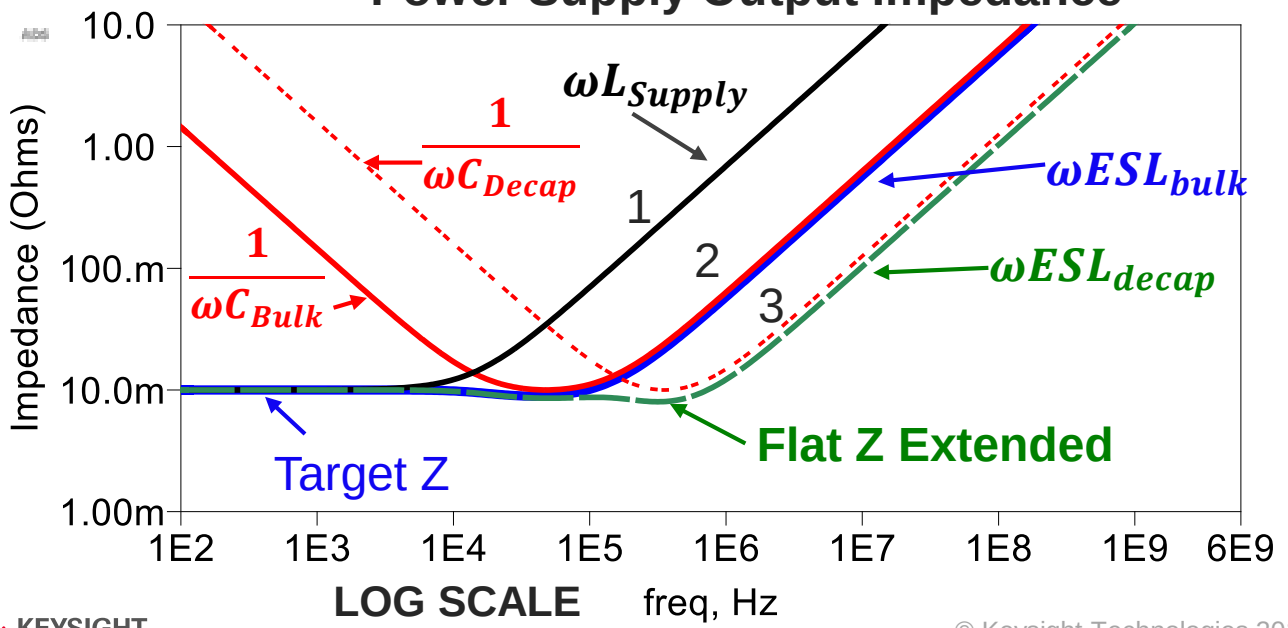
**PROBLEM**
Capacitor is not Ideal, it has series inductance!

**1st Order SOLUTION**
Add another decoupling capacitor to extend the Flat Z to a higher Frequency

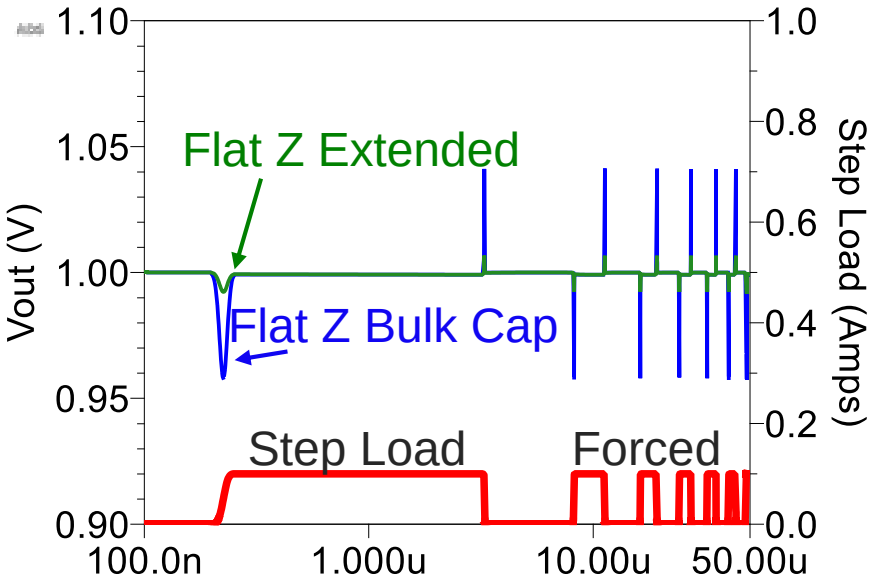



$$C_{decap} = \frac{ESL_{Cbulk}}{Z^2_{Target}}$$

**Frequency Domain**
**Power Supply Output Impedance**




**Time Domain**
**Voltage and Current vs. Time**




***LOG SCALE for time***

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# Maximum Decoupling Capacitor Frequency

## HOW FAST IS THE LOAD CHANGING?

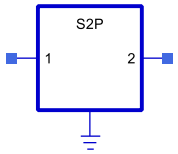
**PROBLEM**

Load $\frac{di}{dt}$ spectral content is difficult to measure and is not in the data sheets ☹.

**1st Order SOLUTION**

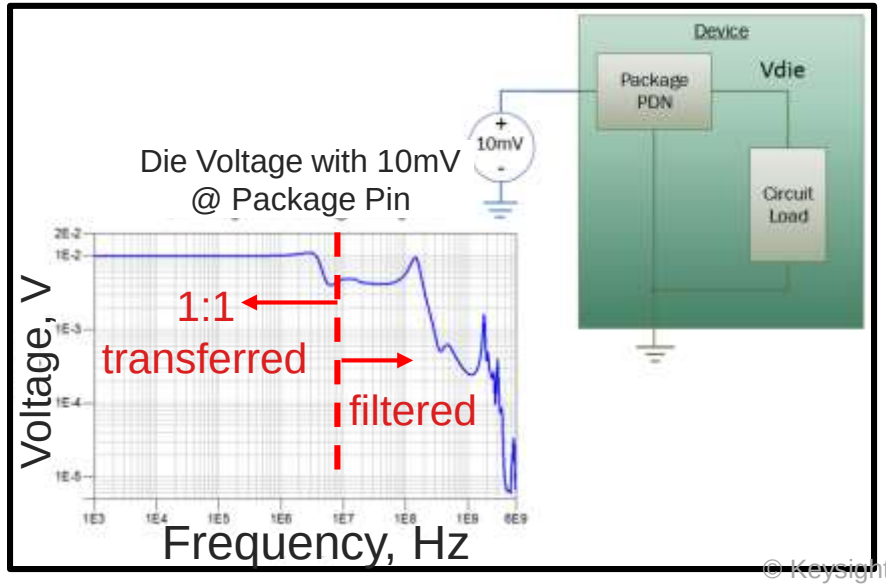
Let the IC vendor design the decoupling above the package C decoupling frequency.

**Package-Die S-Parameter Model Vendor Supplied**

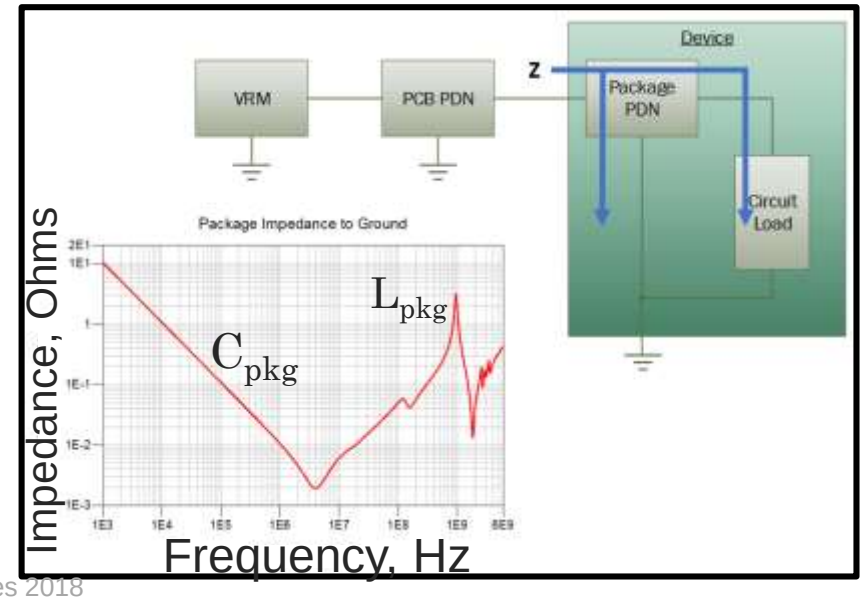



SnP
Package_Die_Model

$V_{ripple}$ Transfer from Package Pin to the Die




Impedance Simulated at the Package Pin

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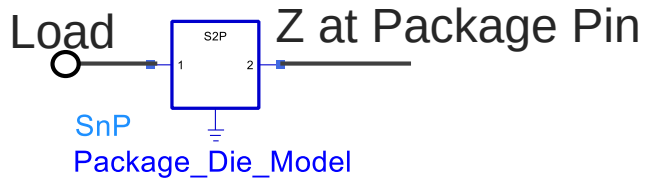
# Transition from PCB PDN Supply to Package/Die Capacitor

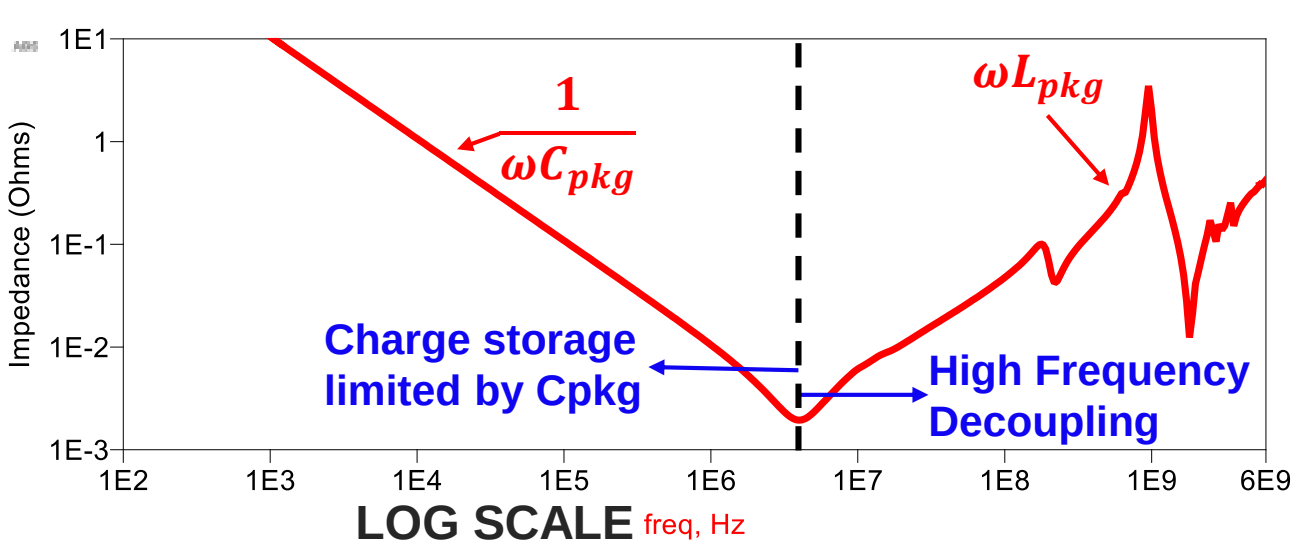
**PACKAGE/DIE PROVIDES MAX FREQUENCY DECOUPLING**

**PROBLEM**
Package/Die has limited high frequency charge storage.

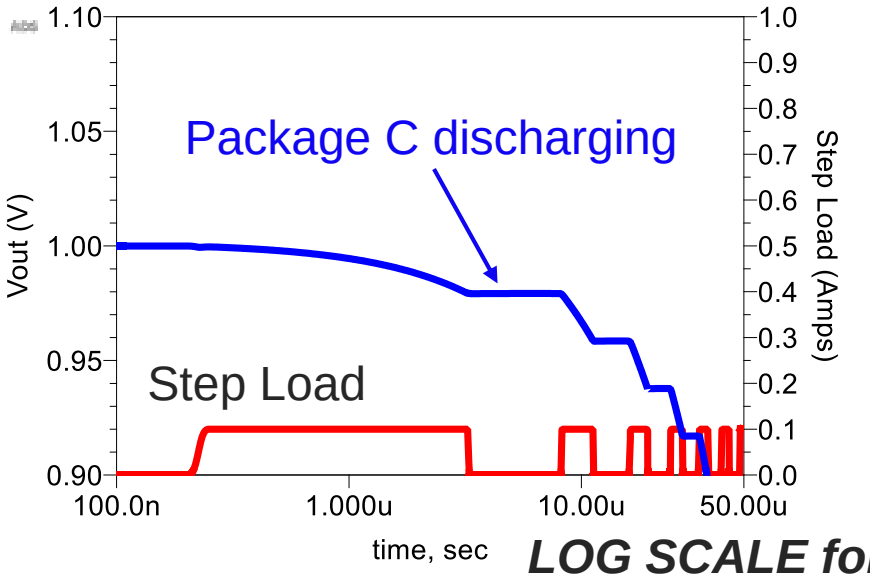
**1st Order SOLUTION**
Add a power supply and PCB PDN to cover the lower frequency decoupling.




**Frequency Domain**
**Impedance at the Package Pin (no PCB PDN)**




**Time Domain**
**Voltage and Current vs. Time**





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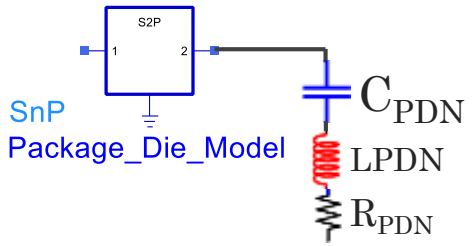
# Calculate Target Z Limit Line for High Frequencies

**TARGET Z AT HIGH FREQUENCIES = MAXIMUM $L_{PDN}$**

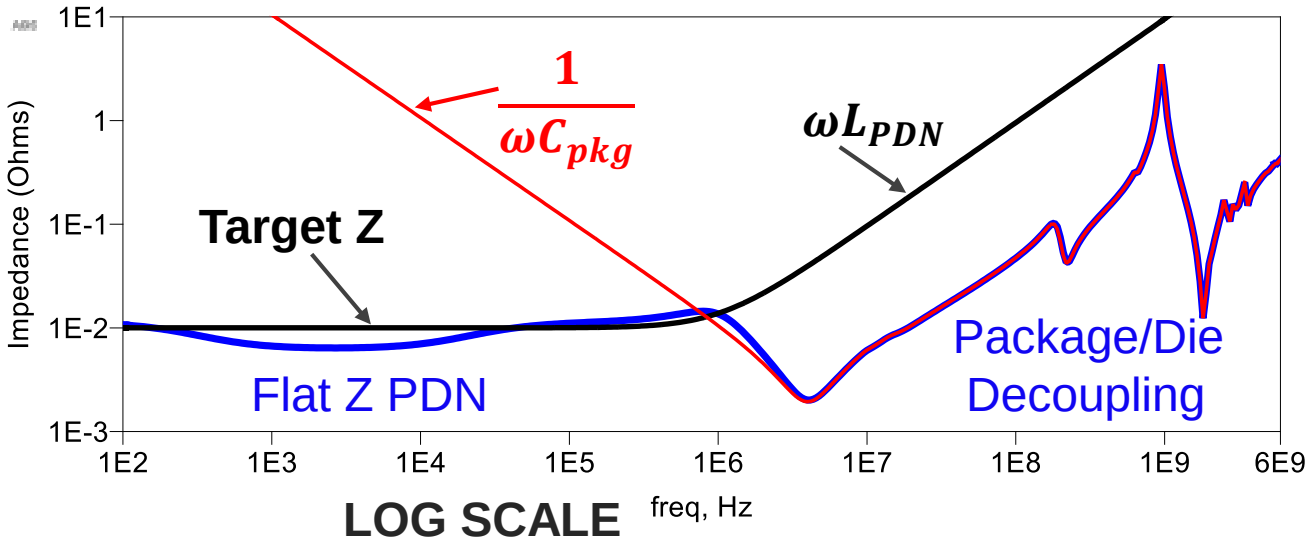
**PROBLEM**
How to calculate the increasing Target Z limit at high frequencies?

**1st Order SOLUTION**
Use the package/die C to calculate a Maximum $L_{PDN}$ that it can flatten to Target Z.



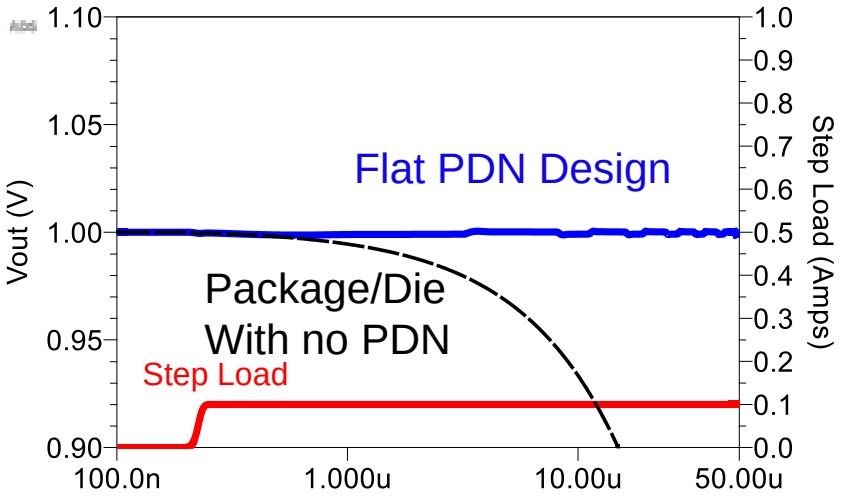

Maximum $L_{PDN} = \frac{C_{pkg}}{Z_{Target}^2}$

**Frequency Domain**
**Impedance at the Package Pin**




**LOG SCALE**

**Time Domain**
**Voltage and Current vs. Time**




***LOG SCALE for time***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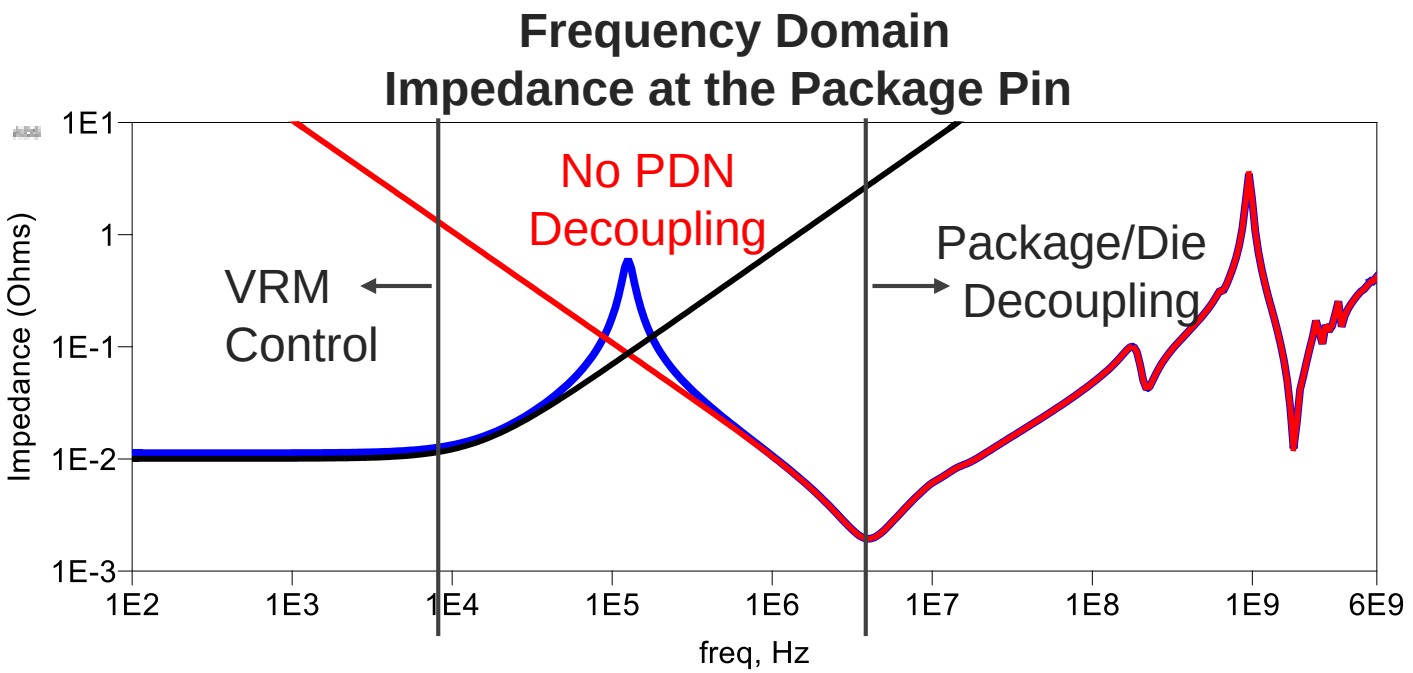
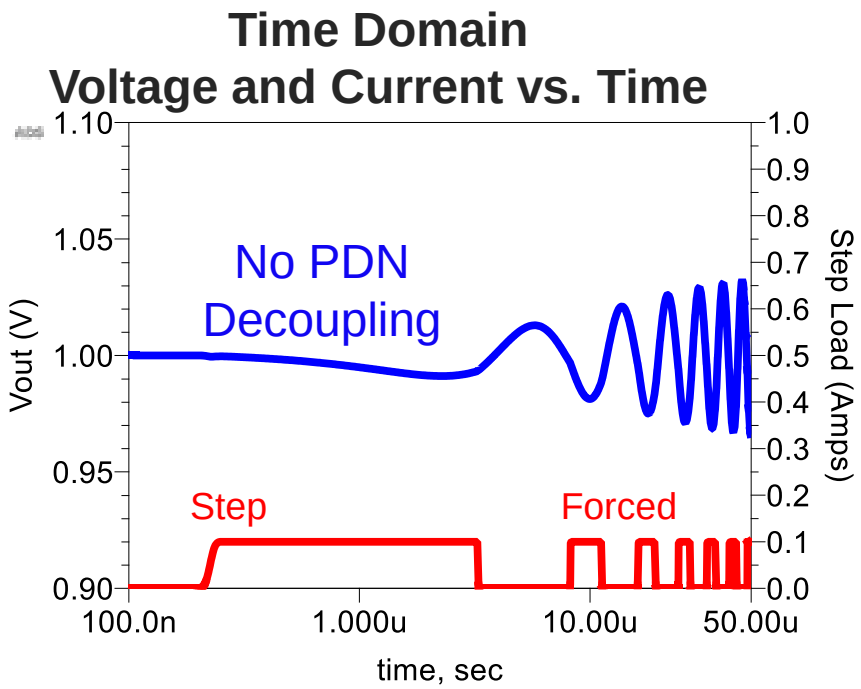
# VRM + Load and No Decoupling Capacitors

## PARALLEL RESONANCE CAUSES IMPEDANCE PEAK





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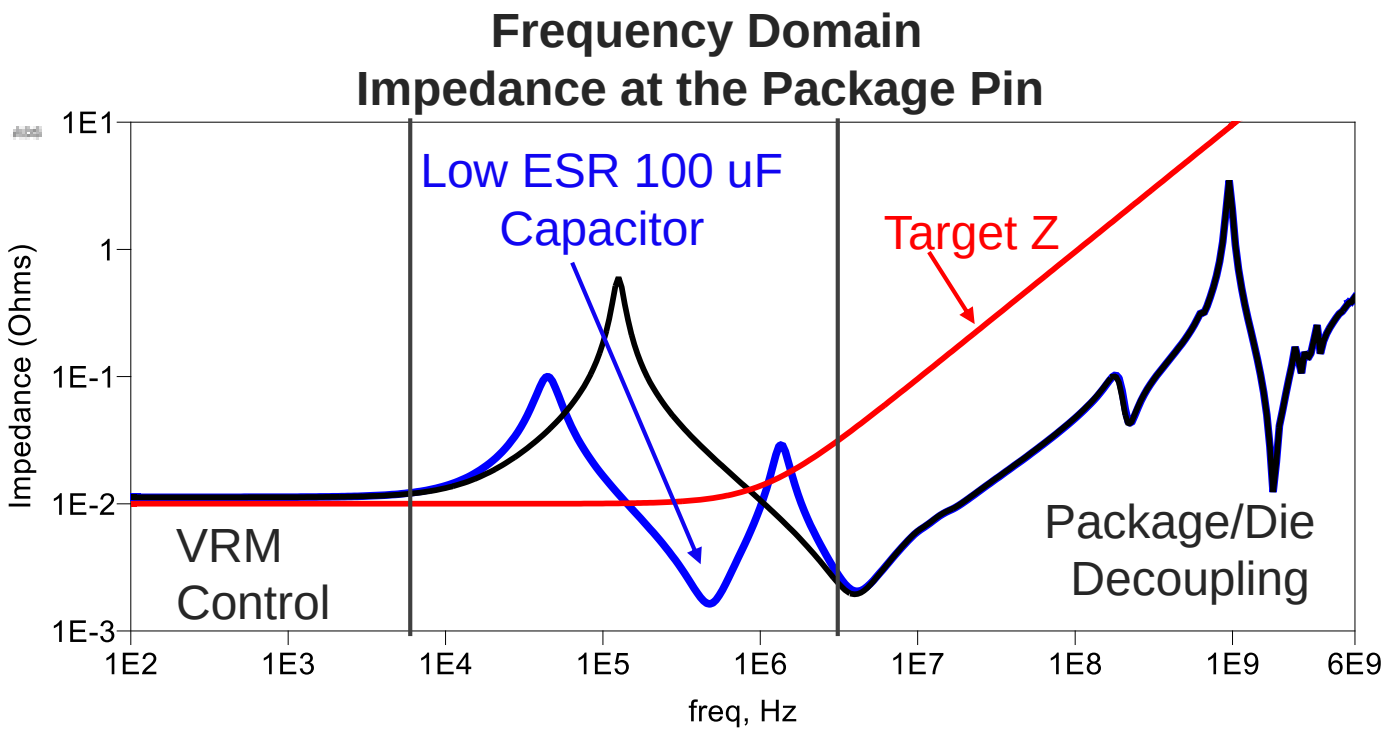
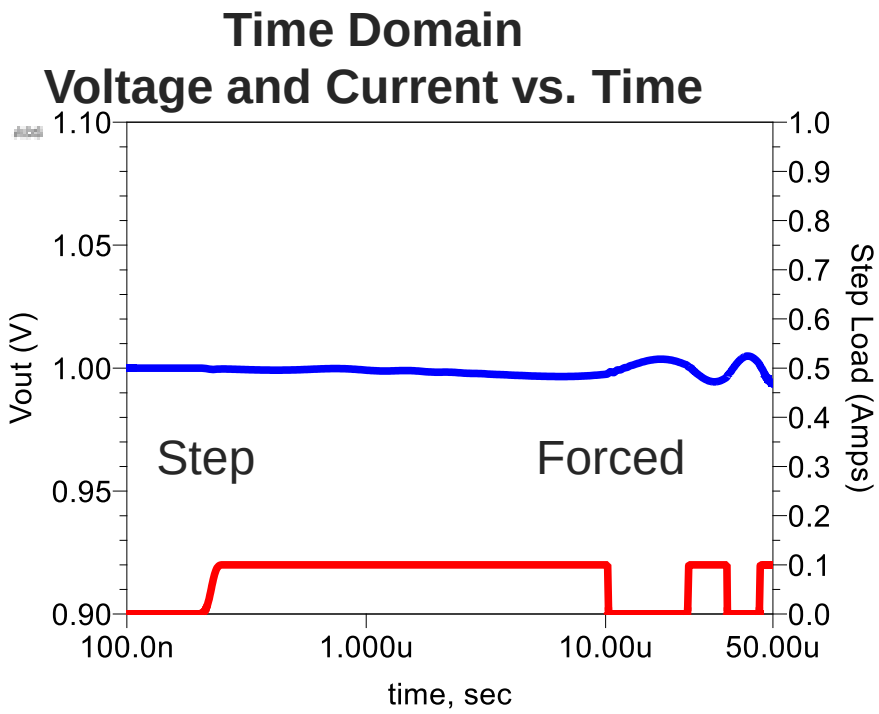
# The Wrong Capacitor Can Add Parallel Resonances

## INCREASES PART COUNT TO REACH TARGET Z





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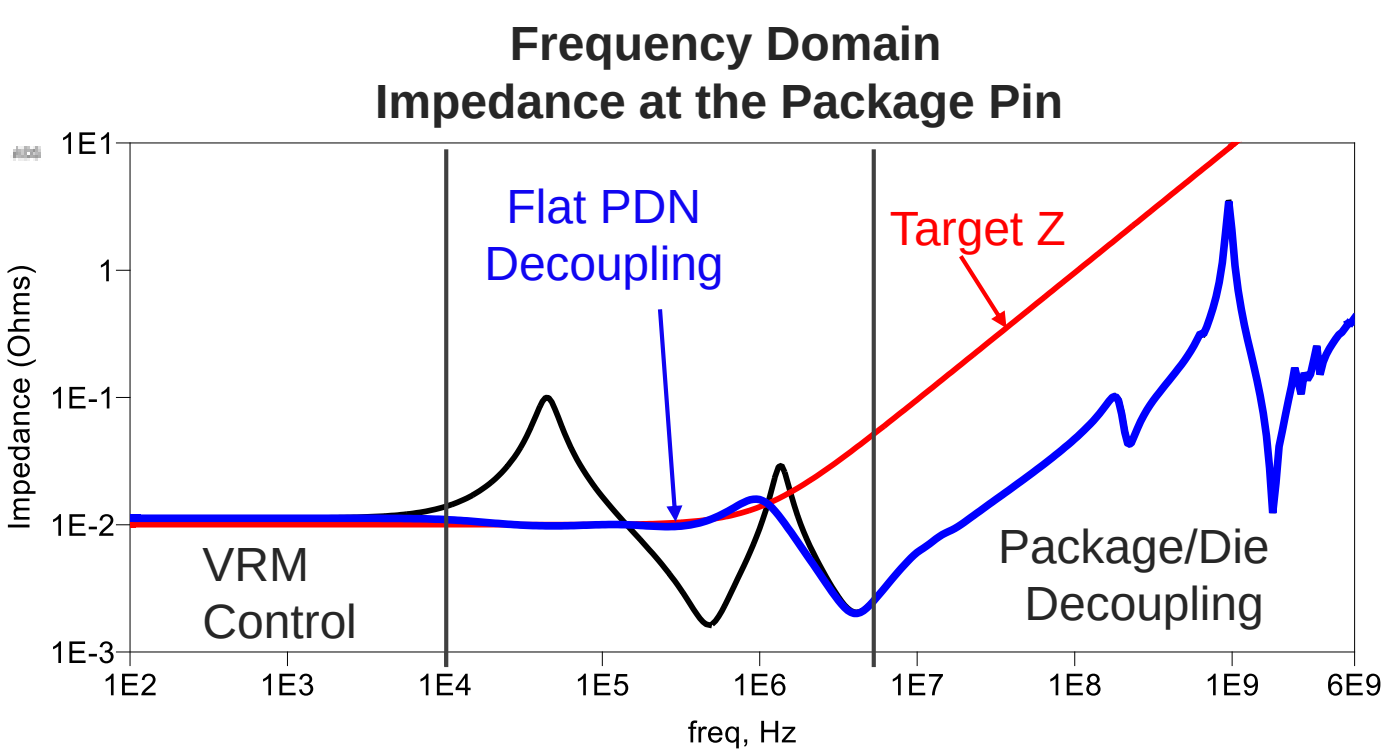
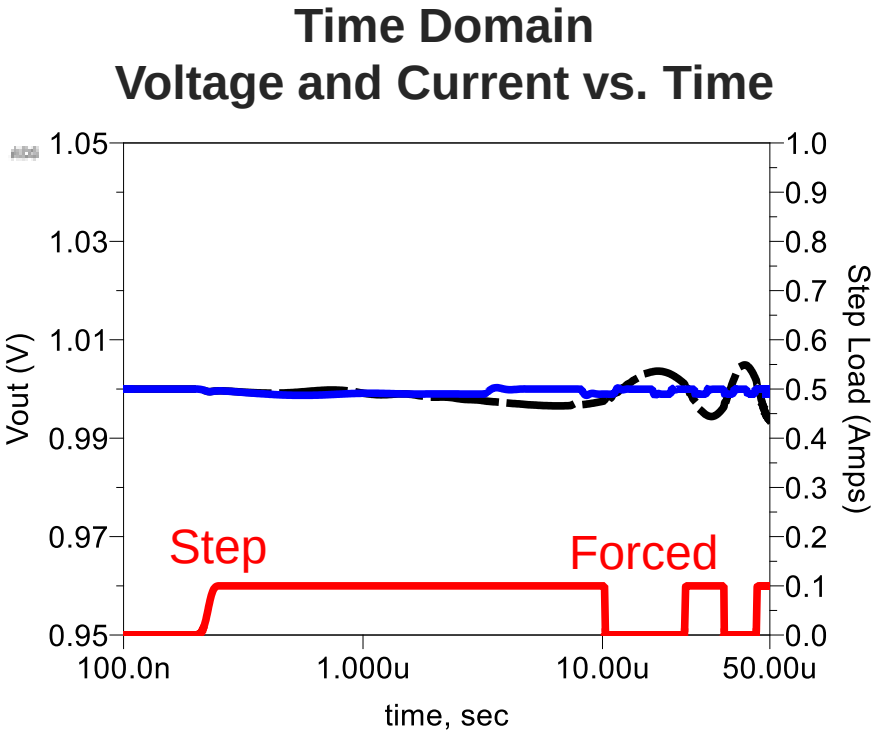
# Flat Impedance PDN Design

**FLAT Z = MAXIMUM STABILITY AND MINIMUM RIPPLE**





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1. Calculate 1st order approximations using simple resistor, inductor, capacitor R-L-C models

2. Use Target Z to optimize the decoupling capacitor selection using high fidelity EM models (ADS PIPro)

3. Validate with full Power Integrity Eco-System simulation in ADS


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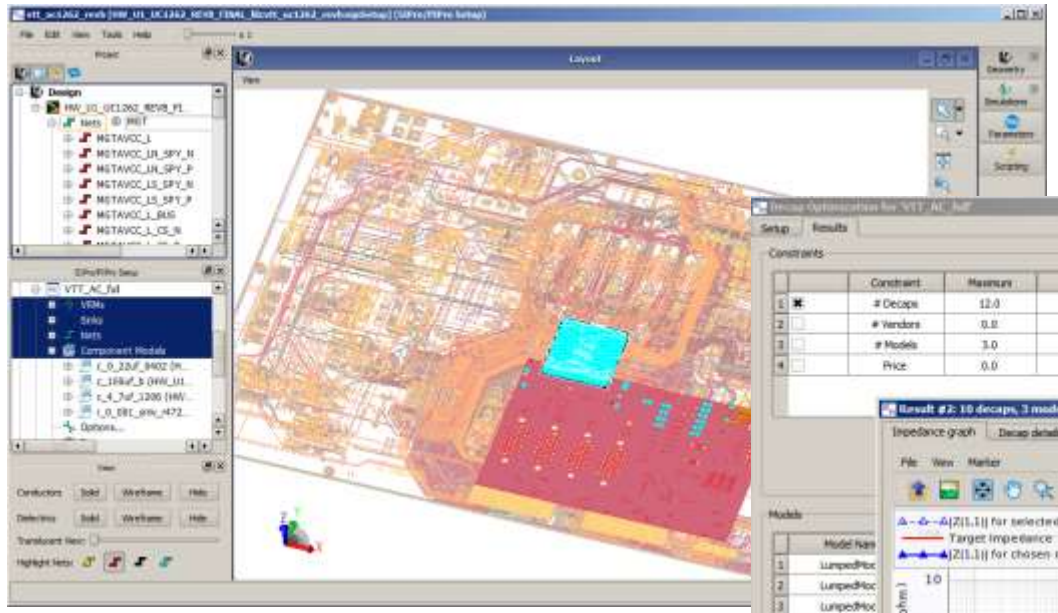
# ADS PIPro EM Simulation of the PCB PDN

## EASY SETUP FOR HIGH PORT COUNT SIMULATIONS

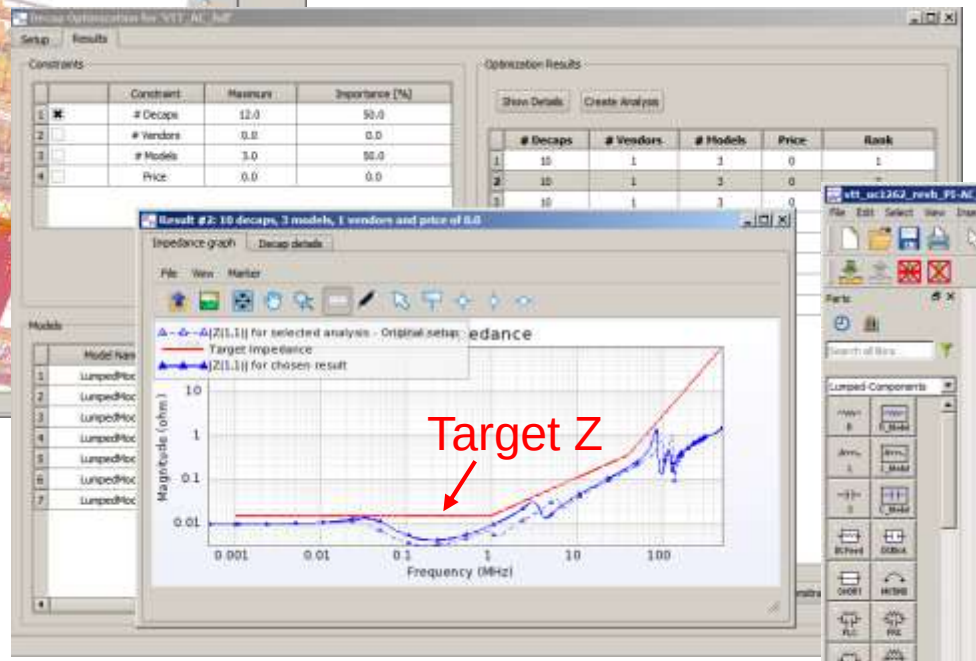
### 1) IMPORT THE PCB

- Select VRM, Sink, Nets, Components
- Run EM AC Frequency Sweep



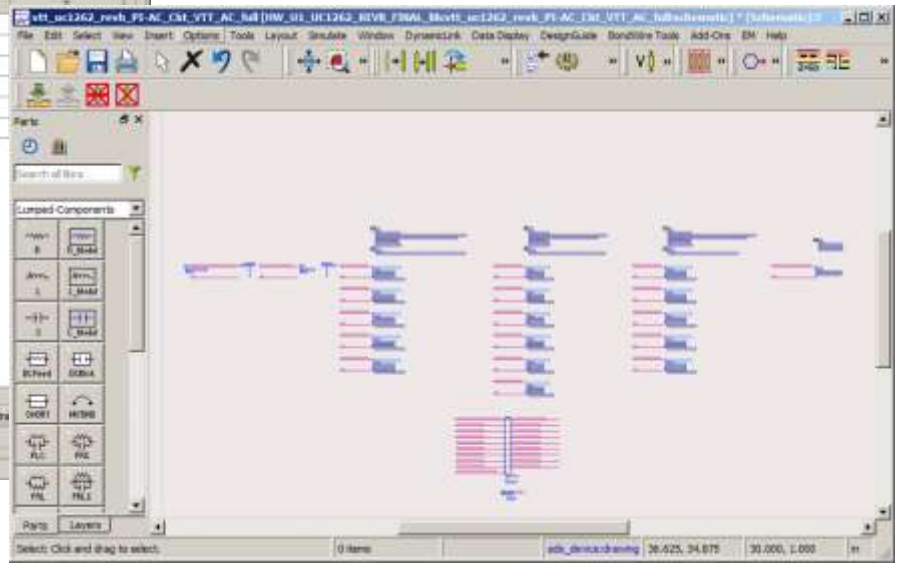
### 2) OPTIMIZE DECOUPLING

- Select capacitor models
- Setup optimization goals
- Run Optimization




### 2) GENERATE SCHEMATIC

- Auto generate schematic with PCB PDN EM model and optimized capacitors.



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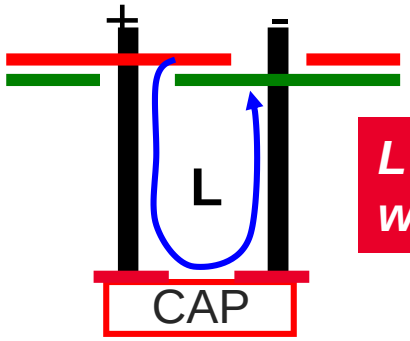
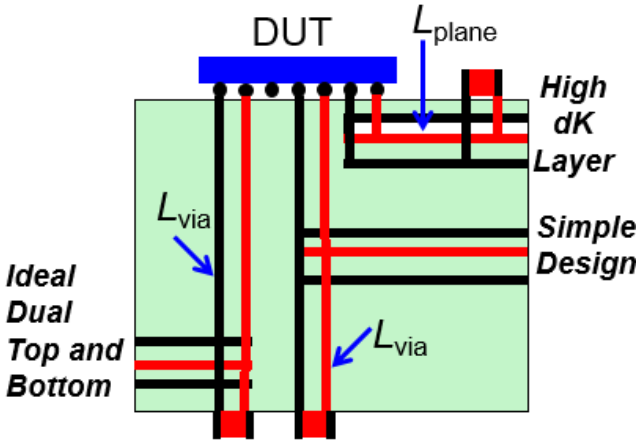
# Future Topic on How to Reduce Inductance in the PDN

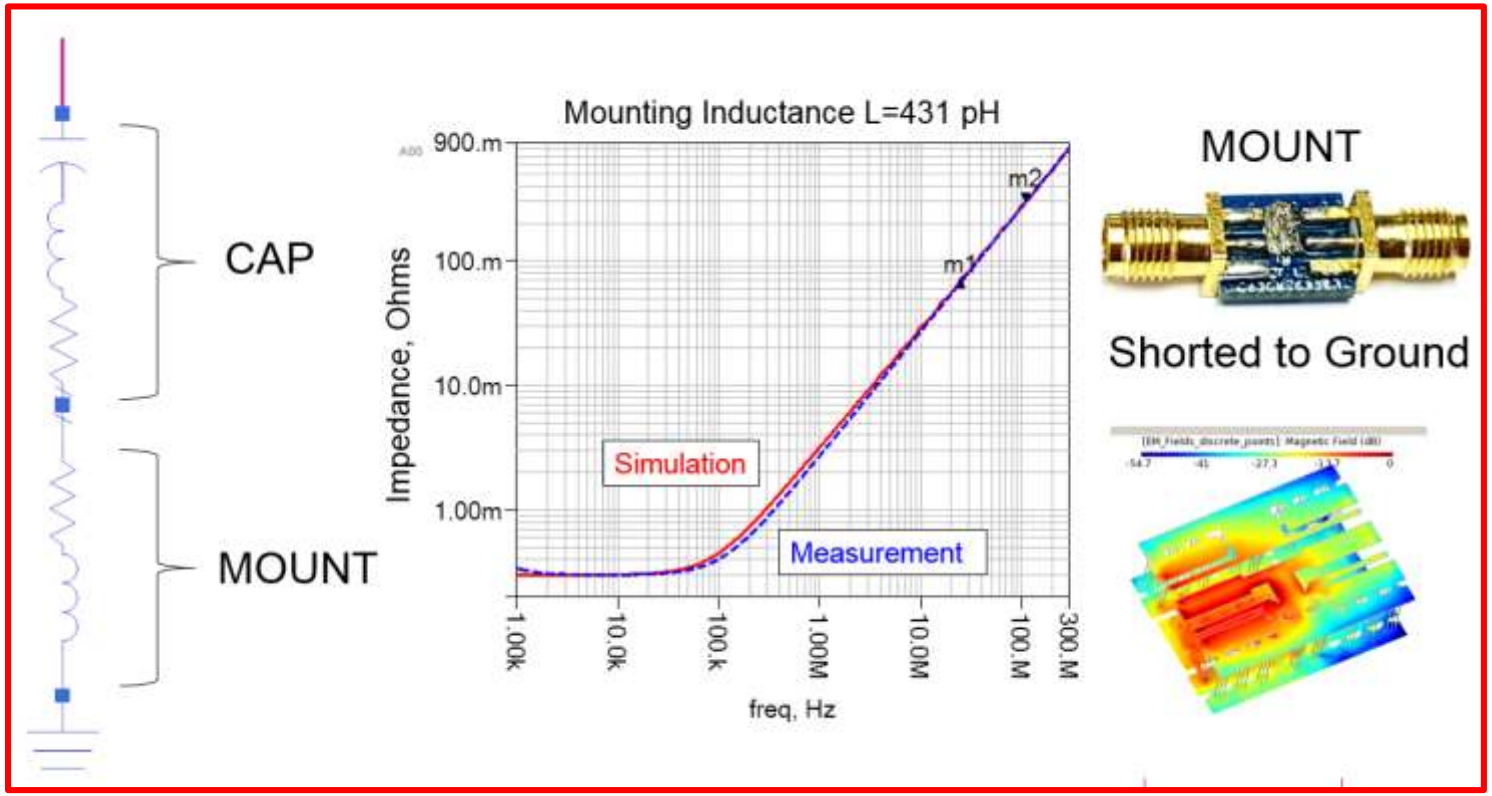
## EM SIMULATORS CAN OPTIMIZE LAYOUT FOR LOW L

### Loop Inductance




***L increases with loop area***





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# 3 Step Decoupling Capacitor Optimization

## DESIGN METHODOLOGY FOR DECAP OPTIMIZATION

1. Calculate 1st order approximations using simple resistor, inductor, capacitor R-L-C models

2. Use Target Z to optimize the decoupling capacitor selection using high fidelity EM models (ADS PIPro)

3. Validate with full Power Integrity Eco-System simulation in ADS


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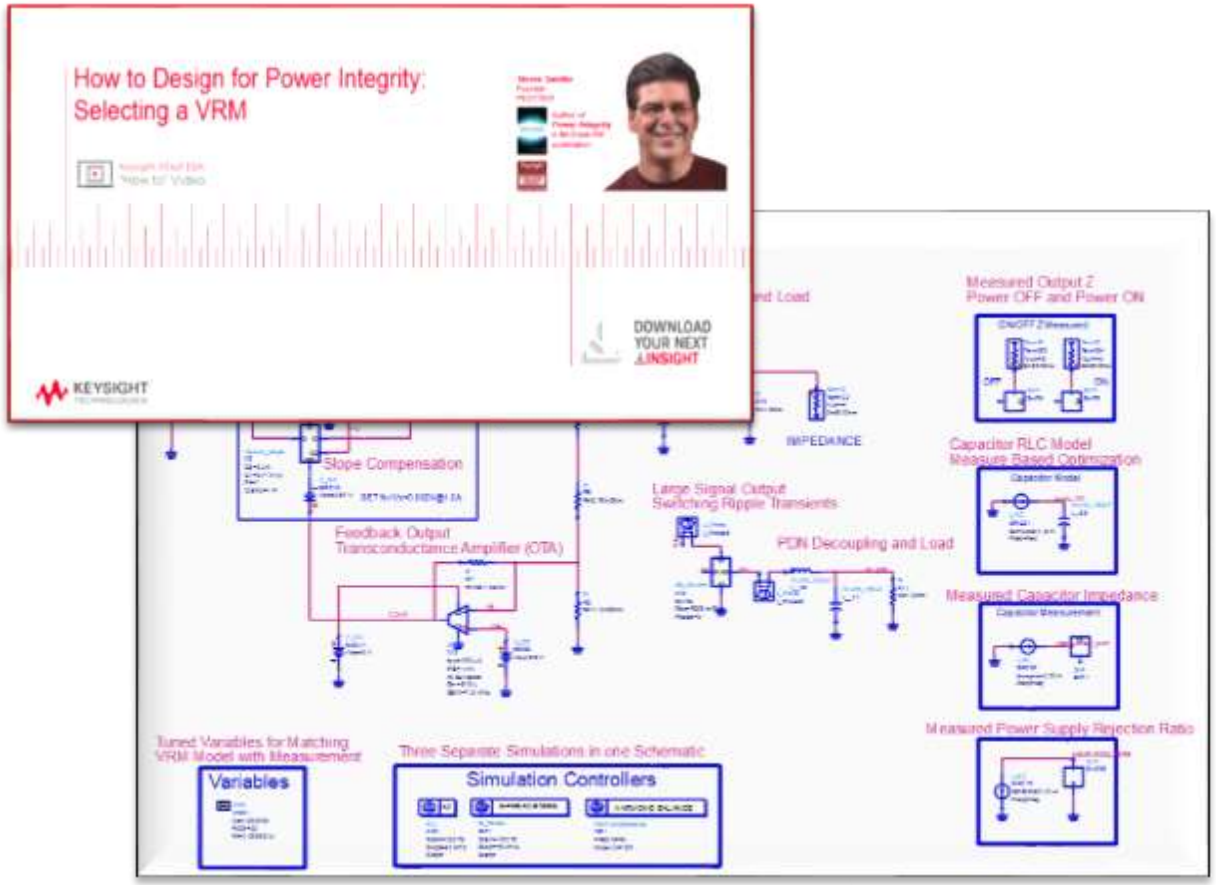
# Voltage Regulator State Spaced Averaged Models

## KEYSIGHT YOUTUBE VIDEO WITH PICOTEST

How to Video

http://tinyurl.com/vrm-video





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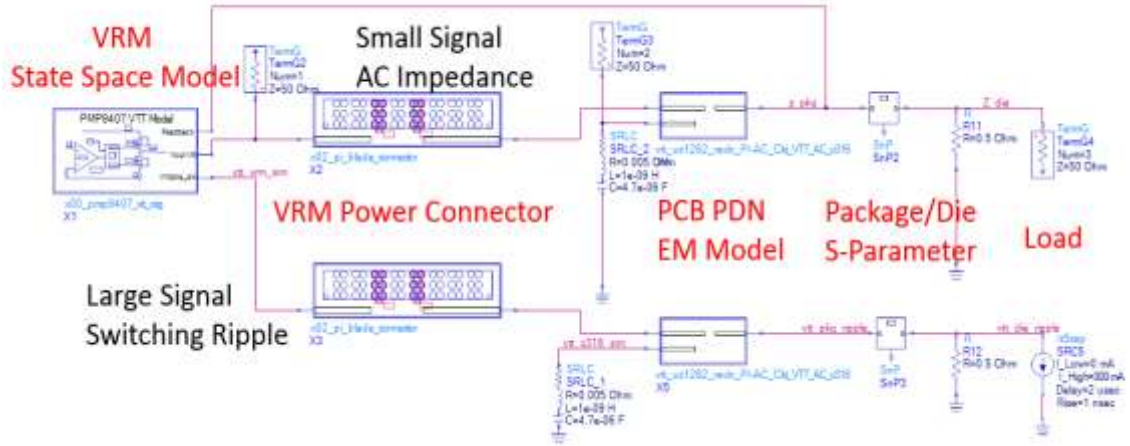
# Modeling the Power Integrity Ecosystem

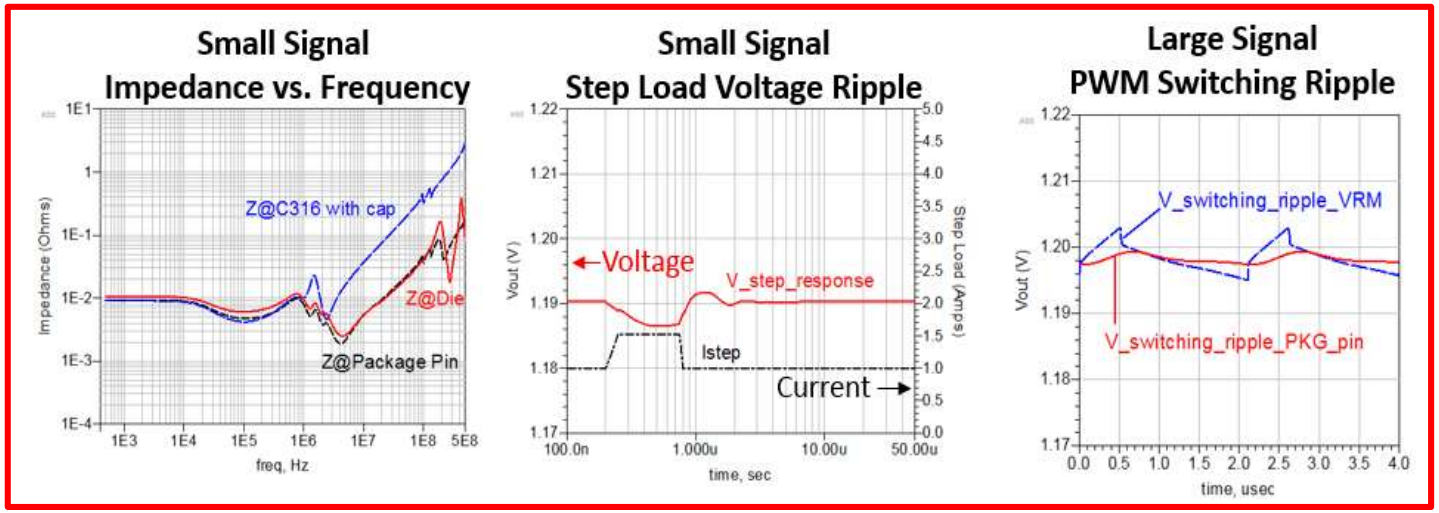
**VRM + PDN + LOAD = PI ECOSYSTEM**

Three Separate Simulations in one Schematic

## Simulation Controllers

| AC | S-PARAMETERS | HARMONIC BALANCE |
|---|---|---|
| AC<br>AC1<br>Start=100 Hz<br>Stop=40 MHz<br>Step= | S_Param<br>SP1<br>Start=100 Hz<br>Stop=40 MHz<br>Step= | HarmonicBalance<br>HB1<br>Freq[1]=Fs<br>Order[1]=256 |





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# Summary

## DESIGN METHODOLOGY FOR DECAP OPTIMIZATION

1. Calculate 1st order approximations

$$C_{bulk} = \frac{L_{supply}}{Z_{Target}^2} \qquad C_{decap} = \frac{ESL_{Cbulk}}{Z_{Target}^2} \qquad \text{Maximum } L_{PDN} = \frac{C_{pkg}}{Z_{Target}^2}$$

2. Decoupling capacitor optimization requires a Target Z input

3. Power Integrity Eco-System includes switching VRM models


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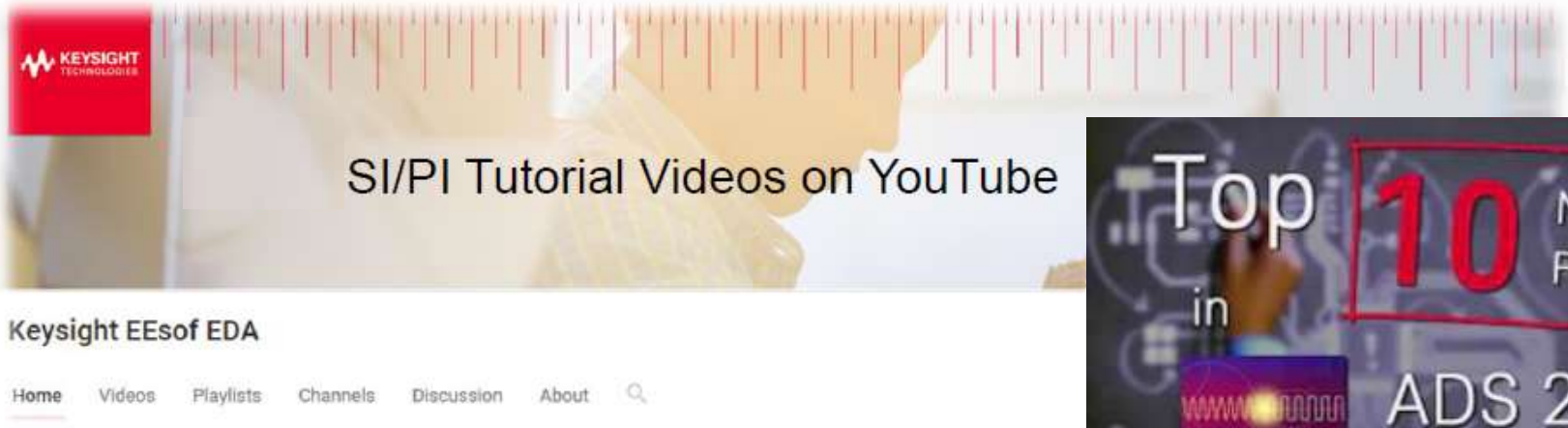
# Where to go next?

Webcast Recording
www.keysight.com/find/eesof-tutorials-signal-integrity

- Signal Integrity & Power Integrity Resources www.keysight.com/find/eesof-sipi-resources
- Where to get a free trial of ADS: www.keysight.com/find/eesof-ads



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- Application Focused
  (10 min each)
- Free workspace

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