Keysight D9050PCIC PCI Express® Gen5 Automated Test Application

Compliance Testing Methods of Implementation

KEYSIGHT TECHNOLOGIES

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PCI Express Gen5 Automated Testing—At A Glance

The Keysight D9050PCIC PCI Express® Gen5 Automated Test Application helps you verify PCI Express device under test (DUT) compliance to specifications using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope. The PCI Express® Gen5 Automated Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE The tests performed by the PCI Express® Gen5 Automated Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

NOTE D9050PCIC PCI Express Compliance Test Application supports two channel scope. In case of two channel scope, only channel 1 and 2 will be available.

NOTE D9050PCIC PCI Express Compliance Test Application supports D9010AGGC Compliance Test Software Measurement Server for using multiple machines/PCs over a network as acquisition engines and processing engines in order to significantly enhance the test execution speed. To know more, please see the D9010AGGC product page on keysight.com.

NOTE This document covers the methods of implementation for PCIe 5.0 devices only. For PCIe 4.0 devices, please see the Keysight D9040PCIC PCI Express Compliance Test Application Methods of Implementation document.

Required Equipment and Software

In order to run the PCI Express automated tests, you need the following equipment and software:

- D9050PCIC PCI Express® Gen5 Automated Test Application software and license
- Use one of the following oscilloscope models:
  - Keysight Z-Series Infiniium Oscilloscopes
  - Keysight Q-Series Infiniium Oscilloscope
  - Keysight UXR Series Infiniium Oscilloscope
- E2688A Serial Data Analysis and Clock Recovery software
- Keyboard, qty = 1, (provided with the Keysight Infiniium Series Oscilloscope)
- Mouse, qty = 1, (provided with the Keysight Infiniium Series Oscilloscope)
- Precision 3.5 mm BNC to SMA male adapter, qty = 2 (provided with the Keysight Infiniium Series Oscilloscope)
- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG-316/U or similar, qty = 2, matched length

In This Book

This manual describes the tests that are performed by the PCI Express® Gen5 Automated Test Application in more detail; it contains information from (and refers to) the base specification, and it describes how the tests are performed.

This manual is divided into following sections:

- “Introduction” covers the software and license installation and test preparation guide.
- “PCI-Express Gen5 2.5 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 2.5 GT/s.
- “PCI Express Gen5 5.0 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 5.0 GT/s.
- “PCI-Express Gen5 8.0 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 8.0 GT/s.
- “PCI Express Gen5 16.0 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 16.0 GT/s.
- “PCI Express Gen5 32.0 GT/s Tests” covers the PCI Express Gen 5 tests and methods of implementation at 32.0 GT/s.
- “Appendices” covers oscilloscope calibration, channel de-skew calibration, and index information.

The chapters in this book are:

- Chapter 1, “Installing the PCI Express Gen5 Compliance Test Application” shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” shows how to start the PCI Express® Gen5 Automated Test Application and gives a brief overview of how it is used.
- Chapter 3, “Reference Clock Tests, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests for all data rates.
- Chapter 4, “Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 2.5 GT/s data rate.
- Chapter 5, “Reference Clock Tests, 2.5 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 2.5 GT/s data rate.
- Chapter 6, “Transmitter (Tx) Tests, 5.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 5.0 GT/s data rate.
- Chapter 7, “Reference Clock Tests, 5.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 5.0 GT/s data rate.
- Chapter 8, “Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 8.0 GT/s data rate.
- Chapter 9, “Reference Clock Tests, 8.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 8.0 GT/s data rate.
- Chapter 10, “Transmitter (Tx) Tests, 16.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 16.0 GT/s data rate.

- Chapter 11, “Reference Clock Tests, 16.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 16.0 GT/s data rate.
- Chapter 12, “Transmitter (Tx) Tests, 32.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 transmitter tests at 32.0 GT/s data rate.
- Chapter 13, “Reference Clock Tests, 32.0 GT/s, PCI-E 5.0” contains more information on the PCI Express version 5.0 reference clock tests at 32.0 GT/s data rate.
- Appendix A, “Calibrating the Digital Storage Oscilloscope” describes how to calibrate the oscilloscope in preparation for running the PCI Express automated tests.
- Appendix B, “INF_SMA_Deskew.set Setup File Details” describes a setup used when performing channel de-skew calibration.

See Also,

The PCI Express® Gen5 Automated Test Application's online help, which describes:

- PCI Express Gen5 Automated Testing—At a Glance
- Creating or Opening a Test Project
- Setting Up the Test Environment
  - Test Mode
  - Device Definition
  - Connection Setup
  - Test Report - User Comments
- Selecting Tests
- Configuring Tests
- Verifying Physical Connections
- Running Tests
  - Options to Start Test Runs
  - Settings to Optimize Test Runs
- Configuring Automation in the Test Application
  - Using Script for Automation
  - Using Files for Automation
  - Running Automation Script or Files
- Viewing Results
- Viewing HTML Test Report
- Exiting the Test Application
- Additional Settings in the Test App
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  - File Menu Options
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  - Help Menu Options
  - Controlling the Application via a Remote PC
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If you purchased the D9050PCIC PCI Express Gen5 Compliance Test Application separately, you need to install the software and license key.

NOTE

D9050PCIC PCI Express Compliance Test Application supports **D9010AGGC Compliance Test Software Measurement Server** for using multiple machines/PCs over a network as acquisition engines and processing engines in order to significantly enhance the test execution speed. To know more, please see the D9010AGGC product page on keysight.com.

Installing the Software

1. To obtain the PCI Express Gen5
   Compliance Test Application, please go to Keysight website:
   http://www.keysight.com/find/D9050PCIC
2. The link for PCI Express Gen5
   Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

   Be sure to accept the installation of the .NET Framework software; it is required in order to run the PCI Express Gen5
   Compliance Test Application.

Installing the License Key

To procure a license, you require the Host ID information that is displayed in the Keysight License Manager application installed on the same machine where you wish to install the license.

Using Keysight License Manager 5

To view and copy the Host ID from Keysight License Manager 5:

1 Launch Keysight License Manager on your machine, where you wish to run the Test Application and its features.

2 Copy the Host ID that appears on the top pane of the application. Note that x indicates numeric values.

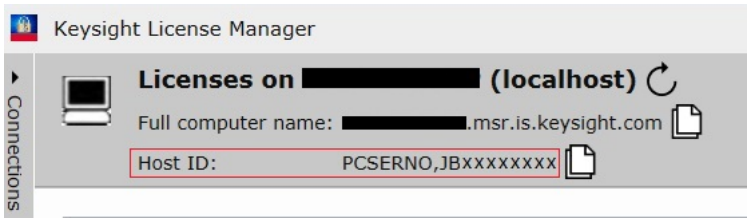

Figure 1 Viewing the Host ID information in Keysight License Manager 5

To install one of the procured licenses using Keysight License Manager 5 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.

2 Launch Keysight License Manager.

3 From the configuration menu, use one of the options to install each license file.

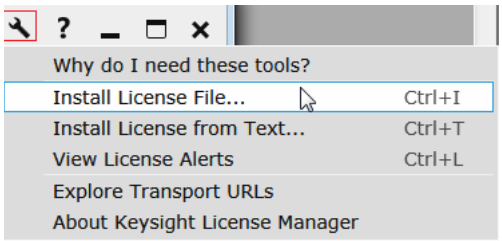

Figure 2 Configuration menu options to install licenses on Keysight License Manager 5

For more information regarding installation of procured licenses on Keysight License Manager 5, refer to Keysight License Manager 5 Supporting Documentation.

Using Keysight License Manager 6

To view and copy the Host ID from Keysight License Manager 6:

1. Launch Keysight License Manager 6 on your machine, where you wish to run the Test Application and its features.
2. Copy the Host ID, which is the first set of alphanumeric value (as highlighted in Figure 3) that appears in the Environment tab of the application. Note that x indicates numeric values.

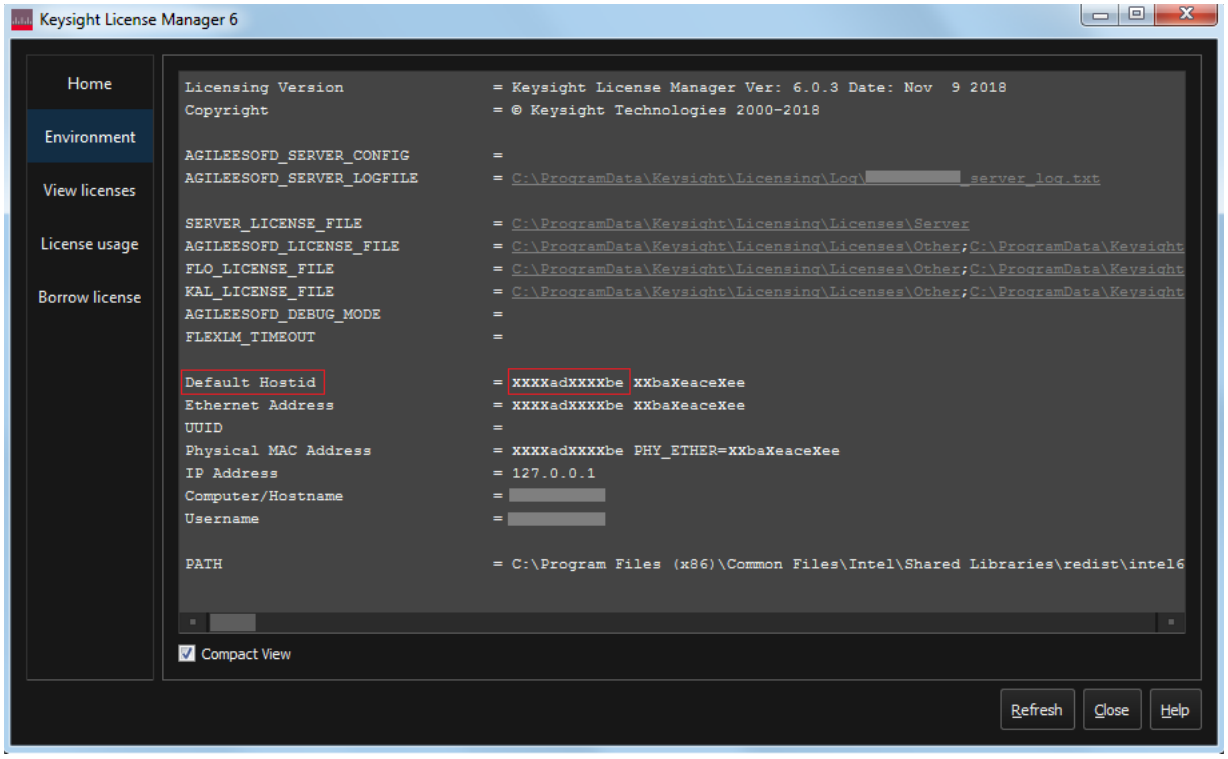

Figure 3 Viewing the Host ID information in Keysight License Manager 6

To install one of the procured licenses using Keysight License Manager 6 application,

1 Save the license files on the machine, where you wish to run the Test Application and its features.
2 Launch Keysight License Manager 6.
3 From the Home tab, use one of the options to install each license file.

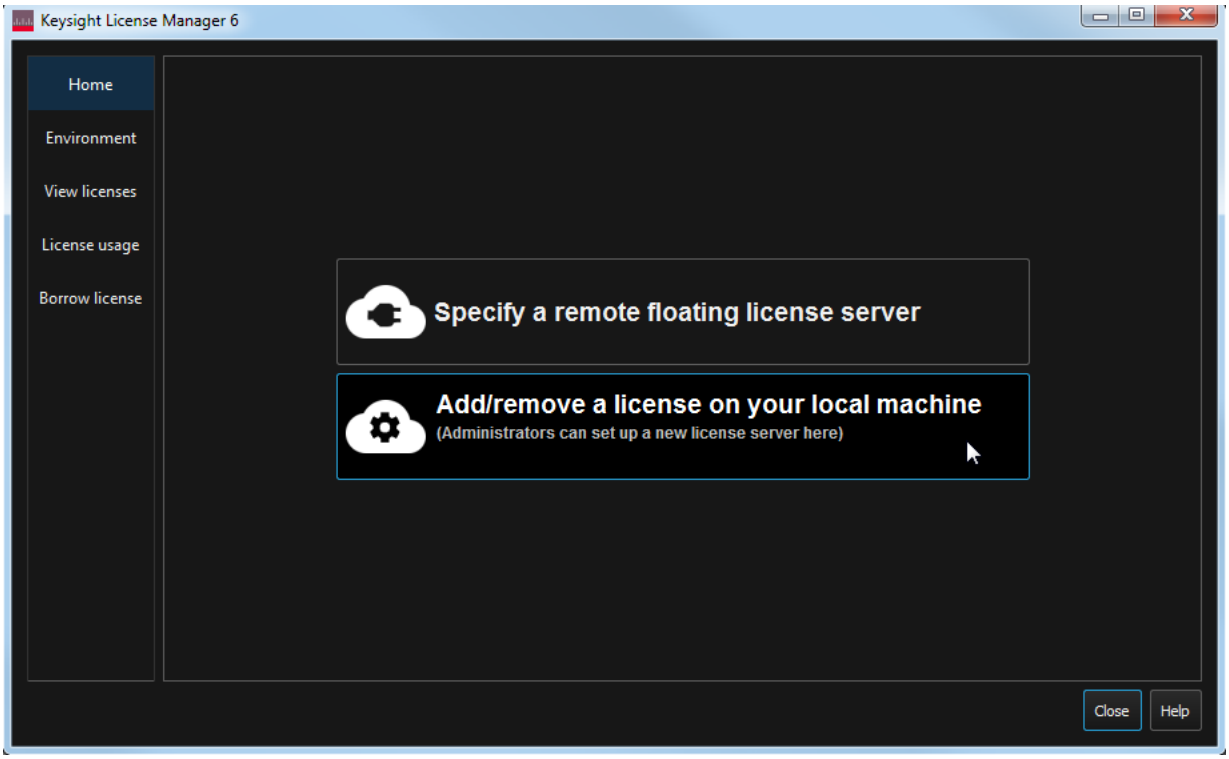

Figure 4 Home menu options to install licenses on Keysight License Manager 6

For more information regarding installation of procured licenses on Keysight License Manager 6, refer to Keysight License Manager 6 Supporting Documentation.

2 Preparing to Take Measurements

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Starting the PCI Express Gen5 Compliance Test Application / 25

Before running the PCI Express automated tests, you should calibrate the oscilloscope. After the oscilloscope has been calibrated, you are ready to start the PCI Express Gen5 Compliance Test Application and perform measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope, see Appendix A, "Calibrating the Digital Storage Oscilloscope.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities > Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration and channel de-skew calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel they were calibrated for.

Starting the PCI Express Gen5 Compliance Test Application

1 From the Infiniium oscilloscope's main menu, choose **Analyze > Automated Test Apps > D9050PCIC PCIExpress Gen5 Test App**.

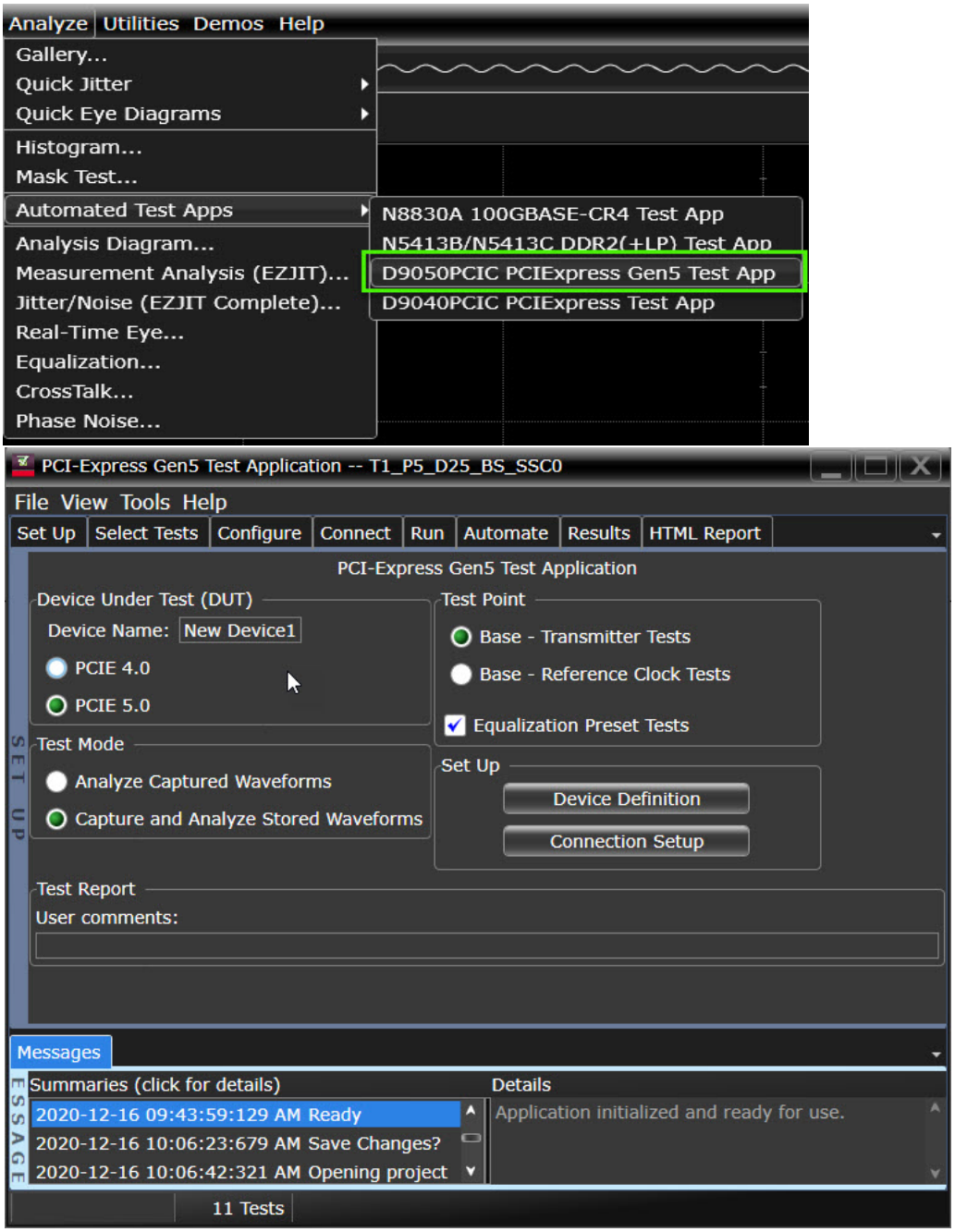

Figure 5 The PCI Express Gen5 Compliance Test Application

NOTE

If PCI Express does not appear in the Automated Test Apps menu, the PCI Express Gen5 Compliance Test Application has not been installed (see Chapter 1, "Installing the PCI Express Gen5 Compliance Test Application).

Figure 5 shows the PCI Express Gen5 Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you identify and set up the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure the test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automate	Allows to automate tests through automation commands
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the PCI Express Gen5 Compliance Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The PCI Express Gen5 Compliance Test Application's online help describes:

- Starting the PCI Express Gen5 Compliance Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up the test environment.
  - To set up InfiniiSim.
  - To load saved waveforms.
- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running tests.
  - To select the "store mode".
  - To run multiple times.
  - To send email on pauses or stops.
  - To specify the event.
  - To set the display preferences.
  - To set the run preferences.
- Viewing test results.
  - To delete trials from the results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
  - To change the test display order.
  - To set trial display preferences.
- Viewing/exporting/printing the HTML test report.
  - To export the report.
  - To print the report.
- Saving test projects.
  - To set AutoRecovery preferences.
- Controlling the application via a remote PC.
  - To check for the App Remote license.
  - To identify the remote interface version.
  - To enable the remote interface.
  - To enable remote interface hints.
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Part II
PCI-Express Gen5
All GT/s Tests

KEYSIGHT
TECHNOLOGIES

3 Reference Clock Tests, PCI-E 5.0

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This section provides the Methods of Implementation (MOIs) for Reference Clock tests, common to all data rates, using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application..

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in Figure 4-25 of the Card Electromechanical Specification.

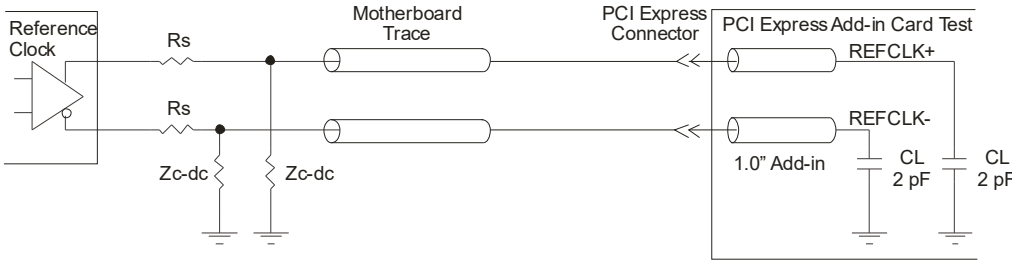


Figure 1 Driver Compliance Test Load.

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. Then, when selecting tests, navigate to the "Reference Clock Tests" group.

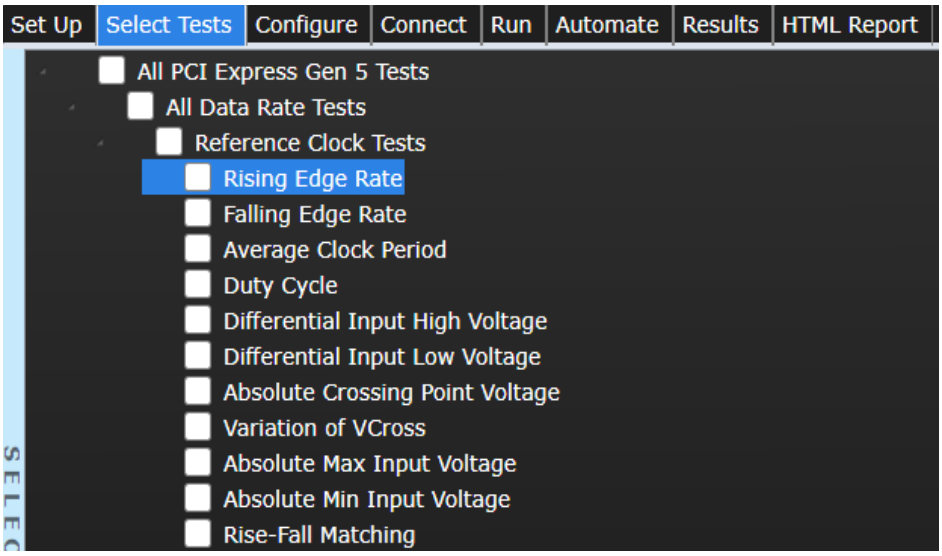


Figure 2 Selecting Reference Clock Tests

Rising Edge Rate Test

The rising edge rate test is measured from -150 mV to +150 mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for rise time and 300 mV measurement window is centered on the differential zero crossing.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
Rise Edge Rate	Rising Edge Rate	0.6 V/ns	4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 8-69.

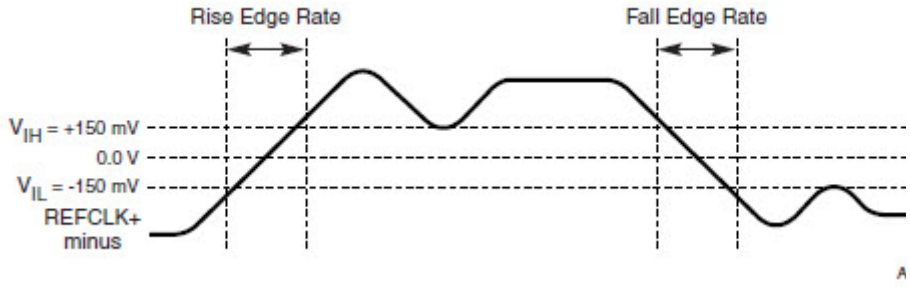


Figure 3 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Fits and displays all sample data on screen.

4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.

5 Measures the maximum rise time using **Rise time** measurement.

6 Zoom to maximum value of rise time.

7 Converts the maximum rise time to units of V/ns as given in the PCIE spec. [0.0000000003 / Maximum Rise Time value].

8 Reports the rising edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as `0.6 V/ns` ≥ Rising Edge Rate ≤ 4.0 V/ns.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

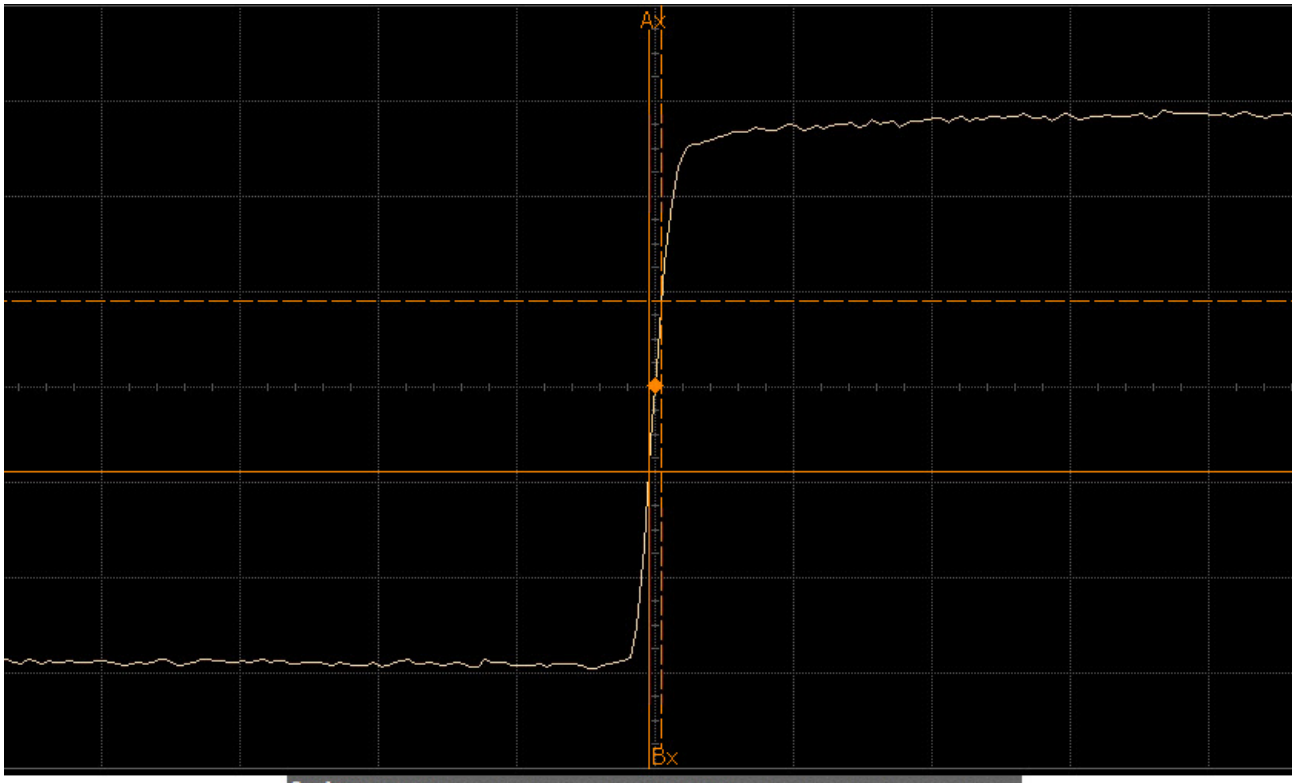


Figure 4 Reference Image for Rising Edge Rate

Falling Edge Rate Test

The falling edge rate test is measured from -150 mV to +150 mV on the differential waveform which is derived from RefClk+ minus RefClk-. The signal must be monotonic through the measurement region for fall time and 300 mV measurement window is centered on the differential zero crossing.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
Fall Edge Rate	Falling Edge Rate	0.6 V/ns	4.0 V/ns

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See, Figure 8-69.

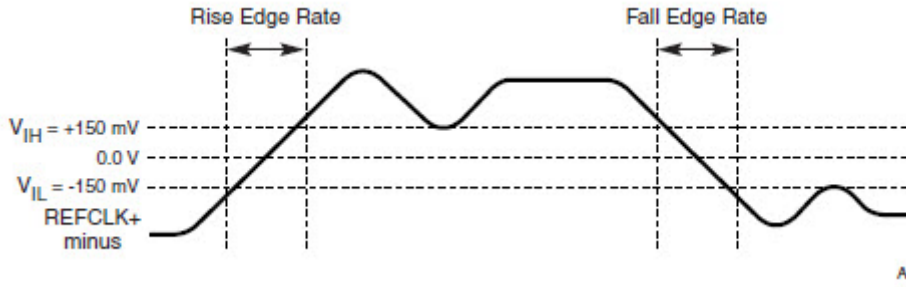


Figure 5 Differential Measurement Points for Rise and Fall Time

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Fits and displays all sample data on screen.

4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.

5 Measures the maximum fall time using **Fall time** measurement.

6 Zoom the resultant waveform to maximum value of fall time.

7 Converts the maximum fall time to units of V/ns as given in the PCIE specification [0.0000000003 / Maximum Fall Time value].

8 Reports the falling edge rate value and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as 0.6 V/ns ≤ Falling Edge Rate ≤ 4.0 V/ns.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

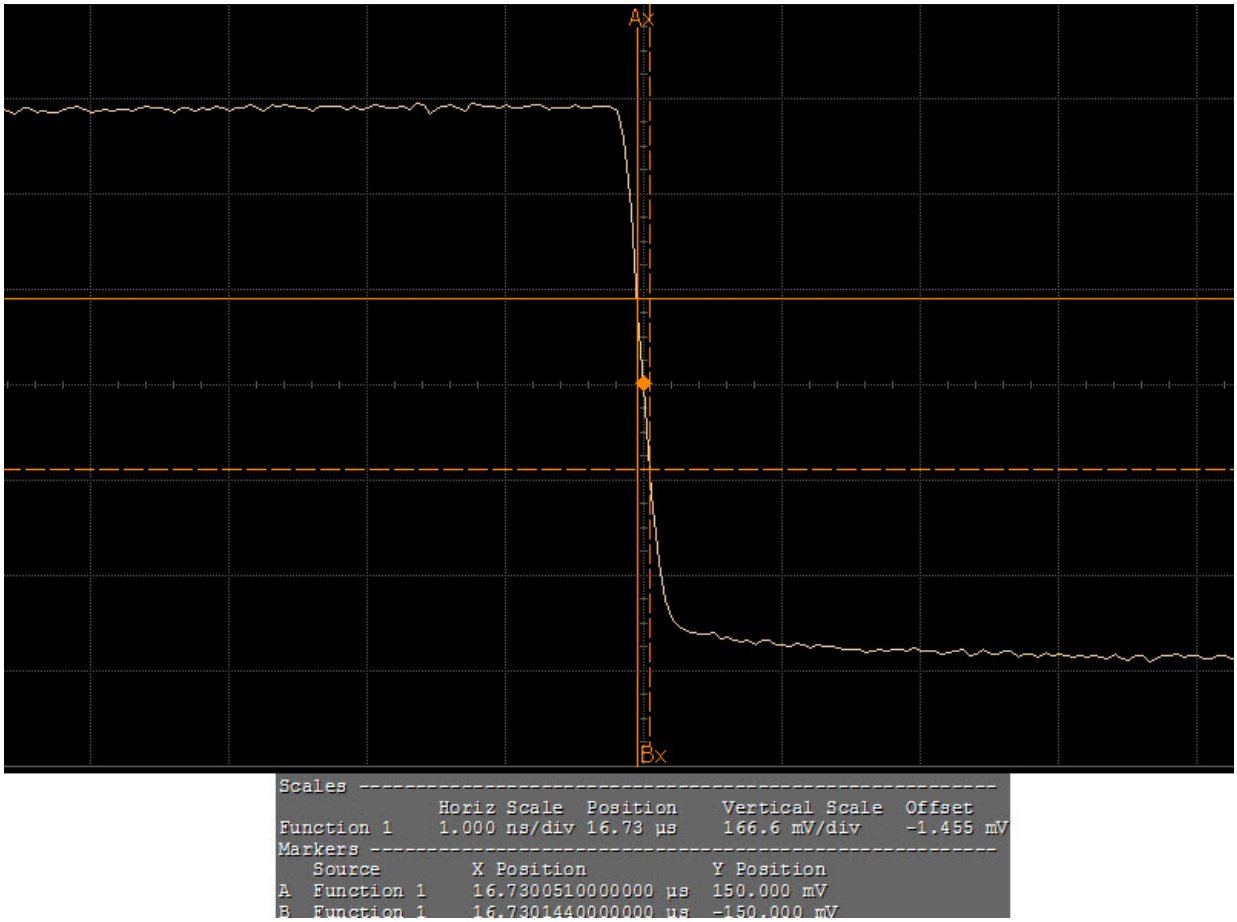


Figure 6 Reference Image for Falling Edge Rate

Average Clock Period Test

This test verifies that the Refclk Average Clock Period is within the conformance limits as specified in PCIE Express Base Specification, Revision 5.0, Section 8.6.2, Table 8-16.

The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100 Hz. A requirement of +/- 300 PPM applies to systems that do not employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	2800 ppm

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For example for 300 PPM, then we have an error budget of 100 Hz/ PPM × 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Configures memory depth and sampling rate as per the data rate.

4 Fits and displays all sample data on screen.

5 Measures the average voltage using **V average** measurement.

6 Configures the **Top Level** threshold to +150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.

7 Measures the average frequency using **Frequency** measurement of **Clock**.

8 Measures the average period using **Period** measurement of **Clock**.

9 Computes the difference between ideal and actual frequency in terms of parts per million of 100MHz as follows:

$$\text{Difference between ideal and actual frequency} = [100MHz - AverageFrequency]/100$$

10 Reports the average clock period accuracy and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

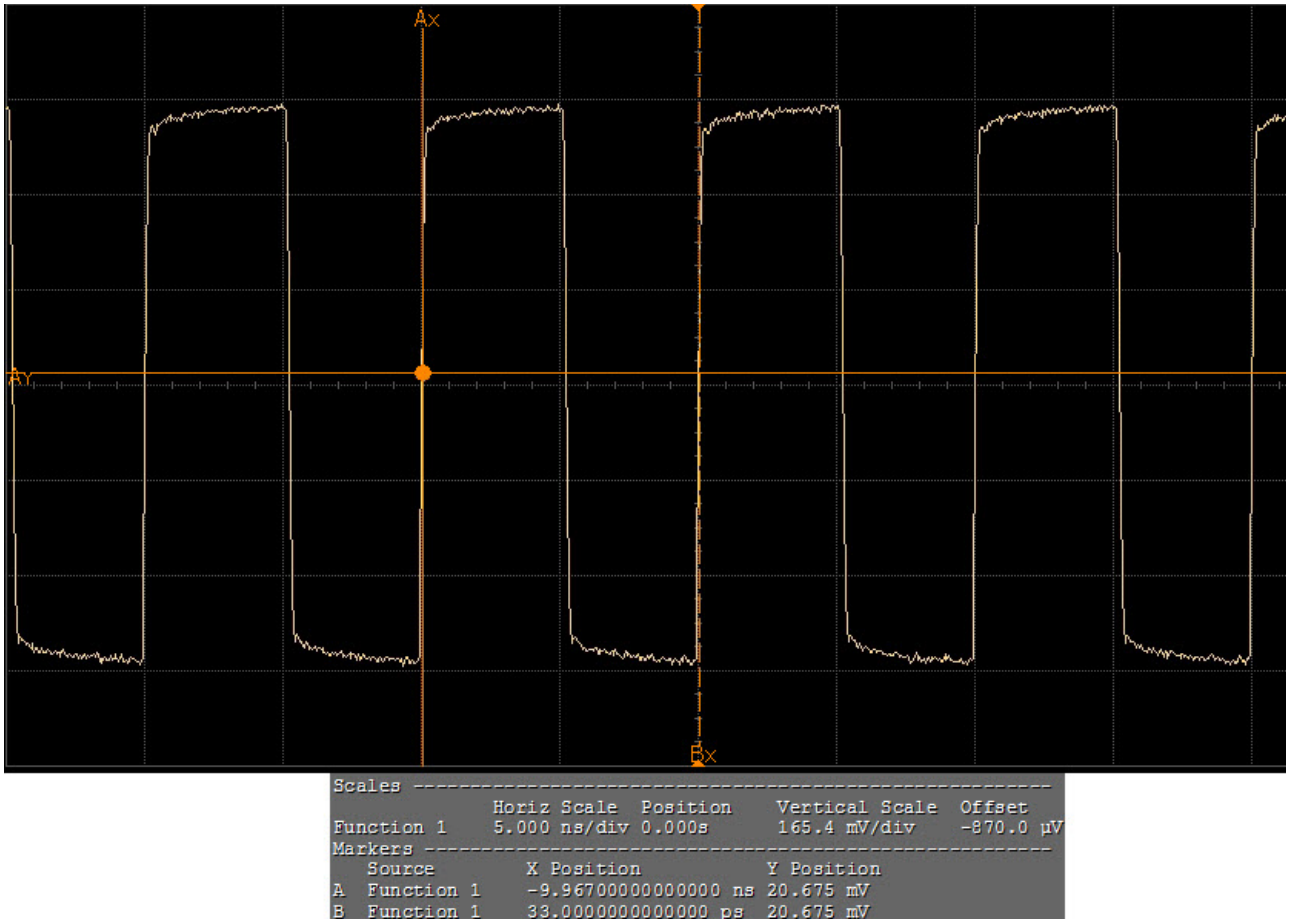


Figure 7 Reference Image for Average Clock Period

Duty Cycle Test

The duty cycle test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)	Max (at 100 MHz Input)
Duty Cycle	Duty Cycle	40%	60%

Test Definition Notes from the Specification

Measurement taken from differential waveform.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Configures memory depth and sampling rate as per the data rate.

4 Fits and displays all sample data on screen.

5 Measures the average voltage using **V average** measurement.

6 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.

7 Measures the duty cycle using the **Duty cycle** measurement.

8 Finds the margin for maximum duty cycle and minimum duty cycle.

9 Compares the margin and choose the largest margin to report the value (worst value) as duty cycle.

10 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as $40\% \leq \text{Duty Cycle} \leq 60\%$.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

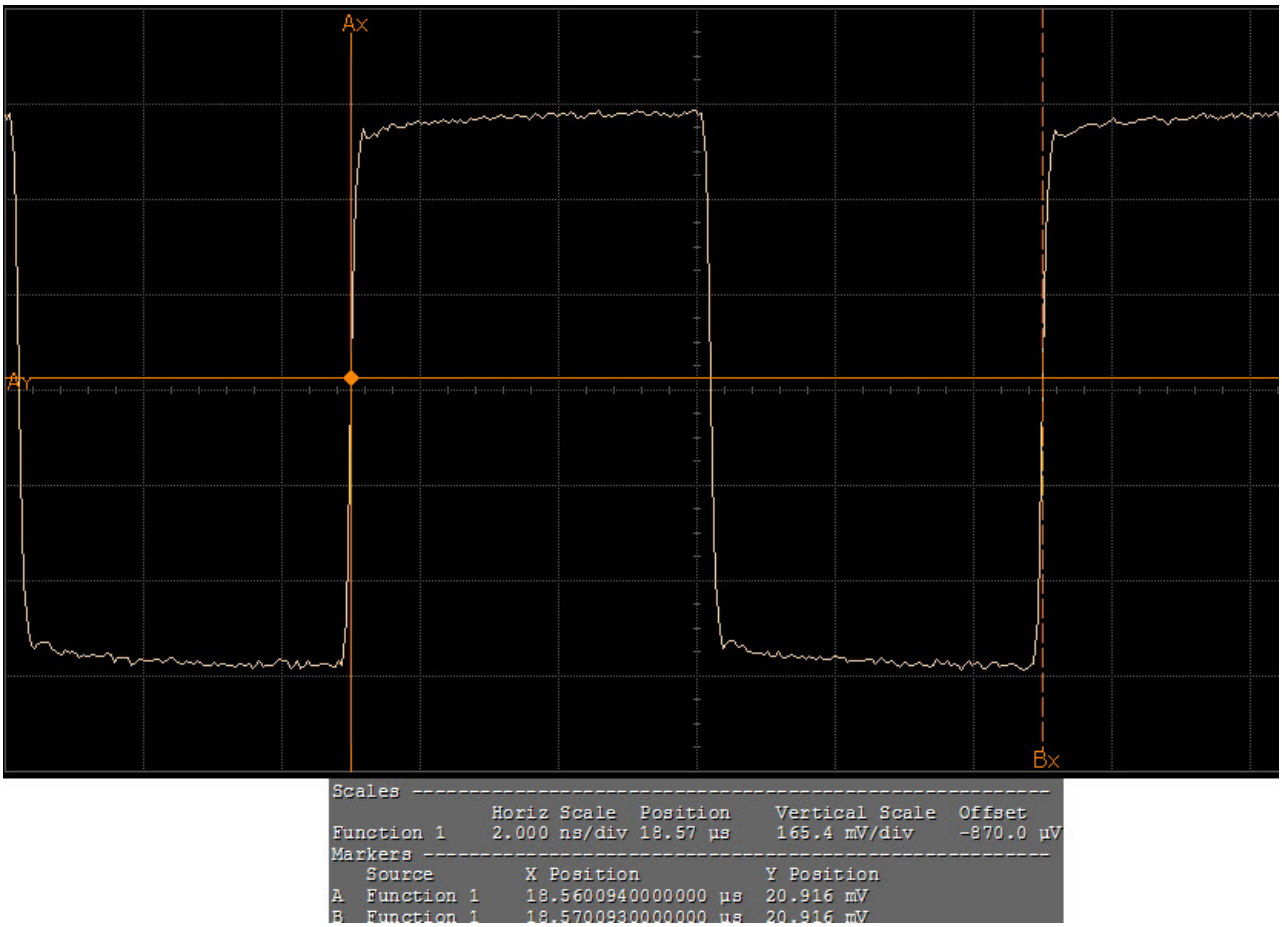


Figure 8 Reference Image for Duty Cycle

Differential Input High Voltage Test

The differential input high voltage test verifies that the reference clock differential input high voltage is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Min (at 100 MHz Input)
V_{IH}	Differential Input High Voltage	150 mV

Test Definition Notes from the Specification

Measurement taken from differential waveform.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Fits and displays all sample data on screen.

4 Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.

5 Measures the maximum voltage using **V max** measurement.

6 Reports the maximum voltage value as differential input high voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as V_{IH} > 150 mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

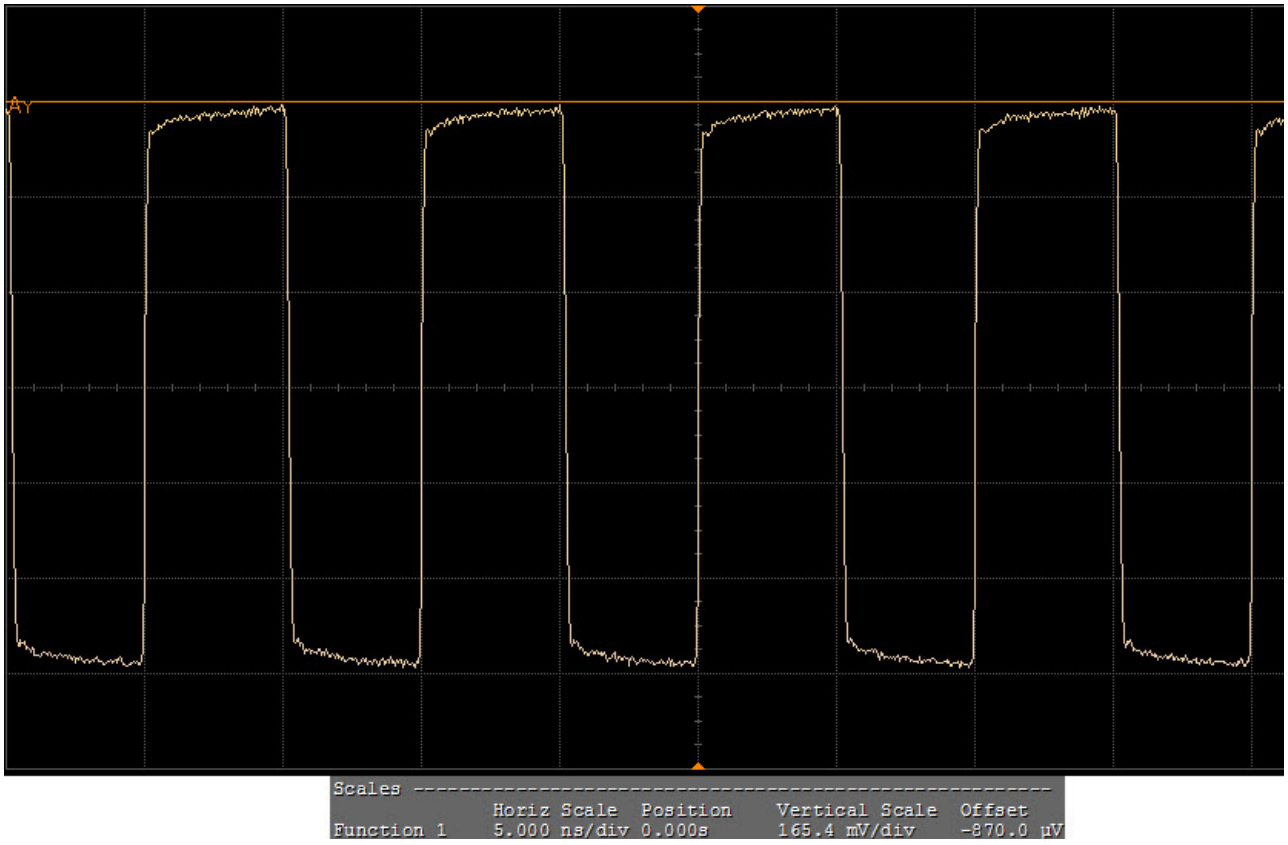


Figure 9 Reference Image for Differential Input High Voltage Test

Differential Input Low Voltage Test

The differential input low voltage test verifies that the reference clock differential input low voltage is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{IL}	Differential Input High Voltage	-150 mV

Test Definition Notes from the Specification

- Measurement taken from differential waveform.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1. Gets the reference clock signal.
2. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
3. Fits and displays all sample data on screen.
4. Configures the **Top Level** threshold to 150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.
5. Measures the minimum voltage using **V min** measurement.
6. Reports the minimum voltage value as differential input low voltage and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 1.1 as $V_{IL} < 150$ mV.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

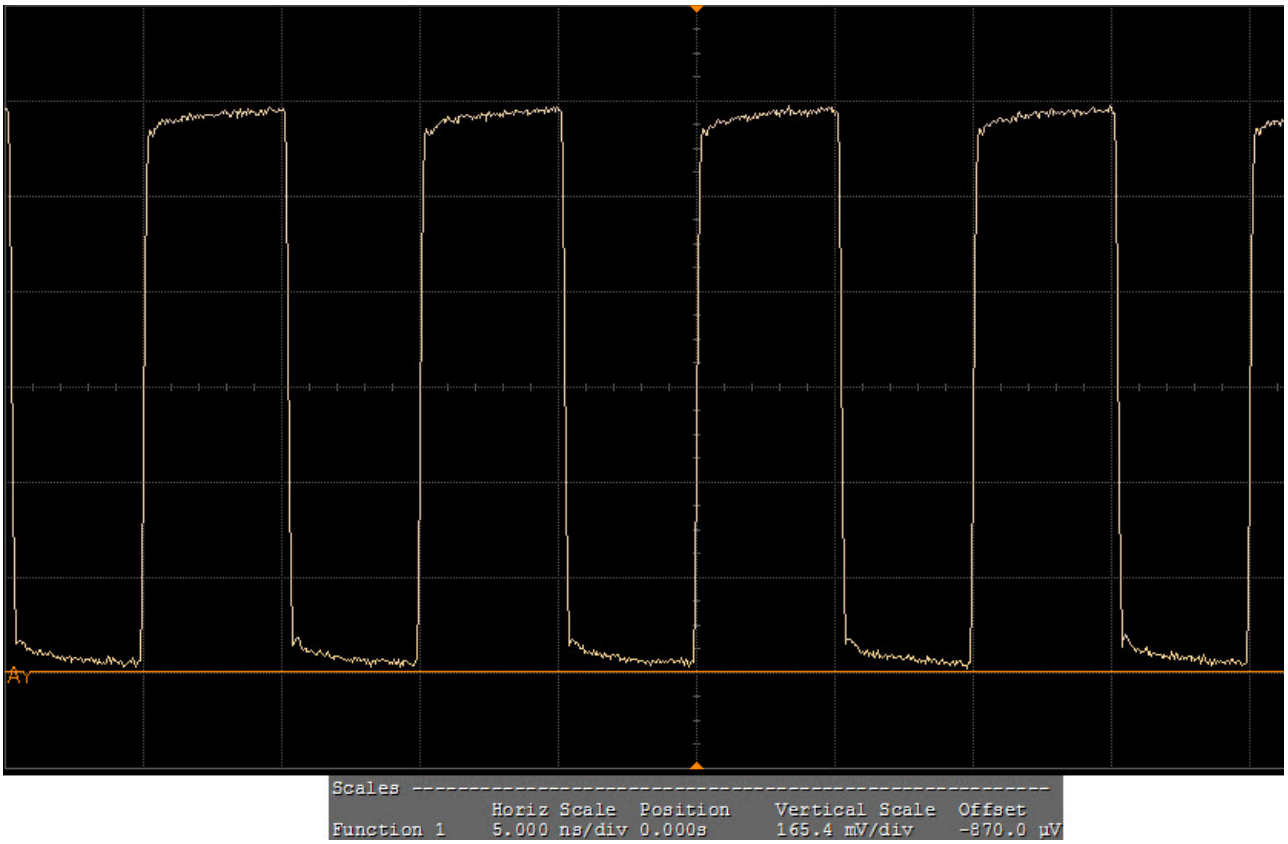


Figure 10 Reference Image for Differential Input Low Voltage Test

Absolute Crossing Point Voltage Test

The absolute crossing point voltage test is measured at crossing point where the instantaneous voltage value of the rising edge of RefClk+ equals the falling edge of RefClk-. It refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Test Definition Notes from the Specification

Table 1 Absolute Crossing Point Voltage Test Details

Symbol	Parameter	Min(at 100 MHz Input)	Max (at 100 MHz Input)
V_{CROSS}	Absolute Crossing Point Voltage	+250 mV	+550 mV

- Measurement taken from single ended waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 8-65.
- Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 8-65.

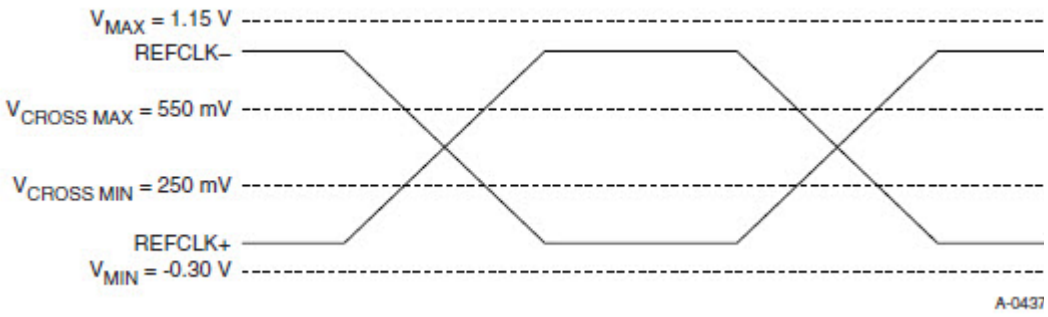


Figure 11 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in section 4.2.10 of the PCI Express Base Specification.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Fits and displays all sample data on screen.

3 Uses MATLAB function to find the absolute crossing point voltage. The MATLAB function does the following:

   a Finds crossing edges for rising and falling edges.

   b Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk-.

4 Computes the margin for minimum crossing point voltage and margin of maximum crossing point voltage.

5 Compares the margin and choose the smallest margin to report the value (worst value) as absolute crossing point voltage.

6 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as `250mV ≤ Absolute Crossing Point Voltage ≤ 550mV`.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Variation of V_{Cross} Test

The variation of V_{Cross} test is measured at crossing point where the instantaneous voltage value of the rising edge of Refclk+ equals the falling edge of Refclk-. It is defined as the total variation of all voltages of rising Refclk+ and falling Refclk-.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{CROSS} Delta	Variation of V_{CROSS} over all rising clock edges	+140 mV

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 8-65.
- Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 8-66.

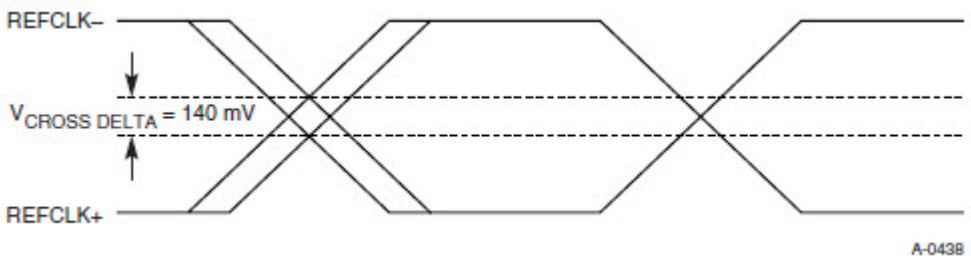


Figure 12 Single-Ended Measurement Points for Delta Cross Point

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Fits and displays all sample data on screen.

2 Uses MATLAB function to find the variation of V_{CROSS}. The MATLAB function does the following:

a Finds crossing edges for rising and falling edges.

b Finds delta crossing for rising edge of RefClk+ and falling edge of RefClk-.

3 Finds the differential value between maximum crossing rising edge and minimum crossing rising edge as variation of V_{Cross}.

4 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as variation of $V_{Cross} < 140\ mV$.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Max Input Voltage Test

The absolute max input voltage test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{MAX}	Absolute Max Input Voltage	+1.15V

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Defined as the maximum instantaneous voltage including overshoot. See Figure 8-65.

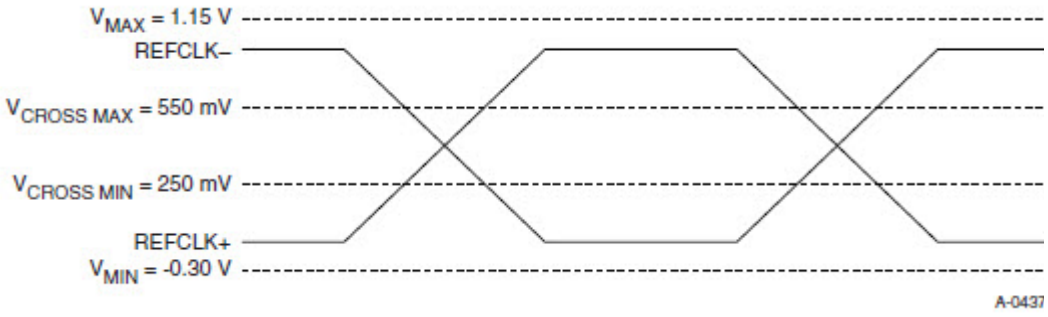


Figure 13 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures memory depth and sampling rate as per the data rate.
3 Fits and displays all sample data on screen.
4 Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.
5 Measures the RefClk+ maximum voltage using **V max** measurement.
6 Measures the RefClk- maximum voltage using **V max** measurement.
7 Compares the RefClk+ maximum voltage and the RefClk- maximum voltage.
8 Reports the largest value (worst value) as the Absolute Max Input Voltage.
9 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as variation of $V_{MAX} < +1.15V$.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

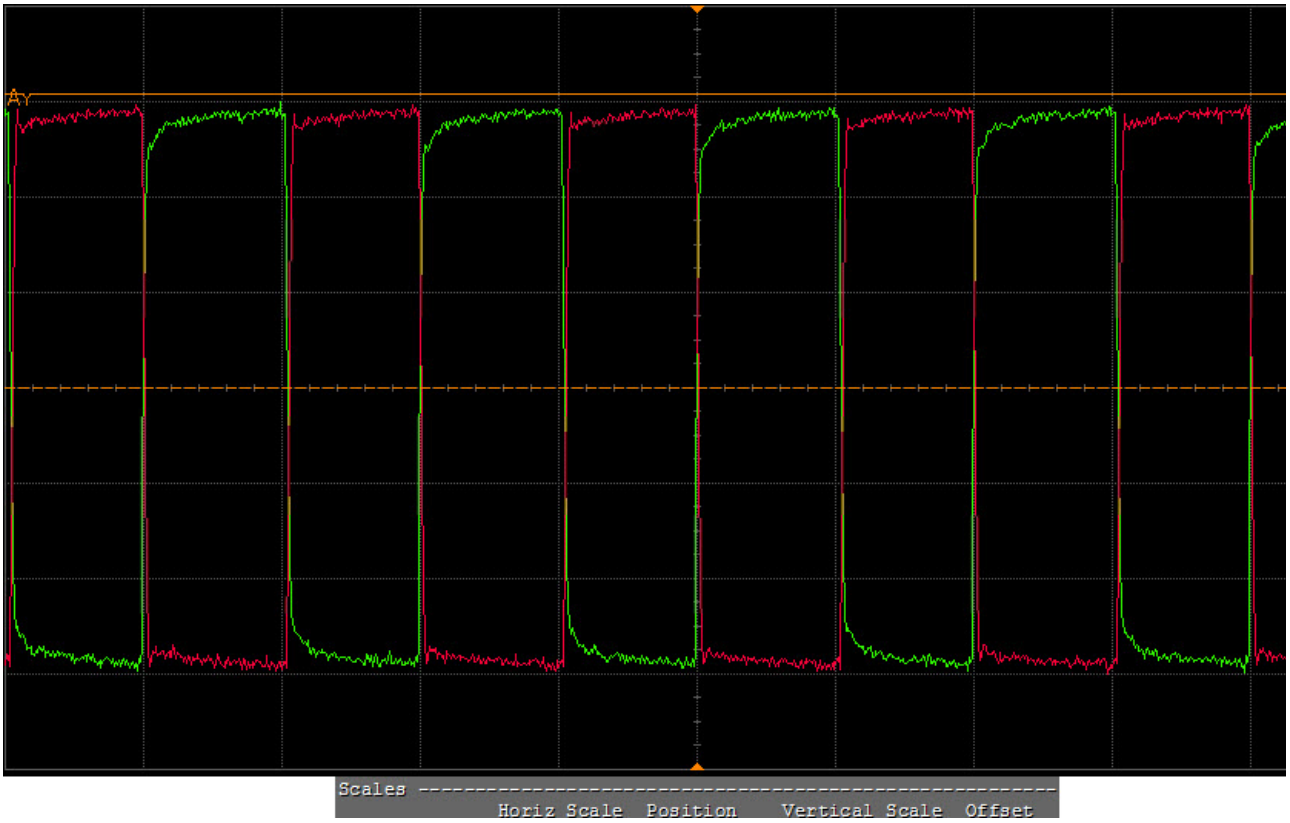


Figure 14 Reference Image for Absolute Max Input Voltage Test

Absolute Min Input Voltage Test

The absolute min input voltage test verifies that the reference clock average clock period is within the conformance limits specified in PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
V_{MIN}	Absolute Min Input Voltage	-0.3 V

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Defined as the minimum instantaneous voltage including undershoot. See Figure 8-65.

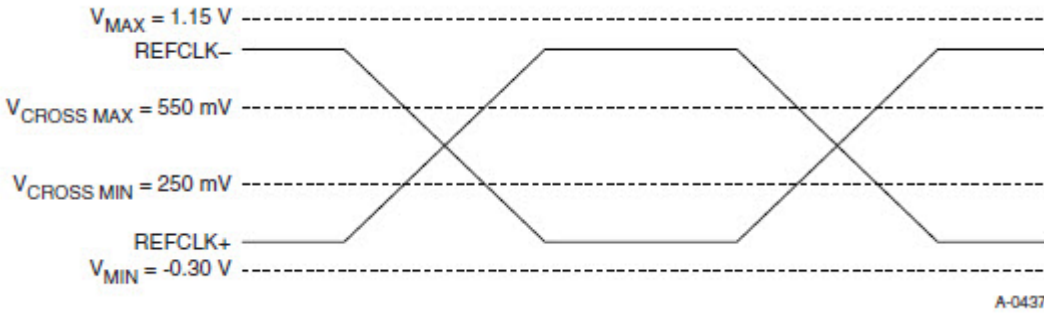


Figure 15 Single-Ended Measurement Points for Absolute Cross Point and Swing

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Configures memory depth and sampling rate as per the data rate.
3 Fits and displays all sample data on screen.
4 Turns on the **Measurement Analysis (EZJIT)** and checks **Measure All Edges**.
5 Measures the RefClk+ minimum voltage using **V min** measurement.
6 Measures the RefClk- minimum voltage using **V min** measurement.
7 Compares the RefClk+ minimum voltage and the RefClk- minimum voltage.
8 Reports the smallest value (worst value) as the Absolute Min Input Voltage.
9 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as variation of $V_{MIN} < -0.3V$.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

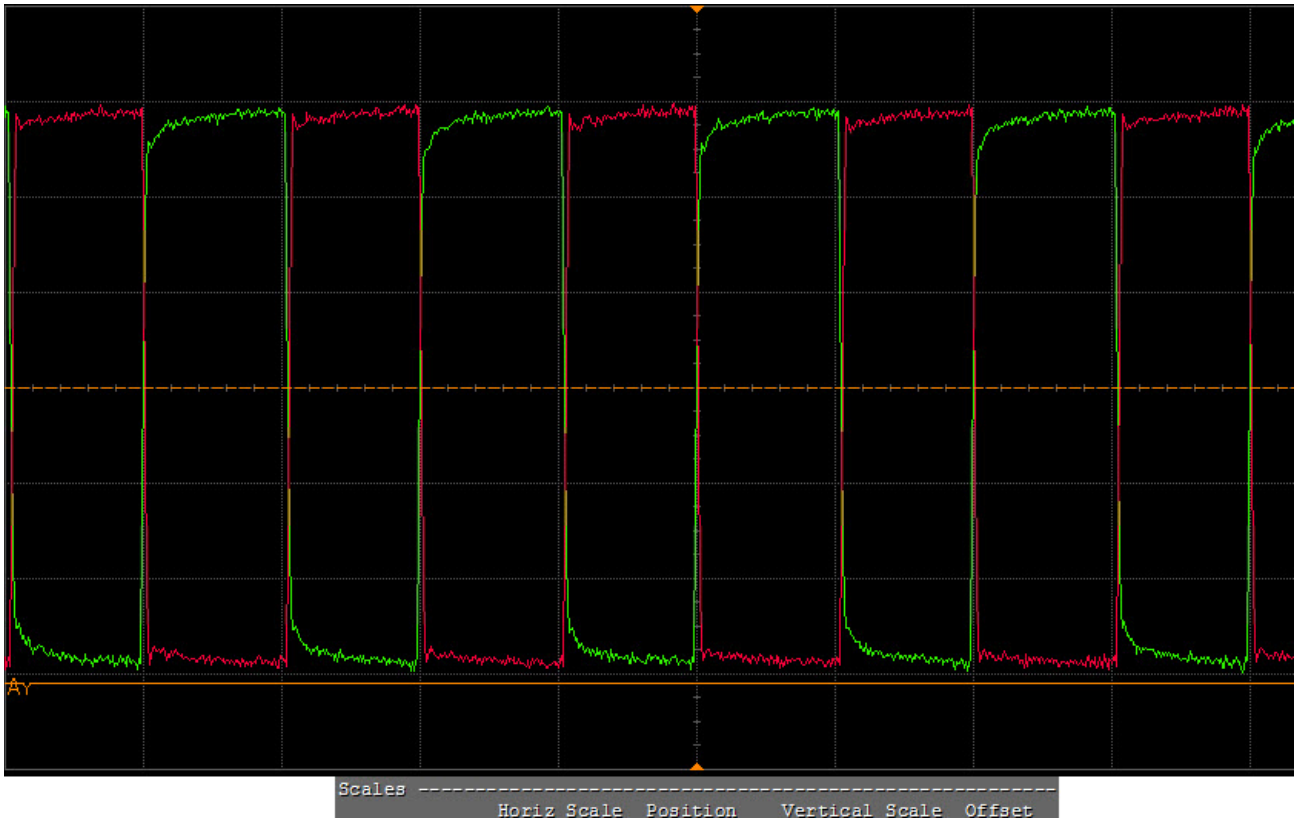


Figure 16 Reference Image for Absolute Min Input Voltage Test

Rise-Fall Matching Test

The rise-fall matching test matching applies to rising edge rate for RefClk+ and falling edge rate for RefClk-. It is measured using +/-75 mV window centered on the median cross point where RefClk+ rising meets RefClk- falling. The median cross point is used to calculate the voltage thresholds and oscilloscope is used to calculate the edge rate calculations. The rise edge rate of RefClk+ should be compared to the fall edge rate of RefClk-, the maximum allowed difference should not exceed 20% of the slowest edge rate.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 is used as reference to check the compliance of the DUT.

Symbol	Parameter	Max (at 100 MHz Input)
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching	20%

Test Definition Notes from the Specification

- Measurement taken from single ended waveform.
- Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 8-67.

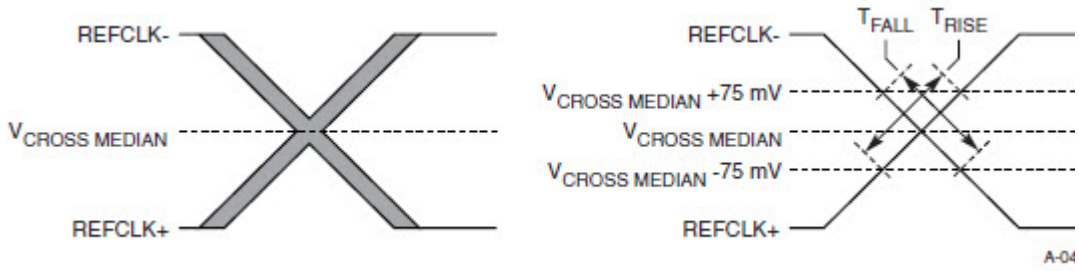


Figure 17 Single-Ended Measurement Points for Rise and Fall Time Matching

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures memory depth and sampling rate as per the data rate.
2 Fits and displays all sample data on screen.
3 Sets the Middle Threshold by ([maximum crossing rising edge value +minimum crossing rising edge value] / 2).
4 Sets the **Upper Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** + 75mV].
5 Sets the **Lower Level** of **Custom Thresholds** as **Middle Level** of **Custom Thresholds** - 75mV].
6 Measures RefClk+ rise time using **Rise time** measurement.
7 Measures the RefClk- fall time using **Fall time** measurement.
8 Finds the slowest edge between RefClk+ rise time and RefClk- fall time.
9 Computes the Rise-Fall matching value as follows:

$$\text{.Rise-Fall Matching} = \frac{Abs|\text{RefClk+ rise time} - \text{RefClk- fall time}|}{\text{Slowest Edge Value} \times 100}$$

10 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 as variation of `Rise-Fall Matching < 20%.`

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

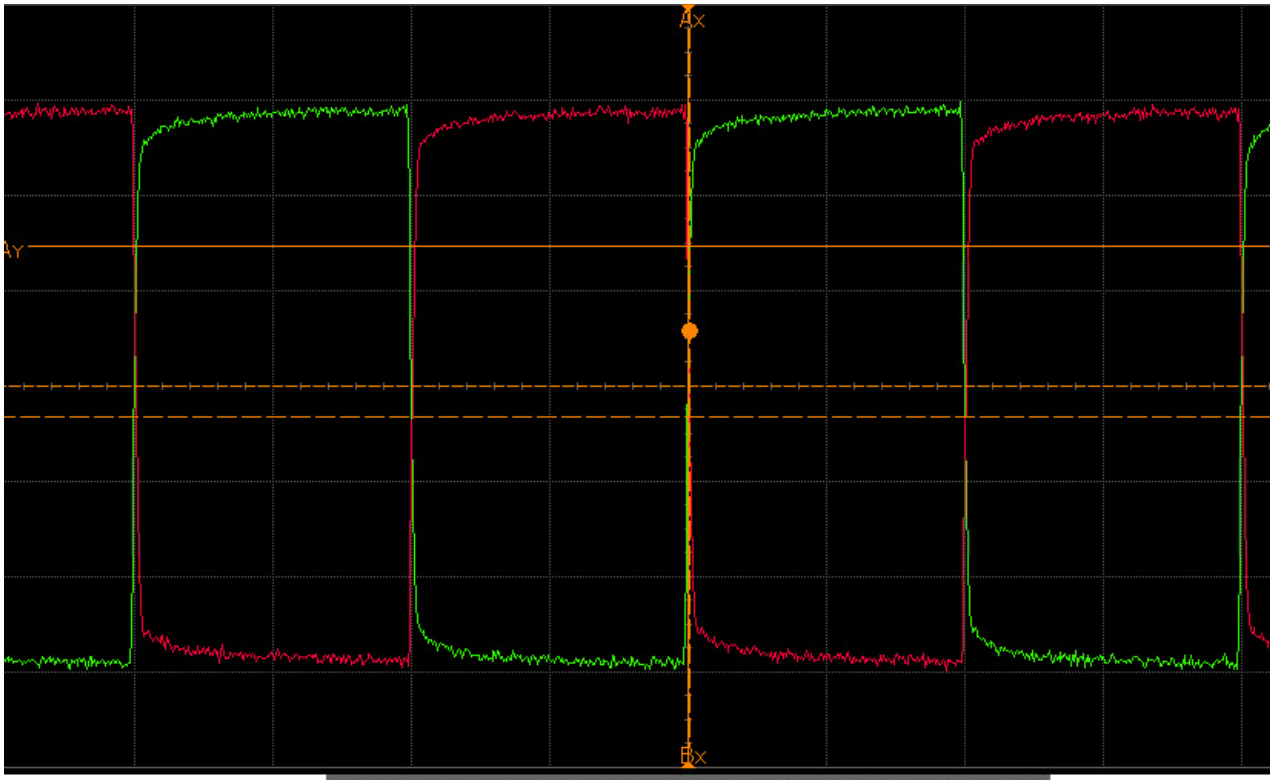


Figure 18 Reference Image for Rise-Fall Matching

RefClk SSC Frequency Range Test

This test verifies that the measured reference clock frequency is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters).

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 2 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal frequency is ~ 100 MHz.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Period** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RefClk SSC Deviation Test

This test verifies that the measured reference clock SSC deviation is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters).

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 3 SSC Deviation Test Details

Symbol	Description	Min/Max
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	-0.5 /0.0%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal frequency is ~ 100 MHz.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Period** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min, and Period_average.
9 Computes SSC deviation Max(%) = ((1 / 100MHz) - SSC's Minimum UI) / (1 / 100MHz) * 100
10 Computes SSC deviation Min(%) = ((1 / 100MHz) - SSC's Maximum UI) / (1 / 100MHz) * 100
11 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

RefClk Max SSC df/dt (Slew Rate) Test

This test verifies that the reference clock maximum SSC df/dt is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 4 RefClk Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$	Max SSC df/dt	1250 ppm/µs

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1^{st} order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures memory depth and sampling rate as per the data rate.

3 Fits and displays all sample data on screen.

4 Analyzes **Period** measurement using the **Measurement Analysis (EZJIT)...** option.

5 Analyzes measurements trend using the jitter **Meas Trend** function.

6 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:

a Generates a differential plot (x_n - x_{n-1}).

b The maximum slew rate corresponds to the peak of the differential plot.

7 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

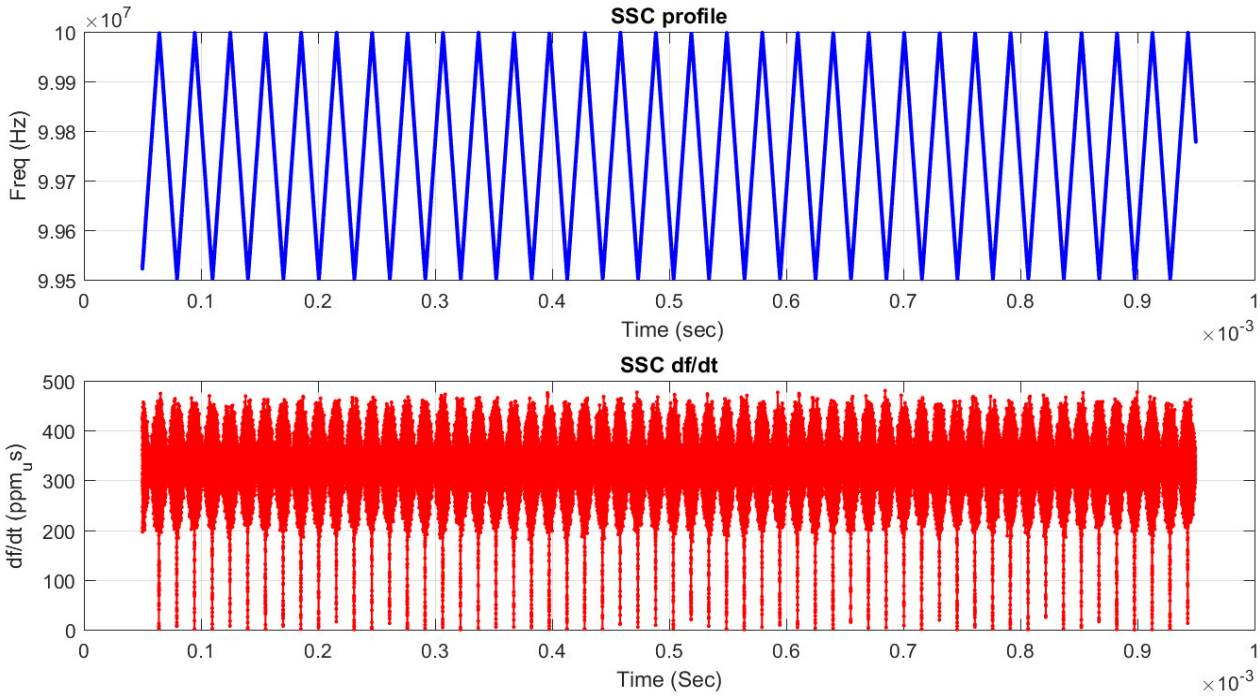


Figure 19 Maximum SSC Slew Rate

Part III
PCI-Express Gen5 2.5 GT/s Tests

KEYSIGHT TECHNOLOGIES

4 Transmitter (Tx) Tests, 2.5 GT/s, PCI-E 5.0

Tx Compliance Test Load / 64
Running Tx Tests / 65

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 2.5 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

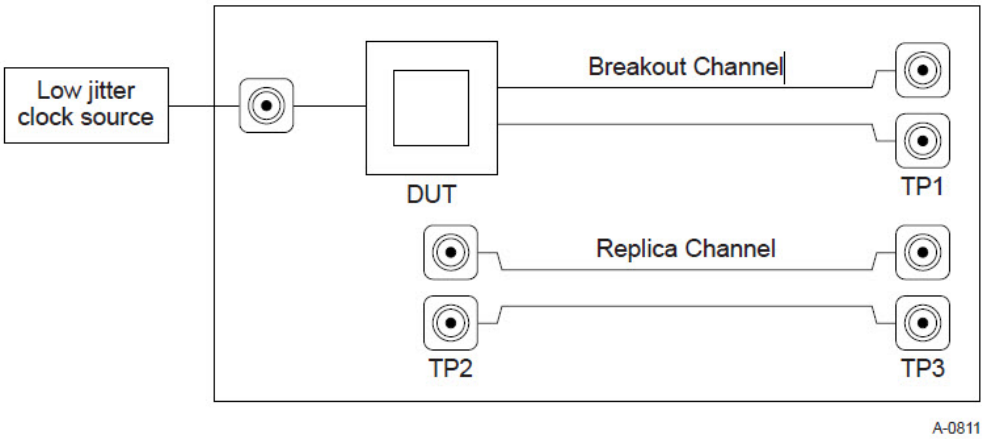


Figure 20 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. In the **Select Tests** tab, navigate to **All PCI Express Gen 5 Tests** > **2.5 GT/s Tests** > **Transmitter (Tx) Tests**.

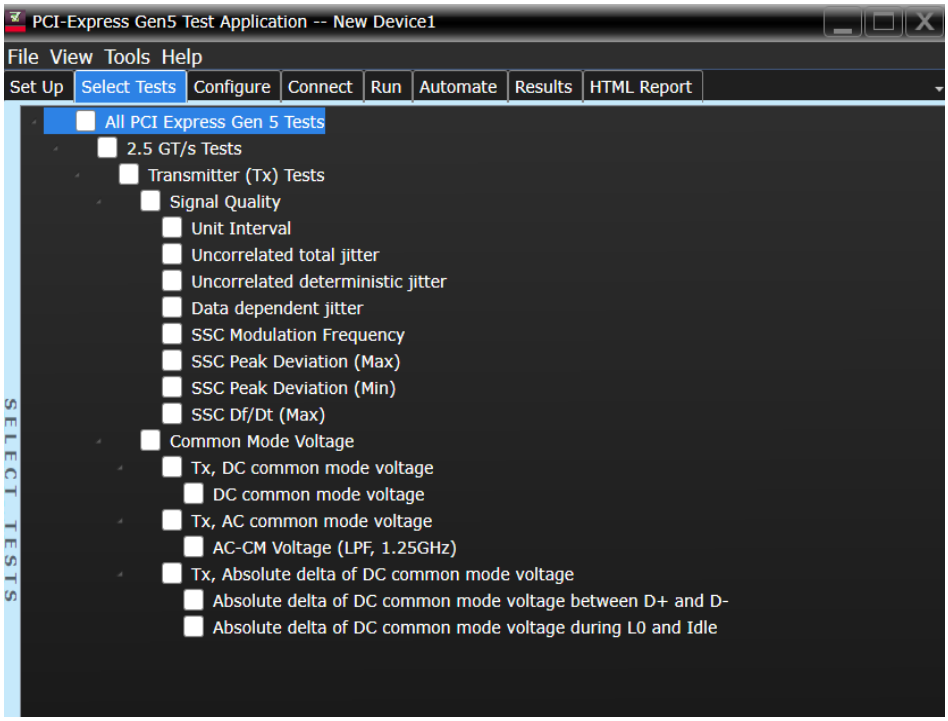


Figure 21 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 5 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	399.88 ps	400.12 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

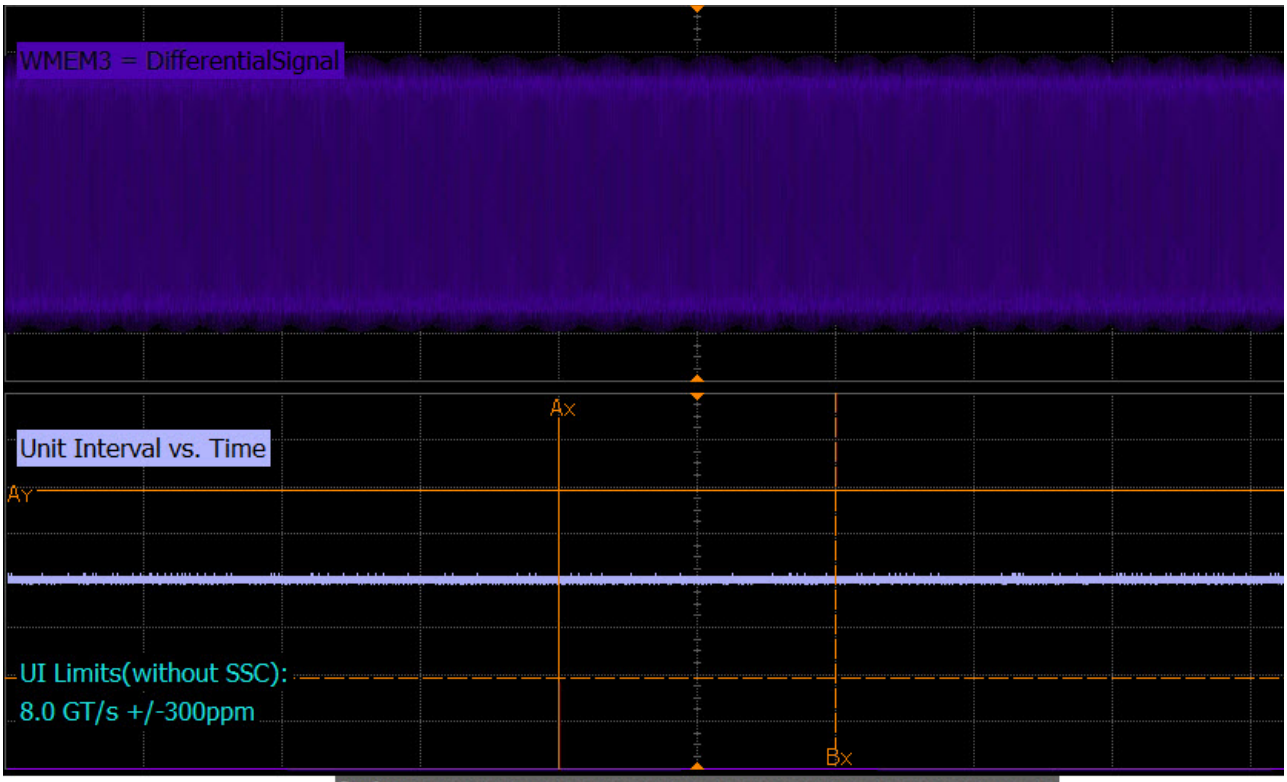
The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean, and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 3	20.00 µs/div	0.000s	20.00 fs/div	125.0 ps
Memory 3	20.00 µs/div	0.000s	191.3 mV/div	6.566 mV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers

	Source	X Position	Y Position
A	Function 3	-19.9999999890000 µs	100 pV
B	Function 3	19.9999999890000 µs	100 pV

Figure 22 Reference Image for Unit Interval Test

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 6 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	100.00 ps PP at 10^{-12}

Test Definition Notes from the Specification

- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.
- See Section 8.3.5.8 (Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) (T_{TX-UTJ} and $T_{TX-UDJDD}$)) of the PCI Express Base Specification, Revision 5.0 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX\text{-}UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 7 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX\text{-}UDJDD}$	Tx uncorrelated deterministic jitter	100 ps PP

Test Definition Notes from the Specification

- See Section 8.3.5.8 (Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) ($T_{TX\text{-}UTJ}$ and $T_{TX\text{-}UDJDD}$)) of the PCI Express Base Specification, Rev 5.0 for details.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter (Information-Only Test)

This test verifies that the maximum data dependent jitter, $T_{TX\text{-}DDJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.5.7 (Data Dependent Jitter) is used as reference.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 8 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground. See also the $I_{TX\text{-}SHORT}$.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate, and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Sets up DC common mode voltage as follows:
   a Enables and displays common mode measurements.
   b Loads common mode signal to waveform memory.
   c Loads and enhance dynamic range D+ signal and D- signal.
   d Enables the average common mode measurement.
   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).
4 Measures the average value of D+ and D- signal.
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0 as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

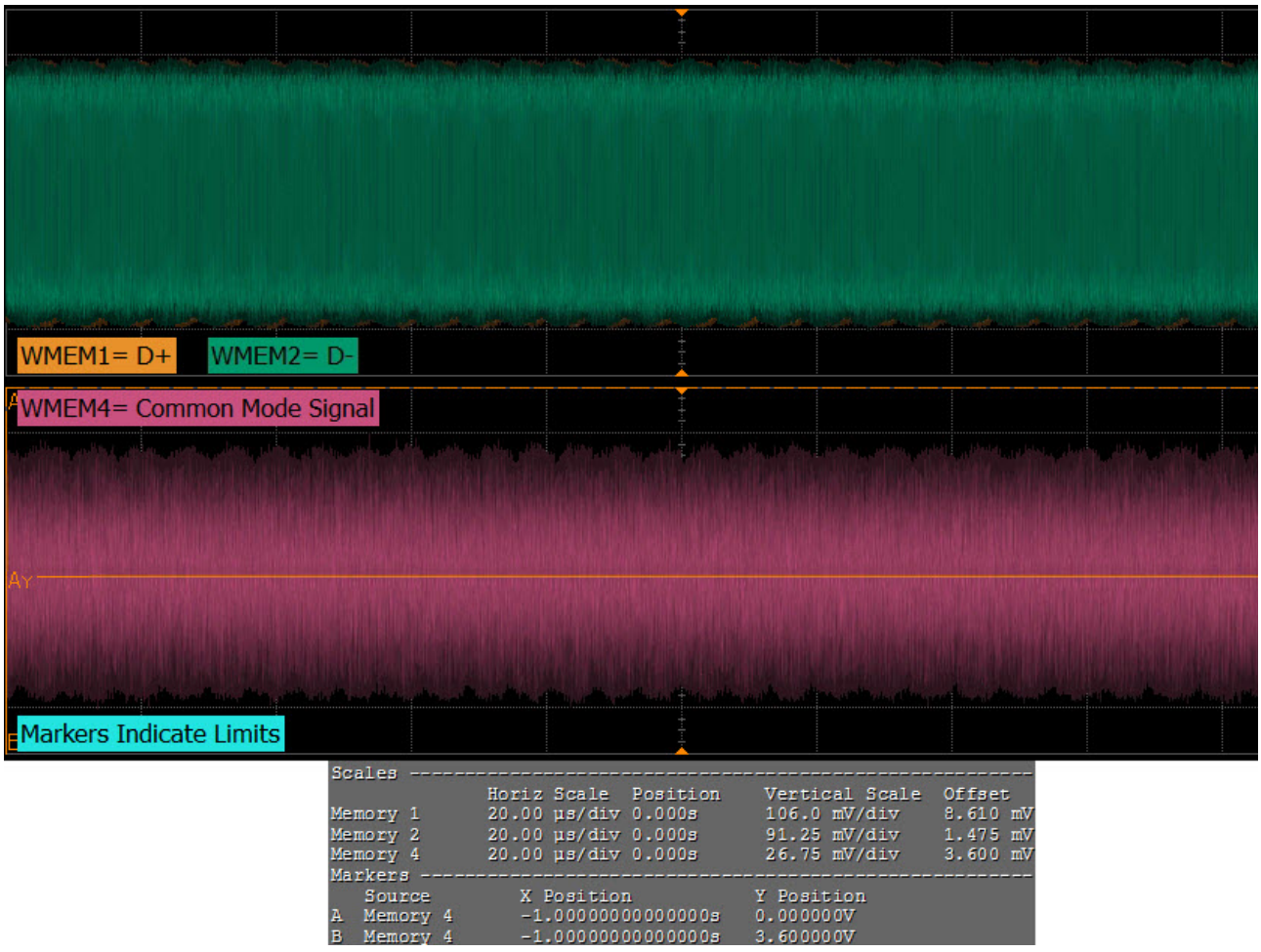


Figure 23 Reference Image for DC Common Mode Voltage Test

AC Common-Mode Voltage (LPF, 1.25 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 9 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-AC-CM-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $VT_{X-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 1.25 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

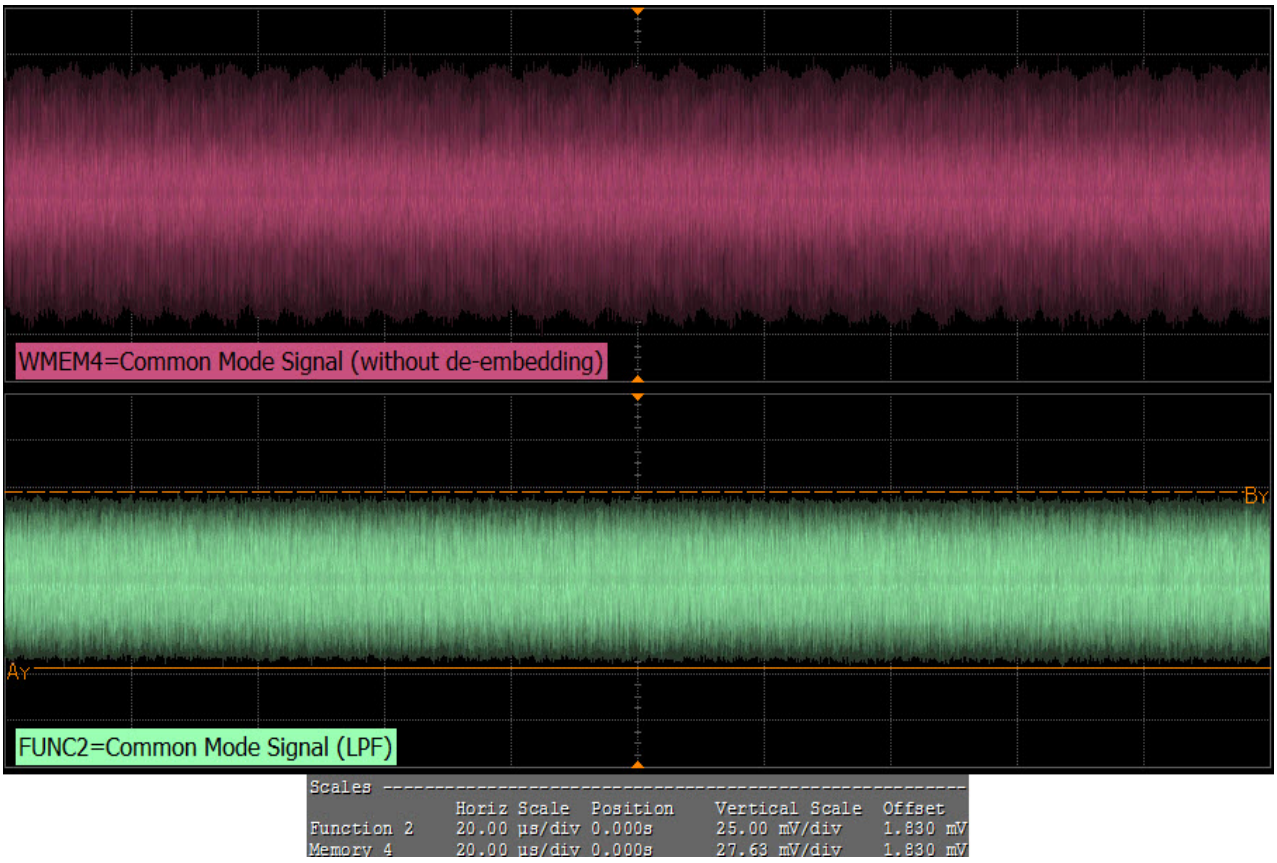


Figure 24 Reference Image for AC-CM voltage (4GHz LPF) Test

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX-CM-DC-LINE-DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX-CM-DC-D+[during\ L0]} - V_{TX-CM-DC-D-[during\ L0]}| \leq 25\ mV$

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $|V_{TX-D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 10 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}\ of\ |V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}\ of\ |V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT..

Table 11 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

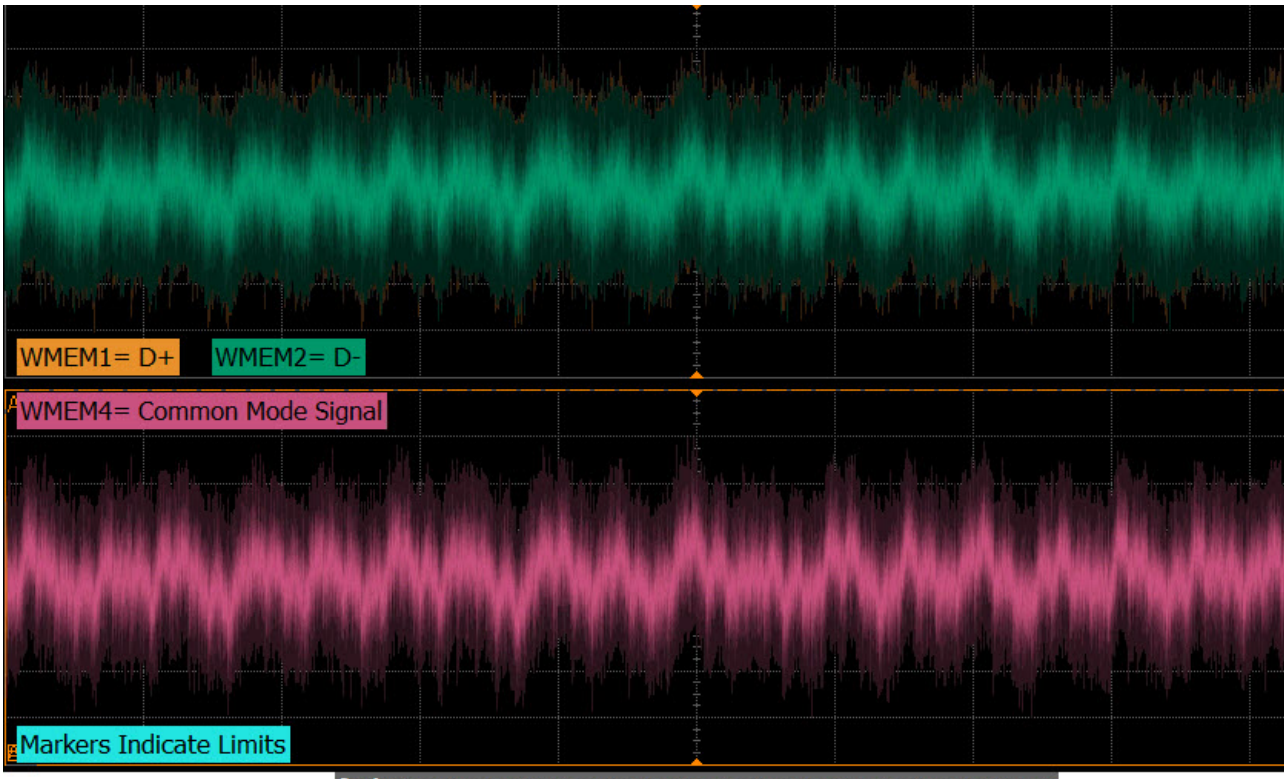
The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	20.00 µs/div	0.000s	787.5 µV/div	2.755 mV
Memory 2	20.00 µs/div	0.000s	762.5 µV/div	8.203 mV
Memory 4	20.00 µs/div	0.000s	582.5 µV/div	5.479 mV

Markers

	Source	X Position	Y Position
A	Memory 4	-1.00000000000000s	0.000000V
B	Memory 4	-1.00000000000000s	3.600000V

Figure 25 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 12 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the data signal.
2 Verifies that the data rate is 2.5 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 13 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	0.0%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 2.5 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option..
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 14 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.5%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 2.5 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 15 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt	1250 ppm/µs

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1^{st} order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures memory depth and sampling rate as per the data rate.

3 Fits and displays all sample data on screen.

4 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.

5 Analyzes measurements trend using the jitter **Meas Trend** function.

6 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:

a Generates a differential plot (x_n - x_{n-1}).

b The maximum slew rate corresponds to the peak of the differential plot.

7 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

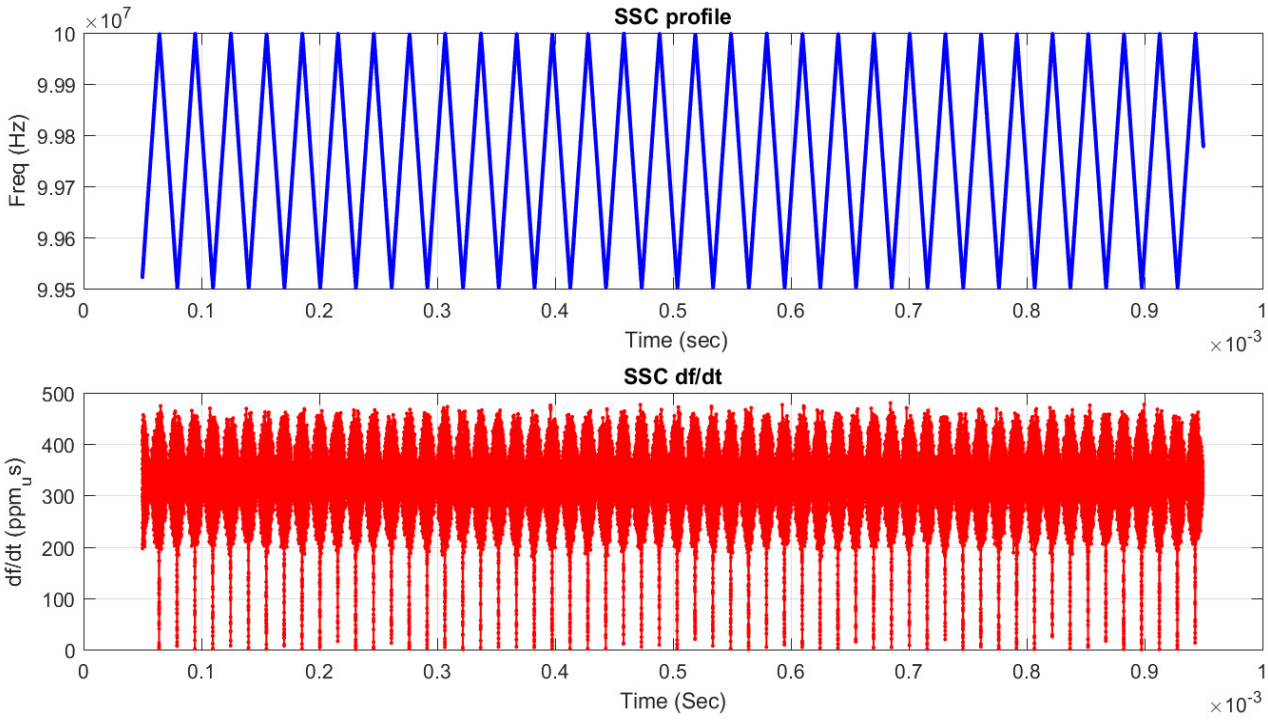


Figure 26 Maximum SSC Slew Rate

5 Reference Clock Tests, 2.5 GT/s, PCI-E 5.0

Reference Clock Architectures / 86
Reference Clock Measurement Point / 88
Running Reference Clock Tests / 89

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 2.5 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

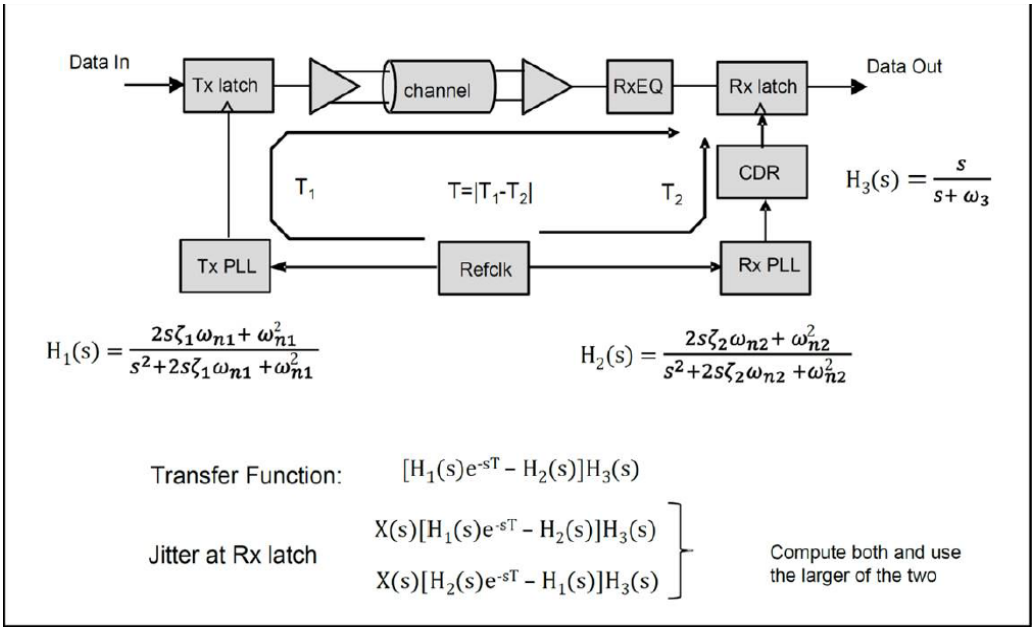
NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 5.0 GT/s, PCI-E 5.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 2.5 GT/s

PLL #1, PLL #2	0.01 dB peaking	3.0 dB peaking
BW_{PLL}(min) = 1.5 MHz	ω_{n1}= .336 Mrad/s ζ_1 = 14	ω_{n1}= 5.09 Mrad/s ζ_1 = 0.54
BW_{PLL}(max) = 22 MHz	ω_{n1}= 4.93 Mrad/s ζ_1 = 14	ω_{n1}= 74.68 Mrad/s ζ_1 = 0.54

BW_{CDR}(min) = 1.5 MHz, 1st order — CDR

16 combinations

2.5 GT/s

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73	BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73	BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15

BW_{CDR}(min) = 10 MHz, 1st order

64 combinations

8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.6.1, Figure 8-64.

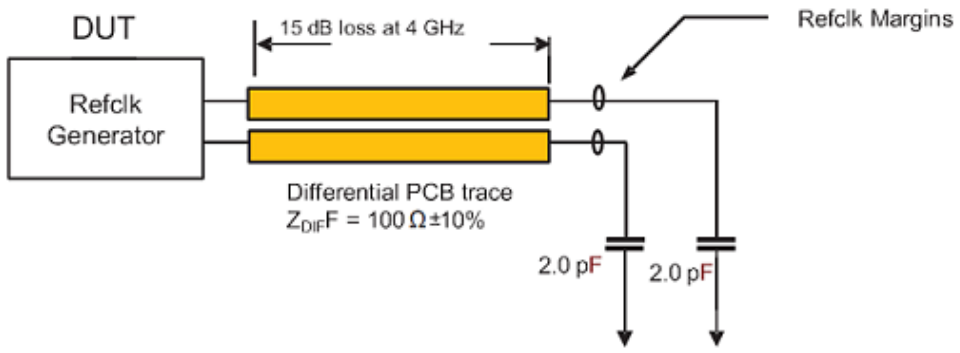


Figure 27 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. Then, when selecting tests, navigate to "Reference Clock Tests" in the "PCIE 4.0 Tests" group.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

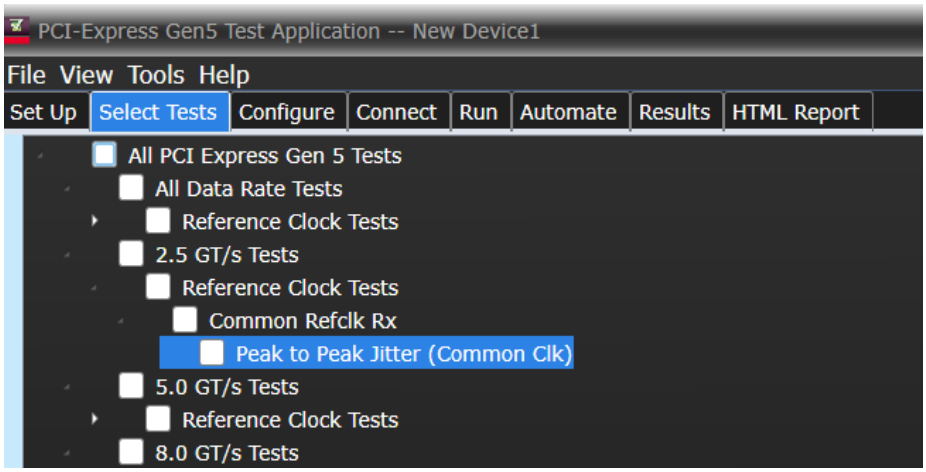


Figure 28 Selecting Reference Clock Tests when SSC or Clean Clock is Selected

Peak to Peak Jitter (Common Clk) Test

This test verifies that the measured peak to peak jitter, $T_{REFCLK-PP-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 16 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-PP-CC}$	Peak to Peak Refclk jitter for common Refclk architecture	86 ps PP

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-73 (Common Refclk Rx Architecture for all Data Rates Except 32.0 GT/s); section 8.6.6 of PCI Express Base Specification Revision 5.0.
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Verifies that the signal period is ~100 MHz.

3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.

4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

5 Configures memory depth and sampling rate as per the data rate.

6 Fits and displays all sample data on the screen.

7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.

8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 Gsa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.

9 Stitches each acquired acquisition to make a continuous TIE data.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies the PLL filter using parameters for common clocked architecture.
   c Converts back the frequency domain TIE data to time domains.
   d Computes the filtered peak-peak jitter.
11 Reports filtered peak-peak jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

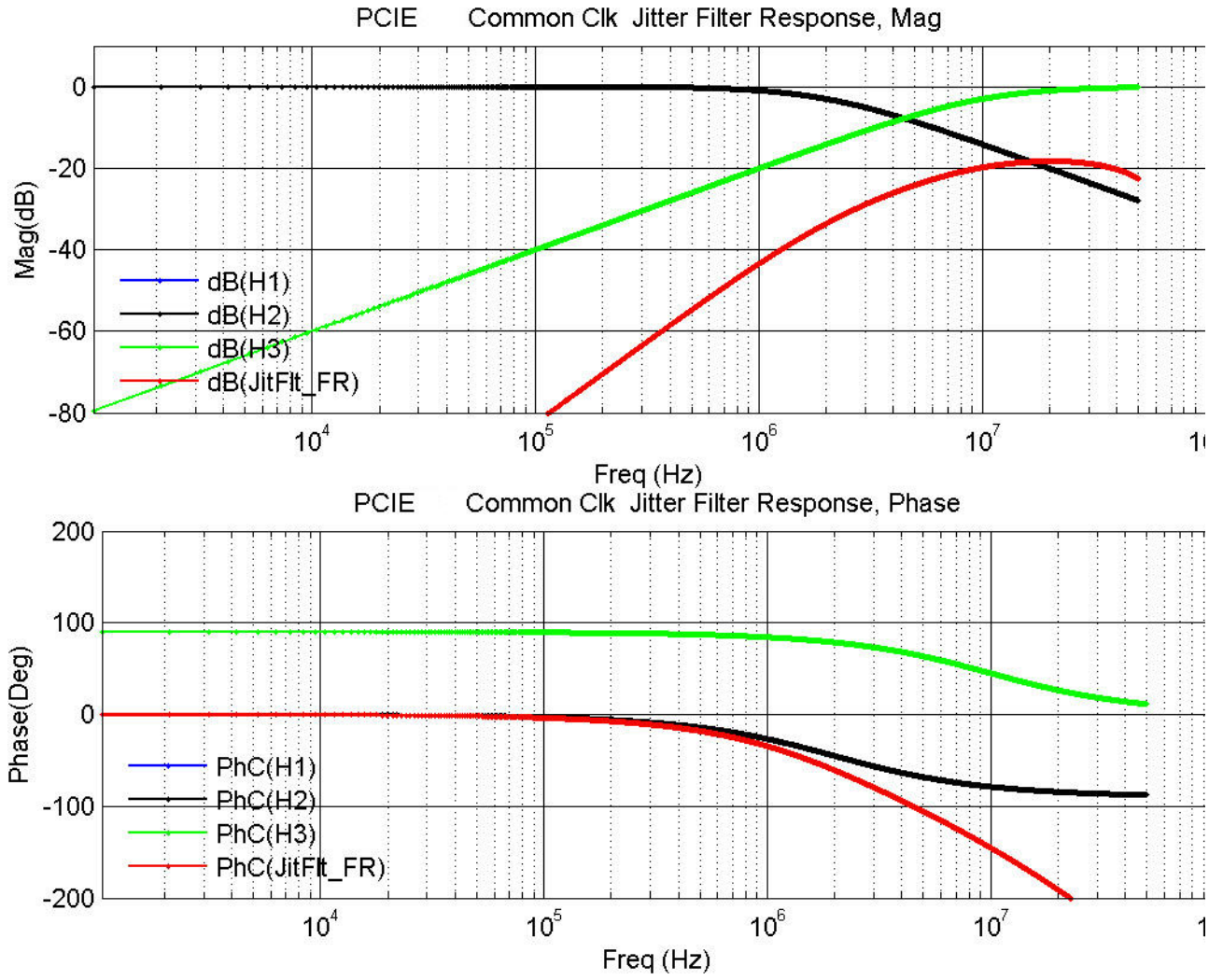


Figure 29 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

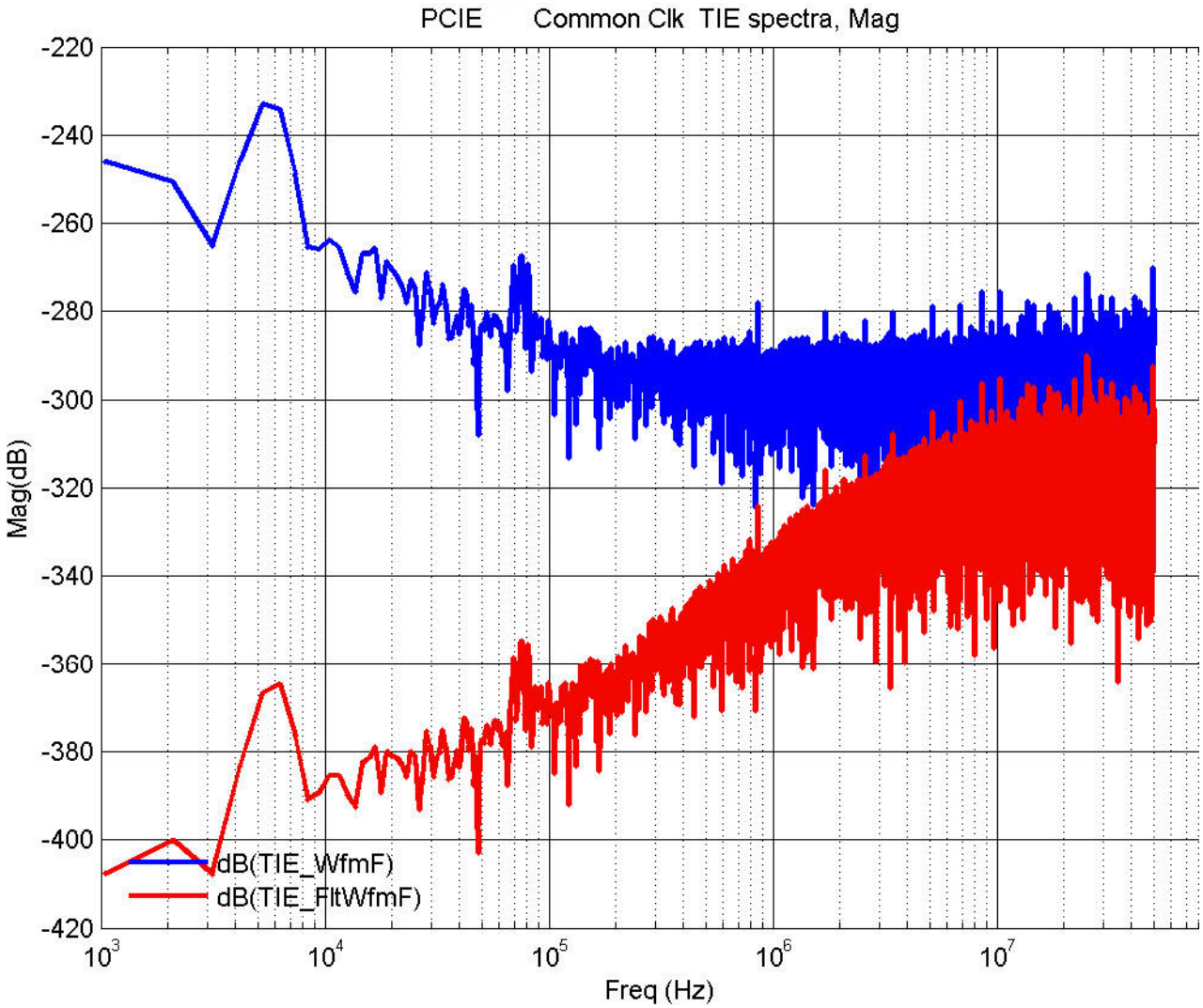


Figure 30 Reference Image for Common Clock TIE Spectra RMS Jitter Test

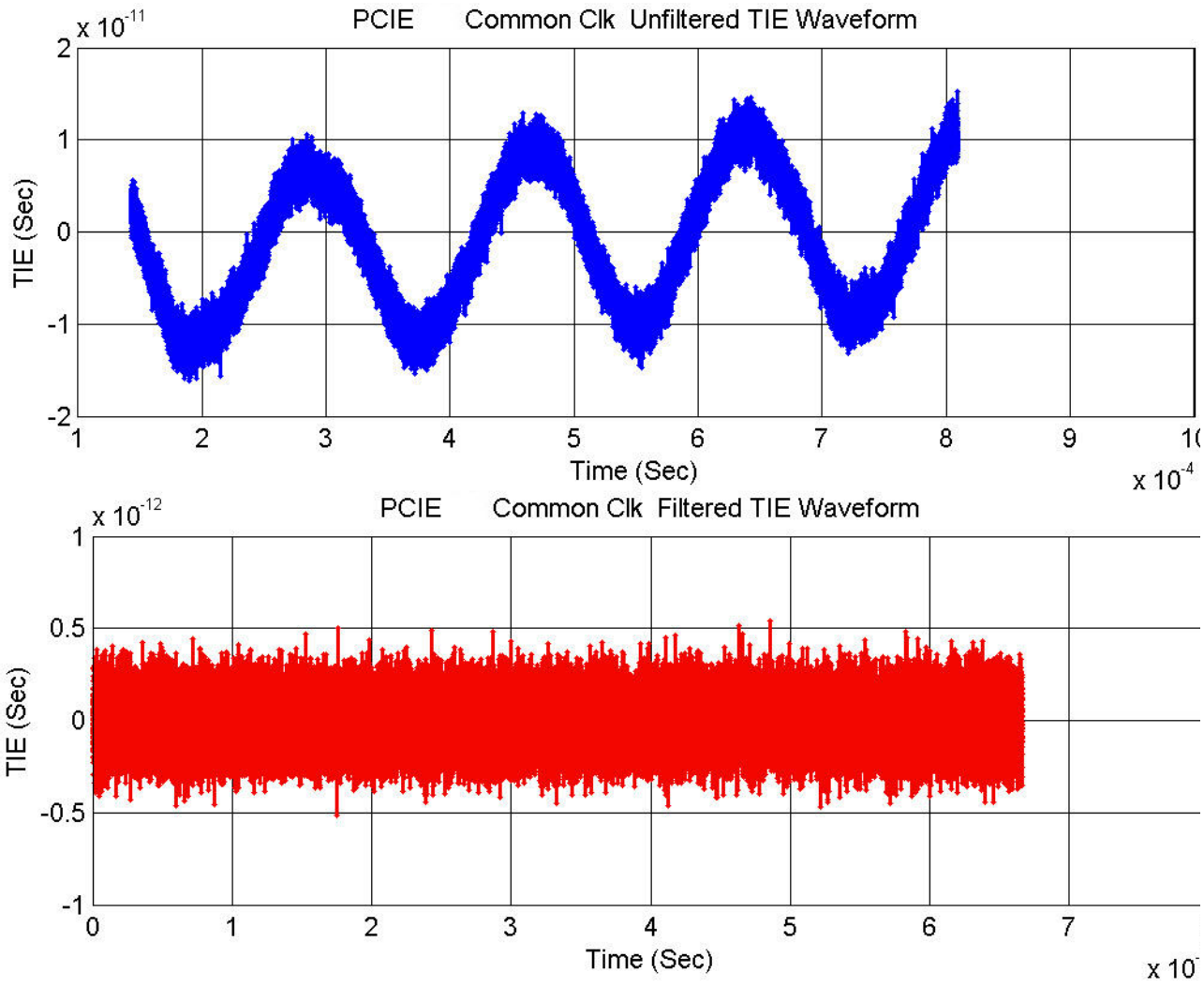


Figure 31 Reference Image for TIE Waveform RMS Jitter Test

Part IV
PCI-Express Gen5
5.0 GT/s Tests

KEYSIGHT
TECHNOLOGIES

6 Transmitter (Tx) Tests, 5.0 GT/s, PCI-E 5.0

Tx Compliance Test Load / 98
Running Tx Tests / 99

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 5.0 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

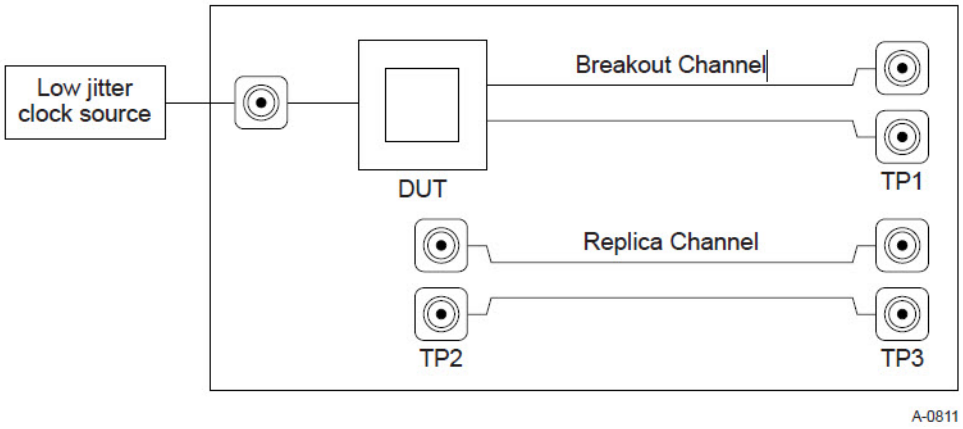


Figure 32 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. In the **Select Tests** tab, navigate to **All PCI Express Gen 5 Tests** > **5.0 GT/s Tests** > **Transmitter (Tx) Tests**.

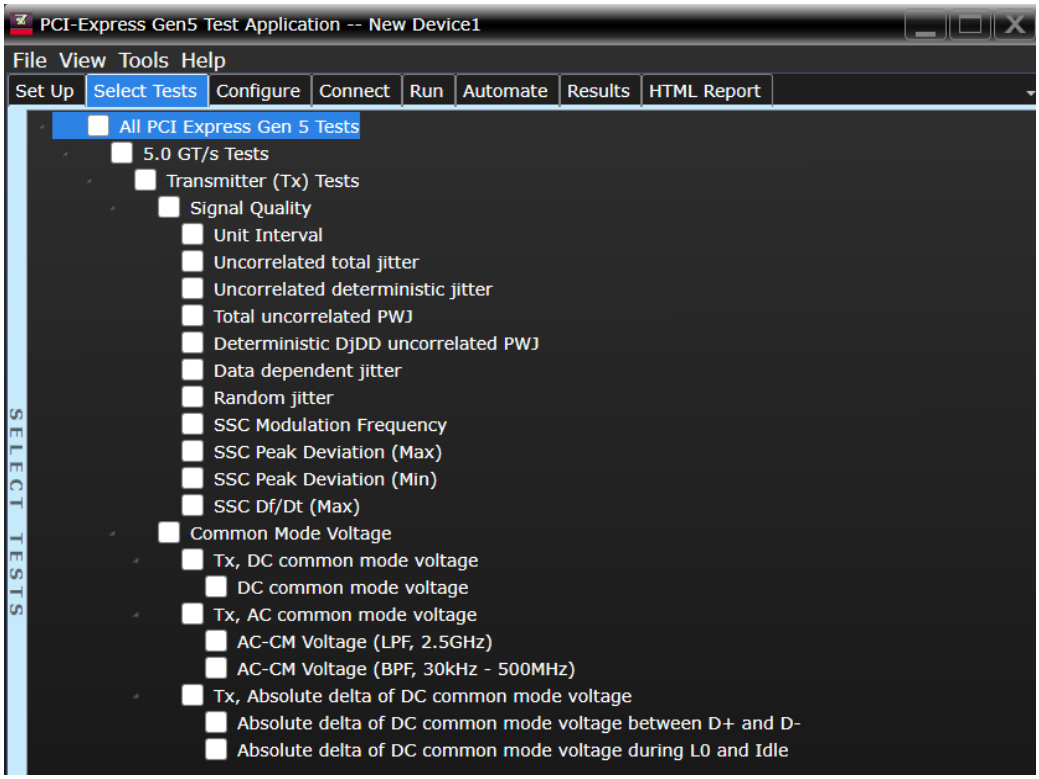


Figure 33 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 17 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	199.94 ps	200.06 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

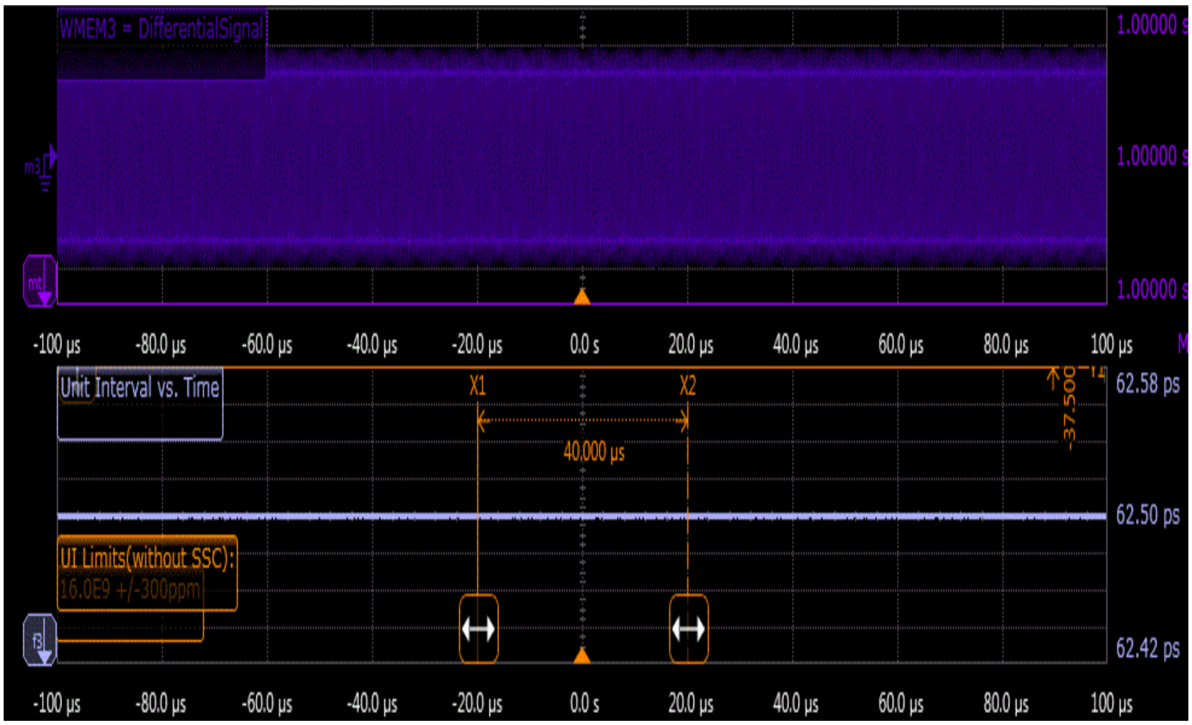


Figure 34 Reference Image for Unit Interval Test

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 18 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	50 ps PP at 10^{-12}

Test Definition Notes from the Specification

- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.
- See PCI Express Base Specification, Revision 5.0, Section 8.3.5.8 (Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) (T_{TX-UTJ} and $T_{TX-UDJDD}$))

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 19 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	30 ps PP

Test Definition Notes from the Specification

- See PCI Express Base Specification, Revision 5.0, Section 8.3.5.8 (Uncorrelated Total Jitter and Deterministic Jitter (Dual Dirac Model) (T_{TX-UTJ} and $T_{TX-UDJDD}$))

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 20 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	40 ps PP at 10^{-12}

Test Definition Notes from the Specification

- See PCI Express Base Specification, Rev 5.0, Section 8.3.5.10 (Uncorrelated Total and Deterministic PWJ ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 21 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	40 ps PP

Test Definition Notes from the Specification

- See PCI Express Base Specification, Rev 5.0, Section 8.3.5.10 (Uncorrelated Total and Deterministic PWJ ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$)

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter (Information-Only Test)

This test verifies that the maximum data dependent jitter, $T_{TX\text{-}DDJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.5.7 (Data Dependent Jitter) is used as reference.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test (Information Only Test)

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT. .

Table 22 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	1.4 - 3.6 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJ-DD}$.
- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 23 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Sets up DC common mode voltage as follows:
   a Enables and displays common mode measurements.
   b Loads common mode signal to waveform memory.
   c Loads and enhance dynamic range D+ signal and D- signal.
   d Enables the average common mode measurement.
   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).
4 Measures the average value of D+ and D- signal.
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0 as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 2.5 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 24 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}AC\text{-}CM\text{-}PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50 mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 2.5 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 25 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	100 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50 mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 2.5 GHz) test.

1 Gets PCIE5 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D-[during\ L0]}| \leq 25\ mV$

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $|V_{TX\text{-}D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 26 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 (Data Rate Independent Tx Parameters) is used as reference to check the compliance of the DUT.

Table 27 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

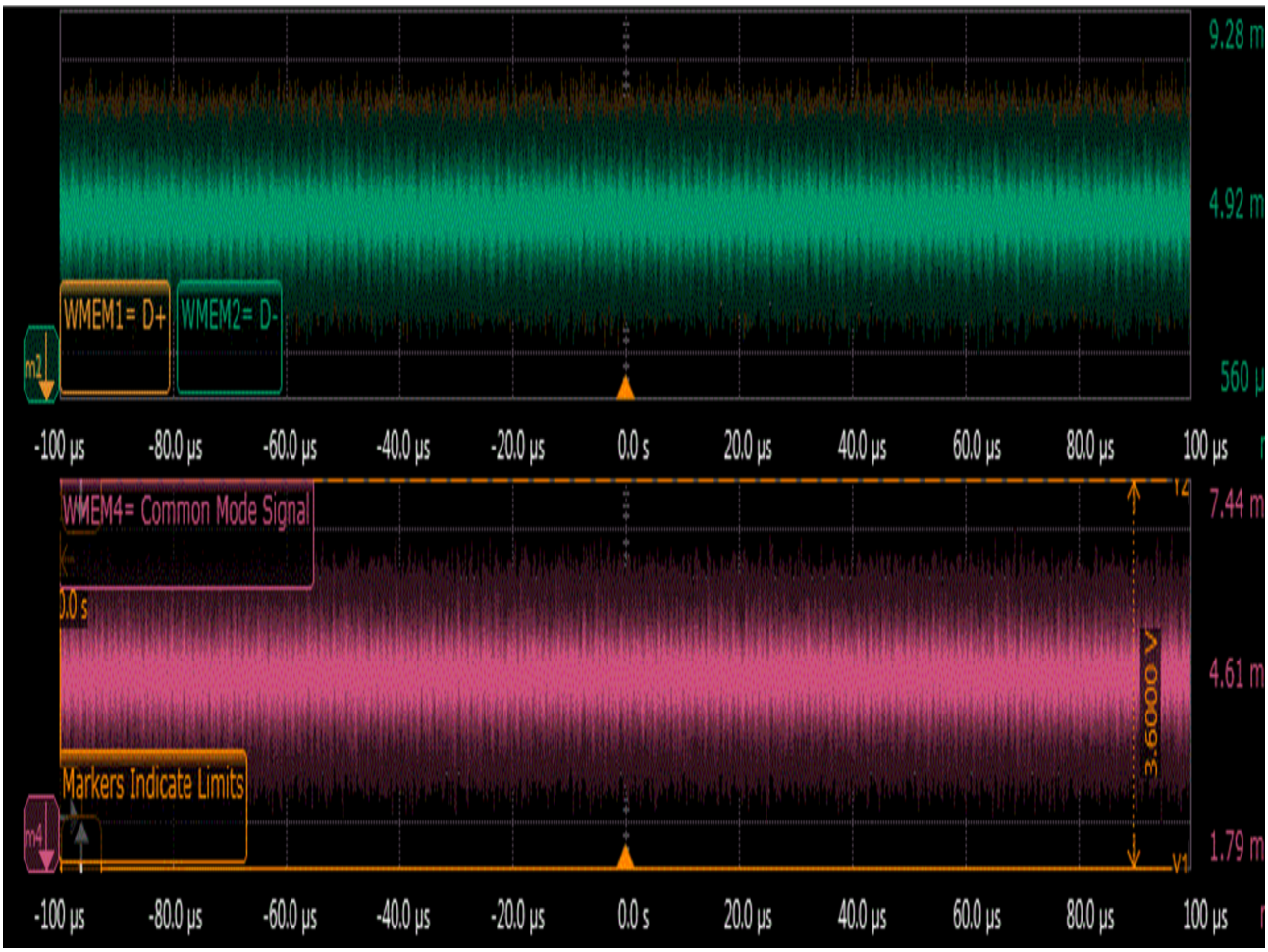


Figure 35 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 28 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 5.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 29 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	0.0%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 5.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 30 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.5%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 5.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 31 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt	1250 ppm/µs

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1^{st} order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures memory depth and sampling rate as per the data rate.

3 Fits and displays all sample data on screen.

4 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.

5 Analyzes measurements trend using the jitter **Meas Trend** function.

6 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:

a Generates a differential plot (x_n - x_{n-1}).

b The maximum slew rate corresponds to the peak of the differential plot.

7 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

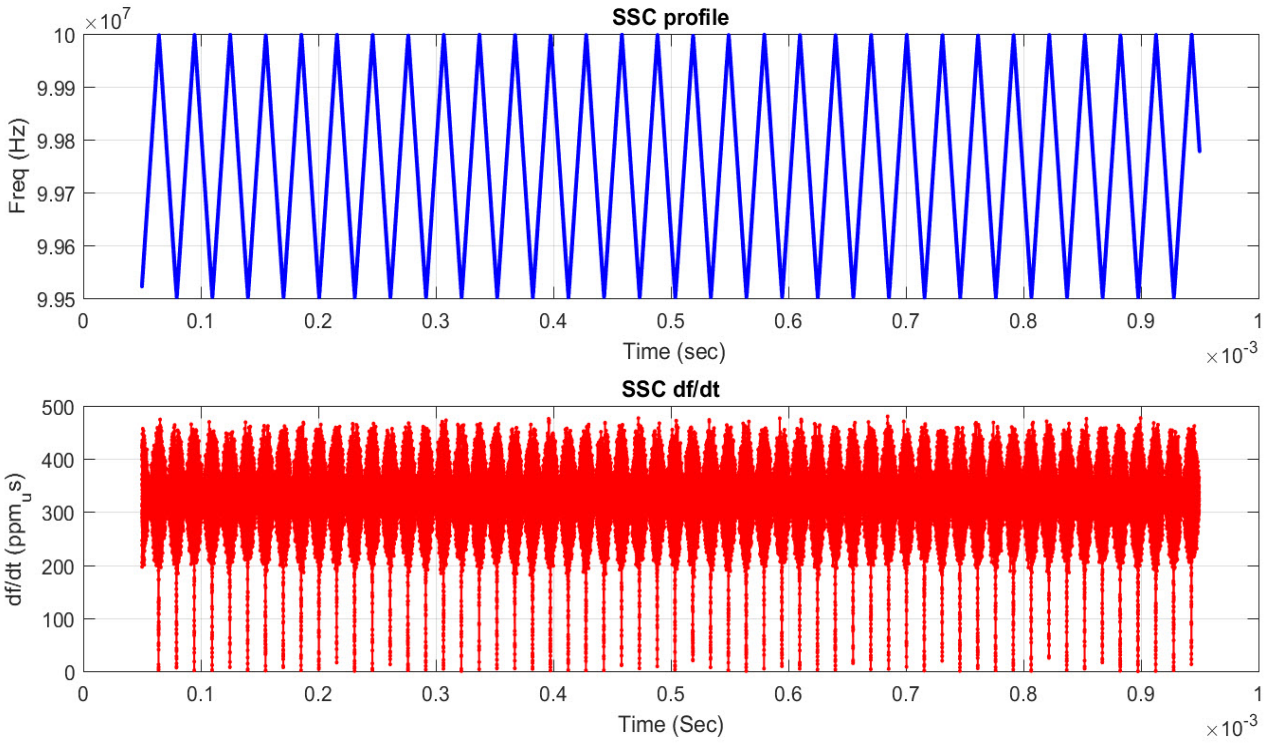


Figure 36 Maximum SSC Slew Rate

7 Reference Clock Tests, 5.0 GT/s, PCI-E 5.0

Reference Clock Architectures / 124
Reference Clock Measurement Point / 126
Running Reference Clock Tests / 127

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 5.0 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

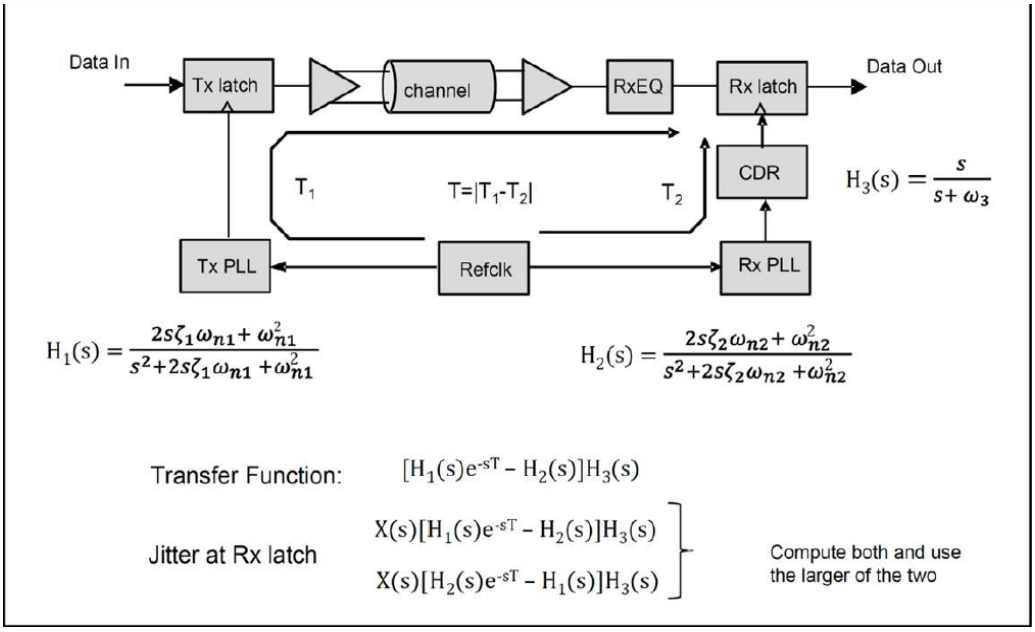
NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 5.0 GT/s, PCI-E 5.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 5 GT/s

PLL #1	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 5.0 MHz	ω_{n1}= 1.12 Mrad/s ζ_1 = 14	ω_{n1}= 11.01 Mrad/s ζ_1 = 1.16
BW_{PLL}(max) = 16 MHz	ω_{n1}= 3.58 Mrad/s ζ_1 = 14	ω_{n1}= 35.26 Mrad/s ζ_1 = 1.16

PLL #2	0.01 dB peaking	3.0 dB peaking
BW_{PLL}(min) = 8.0 MHz	ω_{n2}= 1.79 Mrad/s ζ_2 = 14	ω_{n2}= 26.86 Mrad/s ζ_2 = 0.54
BW_{PLL}(max) = 16 MHz	ω_{n2}= 3.58 Mrad/s ζ_2 = 14	ω_{n2}= 53.73 Mrad/s ζ_2 = 0.54

BW_{CDR}(min) = 5 MHz, 1st order

64 combinations

5 GT/s

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73	BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73	BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15
BW_{CDR}(min) = 10 MHz, 1st order	64 combinations				

8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.6.1, Figure 8-64.

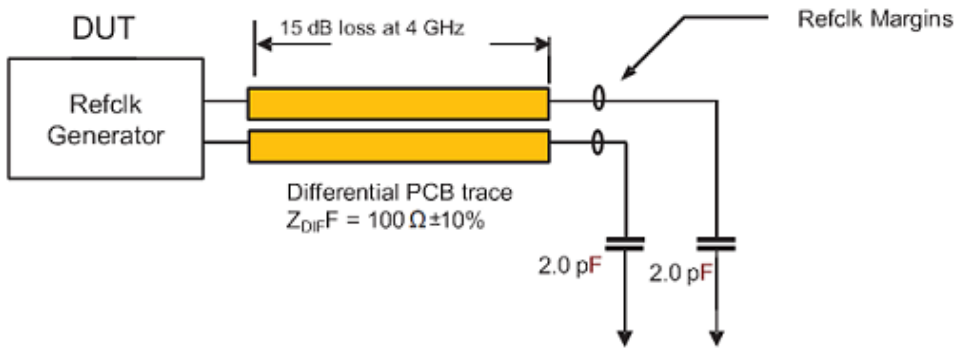


Figure 37 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. Then, when selecting tests, navigate to "Reference Clock Tests" in the "PCIE 4.0 Tests" group.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

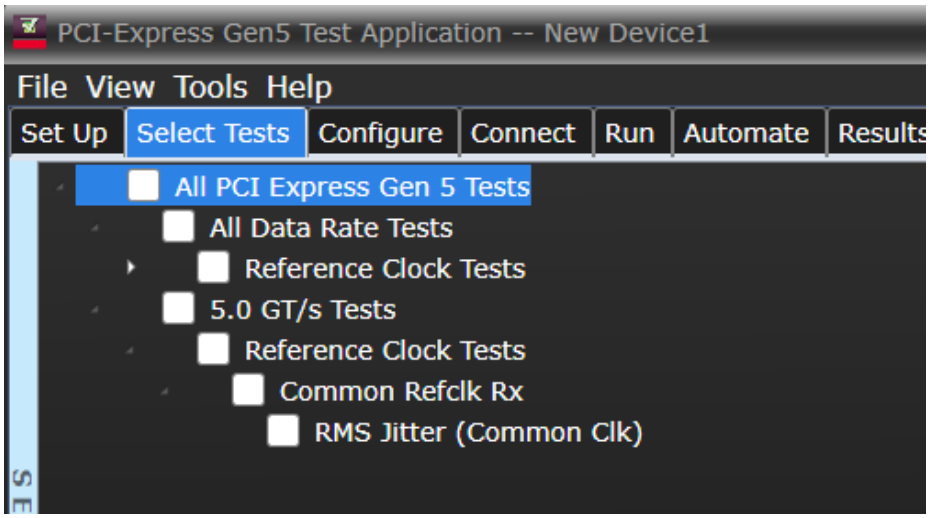


Figure 38 Selecting Reference Clock Tests when SSC or Clean Clock is Selected

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 32 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	3.1 ps RMS

Test Definition Notes from the Specification

- The Refclk jitter is measured after applying the filter function in Figure 8-73 (Common Refclk Rx Architecture for all Data Rates Except 32.0 GT/s); section 8.6.6 of PCI Express Base Specification Revision 5.0.
- Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope (RTO) with a sample rate of 20 GSa/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50 M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9 Stitches each acquired acquisition to make a continuous TIE data.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:

   a Converts time domain TIE data to frequency domain.

   b Applies the PLL filter using parameters for common clocked architecture.

   c Converts back the frequency domain TIE data to time domains.

   d Computes the filtered peak-peak jitters and RMS jitter.

11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

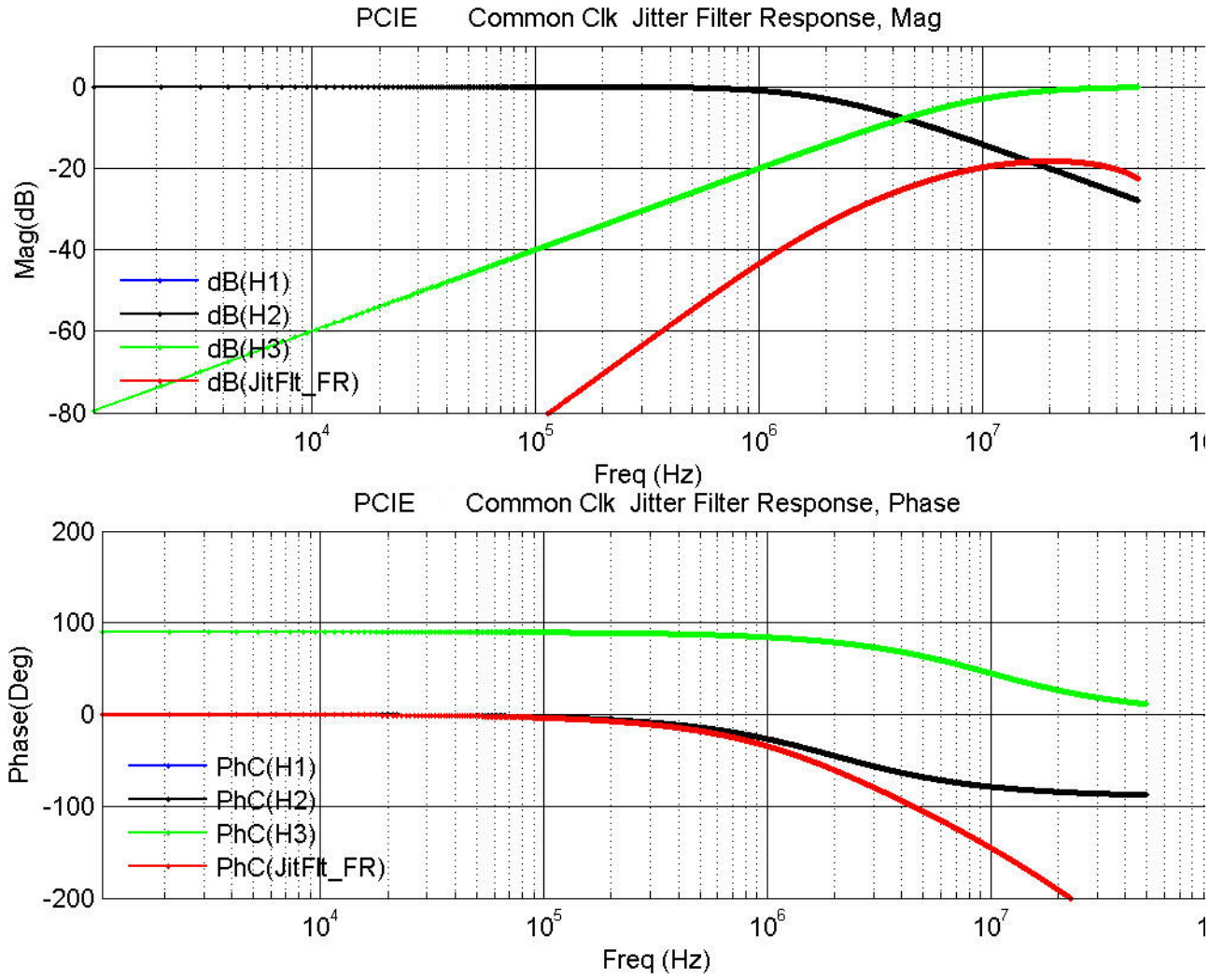


Figure 39 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

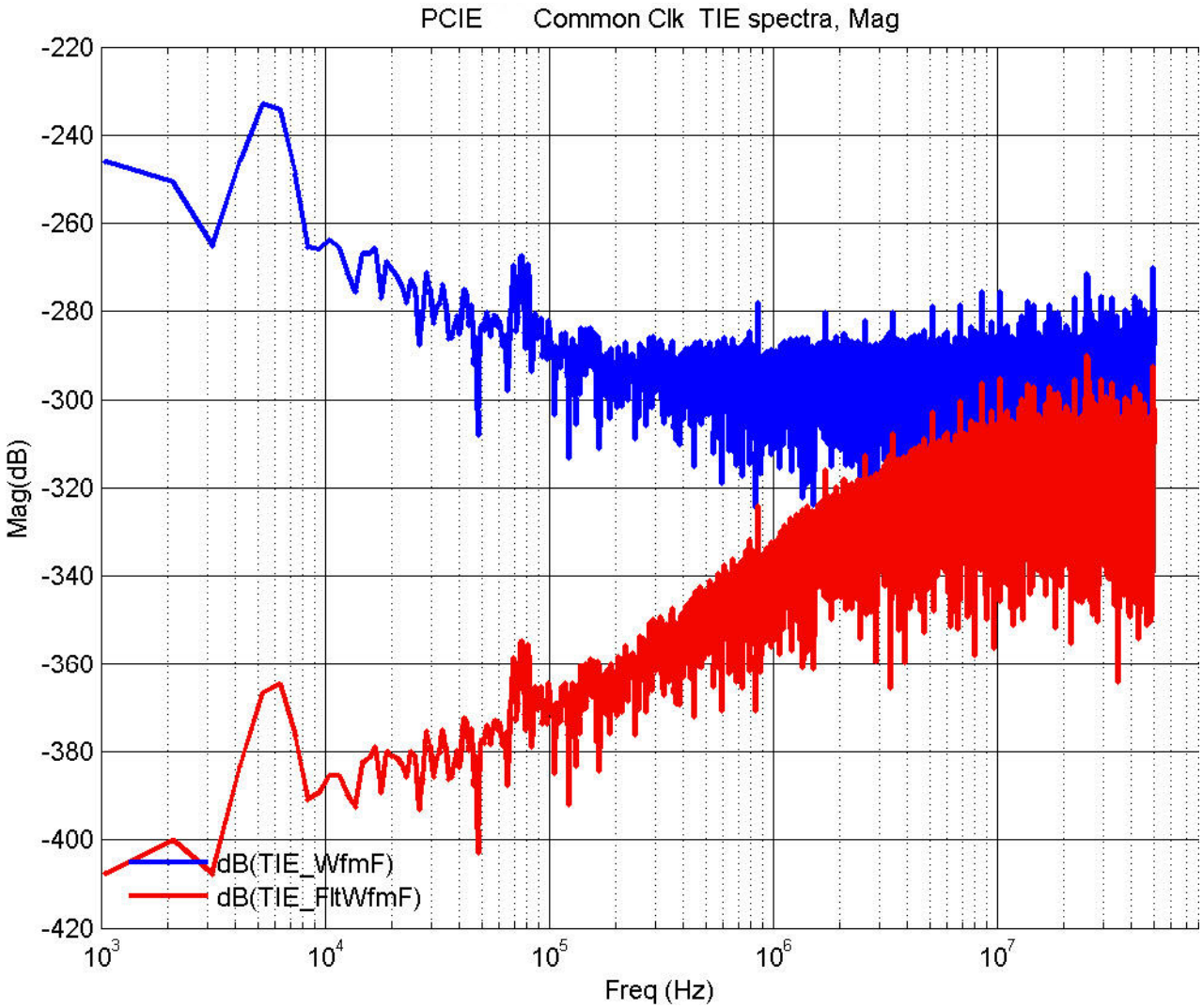


Figure 40 Reference Image for Common Clock TIE Spectra RMS Jitter Test

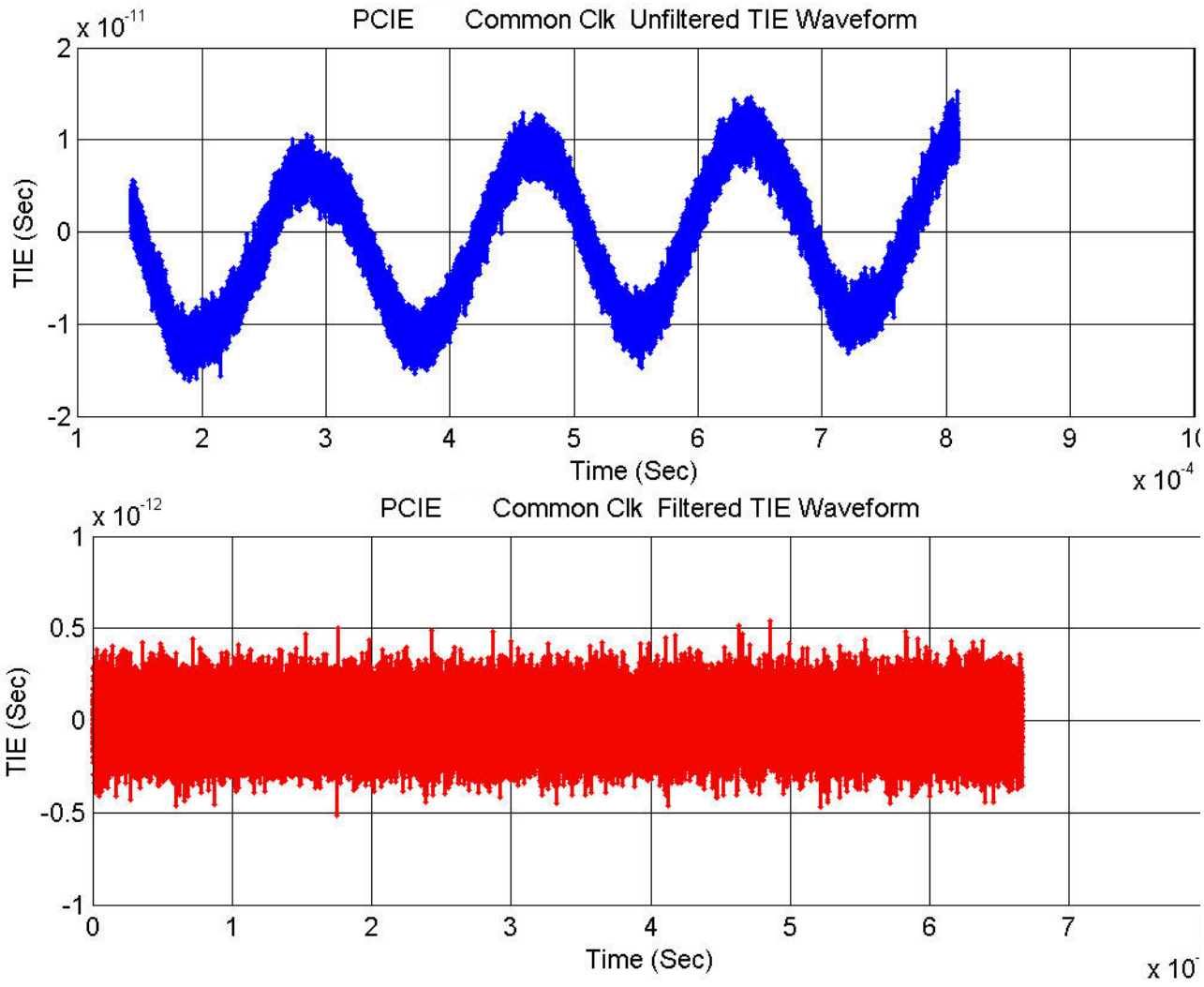


Figure 41 Reference Image for TIE Waveform RMS Jitter Test

Part V
PCI-Express Gen5 8.0 GT/s Tests

KEYSIGHT TECHNOLOGIES

8 Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 5.0

Tx Compliance Test Load / 136
Running Tx Tests / 137

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 8.0 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

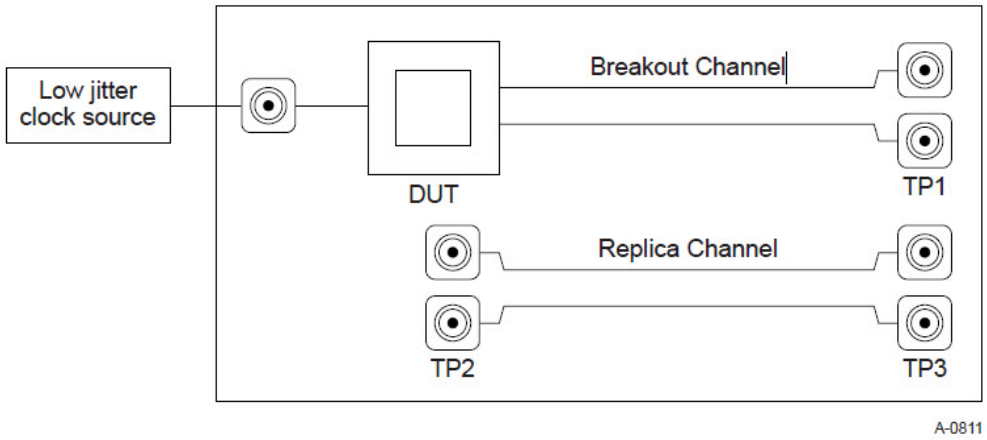


Figure 42 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. In the **Select Tests** tab, navigate to **All PCI Express Gen 5 Tests** > **8.0 GT/s Tests** > **Transmitter (Tx) Tests**.

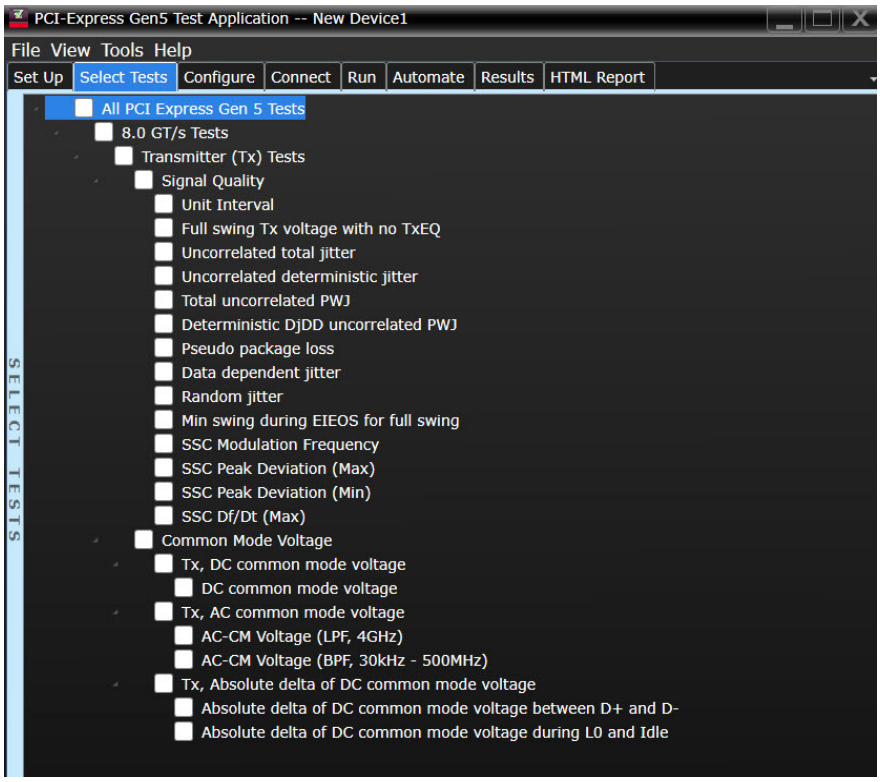


Figure 43 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 33 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	Clean Clock: 124.9625 ps	Clean Clock 125.0375 ps
		SSC: 124.9625 ps	SSC: 125.6603 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean, and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

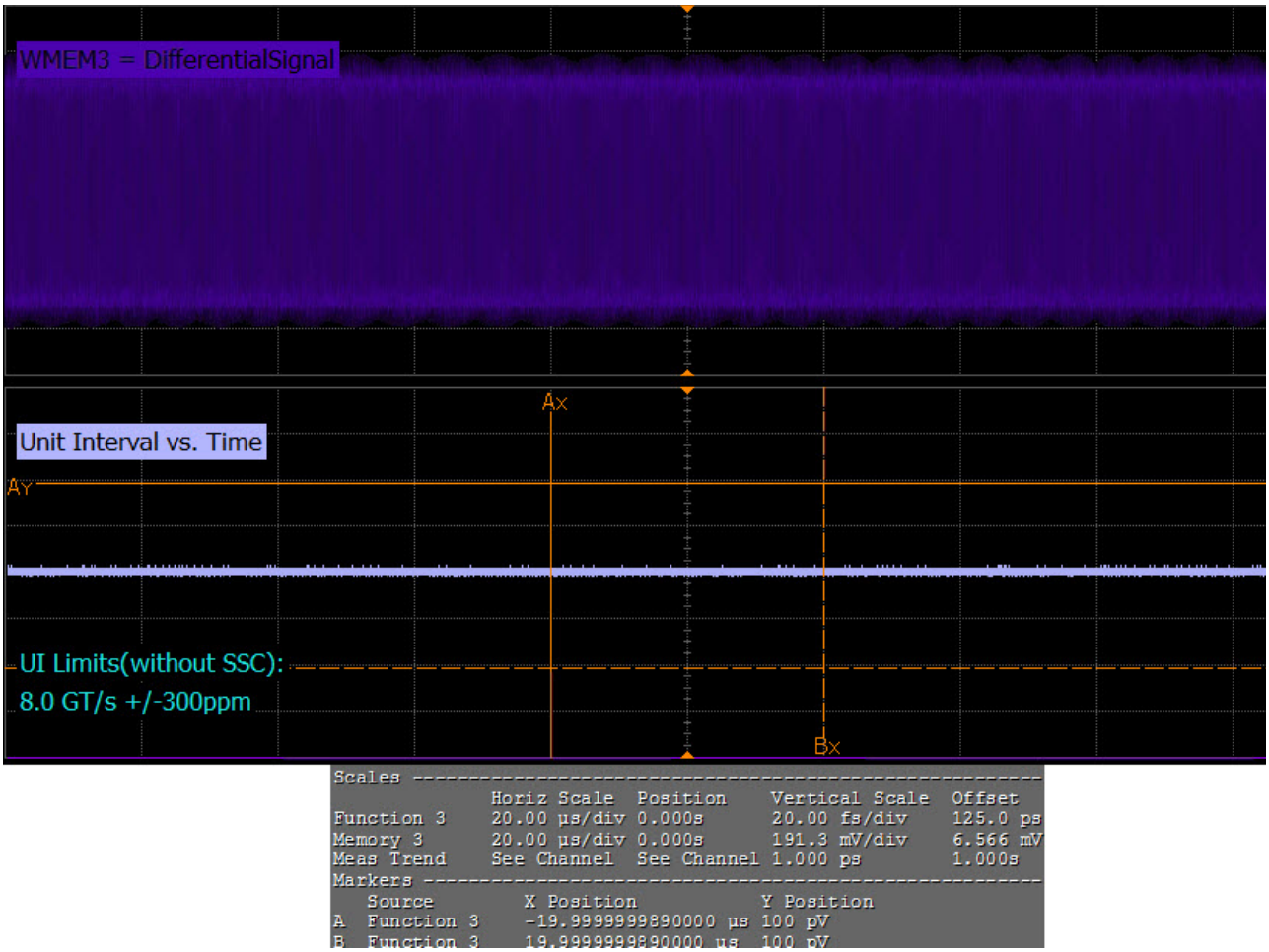


Figure 44 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 45. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP}$ is used as reference to check the compliance of the DUT.

Table 34 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX-FS-NO-EQ}$	Full swing Tx voltage with no TxEQ	800 mV_{PP}	1300 mV_{PP}

Test Definition Notes from the Specification

- 2.5 and 32.0 GT/s specify only one combination of PLL BW and jitter.
- A single combination of PLL BW and peaking is specified for 2.5 and 32.0 GT/s implementations. For other data rates, two combinations of PLL BW and peaking are specified to permit designers to make a trade-off between the two parameters.
- The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. The PLL BW is defined at the point where its transfer function crosses the -3dB point.

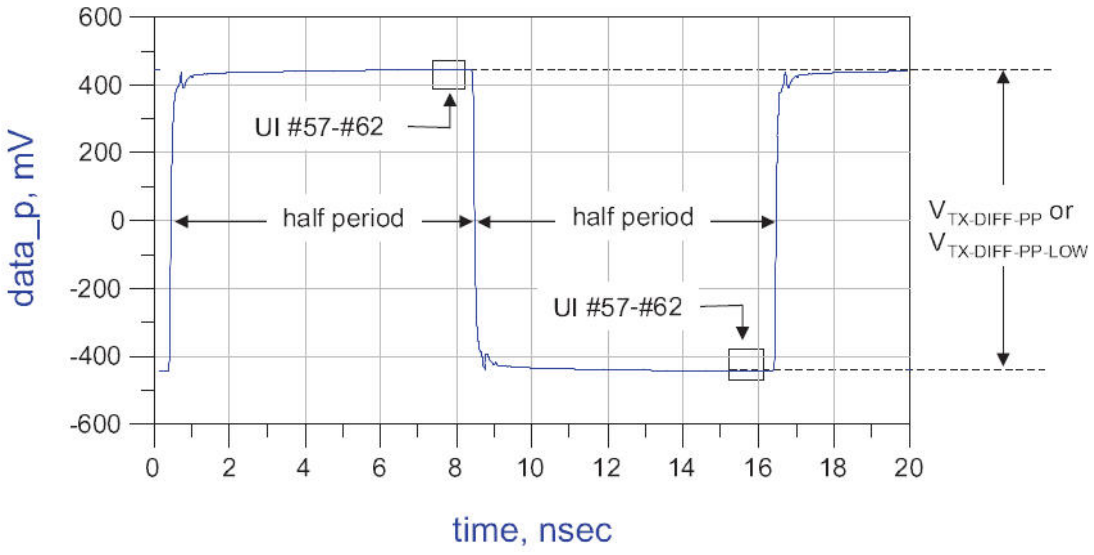


Figure 45 $V_{TX-FS-NO-EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP-LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 46. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 4.3.3.13.1, Table 4-19, $V_{TX-DIFF-PP-LOW}$ is used as reference to check the compliance of the DUT.

Table 35 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX-RS-NO-EQ}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mVPP	1300 mVPP

Test Definition Notes from the Specification

As measured with compliance test load. Defined as 2 × | VTXD+-VbTXD-|

See Section 8.3.3.4 and Section 8.3.3.5 for measurement details. For 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s no minimum voltage swing is specified as it is captured by VTX-BOOST-FS and VTX-BOOST-RS parameters.

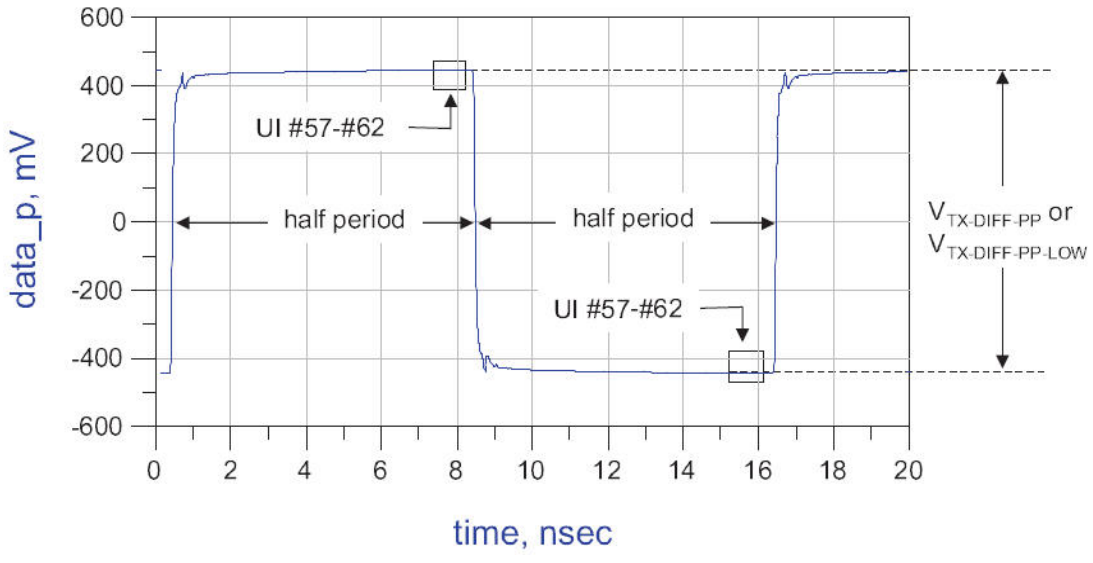


Figure 46 $V_{TX-FS-NO-EQ}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX-EIEOS-FS}$ is within the allowed range.

$V_{TX-EIEOS-FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI at 8.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 36 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0 and 32.0 GT/s that ensures that these parameters are met.

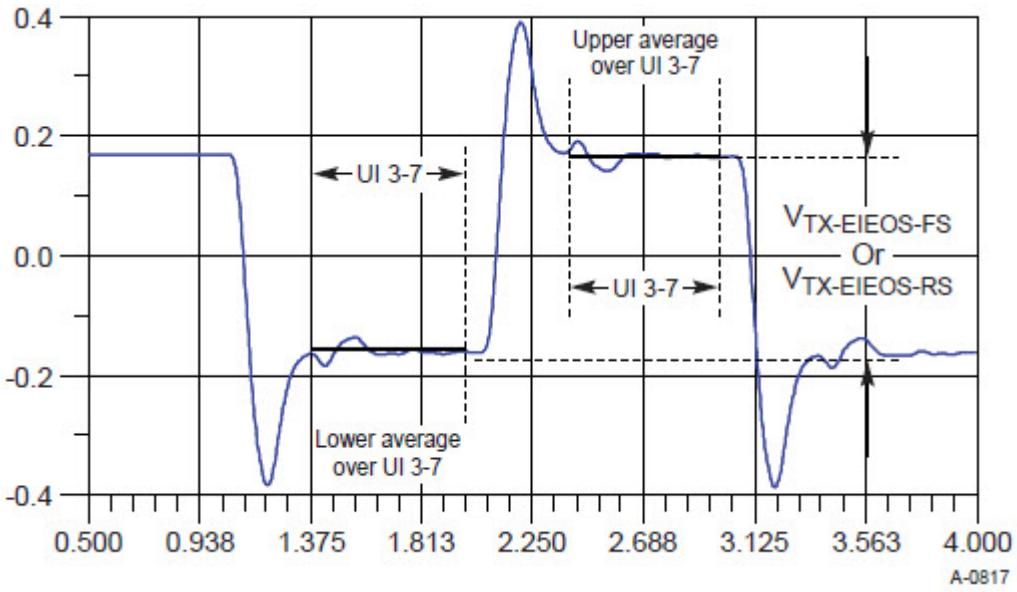


Figure 47 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTestWrapper tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX-EIEOS-RS}$ is within the allowed range.

$V_{TX-EIEOS-RS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of eight consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c+1 coefficient value of -0.33 and a c-1 coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 4-19. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c+1 coefficient value of -0.167 and a c-1 coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only the middle five UI. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 (Data Rate Dependent Transmitter Parameters) is used as reference to check the compliance of the DUT.

Table 37 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-RS}$	Minimum voltage swing during EIEOS for reduced swing signaling	232 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, and 32.0 GT/s that ensures that these parameters are met.

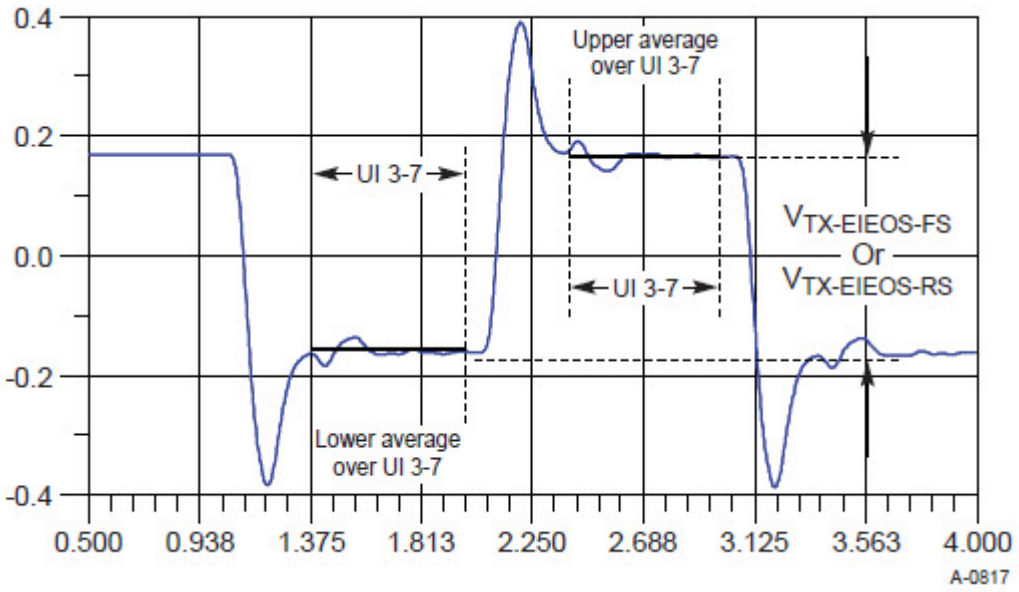


Figure 48 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 38 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	27.55 ps PP at 10^{-12}

Test Definition Notes from the Specification

For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 39 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	12 ps PP

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 40 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	24 ps PP at 10^{-12}

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 41 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	10 ps PP

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the peak deterministic DjDD uncorrelated PWJ value.
8. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter (Information-Only Test)

This test verifies that the maximum data dependent jitter, $T_{TX\text{-}DDJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.5.7 is used as reference.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V111) against a 1010 pattern (V101). Tx package loss measurement is made with c-1 and c+1 both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V101 and V111. Multiple measurements shall be made and averaged to obtain stable values for V101 and V111. Due to the HF content of V101, ps21 TX measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V101 and V111 is made towards the end of each interval to minimize ISI and low frequency effects. V101 is defined as the peak-peak voltage between minima and maxima of the clock pattern. V111 is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 42 Pseudo Package Loss Test Details

Symbol	Parameter	Max
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for a device containing root ports	3.0 dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for all devices not containing root ports	3.0 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.

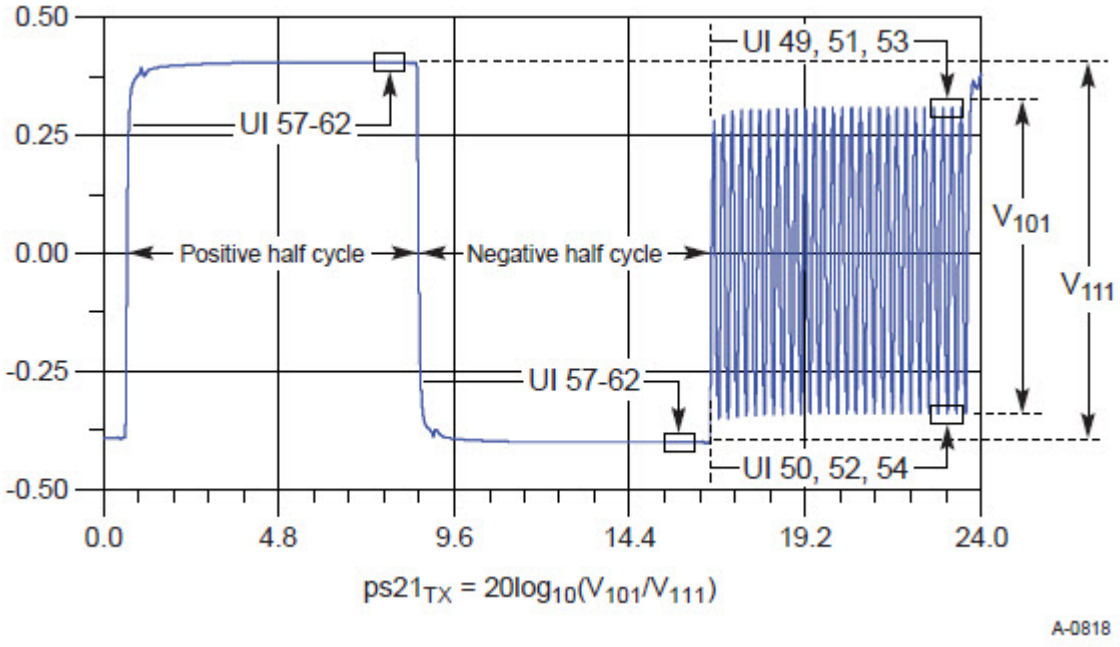


Figure 49 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the number of package loss measurements taken.
8 Reports the package loss ration value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 43 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	1.17 - 1.97 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJ-DD}$.
- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 44 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate, and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Sets up DC common mode voltage as follows:
   a Enables and displays common mode measurements.
   b Loads common mode signal to waveform memory.
   c Loads and enhance dynamic range D+ signal and D- signal.
   d Enables the average common mode measurement.
   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).
4 Measures the average value of D+ and D- signal.
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 2.0 as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

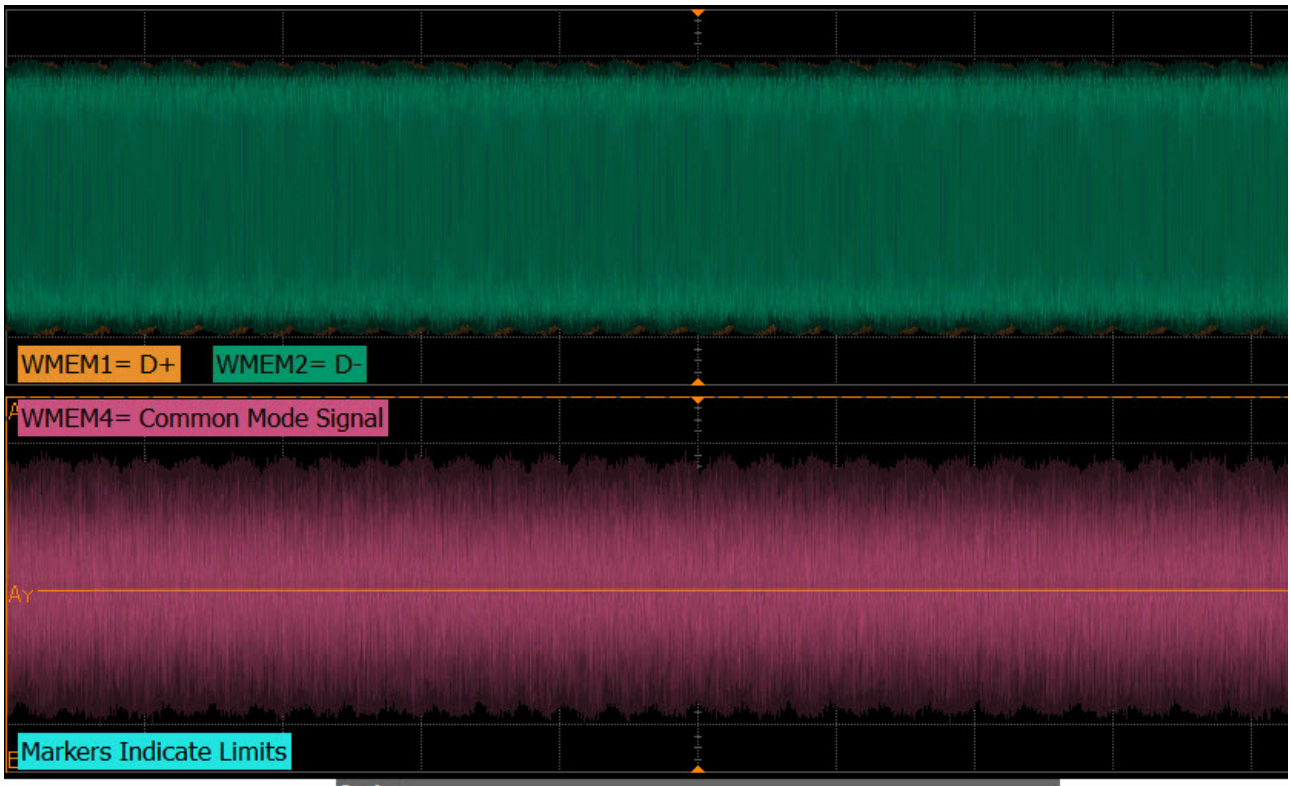


Figure 50 Reference Image for DC Common Mode Voltage Test

AC Common-Mode Voltage (LPF, 4 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 45 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- VTX-AC-CM-PP is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.8 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 4GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

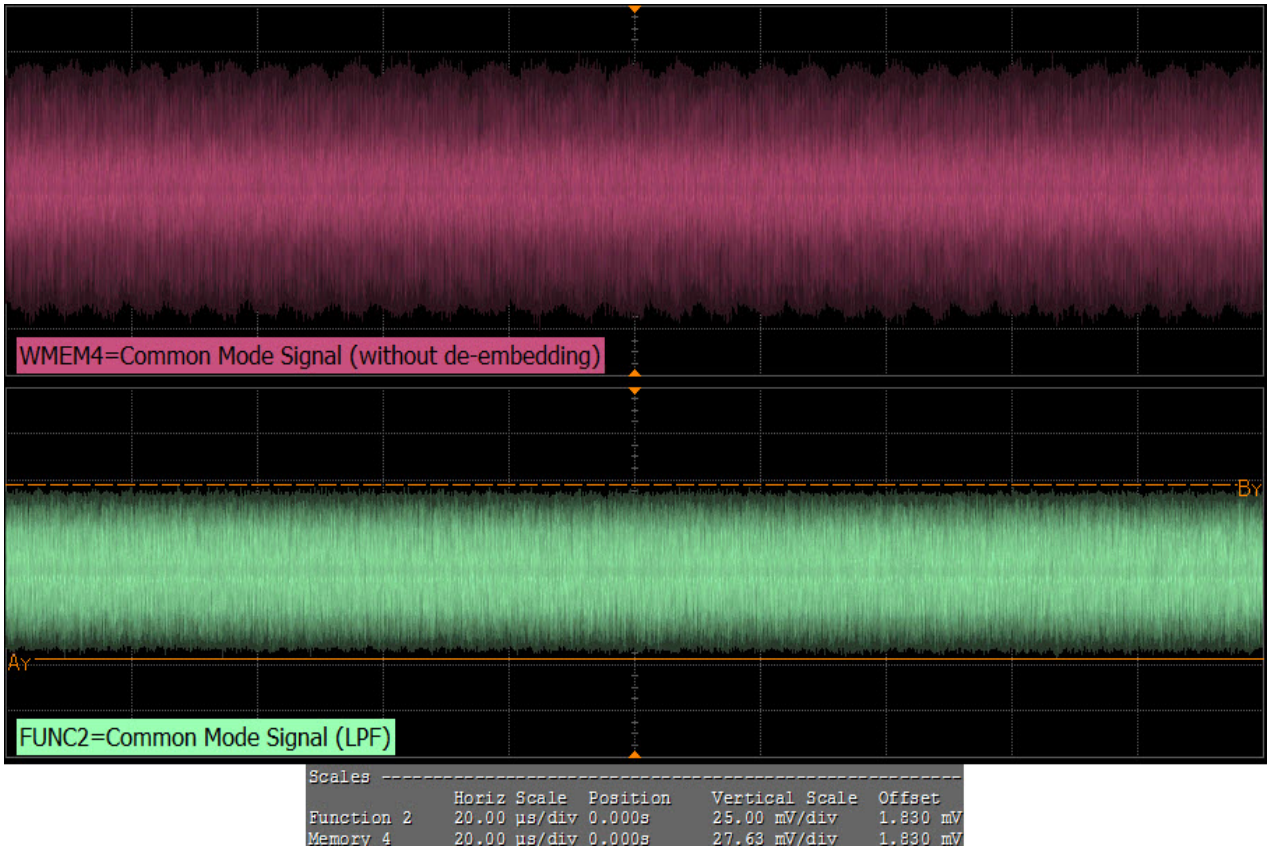


Figure 51 Reference Image for AC-CM voltage (4GHz LPF) Test

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 46 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 4 GHz) test.

1 Gets PCIE5 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

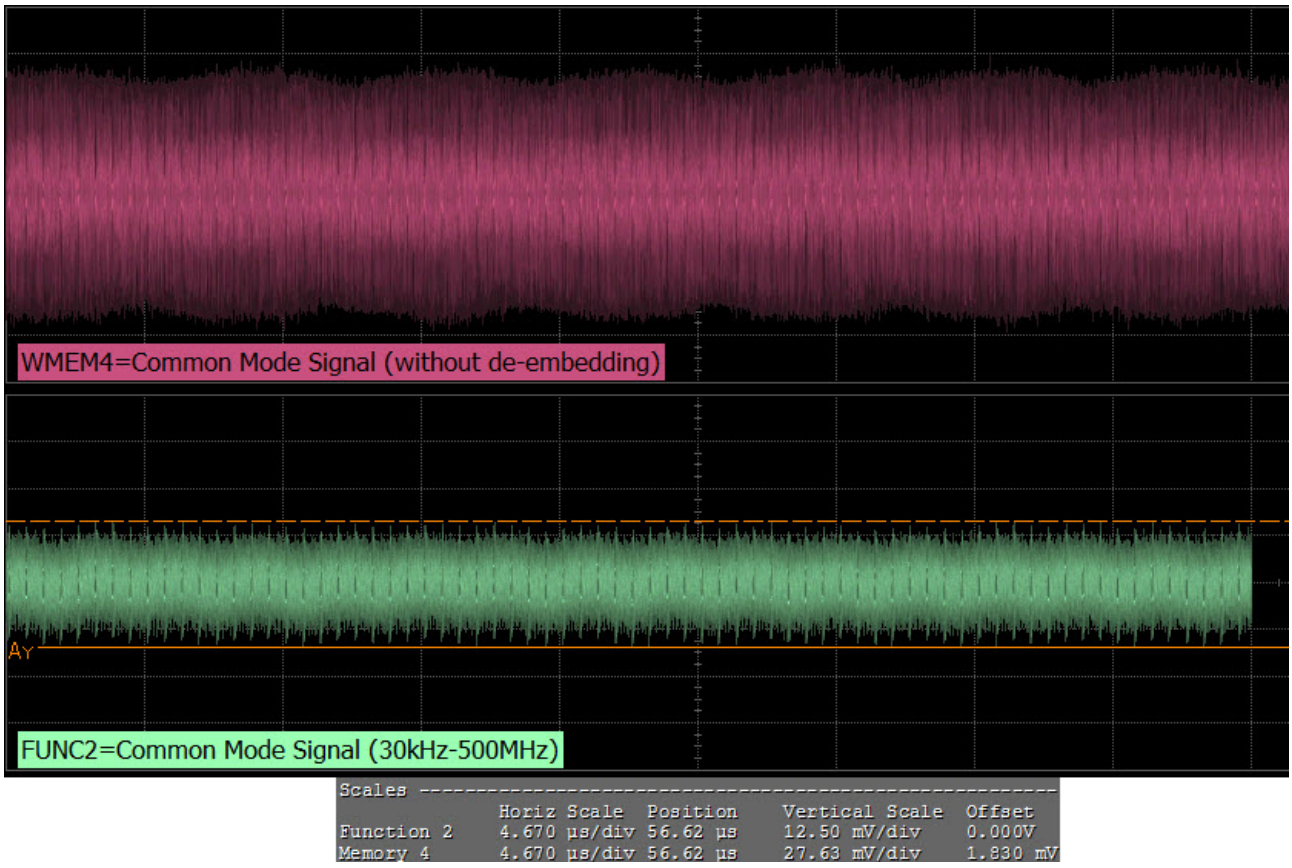


Figure 52 Reference Image for AC-CM voltage (30KHz - 500MHz) Test

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D-[during\ L0]}| \leq 25\ mV$

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $|V_{TX\text{-}D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 47 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT..

Table 48 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

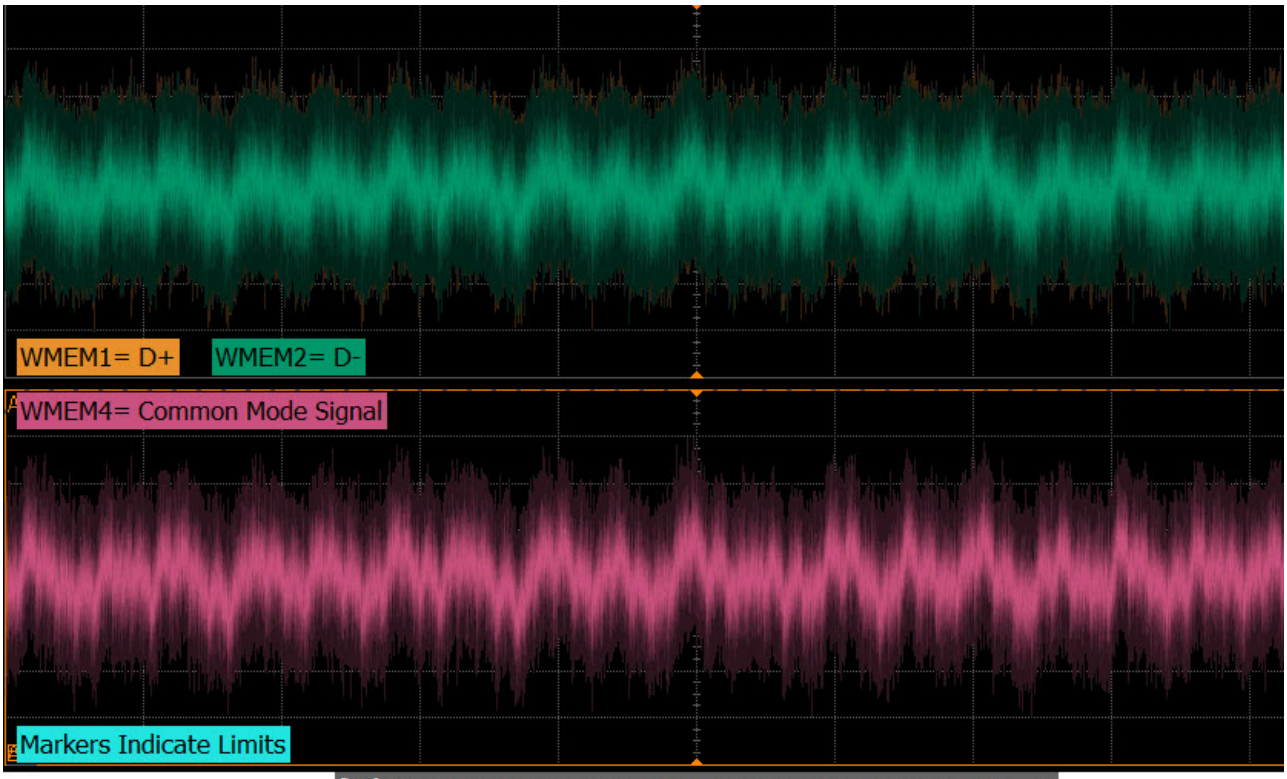
The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Memory 1	20.00 µs/div	0.000s	787.5 µV/div	2.755 mV
Memory 2	20.00 µs/div	0.000s	762.5 µV/div	8.203 mV
Memory 4	20.00 µs/div	0.000s	582.5 µV/div	5.479 mV

Markers

	Source	X Position	Y Position
A	Memory 4	-1.00000000000000s	0.000000V
B	Memory 4	-1.00000000000000s	3.600000V

Figure 53 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 49 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 8.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 50 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	0.0%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 8.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 51 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.5%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 8.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 52 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt	1250 ppm/µs

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1^{st} order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures memory depth and sampling rate as per the data rate.

3 Fits and displays all sample data on screen.

4 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.

5 Analyzes measurements trend using the jitter **Meas Trend** function.

6 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:

a Generates a differential plot (x_n - x_{n-1}).

b The maximum slew rate corresponds to the peak of the differential plot.

7 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

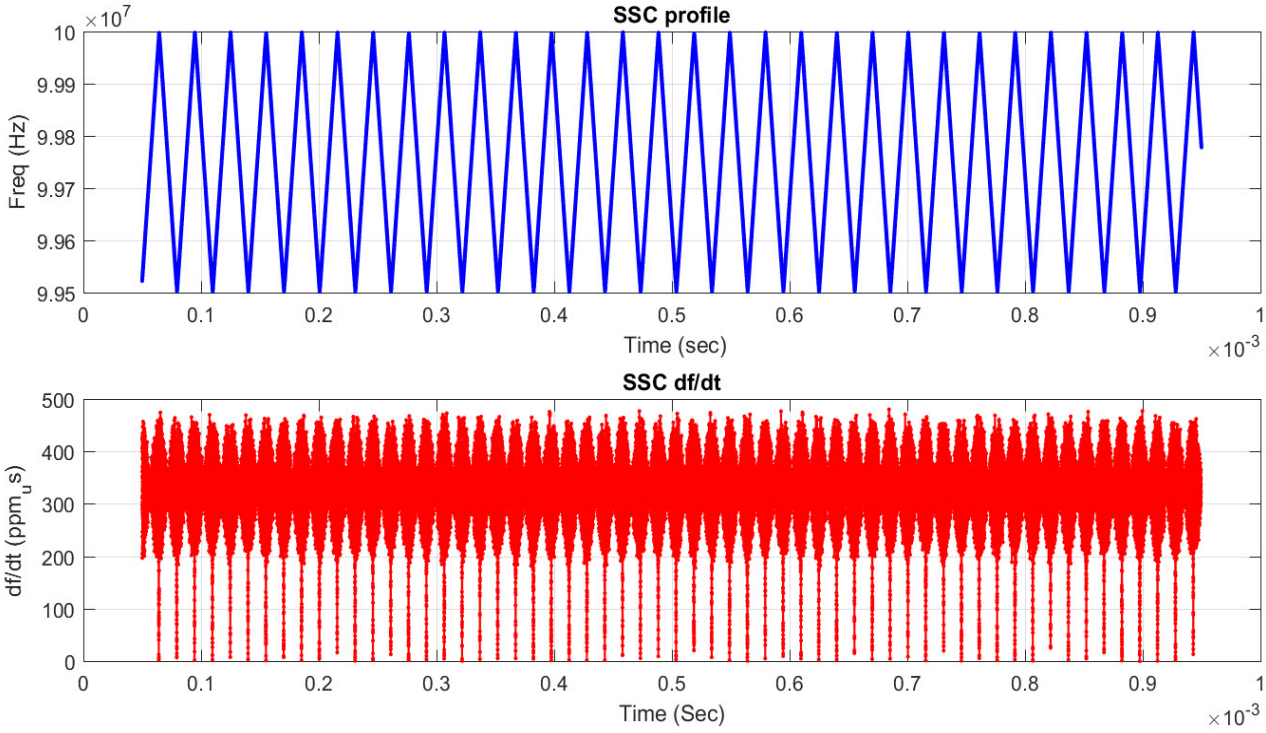


Figure 54 Maximum SSC Slew Rate

Running Equalization Presets Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. Then, when selecting tests, navigate to “Equalization Presets Tests” in the “PCIE 5.0 Tests” group.

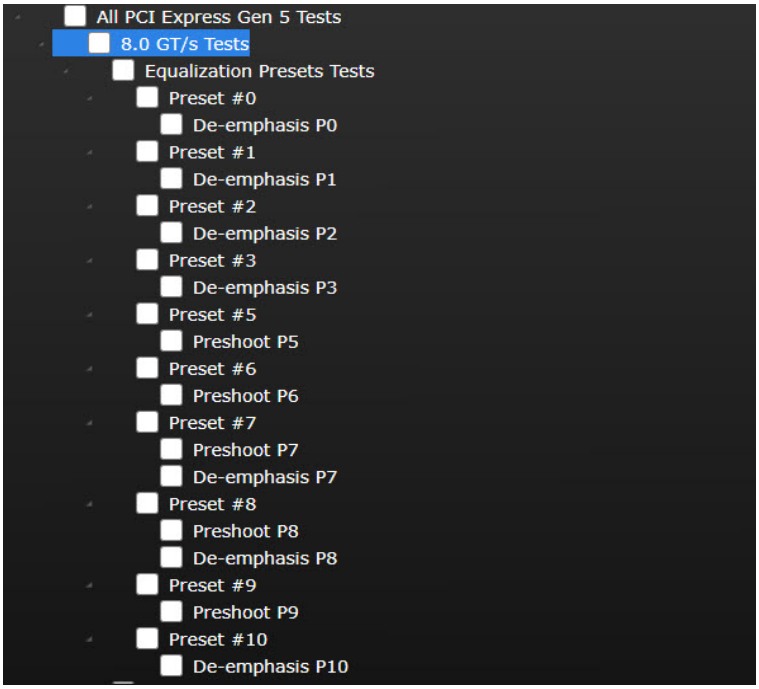


Figure 55 Selecting Equalization Presets Tests

Preset #1 Measurement (P1), De-emphasis Test

This test verifies that the de-emphasis of the preset number P1 is within the conformance limits as specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 56.

Table 53 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P1	P1/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

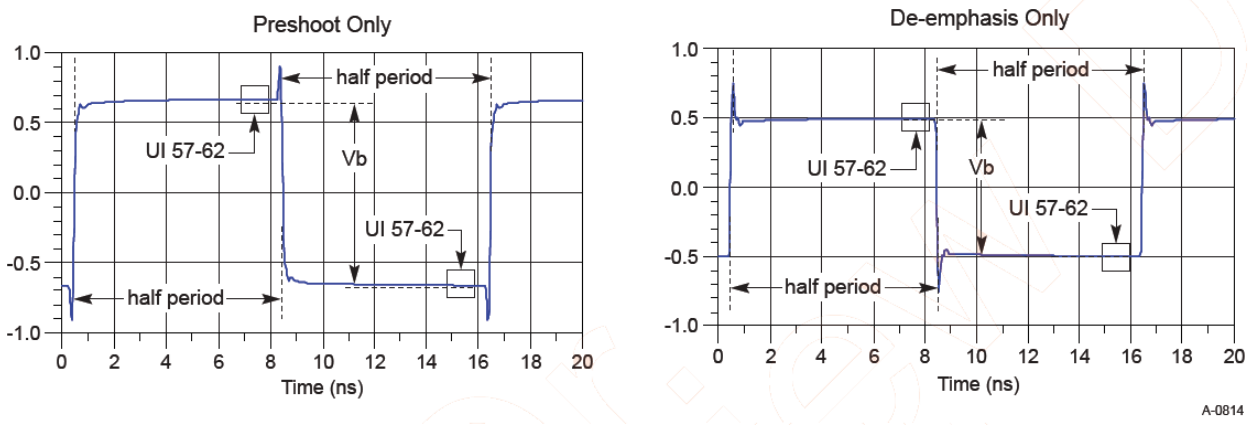


Figure 56 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 54 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P1	0.0	−3.5 ± 1 dB	0.000	−0.167	1.000	0.668	0.668

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P1.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P1 signal in *.bin format.
12 Inputs the P4 and P1 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P1.
14 Reports the measurement of Vb during preset values P1 and P4.
15 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #0 Measurement (P0), De-emphasis Test

This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 57.

Table 55 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P0	P0/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

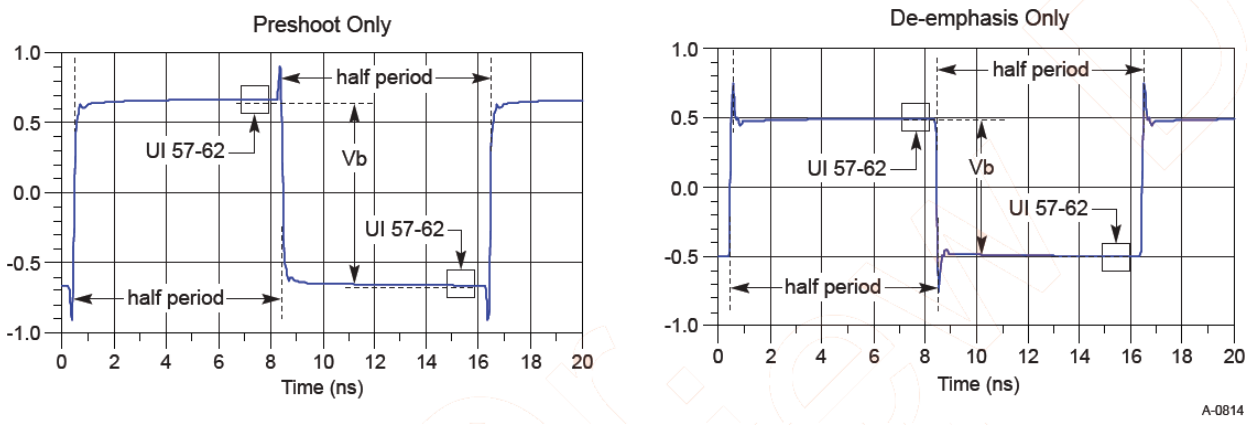


Figure 57 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 56 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P0	0.0	−6.0 ± 1.5 dB	0.000	−0.250	1.000	0.500	0.500

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P0.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P0 signal in *.bin format.
12 Inputs the P4 and P0 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P0.
14 Reports the measurement of Vb during preset values P0 and P4.
15 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #9 Measurement (P9), Preshoot Test

This test verifies that the preshoot of the preset number P9 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 58.

Table 57 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P9	N/A	P4/P9

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

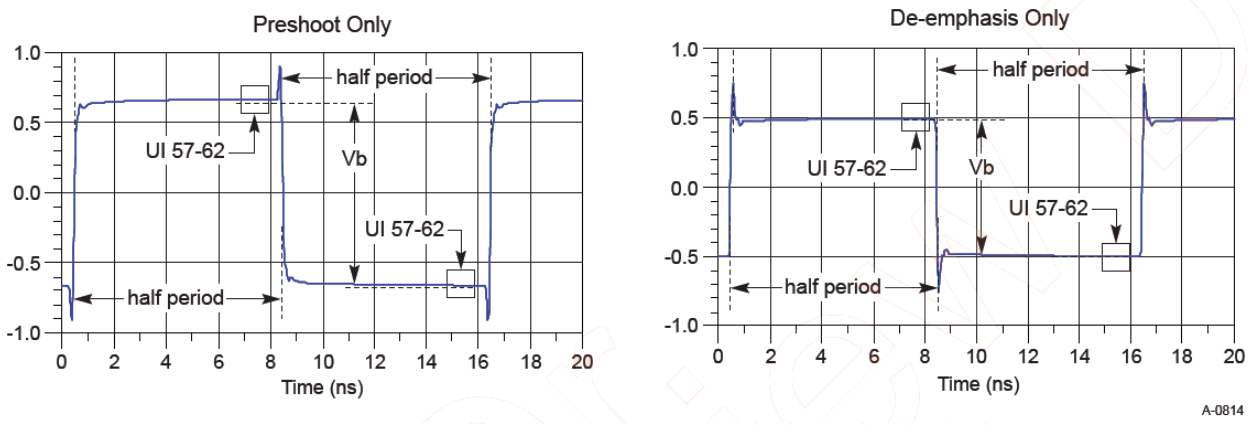


Figure 58 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 58 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P9	3.5 ± 1 dB	0.0	–0.166	0.000	0.668	0.668	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P4.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P4 signal into *.bin format.

7 Configures the DUT to operate in preset value #P9.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P9 signal in *.bin format.

12 Inputs the P4 and P9 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P9.

14 Reports the measurement of Vb during preset values P9 and P4.

15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), De-emphasis Test

This test verifies that the de-emphasis of the preset number P8 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 59.

Table 59 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

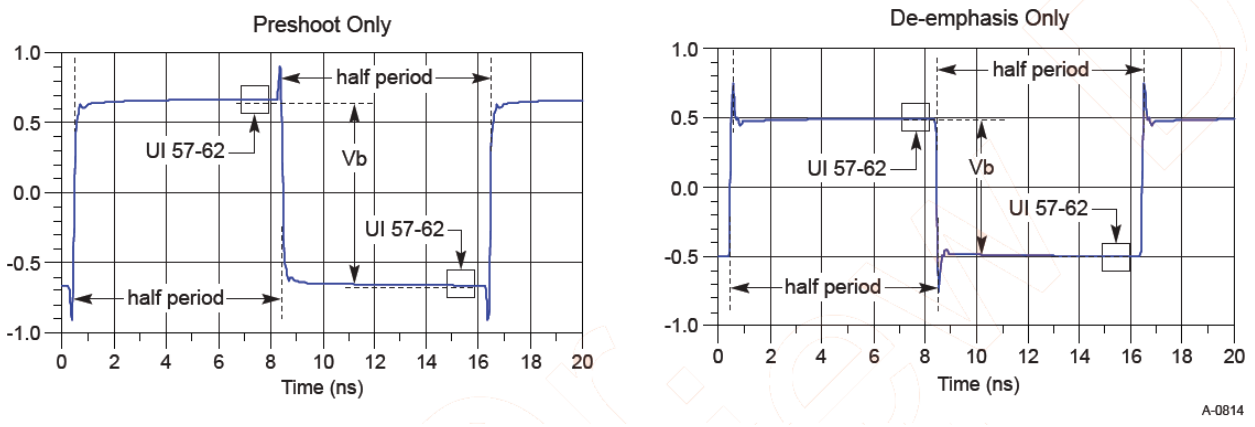


Figure 59 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 60 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	–3.5 ± 1 dB	–0.125	–0.125	0.750	0.500	0.750

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P6.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P6 signal into *.bin format.
7 Configures the DUT to operate in preset value #P8.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P8 signal in *.bin format.
12 Inputs the P6 and P8 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P8.
14 Reports the measurement of Vb during preset values P6 and P8.
15 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #8 Measurement (P8), Preshoot Test

This test verifies that the preshoot of the preset number P8 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 60.

Table 61 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P8	P8/P6	P3/P8

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

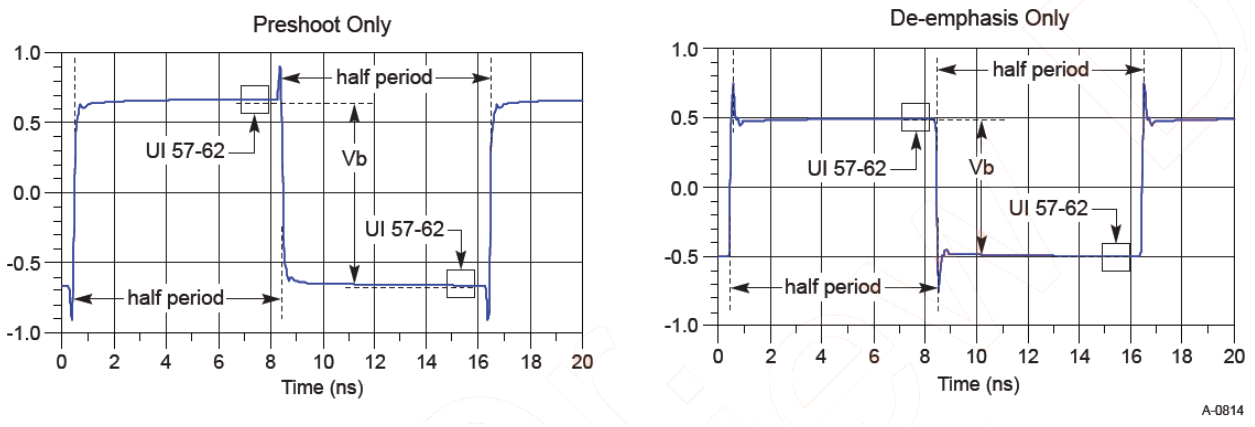


Figure 60 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 62 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P8	3.5 ± 1 dB	–3.5 ± 1 dB	–0.125	–0.125	0.750	0.500	0.750

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures the DUT to operate in preset value #P3.

3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

4 Sets the **Horizontal Domain Scale** to 20.0 µs.

5 Fits and displays all sample data on screen.

6 Saves the P3 signal into *.bin format.

7 Configures the DUT to operate in preset value #P8.

8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.

9 Sets the **Horizontal Domain Scale** to 20.0 µs.

10 Fits and displays all sample data on screen.

11 Saves the P8 signal in *.bin format.

12 Inputs the P3 and P8 saved waveform into SigTest tool.

13 Computes the preshoot at preset value P8.

14 Reports the measurement of Vb during preset values P3 and P8.

15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), De-emphasis Test

This test verifies that the de-emphasis of the preset number P7 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 61.

Table 63 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

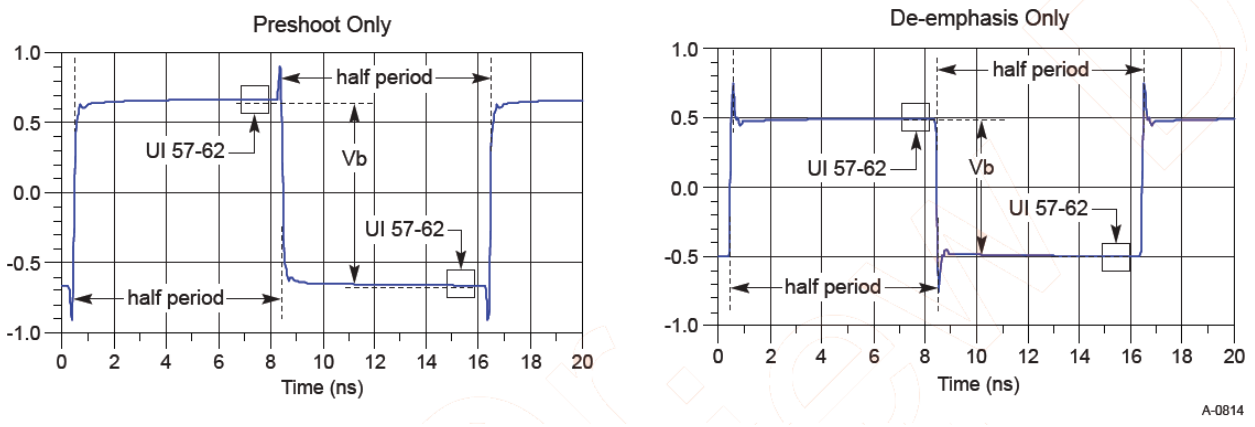


Figure 61 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 64 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	–6.0 ± 1.5 dB	–0.100	–0.200	0.800	0.400	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P5.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P5 signal into *.bin format.
7 Configures the DUT to operate in preset value #P7.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P7 signal in *.bin format.
12 Inputs the P5 and P7 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P7.
14 Reports the measurement of Vb during preset values P5 and P7.
15 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #7 Measurement (P7), Preshoot Test

This test verifies that the preshoot of the preset number P7 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 62.

Table 65 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P7	P7/P5	P2/P7

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

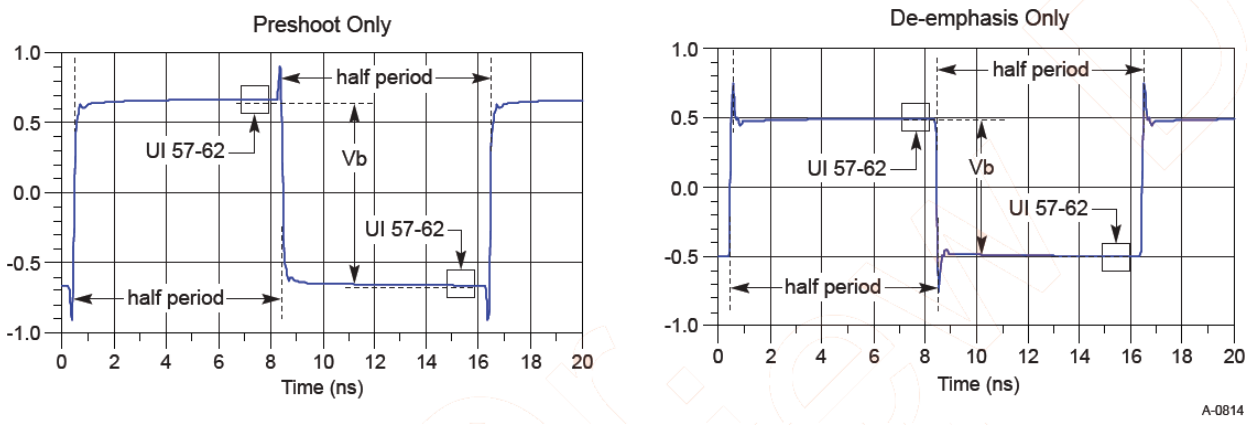


Figure 62 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 66 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P7	3.5 ± 1 dB	–6.0 ± 1.5 dB	–0.100	–0.200	0.800	0.400	0.600

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P2.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P2 signal into *.bin format.
7 Configures the DUT to operate in preset value #P7.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P7 signal in *.bin format.
12 Inputs the P2 and P7 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P7.
14 Reports the measurement of Vb during preset values P2 and P7.
15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #5 Measurement (P5), Preshoot Test

This test verifies that the preshoot of the preset number P5 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 63

Table 67 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P5	N/A	P4/P5

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

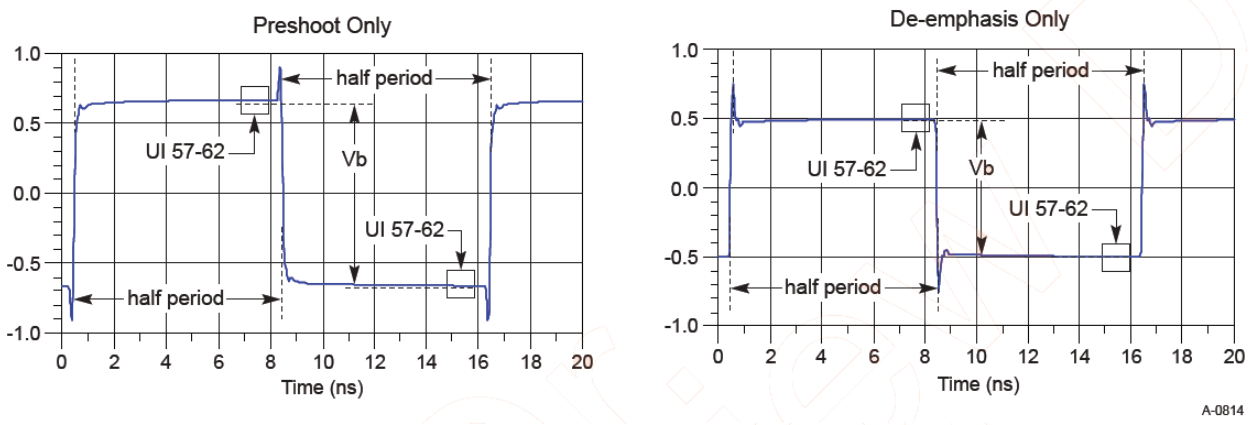


Figure 63 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 68 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P5.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P5 signal in *.bin format.
12 Inputs the P4 and P5 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P5.
14 Reports the measurement of Vb during preset values P4 and P5.
15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #6 Measurement (P6), Preshoot Test

This test verifies that the preshoot of the preset number P6 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 64.

Table 69 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P6	N/A	P4/P6

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

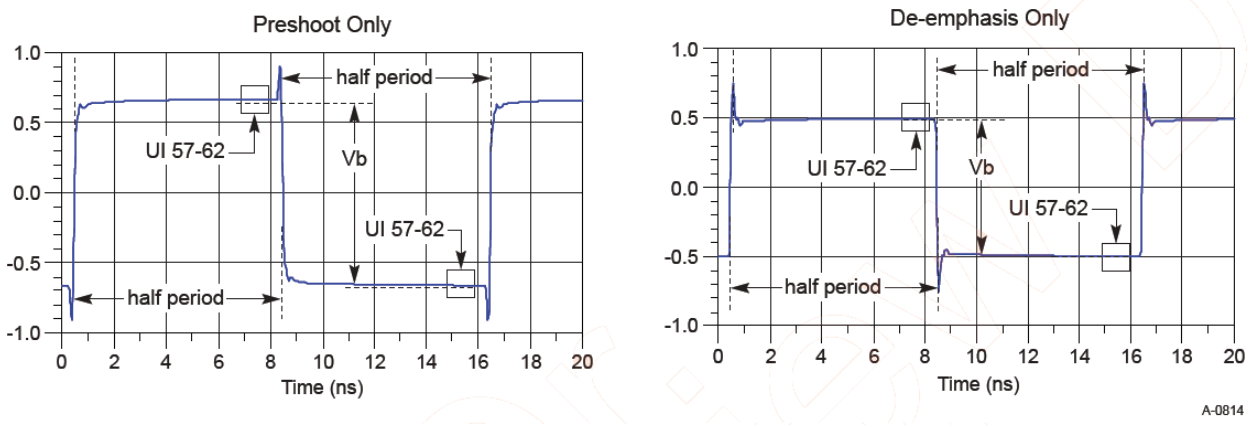


Figure 64 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 70 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P6	2.5 ± 1 dB	0.0	–0.125	0.000	0.750	0.750	1.000

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P6.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P6 signal in *.bin format.
12 Inputs the P4 and P6 saved waveform into SigTest tool.
13 Computes the preshoot at preset value P6.
14 Reports the measurement of Vb during preset values P6 and P4.
15 Compares the preshoot value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #3 Measurement (P3), De-emphasis Test

This test verifies that the de-emphasis of the preset number P3 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 65.

Table 71 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P3	P3/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

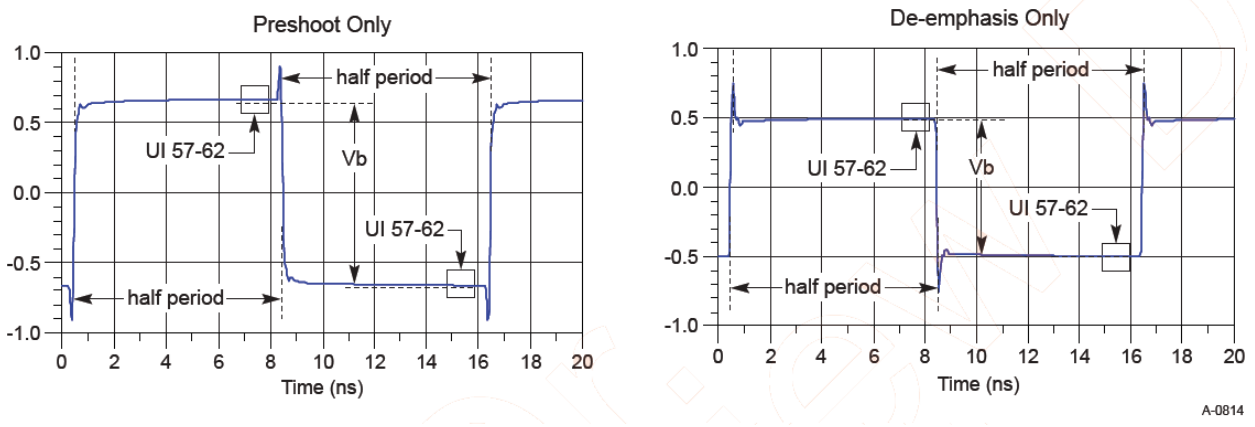


Figure 65 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 72 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	−2.5 ± 1 dB	0.000	−0.125	1.000	0.750	0.750

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P3.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P3 signal in *.bin format.
12 Inputs the P4 and P3 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P3.
14 Reports the measurement of Vb during preset values P1 and P3.
15 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #2 Measurement (P2), De-emphasis Test

This test verifies that the de-emphasis of the preset number P0 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 66.

Table 73 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P2	P2/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

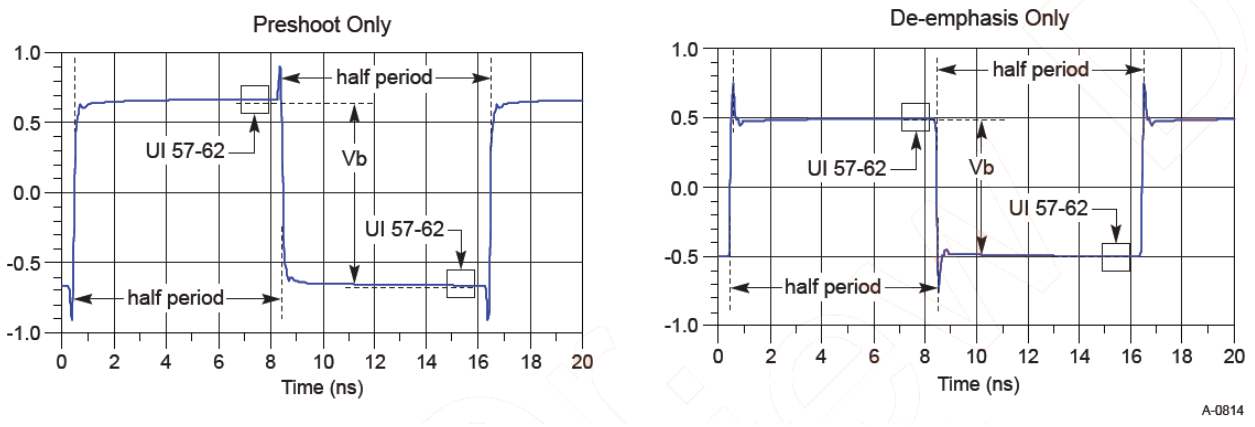


Figure 66 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 74 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P2	0.0	−4.4 ± 1.5 dB	0.000	−0.200	1.000	0.600	0.600

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain** Scale to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P2.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P2 signal in *.bin format.
12 Inputs the P4 and P2 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P2.
14 Reports the measurement of Vb during preset values P2 and P4.
15 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Preset #10 Measurement (P10), De-emphasis Test

This test verifies that the de-emphasis of the preset number P10 is within the conformance limits specified in PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1.

8.0 GT/s, 16.0 GT/s and 32.0 GT/s PCIe signaling must support the full range of presets given in Table 8-1 (PCIE Base Specification Revision 5.0). Presets are defined in terms of ratios, relating the pre-cursor and post-cursor equalization voltages. The pre-cursor (Vc) is referred to as pre-shoot, while the post-cursor (Vb) is referred to as de-emphasis. This convention permits the specification to retain the existing 2.5 GT/s and 5.0 GT/s definitions for Tx equalization, where only de-emphasis is defined, and it allows preshoot and de-emphasis to be defined such that each is independent of the other. The tolerances in Table 8-1 (PCIE Base Specification Revision 5) also apply to 2.5 and 5.0 GT/s de-emphasis. The maximum swing, Vd, is also shown to illustrate that, when both c_{+1} and c_{-1} are nonzero, the swing of Va does not reach the maximum as defined by Vd. The high frequency nature of PCIe signaling makes measurement of single UI pulse heights impractical. Consequently all amplitude measurements are made with low frequency waveforms as shown in Figure 67.

Table 75 Preset Measurement Cross Reference Table

Preset Number	De-emphasis (dB) $20\log_{10}$ (Vb(i)/Vb(j))	Preshoot (dB) $20\log_{10}$ (Vb(i)/Vb(j))
P10	P10/P4	N/A

With the exception of P4 (for which both preshoot and de-emphasis are 0.0 dB), it is not possible to obtain a direct measurement of Va and Vc, because these portions of the waveform are one UI wide and therefore subject to attenuation by the package and the breakout channel. Instead, the Va and Vc values are obtained by setting the DUT to a different preset value where the desired Va or Vc voltage occurs during the Vb interval.

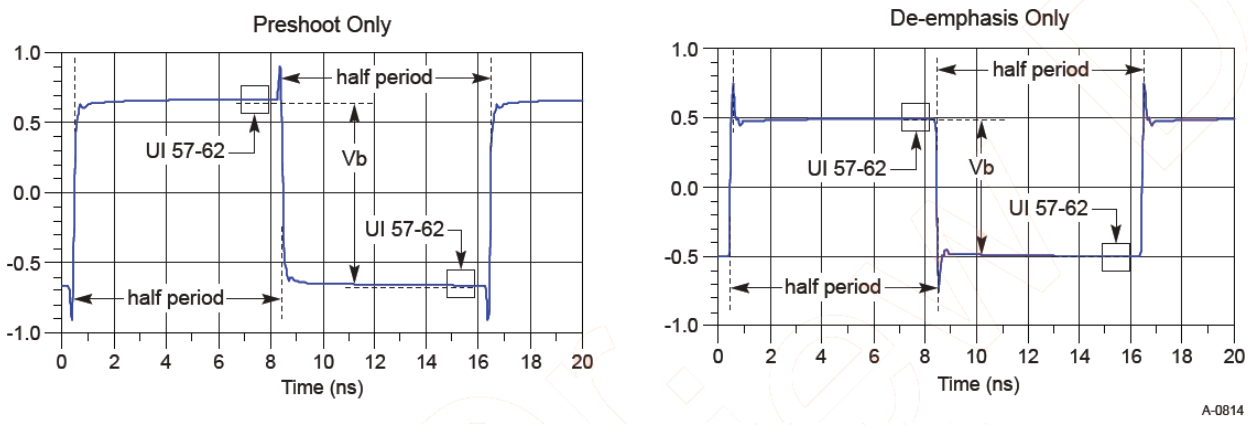


Figure 67 Waveform measurement points for preshoot and de-emphasis

Hence, the Vb interval for each preset value is obtained by measuring the PP voltage on the 64-ones/64-zeroes segment of the compliance pattern for the corresponding preset value. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UIs of each half cycle (UI 57-62 of 64-ones/64-zeroes). High frequency noise is mitigated by averaging over multiple readings until the PP noise over the area of interest is less than 2% of the magnitude of Vb.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.3.3.3, Table 8-1 is used as reference to check the compliance of the DUT.

Table 76 Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P10	0.0	See below Note.	0.000	See below Note.	1.000	See below Note.	See below Note.

Test Definition Notes from the Specification

P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Understanding the Test Flow

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Configures the DUT to operate in preset value #P10.
8 Configures memory depth as per the data rate. Sampling rate is set through the **Configure** tab. In case, the selected sampling rate is higher than the maximum supported sampling rate of the oscilloscope, then max supported scope sampling rate is used. In case of Z-series and Q-series oscilloscopes, the scope sampling rate is fixed at 160 GSa/s when real edge channels are used.
9 Sets the **Horizontal Domain Scale** to 20.0 µs.
10 Fits and displays all sample data on screen.
11 Saves the P10 signal in *.bin format.
12 Inputs the P4 and P1 saved waveform into SigTest tool.
13 Computes the de-emphasis at preset value P10.
14 Reports the measurement of Vb during preset values P10 and P4.
15 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

9 Reference Clock Tests, 8.0 GT/s, PCI-E 5.0

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Running Reference Clock Tests / 215

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 8.0 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

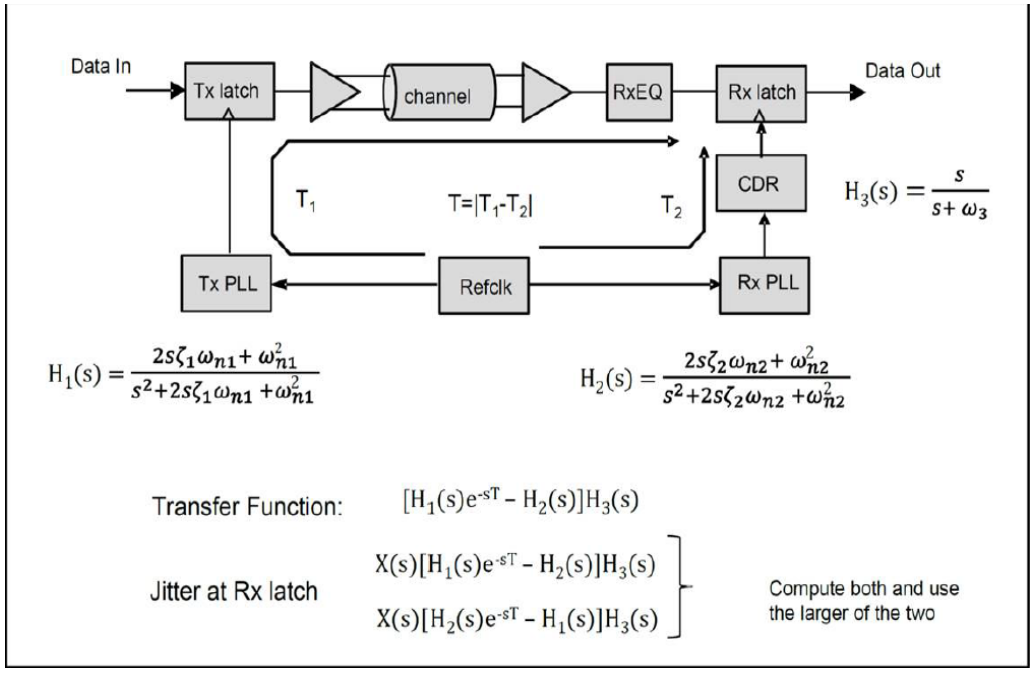
NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 8.0 GT/s, PCI-E 5.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

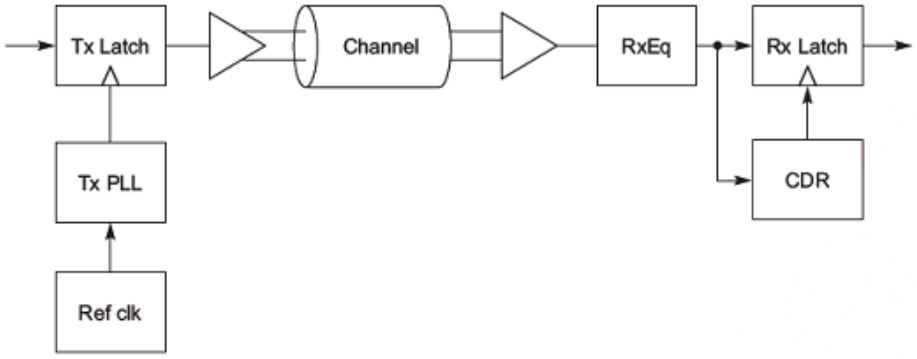
Common Clock Architecture

This section describes the common Refclk Rx architecture.



Data Clock Architecture

This section describes the data driving architecture.



$$H_1(s) = \left[\frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1}^2 + \omega_{n1}^2}\right] \qquad H_3(s) = \left[\frac{2s\zeta_3\omega_{n3} + \omega_{n3}^2}{s^2 + 2s\zeta_3\omega_{n3}^2 + \omega_{n3}^2}\right]$$

$$H(s) = H_1(s)[1 - H_3(s)]$$

	0.01 dB Peaking	2.0 dB Peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1} = 0.448 Mrad/s ζ_1 = 14	ω_{n1} = 6.02 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 4.0 MHz	ω_{n1} = 0.896 Mrad/s ζ_1 = 14	ω_{n1} = 12.04 Mrad/s ζ_1 = 0.73

	0.01 dB Peaking	1.0 dB Peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n2} = 0.448 Mrad/s ζ_2 = 14	ω_{n2} = 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 5.0 MHz	ω_{n2} = 1.12 Mrad/s ζ_2 = 14	ω_{n2} = 11.53 Mrad/s ζ_2 = 1.15

	0.5 dB Peaking	2.0 dB Peaking
BW_{CDR}(min) = 10 MHz	ω_{n3} = 16.57 Mrad/s ζ_3 = 1.75	ω_{n3} = 33.8 Mrad/s ζ_3 = 0.73

A-0843

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in Figure 4-25 of the Card Electromechanical Specification.

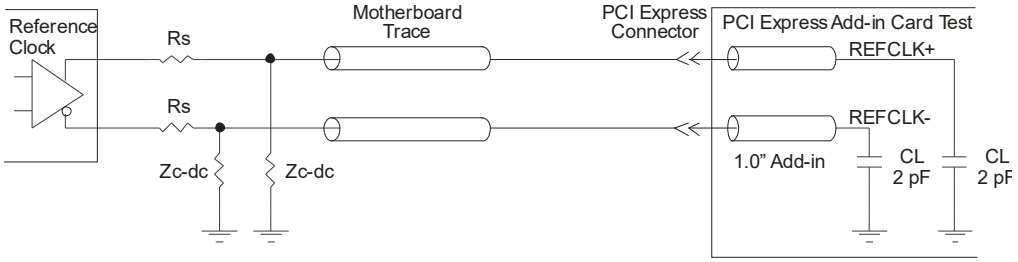


Figure 68 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. Then, when selecting tests, navigate to "Reference Clock Tests" in the "PCIE 3.0 Tests" group.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

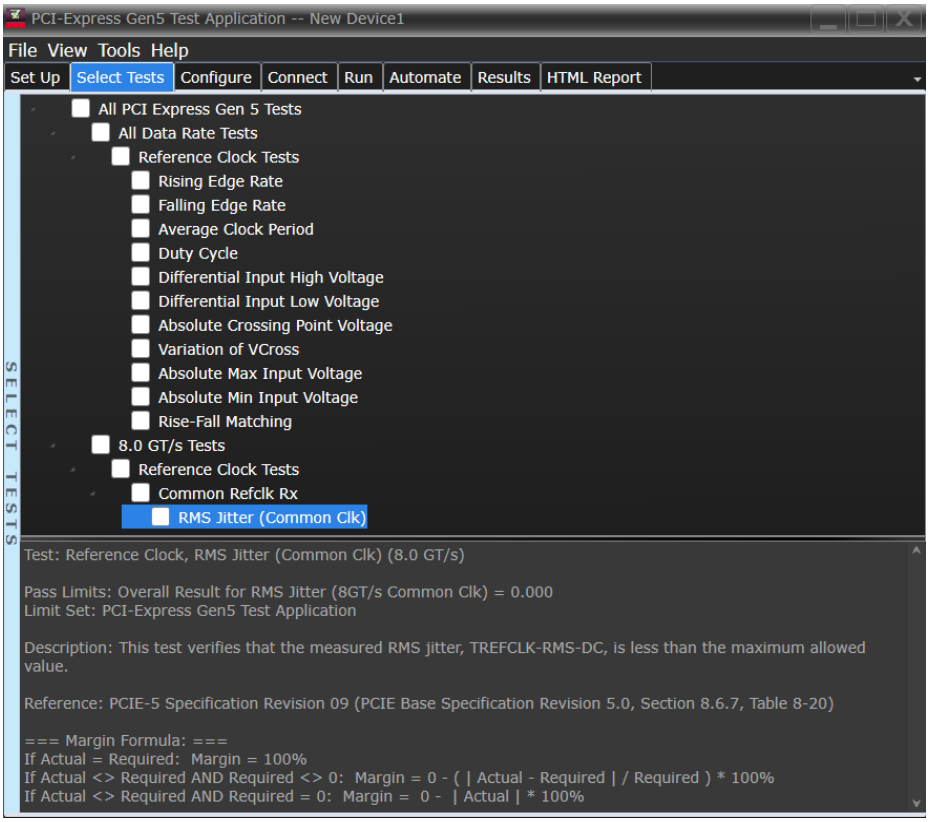


Figure 69 Selecting Reference Clock Tests when Clean Clock or SSC is Selected

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 77 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	1.0 ps RMS

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal frequency is ~100 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 GSa/s, clock rate 100 MHz, each UI takes up 200 points. So for memory depth of 50 M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9 Stitches each acquired acquisition to make a continuous TIE data.
10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies the PLL filter using parameters for common clocked architecture.
   c Converts back the frequency domain TIE data to time domains.
   d Computes the filtered peak-peak jitters and RMS jitter.
11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

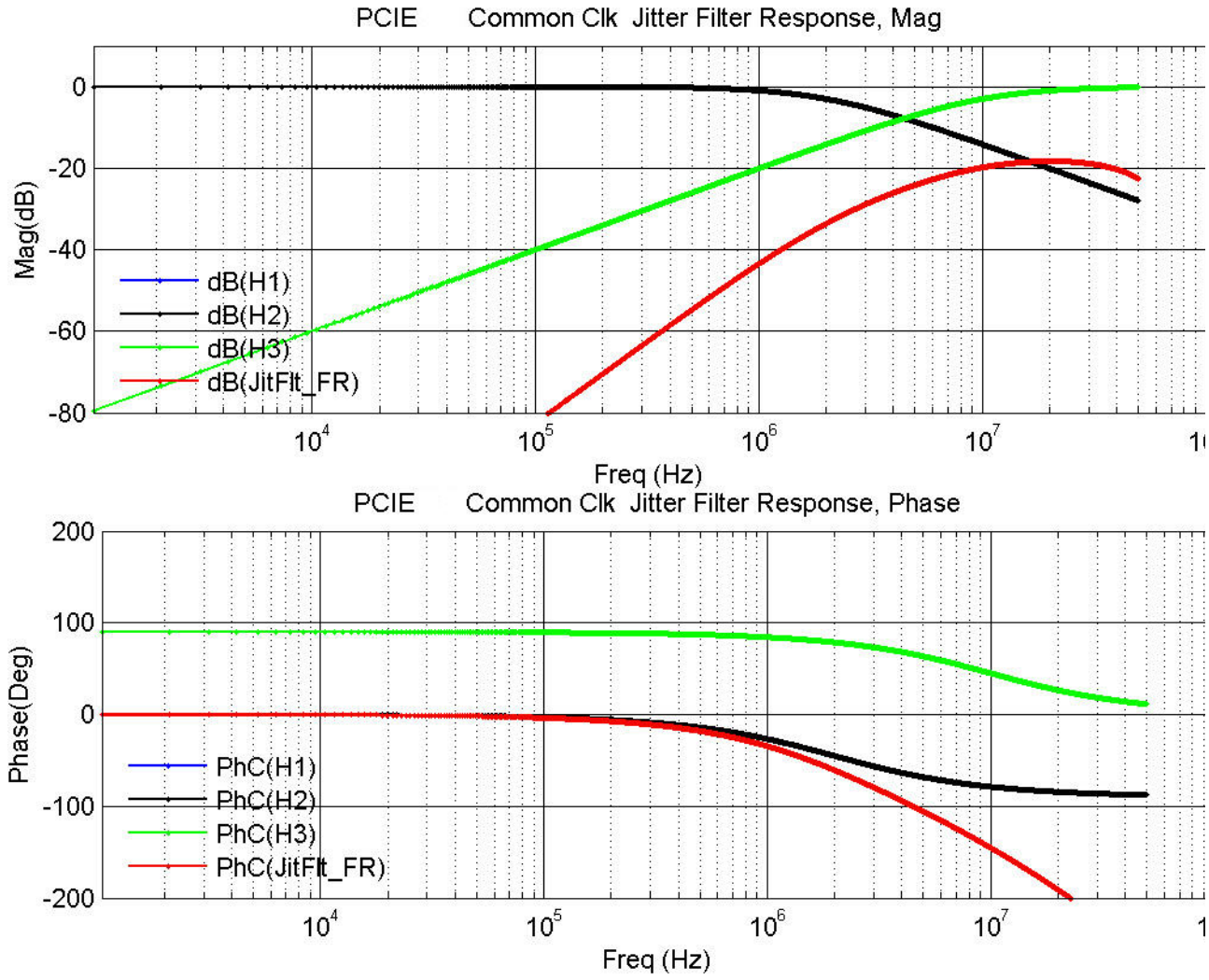


Figure 70 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

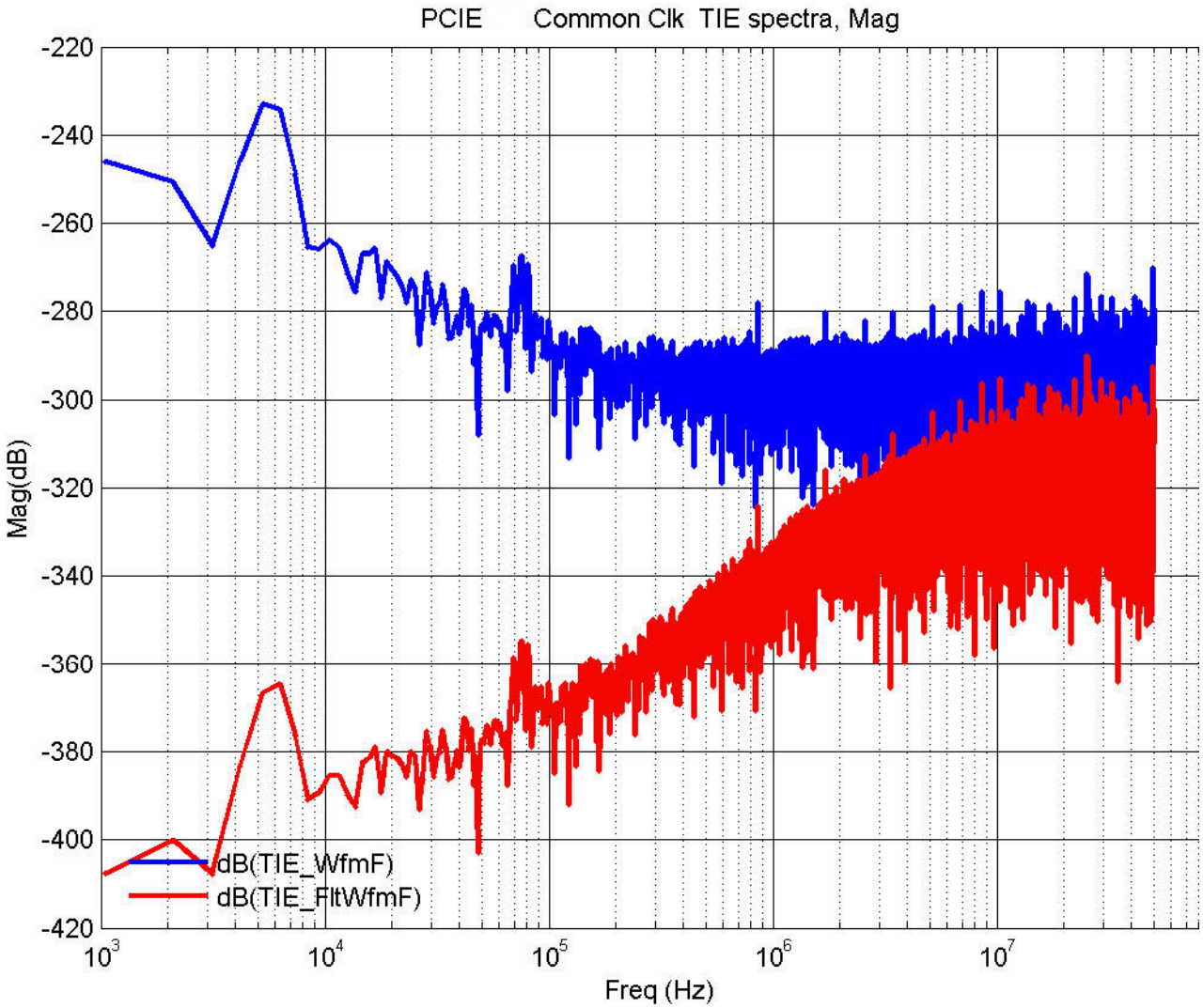


Figure 71 Reference Image for Common Clock TIE Spectra RMS Jitter Test

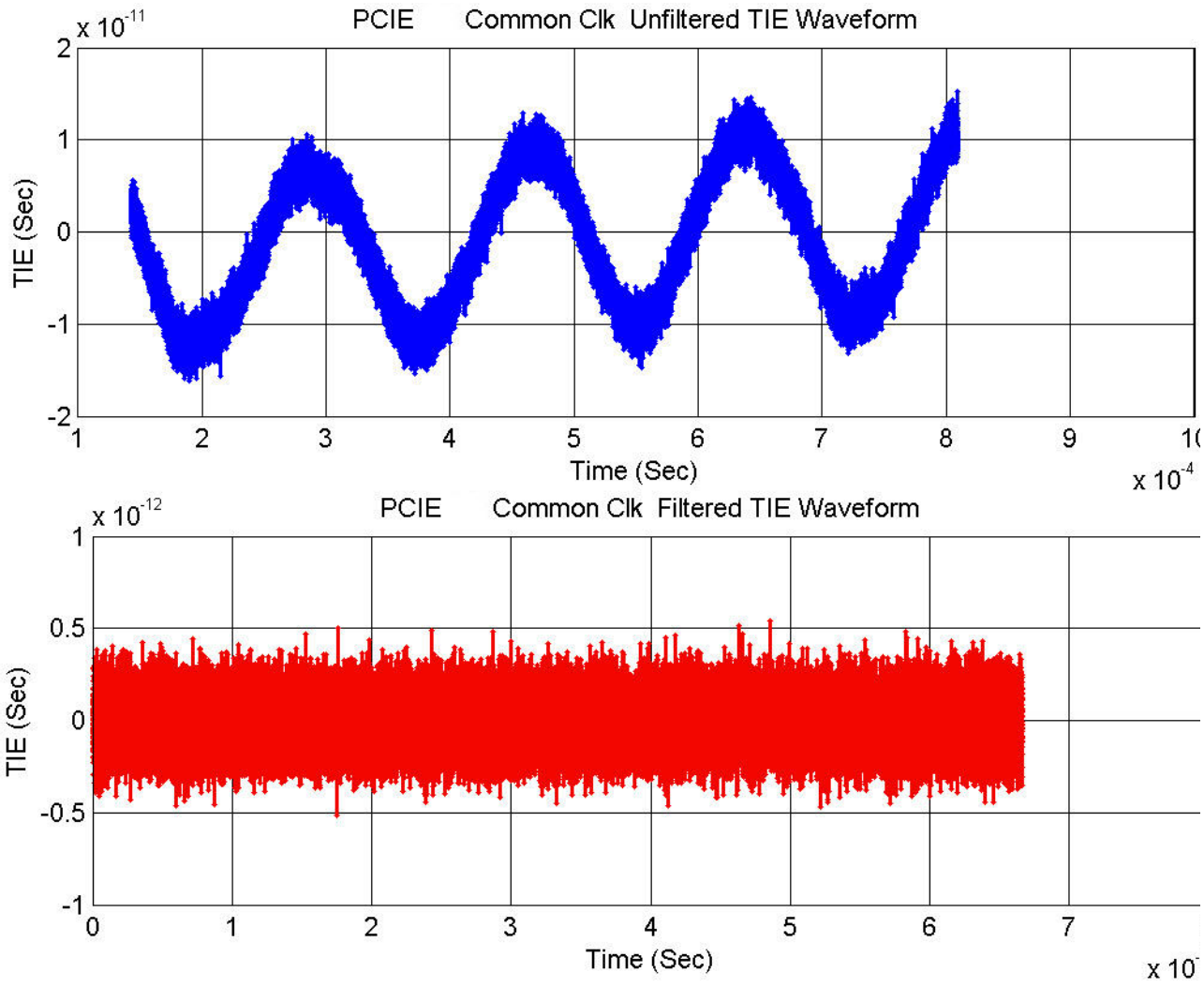


Figure 72 Reference Image for TIE Waveform RMS Jitter Test

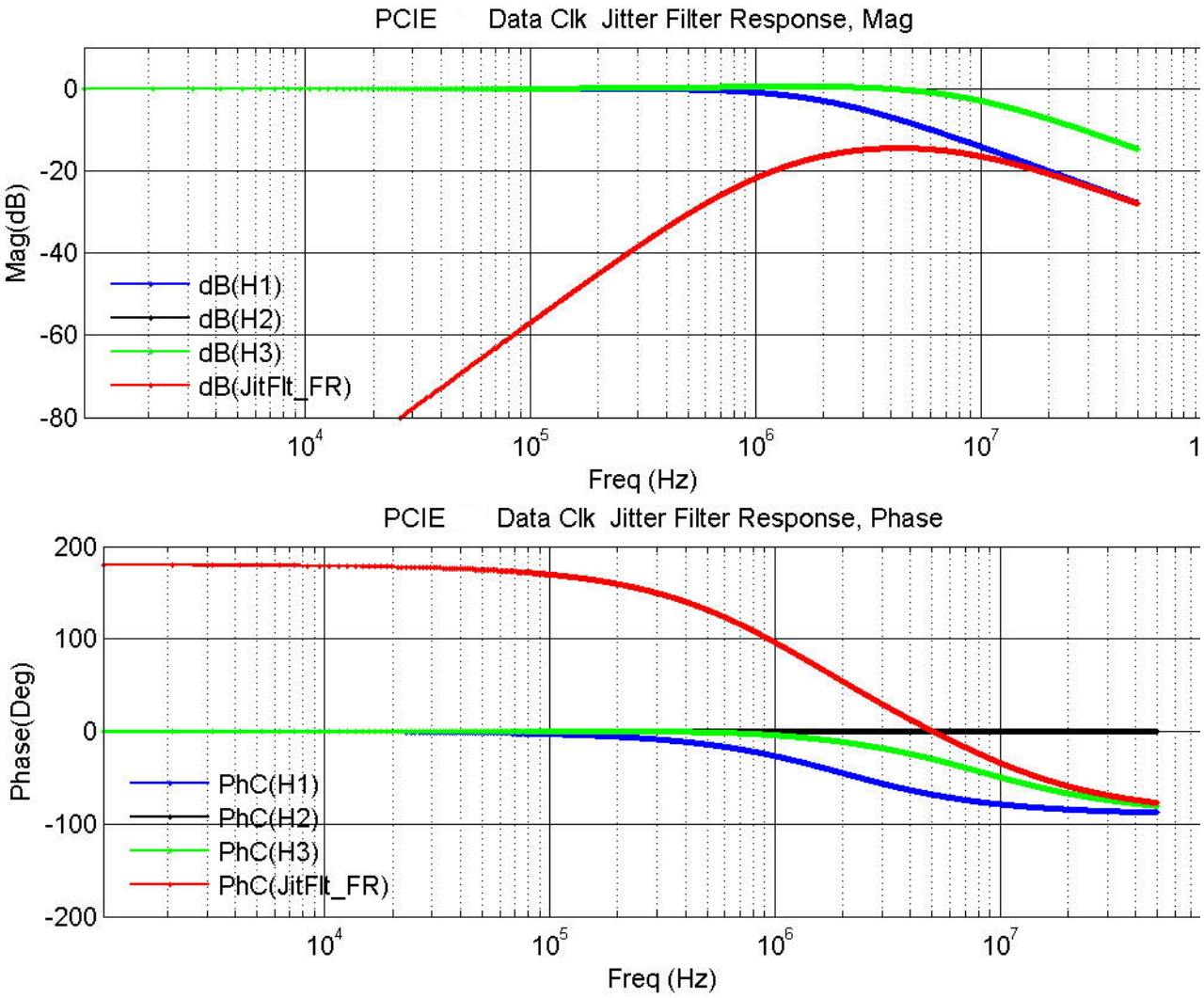


Figure 73 Reference Image for Jitter Filter Response (Data Clock) RMS Jitter Test

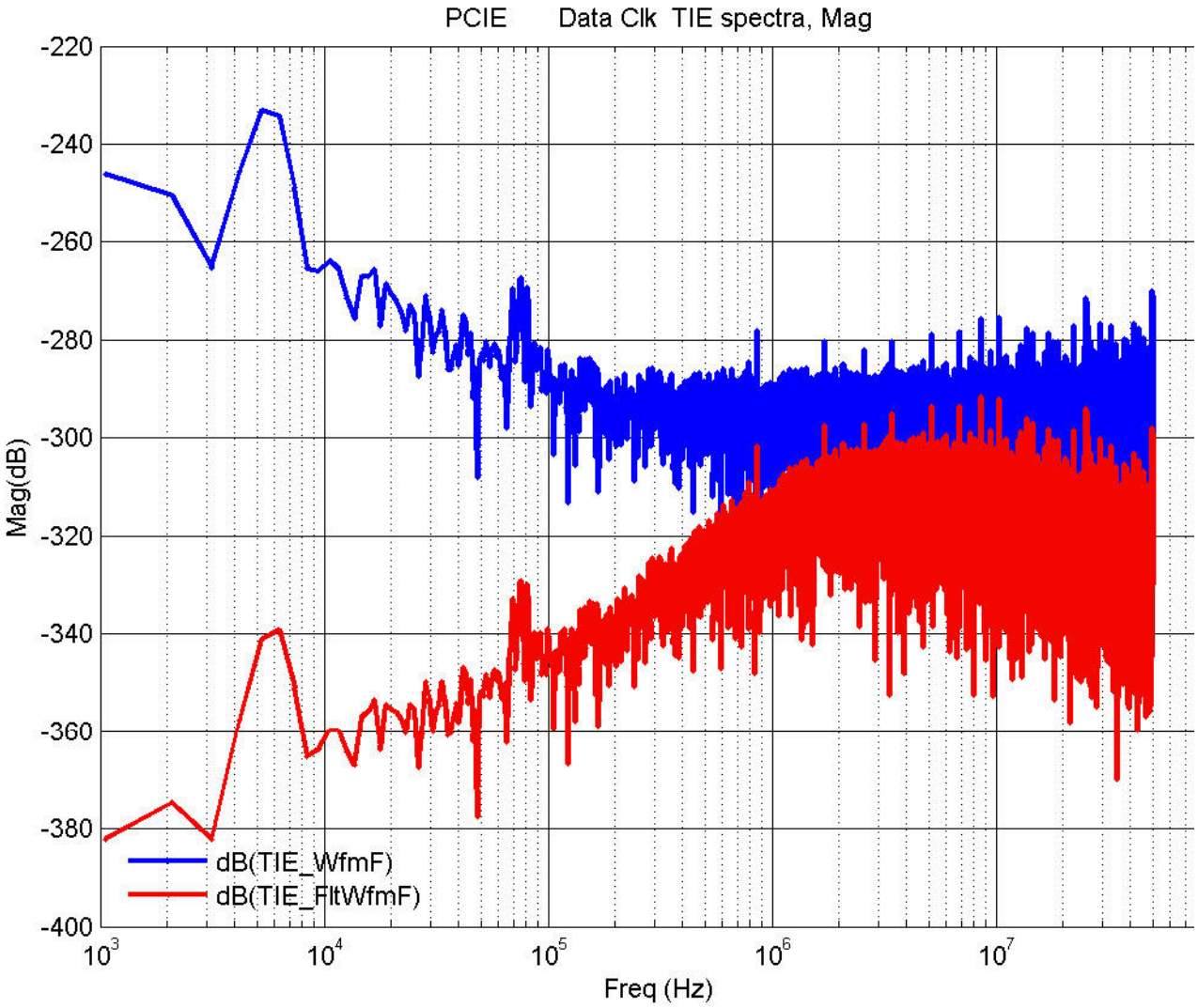


Figure 74 Reference Image for Data Clock TIE Spectra RMS Jitter Test

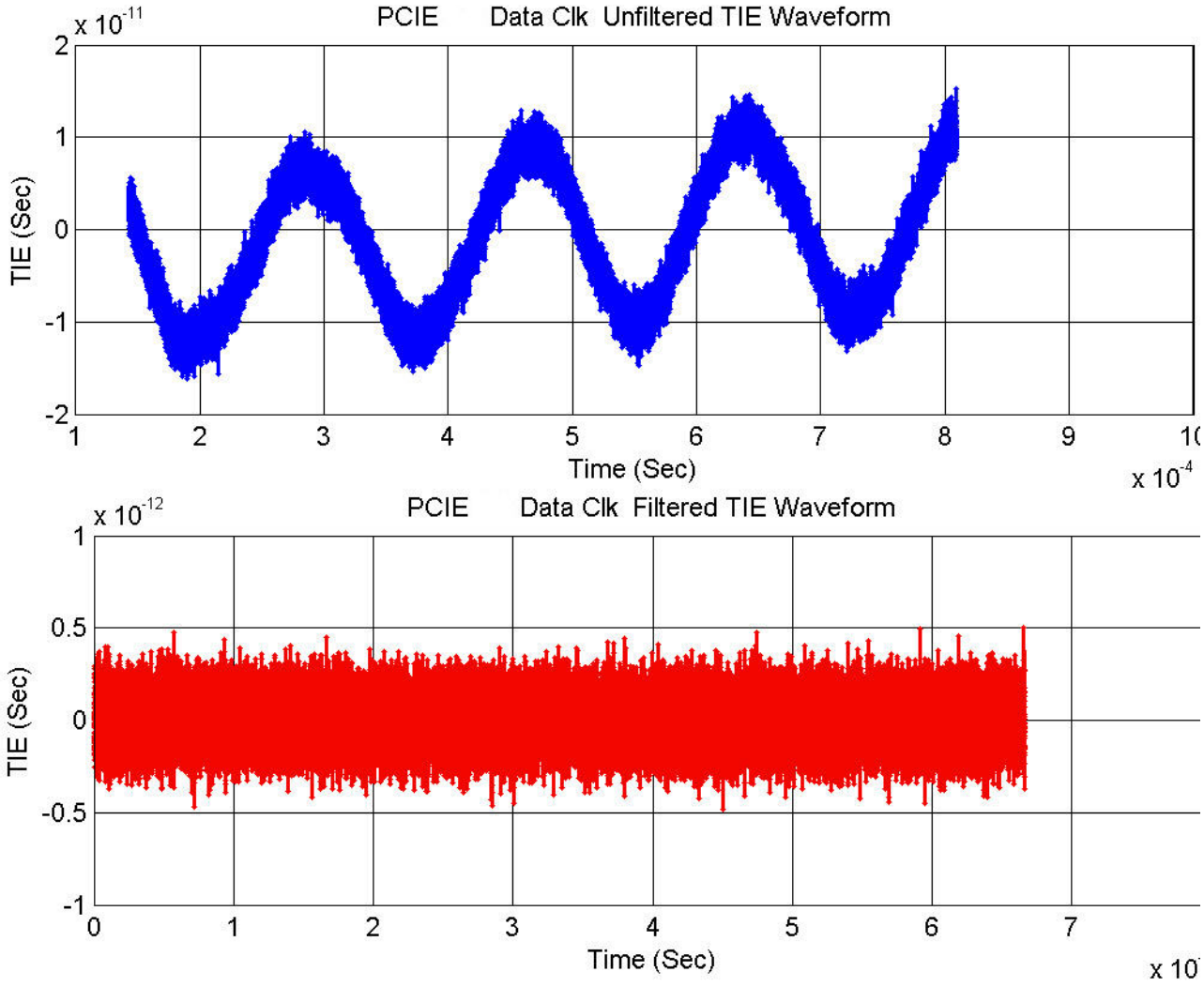


Figure 75 Reference Image for TIE Waveform RMS Jitter Test

Part VI
PCI-Express Gen5 16.0 GT/s Tests

KEYSIGHT TECHNOLOGIES

10 Transmitter (Tx) Tests, 16.0 GT/s, PCI-E 5.0

Tx Compliance Test Load / 226
Running Tx Tests / 227

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 16.0 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

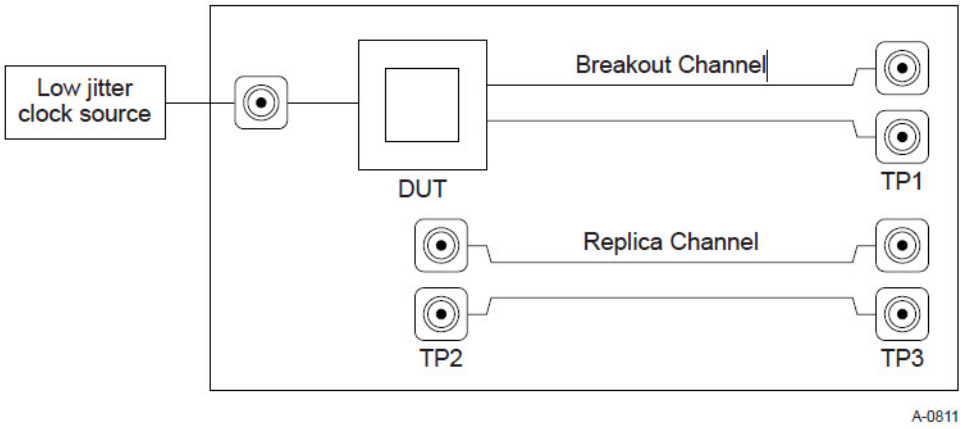


Figure 76 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. In the **Select Tests** tab, navigate to **All PCI Express Gen 5 Tests** > **16.0 GT/s Tests** > **Transmitter (Tx) Tests**.

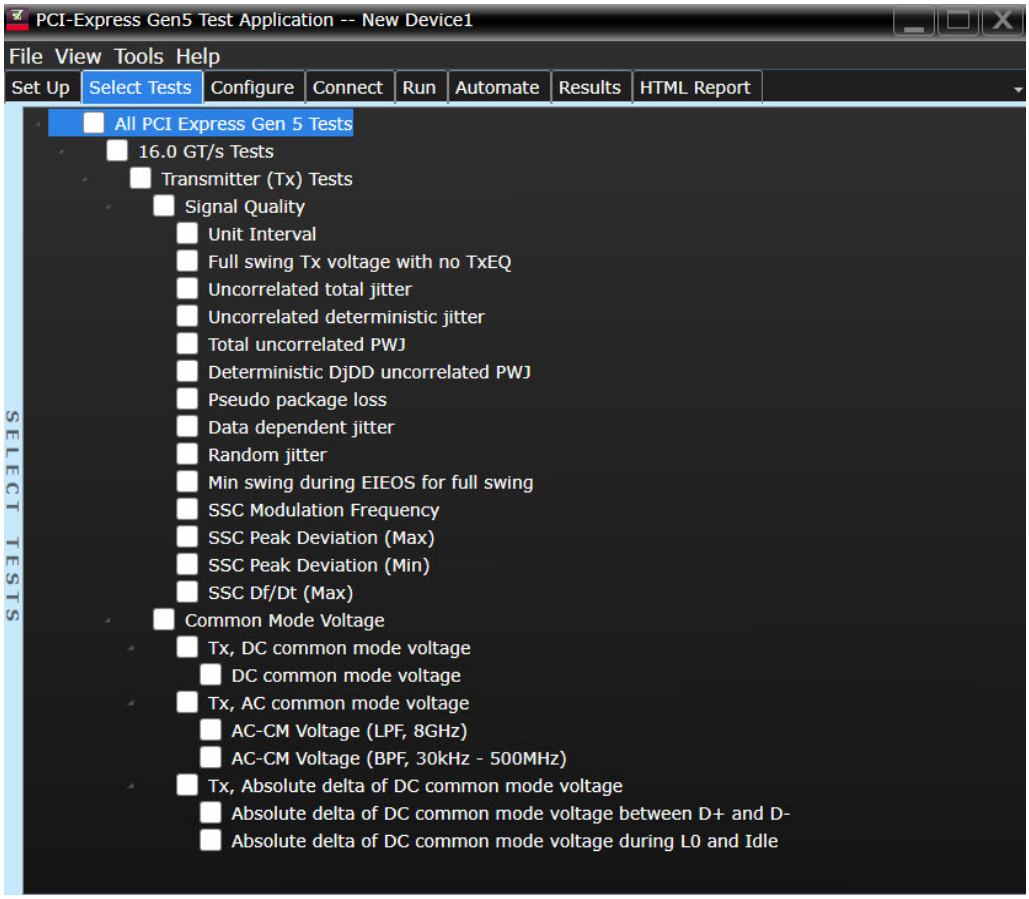


Figure 77 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 78 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	62.48125 ps	62.51875 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-300 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

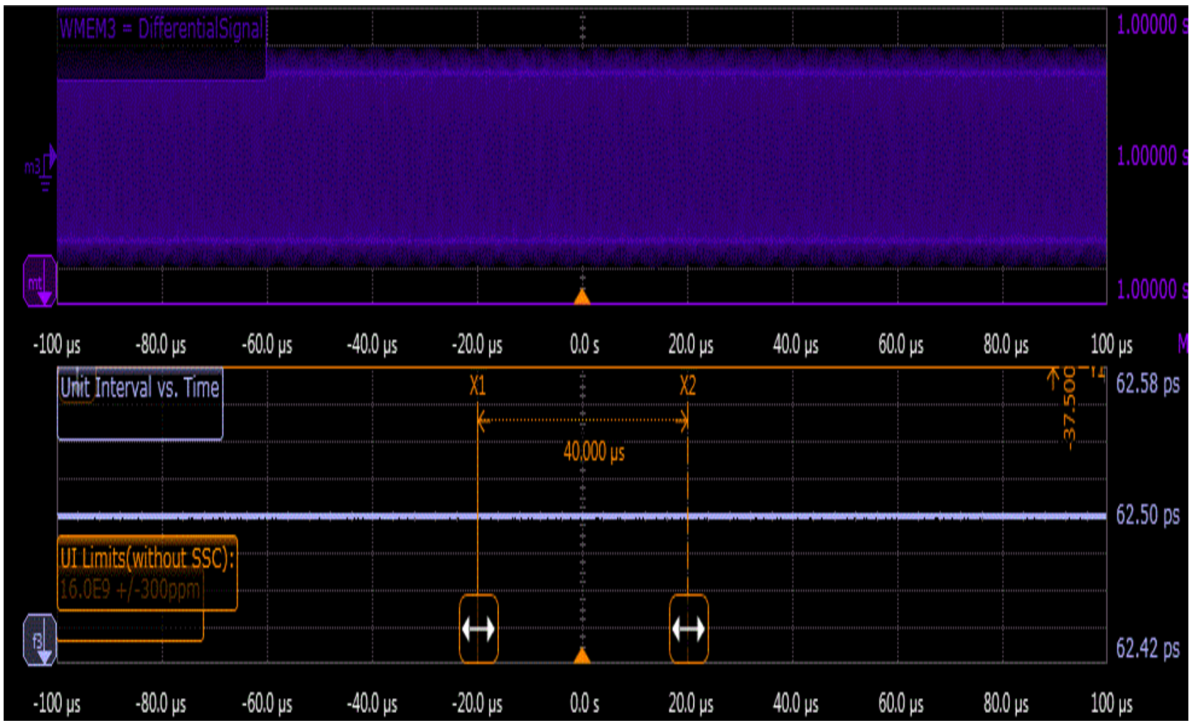


Figure 78 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 79. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP}$ is used as reference to check the compliance of the DUT.

Table 79 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX-FS-NO-EQ}$	Full swing Tx voltage with no TxEQ	800 mV	1300 mVPP

Test Definition Notes from the Specification

- 2.5 and 32.0 GT/s specify only one combination of PLL BW and jitter.
- A single combination of PLL BW and peaking is specified for 2.5 and 32.0 GT/s implementations. For other data rates, two combinations of PLL BW and peaking are specified to permit designers to make a trade-off between the two parameters.
- The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. The PLL BW is defined at the point where its transfer function crosses the -3dB point.

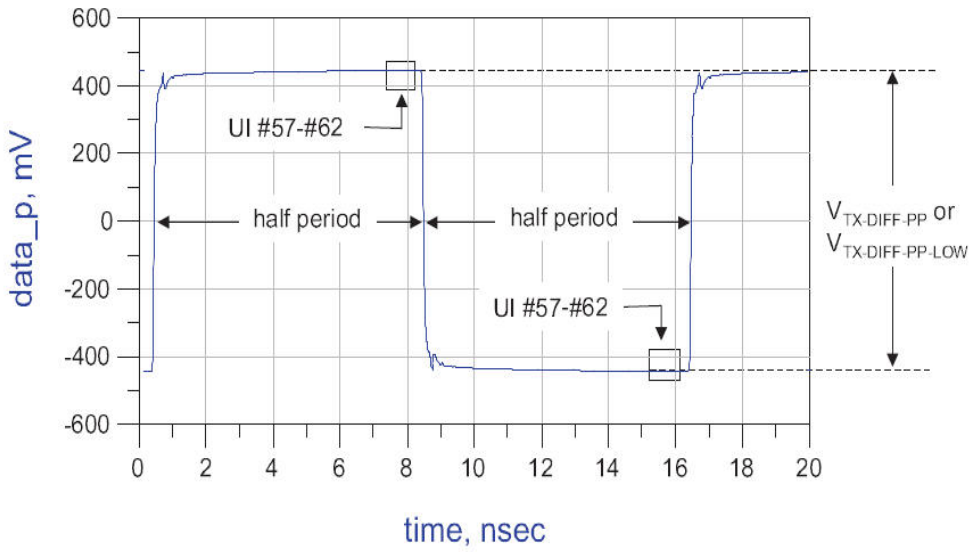


Figure 79 $V_{TX-DIFF-PP}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP-LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 80. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP-LOW}$ is used as reference to check the compliance of the DUT.

Table 80 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX-RS-NO-EQ}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mVPP	1300 mVPP

Test Definition Notes from the Specification

As measured with compliance test load. Defined as 2 × | VTXD+-VbTXD-|
See Section 8.3.3.4 and Section 8.3.3.5 for measurement details. For 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s no minimum voltage swing is specified as it is captured by VTX-BOOST-FS and VTX-BOOST-RS parameters.

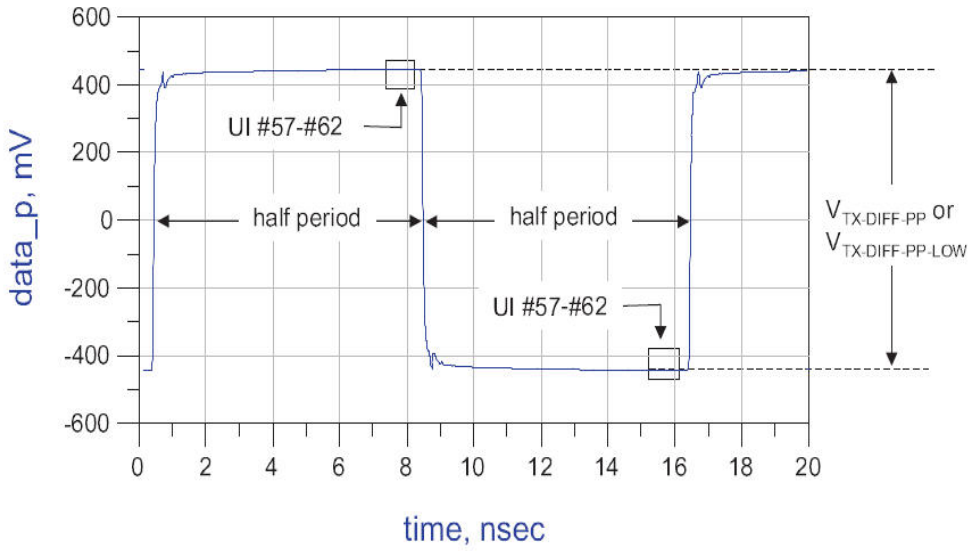


Figure 80 $V_{TX-DIFF-PP-LOW}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX\text{-}EIEOS\text{-}FS}$ is within the allowed range.

$V_{TX\text{-}EIEOS\text{-}FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of sixteen consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX\text{-}EIEOS\text{-}FS}$ for full swing signaling and by $V_{TX\text{-}EIEOS\text{-}RS}$ for reduced swing signaling. $V_{TX\text{-}EIEOS\text{-}RS}$ is smaller than $V_{TX\text{-}EIEOS\text{-}FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $VT_{X\text{-}EIEOS\text{-}FS}$ is measured with a preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6 Data Rate Dependent Transmitter Parameters. For reduced swing signaling $V_{TX\text{-}EIEOS\text{-}RS}$ is measured with preset P1.

Both $V_{TX\text{-}EIEOS\text{-}FS}$ and $V_{TX\text{-}EIEOS\text{-}RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 5-14 at 16.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX\text{-}EIEOS\text{-}FS}$ or $V_{TX\text{-}EIEOS\text{-}RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 81 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX\text{-}EIEOS\text{-}FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

VTX-EIEOS-FS and VTX-EIEOS-RS are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0 and 32.0 GT/s that ensures that these parameters are met.

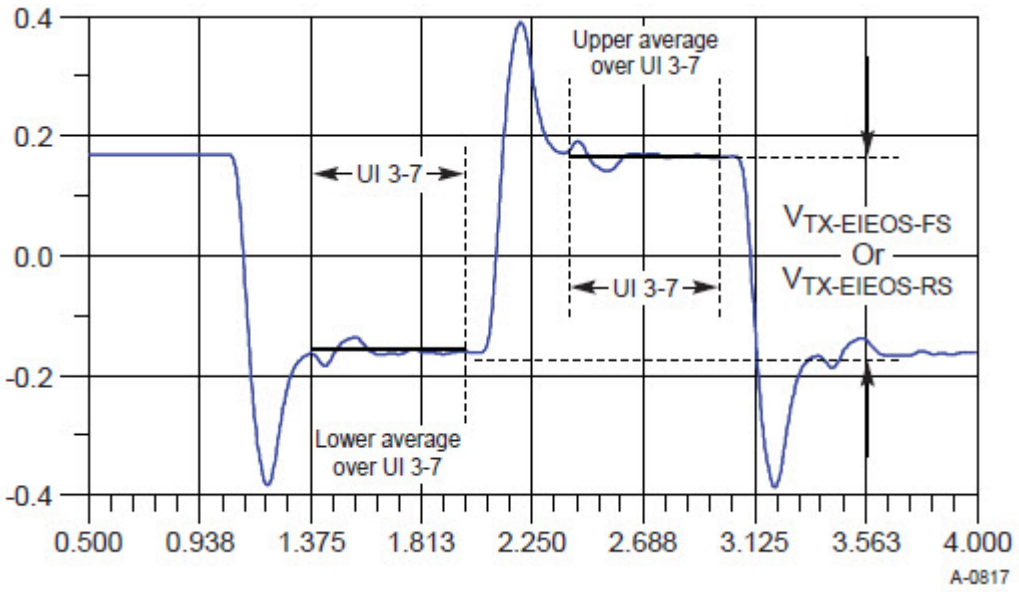


Figure 81 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX-EIEOS-RS}$ is within the allowed range.

$V_{TX-EIEOS-RS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of sixteen consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c_{+1} coefficient value of -0.33 and a c_{-1} coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 9-5. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c_{+1} coefficient value of -0.167 and a c_{-1} coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 5-14. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 82 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232 mVPP

Test Definition Notes from the Specification

VTX-EIEOS-FS and VTX-EIEOS-RS are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, and 32.0 GT/s that ensures that these parameters are met.

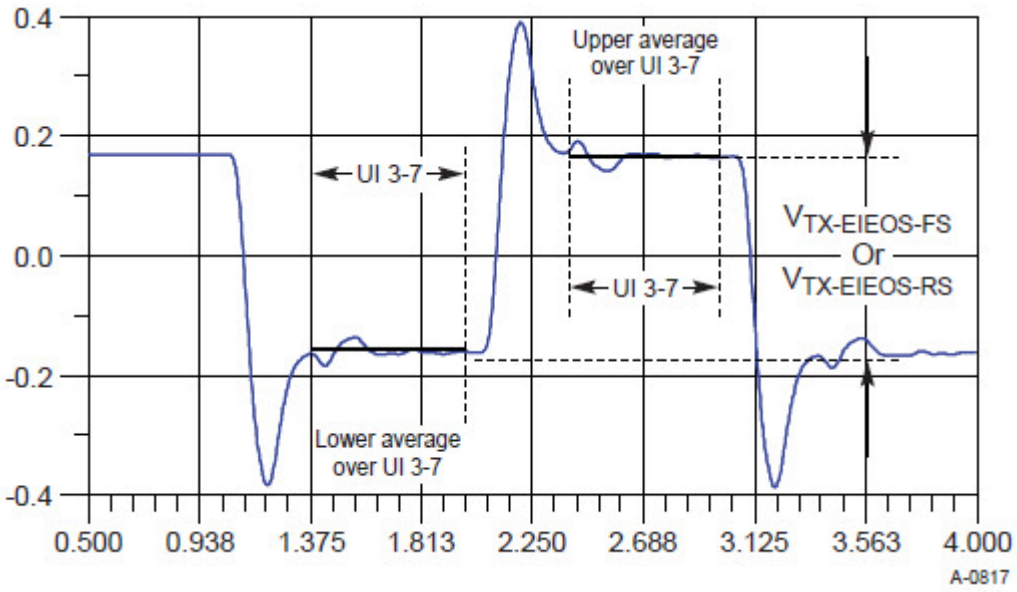


Figure 82 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 83 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	11.8 ps PP at 10^{-12}

Test Definition Notes from the Specification

For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 84 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	6.25 ps PP

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 85 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	12.5 ps PP at 10^{-12}

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 86 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	5 ps PP

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter (Information-Only Test)

This test verifies that the maximum data dependent jitter, $T_{TX\text{-}DDJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.5.7 is used as reference.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

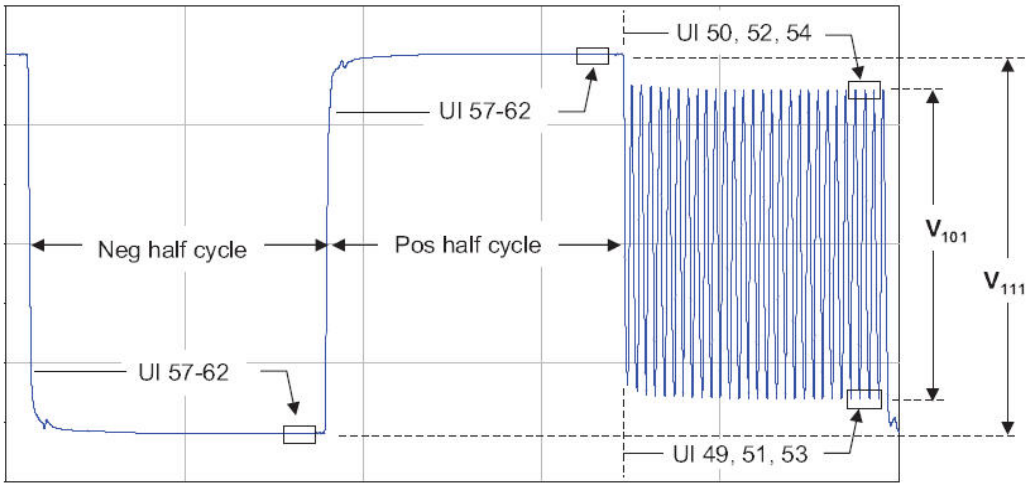
PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 87 Pseudo Package Loss Test Details

Symbol	Parameter	Max
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for a device containing root ports	5.0 dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for all devices not containing root ports	5.0 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 83 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the number of package loss measurements taken.
8. Reports the package loss ration value.
9. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter Test

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 88 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	0.40 - 0.84 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJ-DD}$.
- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 89 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Sets up DC common mode voltage as follows:
   a Enables and displays common mode measurements.
   b Loads common mode signal to waveform memory.
   c Loads and enhance dynamic range D+ signal and D- signal.
   d Enables the average common mode measurement.
   e Uses markers to indicate compliance test limit boundaries (0V to 3.6V).
4 Measures the average value of D+ and D- signal.
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.

6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 4.0 as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 8 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 90 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}CM\text{-}AC\text{-}PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 4 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX-CM-AC-PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX-AC-CM-PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 91 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX-AC-CM-PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 8 GHz) test.

1 Gets PCIE5 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX-CM-DC-LINE-DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX-CM-DC-D+[during\ L0]} - V_{TX-CM-DC-D-[during\ L0]}| \leq 25\ mV$

$V_{TX-CM-DC-D+} = DC_{(avg)}$ of $|V_{TX-D+}|$ [during L0]

$V_{TX-CM-DC-D-} = DC_{(avg)}$ of $|V_{TX-D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 92 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT..

Table 93 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

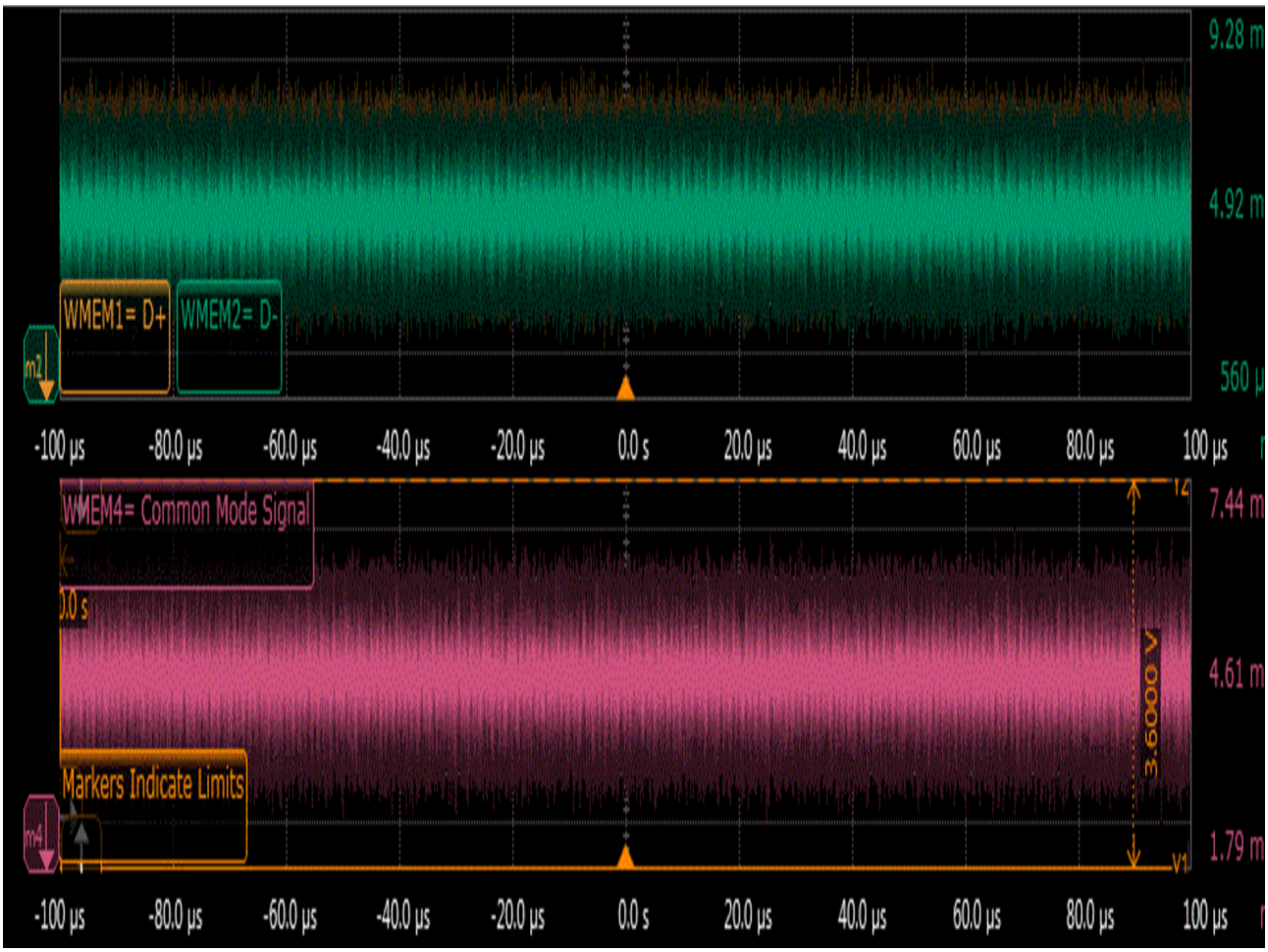


Figure 84 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 94 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 16.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 95 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	0.0%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 16.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 96 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION}$	SSC deviation	-0.5%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 16.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 97 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt	1250 ppm/µs

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1^{st} order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures memory depth and sampling rate as per the data rate.

3 Fits and displays all sample data on screen.

4 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.

5 Analyzes measurements trend using the jitter **Meas Trend** function.

6 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:

a Generates a differential plot (x_n - x_{n-1}).

b The maximum slew rate corresponds to the peak of the differential plot.

7 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

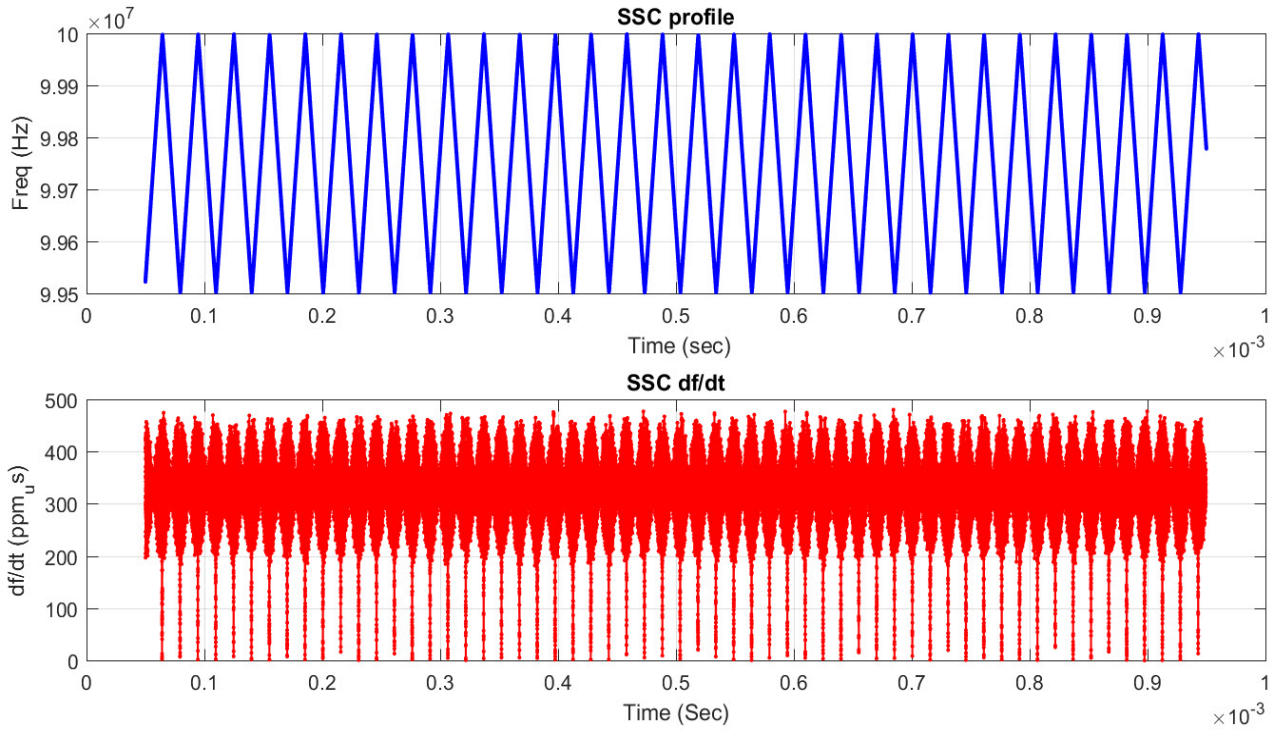


Figure 85 Maximum SSC Slew Rate

Running Equalization Presets Tests

Please refer to section: "Running Equalization Presets Tests" on page 174 in Chapter 8, "Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 5.0"

11 Reference Clock Tests, 16.0 GT/s, PCI-E 5.0

Reference Clock Architectures / 264
Reference Clock Measurement Point / 266
Running Reference Clock Tests / 267

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 16.0 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

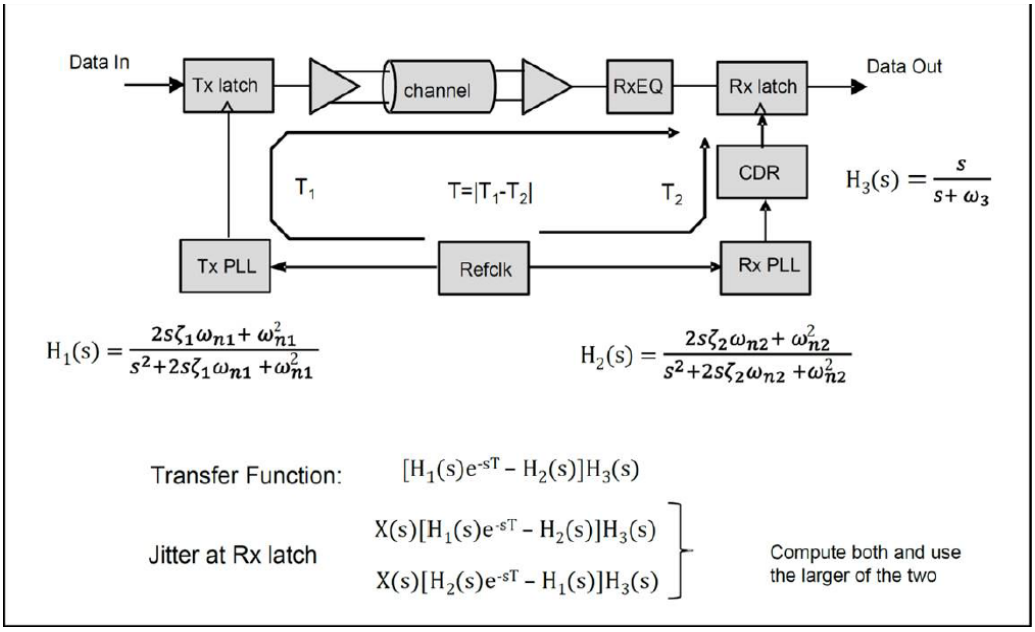
NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 16.0 GT/s, PCI-E 5.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73	BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73	BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15
BW_{CDR}(min) = 10 MHz, 1st order	64 combinations				

8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.6.1, Figure 8-64.

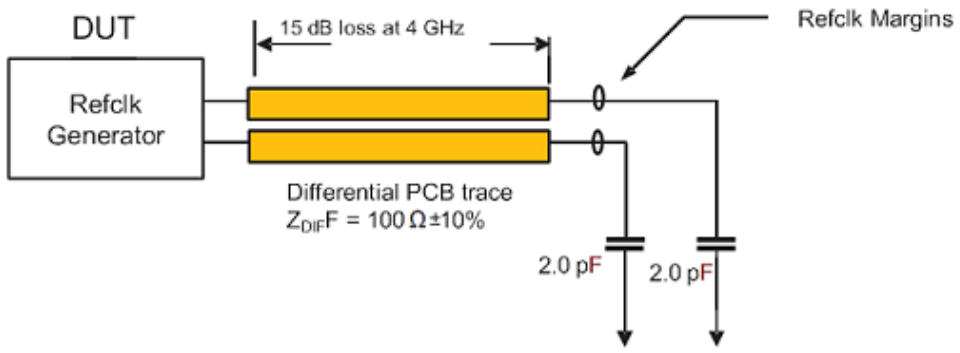


Figure 86 Driver Compliance Test Load

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. Then, when selecting tests, navigate to "Reference Clock Tests" in the "PCIE 4.0 Tests" group.

Note that selecting "SSC" or "Clean Clock" under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

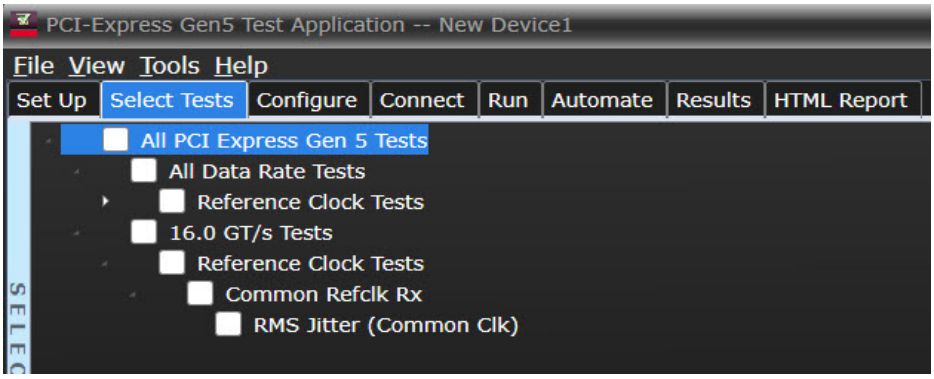


Figure 87 Selecting Reference Clock Tests when SSC or Clean Clock is Selected

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 98 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	0.5 ps RMS

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9 Stitches each acquired acquisition to make a continuous TIE data.
10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies the PLL filter using parameters for common clocked architecture.
   c Converts back the frequency domain TIE data to time domains.
   d Computes the filtered peak-peak jitters and RMS jitter.
11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

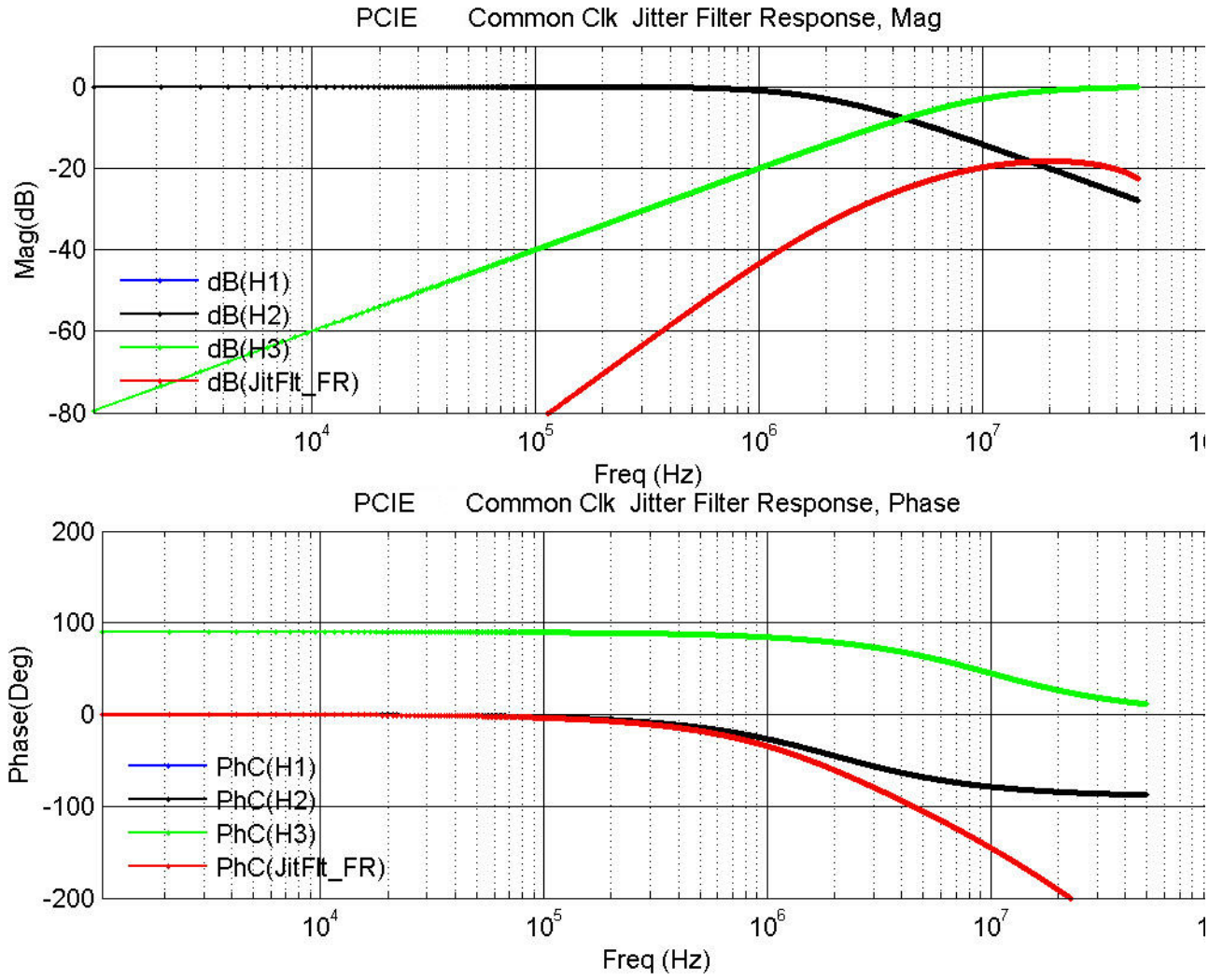


Figure 88 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

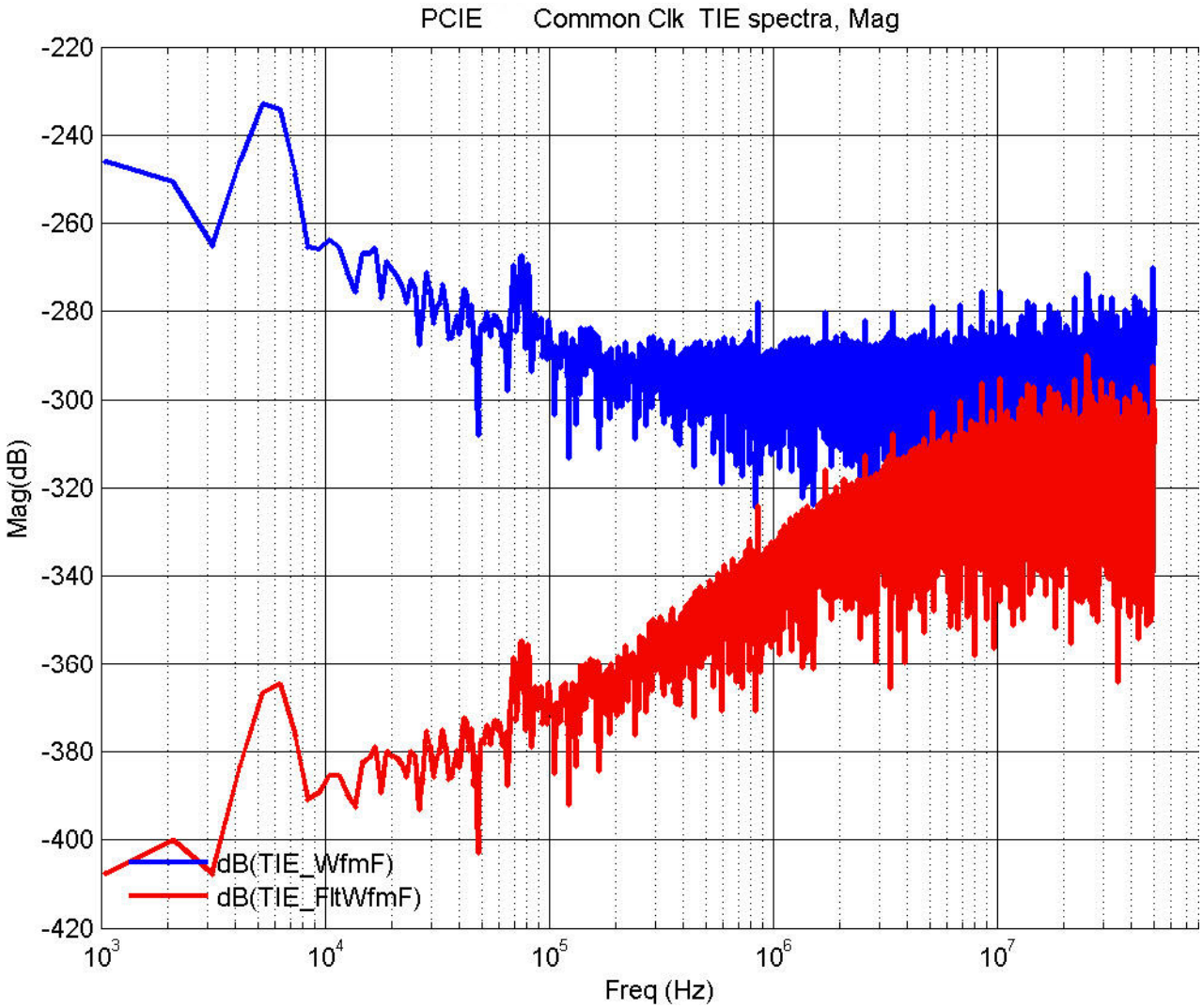


Figure 89 Reference Image for Common Clock TIE Spectra RMS Jitter Test

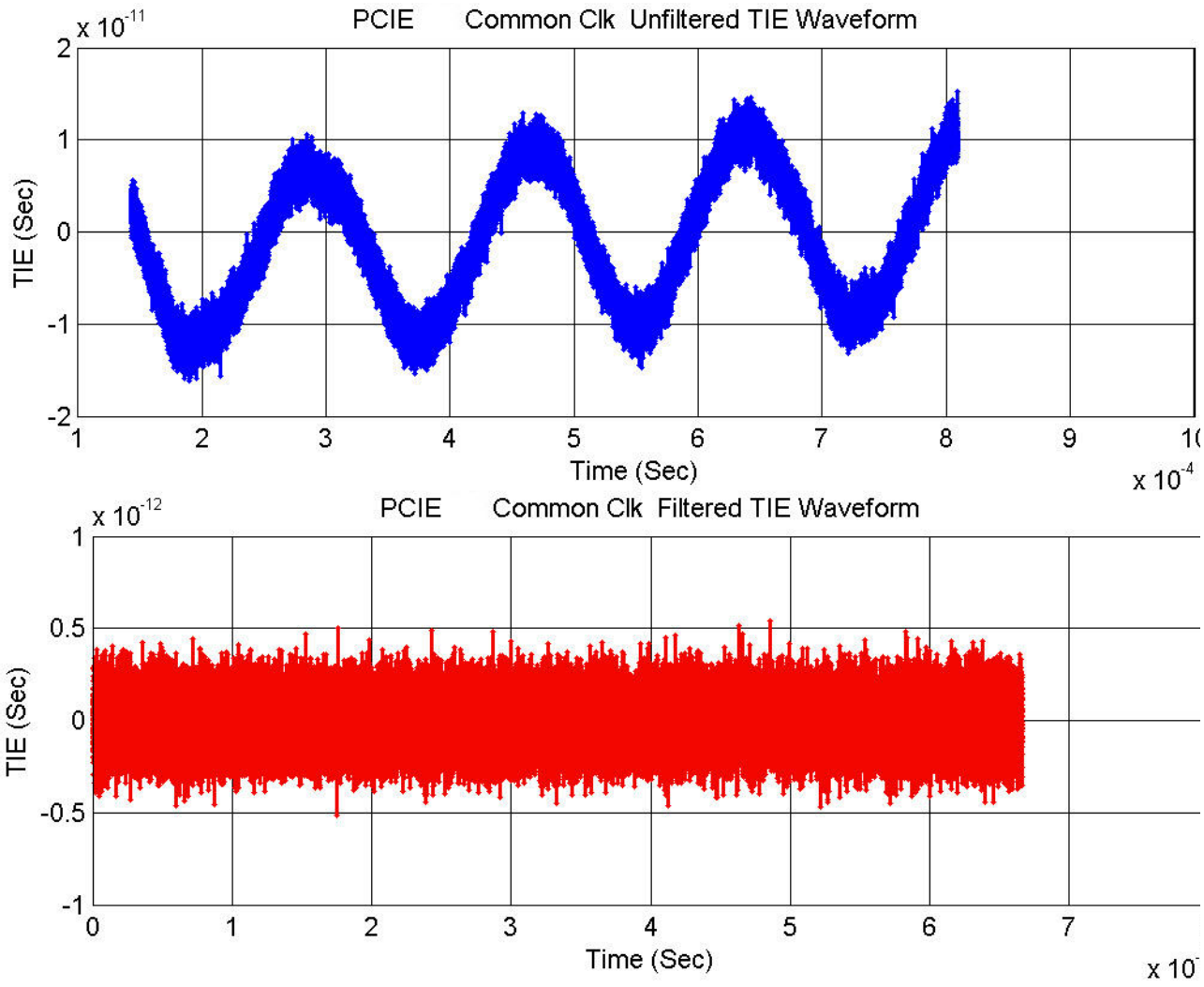


Figure 90 Reference Image for TIE Waveform RMS Jitter Test

Part VII
PCI Express Gen5 32.0 GT/s Tests

KEYSIGHT TECHNOLOGIES

12 Transmitter (Tx) Tests, 32.0 GT/s, PCI-E 5.0

Tx Compliance Test Load / 276
Running Tx Tests / 277

This section provides the Methods of Implementation (MOIs) for PCI-E 5.0 Transmitter (Tx) tests at 32.0 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Tx Compliance Test Load

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.3.1, Figure 8-1.

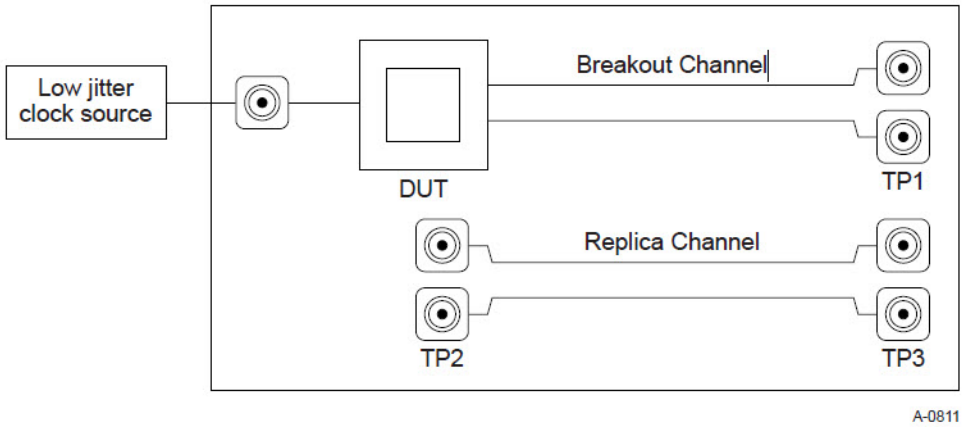


Figure 91 Driver Compliance Test Load

Running Tx Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. In the **Select Tests** tab, navigate to **All PCI Express Gen 5 Tests** > **32.0 GT/s Tests** > **Transmitter (Tx) Tests**.

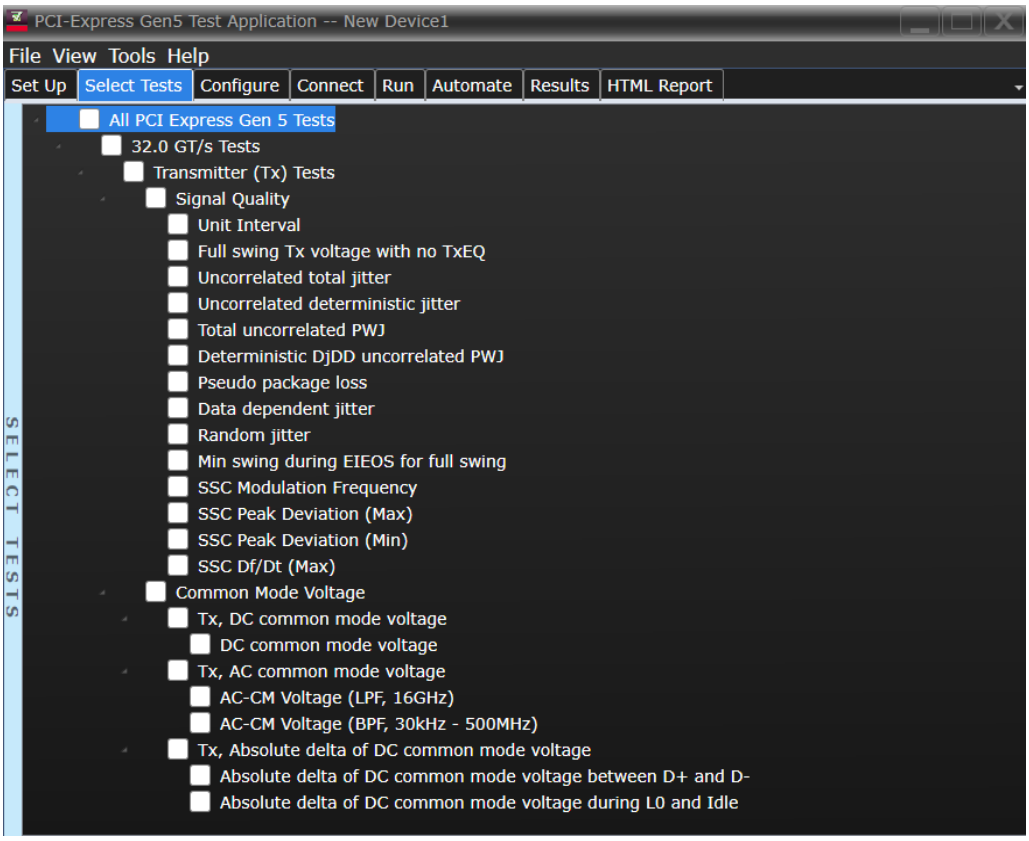


Figure 92 Selecting Transmitter (Tx) Tests

Unit Interval Test

A recovered transmitter unit interval (UI) is calculated over 2,000,000 consecutive unit intervals of sample data as the mean unit interval over the clock recovery window as follows:

$$T_x \qquad UI(p) = Mean \qquad (UI(n))$$

Where,

'n' is the index of UI in the current 2,000,000 UI clock recovery window.

'p' indicates the p^{th} 2,000,000 UI clock recovery window advanced from the beginning of the data by p*100 UI.

The T_X UI is computed over 2,000,000 UI. The clock recovery window is then advanced by 100 UI, and another T_X UI is computed. This process repeats until the clock recovery window advances beyond the end of the data record. The worst case T_X UI is reported.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 99 Unit Interval Test Details

Symbol	Parameter	Min	Max
UI	Unit Interval	31.246875 ps	31.253125 ps

Test Definition Notes from the Specification

- The specified UI is equivalent to a tolerance of +/-100 ppm for each Refclk source.
- Period does not account for SSC induced variations.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Fits and displays all sample data on screen.
3 Analyzes unit interval of the test signal using the **Measurement Analysis (EZJIT)...** option.
   a Selects **Unit Interval** as data measurement analysis unit.
   b Configures the **Smoothing Points** to 3499 in the **Measurement Trend** dialog box.
4 Indicates the upper and lower limit of the measured data using markers.
5 Measures the minimum, mean and maximum values of the UI.
6 Reports mean UI as the measurement result and verifies that the value of UI is as per the conformance limits specified in the PCI Express Base Specification, Rev 5.0.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

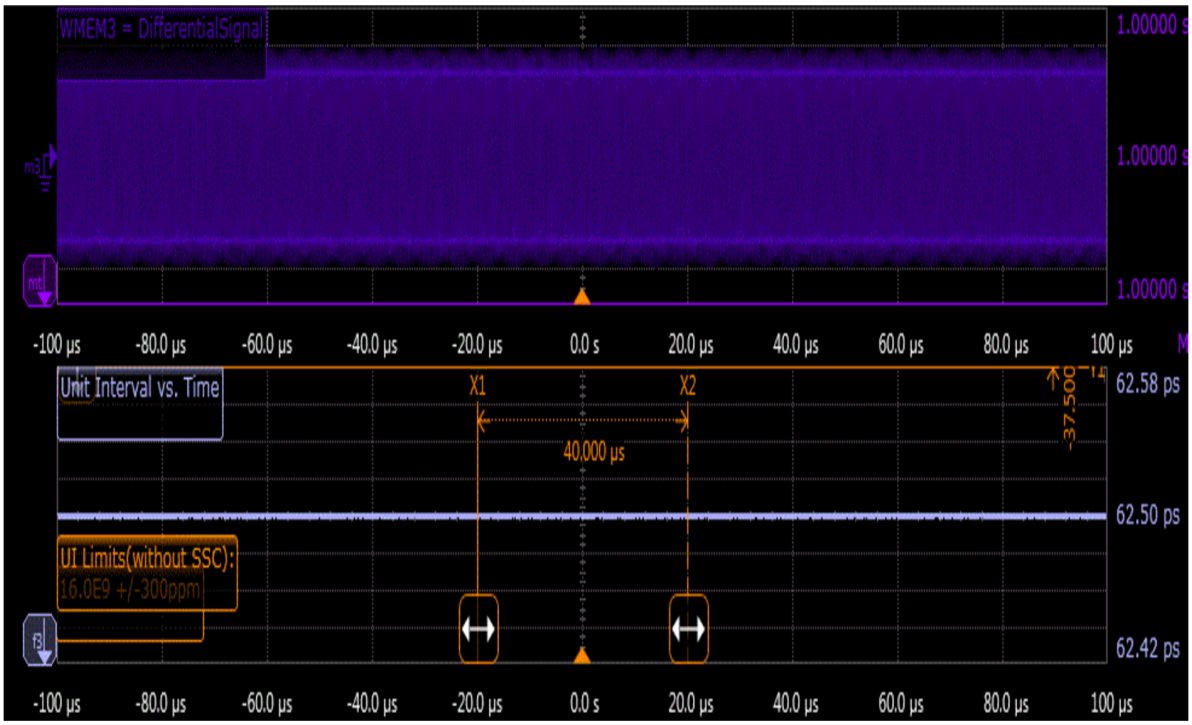


Figure 93 Reference Image for Unit Interval Test

Full Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during full swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX-DIFF-PP}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 94. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX-DIFF-PP}$ is used as reference to check the compliance of the DUT.

Table 100 Full Swing Tx Voltage with no TxEQ Details

Symbol	Parameter	Min	Max
$V_{TX-DIFF-PP}$	Full swing Tx voltage with no TxEQ	800 mV	1300 mVPP

Test Definition Notes from the Specification

- 2.5 and 32.0 GT/s specify only one combination of PLL BW and jitter.
- A single combination of PLL BW and peaking is specified for 2.5 and 32.0 GT/s implementations. For other data rates, two combinations of PLL BW and peaking are specified to permit designers to make a trade-off between the two parameters.
- The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. The PLL BW is defined at the point where its transfer function crosses the -3dB point.

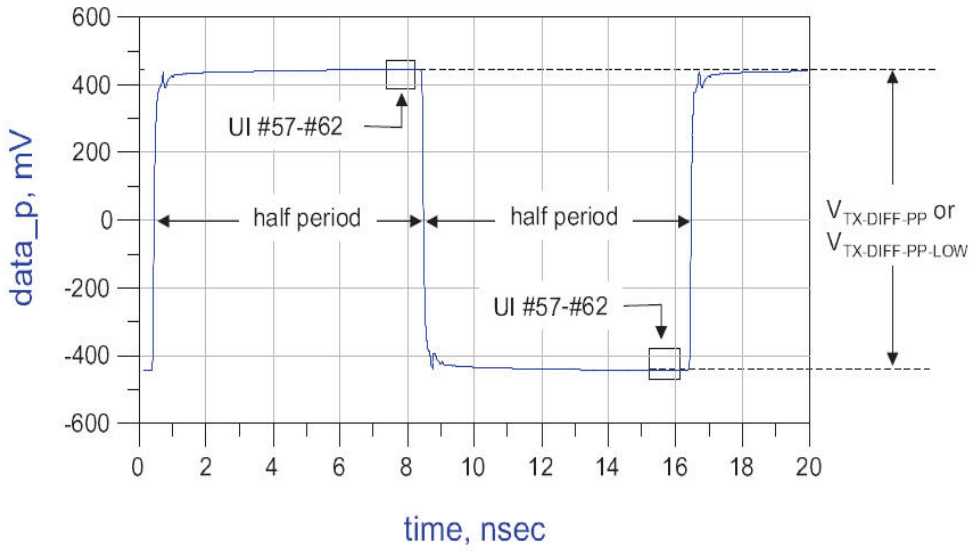


Figure 94 $V_{TX-DIFF-PP}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0 µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Reduced Swing Tx Voltage with no TxEQ Test

This test verifies that the voltage swing at the transmitter with no equalization during reduced (half) swing signaling is within the conformance limits specified in Table 8-6 of the PCIE Base Specification, rev. 5.0. The range for a Transmitter's output voltage swing, (specified by Vd) with no equalization is defined by $V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$, and is obtained by setting c_{-1} and c_{+1} to zero and measuring the peak-peak voltage on the 64-ones/64-zeroes segment of the compliance pattern. The resulting signal effectively measures at the die pad, minus any low frequency package loss. ISI and switching effects are minimized by restricting the portion of the curve over which voltage is measured to the last few UI of each half cycle, as illustrated in Figure 95. High frequency noise is mitigated by averaging over 500 repetitions of the compliance pattern

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6, $V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$ is used as reference to check the compliance of the DUT.

Table 101 Reduced Swing Tx Voltage with no TxEQ Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$	Reduced Swing Tx Voltage with no TxEQ Test	400 mVPP	1300 mVPP

Test Definition Notes from the Specification

As measured with compliance test load. Defined as 2 × | VTXD+-VbTXD-|
See Section 8.3.3.4 and Section 8.3.3.5 for measurement details. For 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s no minimum voltage swing is specified as it is captured by $V_{TX\text{-}BOOST\text{-}FS}$ and $V_{TX\text{-}BOOST\text{-}RS}$ parameters.

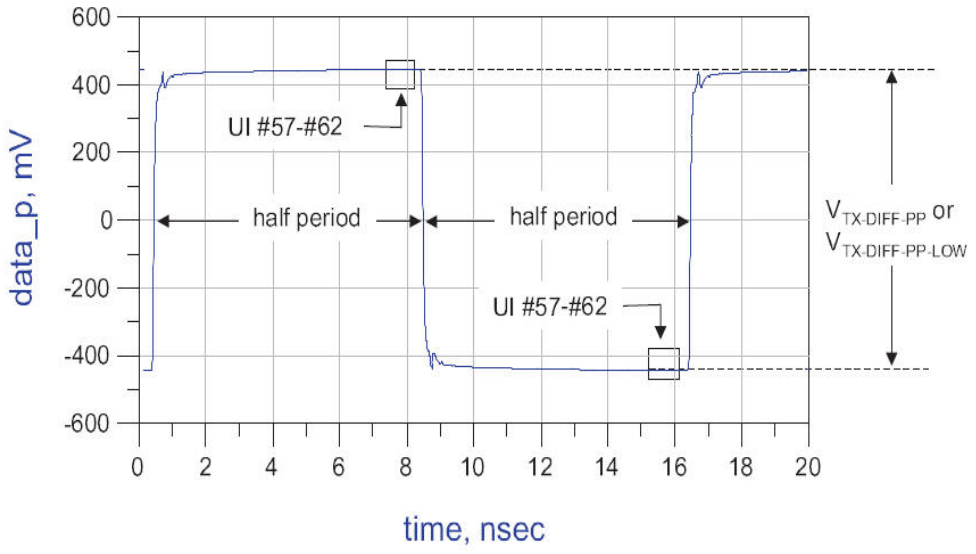


Figure 95 $V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$ Measurement

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures the DUT to operate in preset value #P4.
3 Configures memory depth and sampling rate as per the data rate.
4 Sets the **Horizontal Domain Scale** to 20.0µs.
5 Fits and displays all sample data on screen.
6 Saves the P4 signal into *.bin format.
7 Inputs the P4 saved waveform into SigTest tool.
8 Computes the measurement of Vb at preset value P4.
9 Reports the measurement of Vb during preset values P4.
10 Compares the de-emphasis value to the compliance test limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Full Swing Test

This test verifies that the minimum swing during EIEOS for full swing $V_{TX-EIEOS-FS}$ is within the allowed range.

$V_{TX-EIEOS-FS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of thirty two consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI; at 32.0 GT/s the pattern is repeated for two consecutive blocks. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $VT_{X-EIEOS-FS}$ is measured with a preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 8-6 Data Rate Dependent Transmitter Parameters. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 9-28 at 32.0 GT/s. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages.
UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 102 Min Swing During EIEOS for Full Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-FS}$	Min swing during EIEOS for full swing	250 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, and 32.0 GT/s that ensures that these parameters are met.

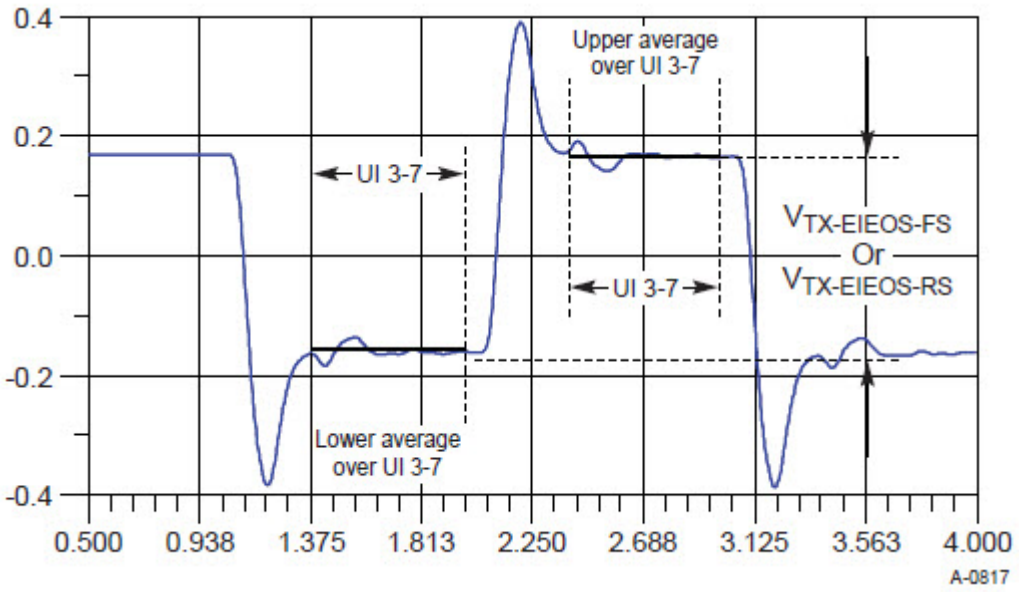


Figure 96 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Min Swing During EIEOS for Reduced Swing Test

This test verifies that the minimum swing during EIEOS for reduced swing $V_{TX-EIEOS-RS}$ is within the allowed range.

$V_{TX-EIEOS-RS}$ are measured using the EIEOS sequence contained within the compliance pattern. This pattern consists of thirty two consecutive ones followed by the same number of consecutive zeros, where the pattern is repeated for a total of 128 UI. The loss effect of the breakout channel may be appreciable at the EIEOS signaling frequency, so its loss effects must be taken into account to yield an equivalent voltage at the Tx pin. Typically this requires de-embedding. A transmitter sends out a unique EIEOS pattern to inform the receiver that the transmitter is signaling an EI Exit. This pattern guarantees the receiver will properly detect the EI Exit condition, something not guaranteed by scrambled data. The Tx EIEOS launch voltage is defined by $V_{TX-EIEOS-FS}$ for full swing signaling and by $V_{TX-EIEOS-RS}$ for reduced swing signaling. $V_{TX-EIEOS-RS}$ is smaller than $V_{TX-EIEOS-FS}$ to reflect the fact that reduced swing is typically supported only for lower loss channels where there is less attenuation at the EIEOS signaling rate.

For full swing signaling $V_{TX-EIEOS-FS}$ is measured with a c_{+1} coefficient value of -0.33 and a c_{-1} coefficient of 0.00, corresponding to preset number P10. This is equivalent to a maximum nominal boost of 9.5 dB and represents the maximum boost attainable in coefficient space. When a boost tolerance of ±1.5 dB is factored in this yields the minimum boost limit of 8.0 dB appearing in Table 9-5. For reduced swing signaling $V_{TX-EIEOS-RS}$ is measured with a c_{+1} coefficient value of -0.167 and a c_{-1} coefficient of 0.00, corresponding to preset P1.

Both $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are referenced to the Tx pin, so any attenuation effects of the breakout channel must be removed from the measurement, typically by de-embedding.

At the far end of a lossy channel the de-emphasis peak will be attenuated; this is why the measurement interval includes only UI number 9-28. The voltage is averaged over this interval for both the negative and positive halves of the waveform. $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$ is defined as the difference between the negative and positive waveform segment averages. UI boundaries are defined with respect to the edge of the recovered data clock.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 103 Min Swing During EIEOS for Reduced Swing Test Details

Symbol	Parameter	Min
$V_{TX-EIEOS-RS}$	Min swing during EIEOS for reduced swing	232 mVPP

Test Definition Notes from the Specification

$V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ are measured at the device pin and include package loss. Voltage limits comprehend both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0, 16.0, and 32.0 GT/s that ensures that these parameters are met.

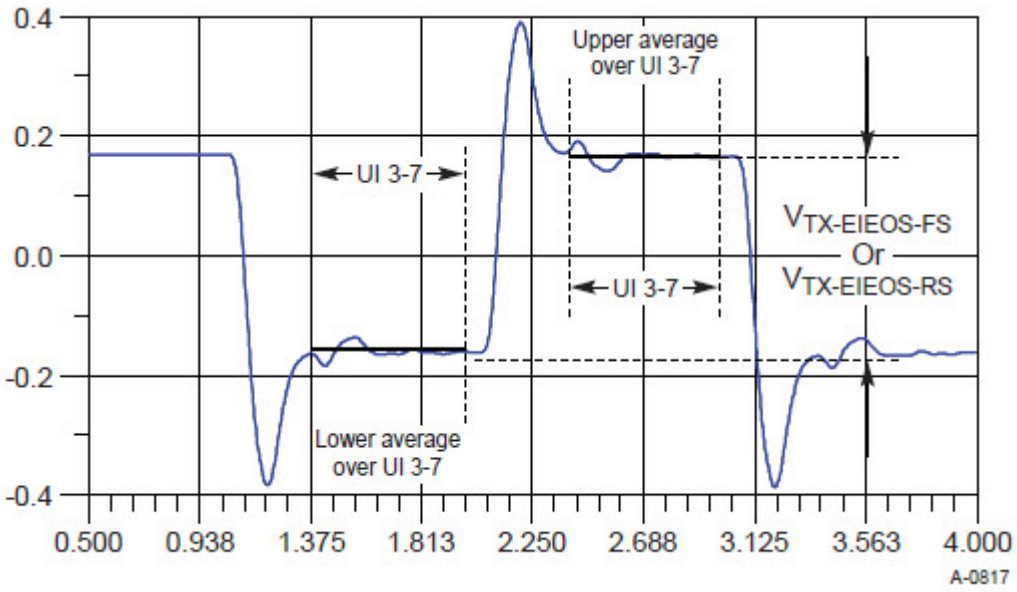


Figure 97 Measurement $V_{TX-EIEOS-FS}$ or $V_{TX-EIEOS-RS}$

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Finds and updates the worst case test result values.
8 Gets the average EIEOS high voltage.
9 Gets the average EIEOS low voltage.
10 Calculates the amplitude of the EIEOS signal by taking the difference between the high and low voltage readings.
11 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Total Jitter Test

This test verifies that the maximum uncorrelated total jitter T_{TX-UTJ} is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 104 Uncorrelated Total Jitter Test Details

Symbol	Parameter	Max
T_{TX-UTJ}	Tx uncorrelated total jitter	6.25 ps PP at 10^{-12}

Test Definition Notes from the Specification

For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the RJ RMS jitter value.
8 Reports the peak total jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Uncorrelated Deterministic Jitter Test

This test verifies that the maximum uncorrelated deterministic jitter $T_{TX-UDJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 105 Uncorrelated Deterministic Jitter Test Details

Symbol	Parameter	Max
$T_{TX-UDJDD}$	Tx uncorrelated deterministic jitter	3.125 ps PP

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak uncorrelated deterministic jitter value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Total Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the total uncorrelated PWJ $T_{TX-UPW-TJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 106 Total uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-TJ}$	Total uncorrelated PWJ	6.25 ps PP at 10^{-12}

Test Definition Notes from the Specification

PWJ parameters are measured after DDJ separation.

Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the random jitter value.
8 Reports the uncorrelated total pulse width jitter value.
9 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Deterministic DjDD Uncorrelated PWJ (Pulse Width Jitter) Test

This test verifies that the maximum deterministic DjDD uncorrelated PWJ $T_{TX-UPW-DJDD}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 107 Deterministic DjDD Uncorrelated PWJ Test Details

Symbol	Parameter	Max
$T_{TX-UPW-DJDD}$	Deterministic DjDD uncorrelated PWJ	2.5 ps PP

Test Definition Notes from the Specification

- PWJ parameters are measured after DDJ separation.
- Measured with optimized preset value after de-embedding to Tx pin.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the peak deterministic DjDD uncorrelated PWJ value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Data Dependent Jitter (Information-Only Test)

This test verifies that the maximum data dependent jitter, $T_{TX\text{-}DDJ}$ is within the allowed range.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.5.7 is used as reference.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Pseudo Package Loss Test

This test verifies that the maximum pseudo package loss, $ps21_{TX}$ is within the allowed range.

Separate $ps21_{TX}$ parameters are defined for packages containing Root Ports (Root Package) and for all other packages (Non-Root Package), based on the assumption that the former tend to be large and require socketing, while the latter are smaller and usually not socketed.

Package loss is measured by comparing the 64-zeroes/64-ones PP voltage (V_{111}) against a 1010 pattern (V_{101}). Tx package loss measurement is made with c_{-1} and c_{+1} both set to zero. A total of 10^6 measurements shall be made and averaged to obtain values for V_{101} and V_{111}. Multiple measurements shall be made and averaged to obtain stable values for V_{101} and V_{111}. Due to the HF content of V_{101}, $ps21_{TX}$ measurement requires that the breakout channel be de-embedded back to the Tx pin.

Measurement of V_{101} and V_{111} is made towards the end of each interval to minimize ISI and low frequency effects. V_{101} is defined as the peak-peak voltage between minima and maxima of the clock pattern. V_{111} is defined as the peak-peak voltage difference between the positive and negative levels of the two half cycles. The measurement should be averaged over multiple compliance patterns until the mean deviates by less than 2% between successive averages.

Test Reference

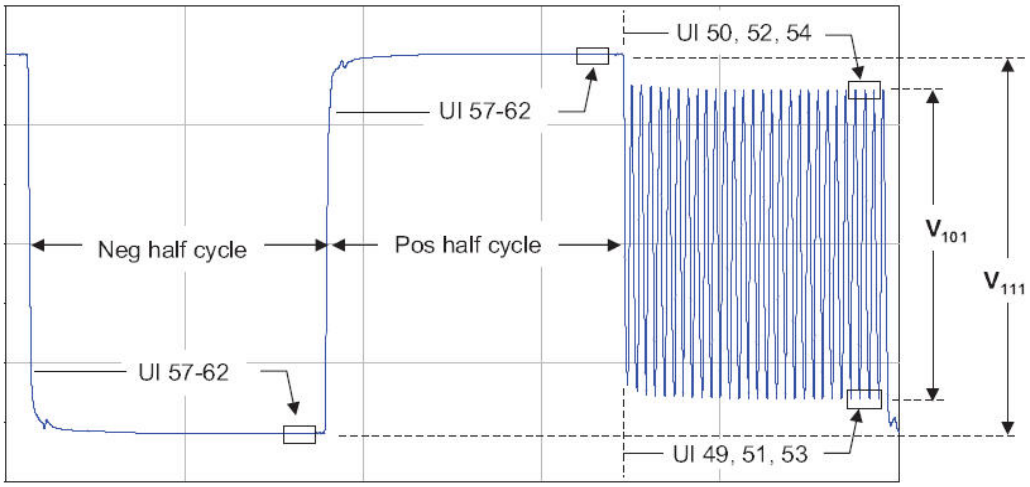
PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 108 Pseudo Package Loss Test Details

Symbol	Parameter	Max
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for a device containing root ports	8.5 dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss for all devices not containing root ports	3.7 dB

Test Definition Notes from the Specification

- The numbers above take into account measurement error. For some Tx package/driver combinations $ps21_{TX}$ may be greater than 0 dB.
- The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model.



$$ps21_{TX} = 20\log_{10}(V_{101}/V_{111})$$

Figure 98 Compliance Pattern and Resulting Package Loss Test Waveform

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1. Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2. Performs actual compliance testing using the SigTest tools.
3. Gets input test waveform data from scope.
4. Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5. Performs the transmitter compliance test function using the SigTest tools.
6. Gets compliance test results from SigTest tools.
7. Reports the number of package loss measurements taken.
8. Reports the package loss ration value.
9. Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Random Jitter

This test verifies that the random jitter, T_{TX-RJ} is within the allowed range.

Random jitter is uncorrelated with respect to data dependent jitter. T_{TX-RJ} may be obtained by subtracting $T_{TX-UDJ-DD}$ from T_{TX-UTJ}. and is included in the specification as an informative parameter only. It is typically used as a benchmark to characterize PLL performance.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.6, Table 8-6 is used as reference to check the compliance of the DUT.

Table 109 Data Dependent Jitter Test Details

Symbol	Parameter	Range
T_{TX-RJ}	Random jitter	0.23 - 0.45 ps RMS

Test Definition Notes from the Specification

- This is an informative parameter only.
- Range of the parameter possible with zero to maximum allowed $T_{TX-UDJDD}$.
- For PCIe 5.0 devices that do not support 32.0 GT/s have the option to use 2 MHz as min of $BW_{TX-PKG-PLL1}$ and $BW_{TX-PKG-PLL2}$ for both 8.0 and 16.0 GT/s. The corresponding T_{TX-UTJ} max value is 31.25 ps at 8.0 GT/s and 12.5 ps at 16.0 GT/s. The range of T_{TX-RJ} is 1.4-2.2 ps at 8 GT/s and 0.45-0.89 ps at 16.0 GT/s. Such devices also have the option to use 1st-order, 10 MHz CDR filter for testing Tx, Reference clock, and CC Rx.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Performs actual compliance testing using the SigTest tools.
3 Gets input test waveform data from scope.
4 Acquires scope sample waveform data (re-iterate to capture at least 1M UI).
5 Performs the transmitter compliance test function using the SigTest tools.
6 Gets compliance test results from SigTest tools.
7 Reports the data dependent value.
8 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

DC Common-Mode Voltage Test

The Average DC Common Mode Voltage measurement computes the DC average of the common mode signal.

$V_{TX\text{-}DC\text{-}CM} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}DC\text{-}}|/2$

The PCIE Base specification states that the Transmitter DC common mode voltage must be held at the same value during all states.

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 110 DC Common Mode Output Voltage Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC Common Mode Voltage	0 V	3.6 V

Test Definition Notes from the Specification

- Total single-ended voltage Tx can supply under any conditions with respect to ground.
- $I_{TX\text{-}SHORT}$ and $V_{TX\text{-}DC\text{-}CM}$ stipulate the maximum current/voltage levels that a transmitter can generate and therefore define the worst case transients that a receiver must tolerate.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Sets up DC common mode voltage as follows:
   a Enables and displays common mode measurements.
   b Loads common mode signal to waveform memory.
   c Loads and enhance dynamic range D+ signal and D- signal.
   d Enables the average common mode measurement.
   e Uses markers to indicate compliance test limit boundaries (0 V to 3.6 V).
4 Measures the average value of D+ and D- signal.
5 Computes DC common mode value by absolute the average of the total average value of D+ and D- signal using the formula mentioned above.
6 Reports the measurement result and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Base Specification, Rev 4.0 as $V_{TX-DC-CM}$ is 0 to 3.6 V (+/- 100 mV).

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common-Mode Voltage (LPF, 16 GHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 111 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}AC\text{-}CM\text{-}PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE Before executing the test, ensure that the DUT is transmitting compliance test pattern defined in Section 4.2.10 of the PCI Express Base Specification, Rev 5.0.

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
2 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
3 Uses UDF LPF (Low Pass Filter) with cut off frequency of 4 GHz to the common mode signal.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

AC Common Mode Voltage (BPF, 30 kHz to 500 MHz) Test

The AC Common Mode Voltage measurement computes the AC peak-to-peak of the common mode signal. The measurement of $V_{TX\text{-}CM\text{-}AC\text{-}PP}$ is the value of difference between the maximum and minimum of the common mode signal.

$V_{CM} = [V_{D+} + V_{D-}]/2$

$V_{TX\text{-}AC\text{-}CM\text{-}PP} = \max (V_{D+} + V_{D-})/2 - \min (V_{D+} + V_{D-})/2$

This test is only available when the single-ended or SMA probing method has been used (as it requires 2 channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 112 AC Common Mode Voltage Test Details

Symbol	Parameter	Max
$V_{TX\text{-}AC\text{-}CM\text{-}PP}$	Tx AC peak-peak common mode voltage	150 mVPP

Test Definition Notes from the Specification

- Over the 0.03-500 MHz range: no more than 100 mVPP at 5.0 GT/s, and no more than 50mVPP at 8.0, 16.0, or 32.0 GT/s.
- $V_{TX\text{-}AC\text{-}CM\text{-}PP}$ is measured at TP1 without de-embedding the breakout channel. This parameter captures device CM (Common Mode) only and is not intended to capture system CM noise. For each data rate an LPF with a -3 dB point of data rate/2 is applied.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the AC-CM Voltage (LPF, 16 GHz) test.

1 Gets PCIE5 compliance signal.
2 Uses MATLAB function (BandPassFilter) to filter the signal with cutoff frequency of 30 KHz and 500 MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Measures the VPP of the filtered signal.
5 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common Mode Voltage Between D+ and D- Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

The DC common-mode line delta measurement computes the absolute difference between the average DC value of the D+ and the average DC value of the D- waveform signals.

$|V_{TX\text{-}CM\text{-}DC\text{-}D+[during\ L0]} - V_{TX\text{-}CM\text{-}DC\text{-}D-[during\ L0]}| \leq 25\ mV$

$V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $|V_{TX\text{-}D+}|$ [during L0]

$V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $|V_{TX\text{-}D-}|$ [during L0]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 113 Absolute Delta of DC Common-Mode Voltage Between D+ and D- Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute delta of DC common-mode voltage between D+ and D-	0 mV	25 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the DC Common Mode Output Voltage test.

1 Reports the following measurement results obtained from running the pre-requisite test Avg. DC Common Mode Output Voltage Test.
   - DC Common Mode Line Delta
   - Average DC value of D+
   - Average DC value of D-
2 Computes the DC Common Mode Line Delta by absolute the difference between average DC value of D+ and average DC value of D-.
3 Reports the measurement result.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test

This test measures $V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$, which is the absolute delta of the DC common-mode voltage during L0 and electrical idle.

$|V_{TX\text{-}CM\text{-}DC\ [during\ L0]} - V_{TX\text{-}CM\text{-}Idle\text{-}DC\ [during\ electrical\ idle]}| \leq 100\ mV$

$V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$

$V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $|V_{TX\text{-}D+} + V_{TX\text{-}D\text{-}}|/2$ [electrical idle]

This test is only available when the single-ended or SMA probing method has been used (as it requires two channels input). When the input data is a differential signal (single channel input used), this test will be disabled.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.3.9, Table 8-7 is used as reference to check the compliance of the DUT.

Table 114 Absolute Delta of DC Common-Mode Voltage During L0 and Idle Test Details

Symbol	Parameter	Min	Max
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$	Absolute delta of DC common-mode voltage during L0 and electrical idle	0 mV	100 mV

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

NOTE This test requires the Average DC Common Mode Output Voltage test.

1 Configures the DUT to operate in the idle stage.
2 Reports the measurement results obtained from running the pre-requisite test, average DC common-mode output voltage test.
   - Average DC value of the common-mode signal
3 Computes the differential between the DC of the active stage and the idle stage.
4 Reports the measurement results.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

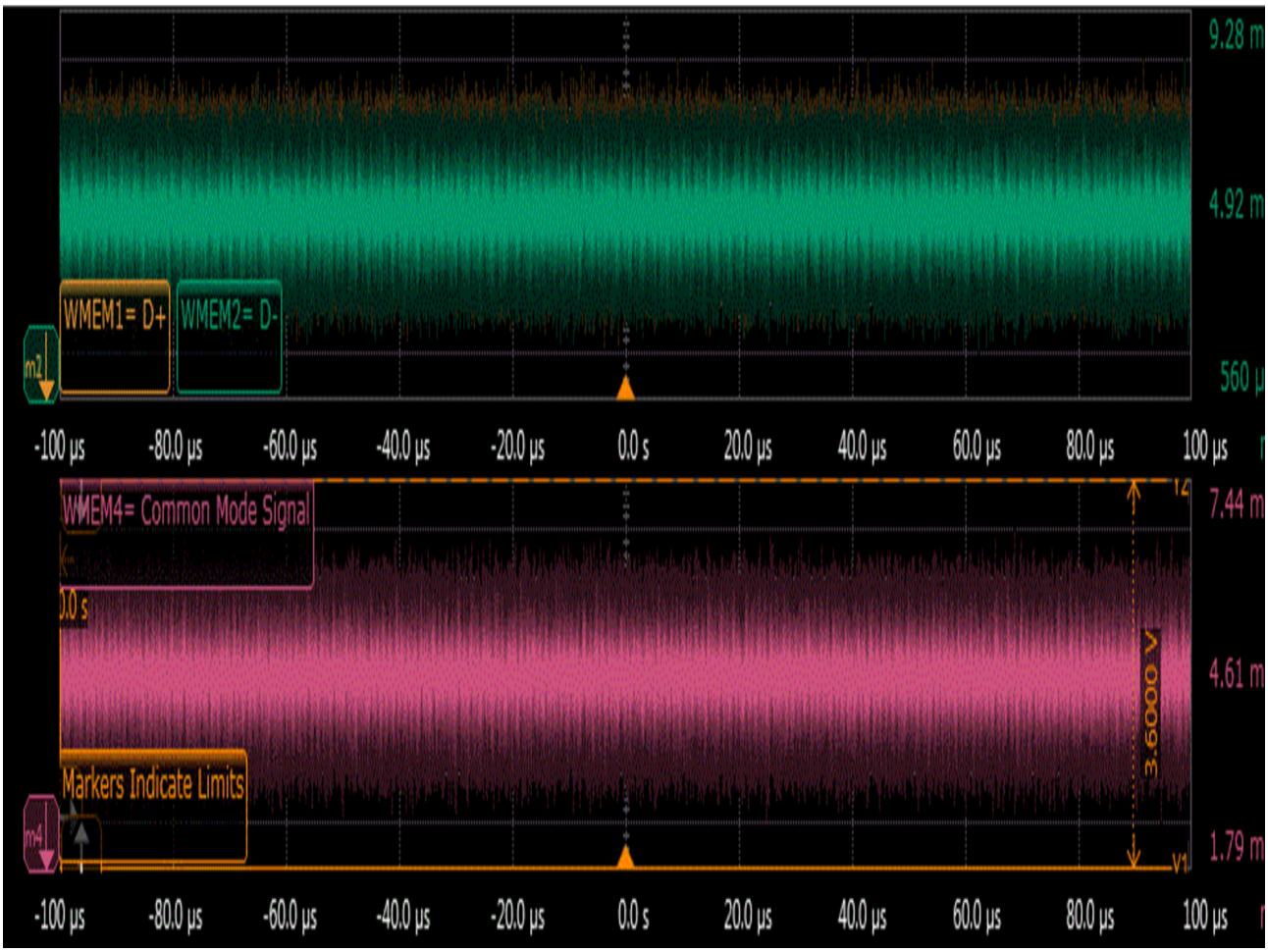


Figure 99 Reference Image for Absolute Delta of DC common mode voltage during L0 and Idle Test

SSC Modulation Frequency

This test verifies that the SSC frequency range is in the allowable range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 115 SSC Frequency Range Test Details

Symbol	Description	Min	Max
F_{SSC}	SSC frequency range	30 kHz	33 kHz

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 32.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Sets the scale and offset of the input channels to their optimum values.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures the frequency of the jitter TREND on WMEM1.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Max)

This test verifies that the SSC maximum deviation is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 116 SSC Deviation Test Details

Symbol	Description	Max
$T_{SSC\text{-}FREQ\text{-}DEVIATION\_32G\_SRIS}$	SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds	0.0%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 32.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Max(%) = ((1 / Data Rate) - SSC's Minimum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Peak Deviation (Min)

This test verifies that the SSC minimum deviation is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 117 SSC Deviation Test Details

Symbol	Description	Min
$T_{SSC\text{-}FREQ\text{-}DEVIATION\_32G\_SRIS}$	SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds	-0.3%

Test Definition Notes from the Specification

When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the data rate is 32.0 GT/s.
3 Sets up labels and grid display settings on the oscilloscope.
4 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.
8 Measures Period_max, Period_min and Period_average.
9 Computes SSC deviation Min(%) = ((1 / Data Rate) - SSC's Maximum UI) / (1 / Data Rate) * 100
10 Compares the SSC deviation Max and SSC deviation Min and reports worst case value as actual result.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

SSC Max df/dt (Slew Rate) Test

This test verifies that the SSC maximum slew rate is within the allowed range.

Test Reference

PCIE Base Specification Revision 5.0, Section 8.6.3, Table 8-17 (Data Rate Independent Refclk Parameters) is used as reference to check the compliance of the DUT.

Table 118 Max SSC df/dt Test Details

Symbol	Description	Max
$T_{SSC-MAX-FREQ-SLEW}$	Max SSC df/dt	1250 ppm/µs

Test Definition Notes from the Specification

- Measurement is made over 0.5 µs time interval with a 1^{st} order LPF with an f_c of 60x the modulation frequency.
- When testing the device configured for the IR reference clock architecture the SSC related parameters must be tested with the Tx output data instead of the reference clock.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

2 Configures memory depth and sampling rate as per the data rate..

3 Fits and displays all sample data on screen.

4 Analyzes **Unit Interval** measurement using the **Measurement Analysis (EZJIT)...** option.

5 Analyzes measurements trend using the jitter **Meas Trend** function.

6 The slew rate of the data is computed using a MATLAB function (DFDT). The Matlab function does the following:

a Generates a differential plot (x_n - x_{n-1}).

b The maximum slew rate corresponds to the peak of the differential plot.

7 Reports the measurement results and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Transmitter Tests:
MemoryDepth = SamplingRate/DataRate.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

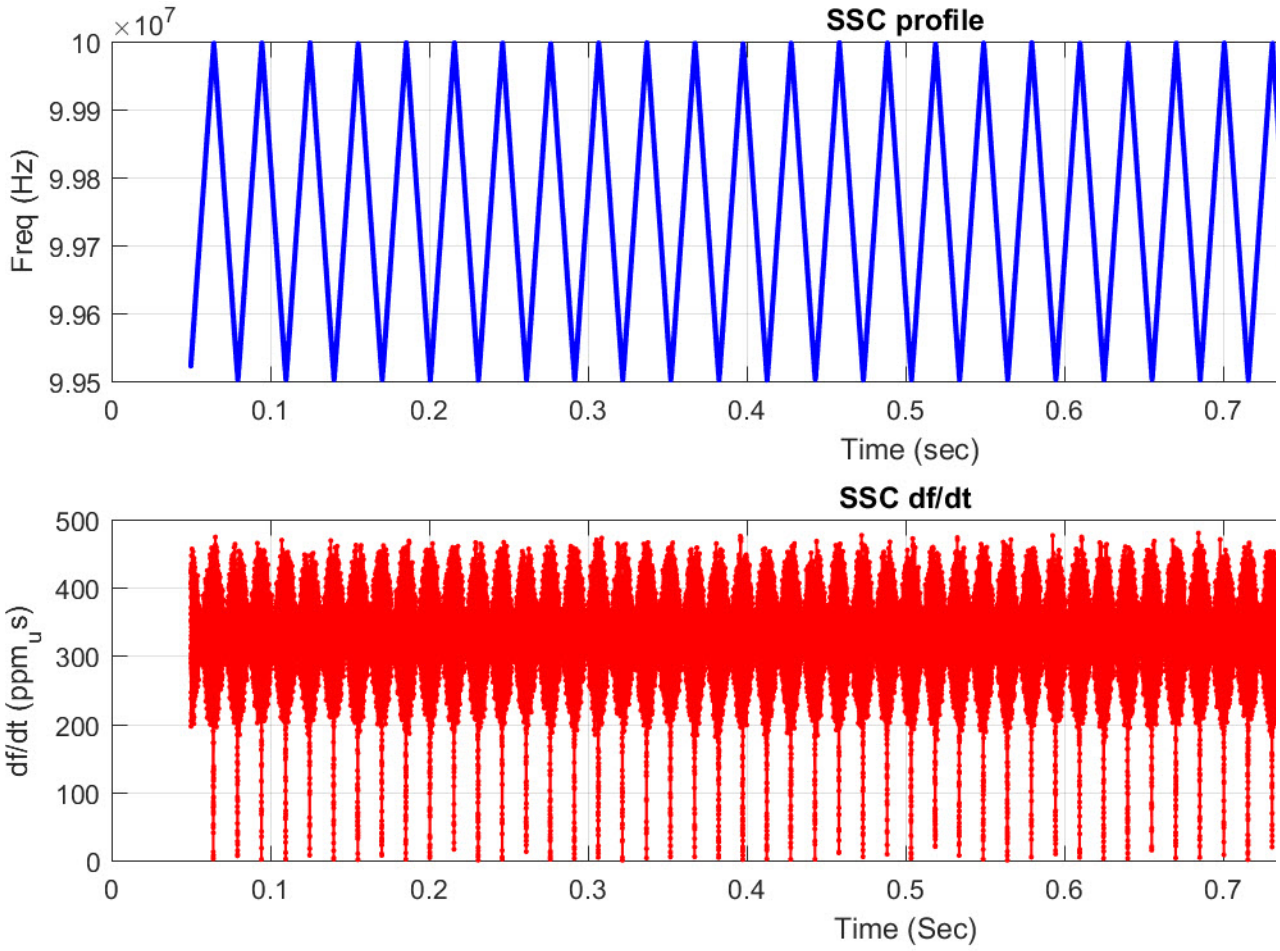


Figure 100 Maximum SSC Slew Rate

Running Equalization Presets Tests

Please refer to section: "Running Equalization Presets Tests" on page 174 in Chapter 8, "Transmitter (Tx) Tests, 8.0 GT/s, PCI-E 5.0"

13 Reference Clock Tests, 32.0 GT/s, PCI-E 5.0

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Running Reference Clock Tests / 317

This section provides the Methods of Implementation (MOIs) for Reference Clock tests at 32.0 GT/s using Keysight Z-Series, Keysight Q-Series, or Keysight UXR Series Infiniium oscilloscope, and the PCI Express Gen5 Compliance Test Application.

NOTE In case of Z-series and Q-Series oscilloscope, 32.0 GT/s data rate tests have to use real edge channels in order to support PCI-E 5.0 compliance testing.

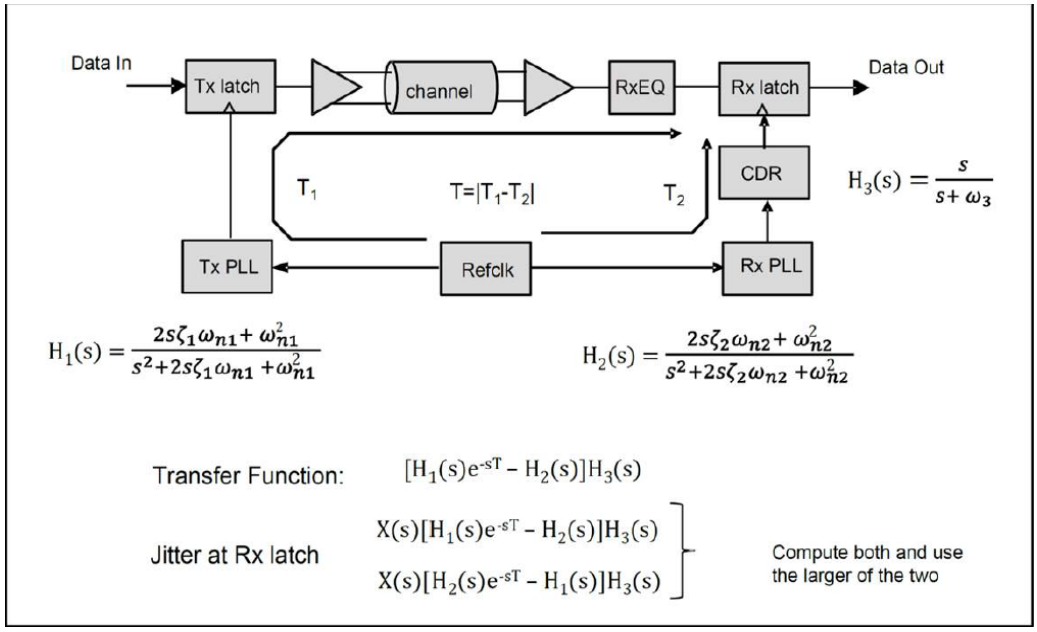
NOTE It is recommended to use normal or non real edge channels on the scope for data rates upto 16.0 GT/s in order to reduce the overall test time.

Reference Clock Architectures

For 32.0 GT/s, PCI-E 5.0, there are two main reference clock architectures – common clock architecture and data clock architecture.

Common Clock Architecture

This section describes the common Refclk Rx architecture.
At 32.0 GT/s the only difference in the figure is the “behavioral CDR transfer function” as defined in PCI Express Base Specification, Rev 5.0, Section 8.3.5.5.



The following tables display the common refclk PLL and CDR characteristics for the different data rates.

Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

PLL #1	0.01 dB peaking	2.0 dB peaking	PLL #2	0.01 dB peaking	1.0 dB peaking
BW_{PLL}(min) = 2.0 MHz	ω_{n1}= 0.448 Mrad/s ζ_1 = 14	ω_{n1}= 6.02 Mrad/s ζ_1 = 0.73	BW_{PLL}(min) = 2.0 MHz	ω_{n2}= 0.448 Mrad/s ζ_2 = 14	ω_{n2}= 4.62 Mrad/s ζ_2 = 1.15
BW_{PLL}(max) = 4.0 MHz	ω_{n1}= 0.896 Mrad/s ζ_1 = 14	ω_{n1}= 12.04 Mrad/s ζ_1 = 0.73	BW_{PLL}(max) = 5.0 MHz	ω_{n2}= 1.12Mrad/s ζ_2 = 14	ω_{n2}= 11.53 Mrad/s ζ_2 = 1.15
BW_{CDR}(min) = 10 MHz, 1st order	64 combinations				

8.0, 16.0 GT/s

Common Ref Clock PLL and CDR Characteristics for 32.0 GT/s

PLL #1, PLL #2	0.01 dB peaking	2.0 dB peaking
BW_{PLL}(min) = 0.5 MHz	ω_{n1}= .112 Mrad/s ζ_1 = 14	ω_{n1}= 1.51 Mrad/s ζ_1 = 0.73
BW_{PLL}(max) = 1.8 MHz	ω_{n1}= .403 Mrad/s ζ_1 = 14	ω_{n1}= 5.42 Mrad/s ζ_1 = 0.73

32.0 GT/s CC **CDR**

16 combinations

32.0 GT/s

Reference Clock Measurement Point

The compliance test load for driver compliance is shown in PCI Express Base Specification, Rev 5.0, Section 8.6.1, Figure 8-64.

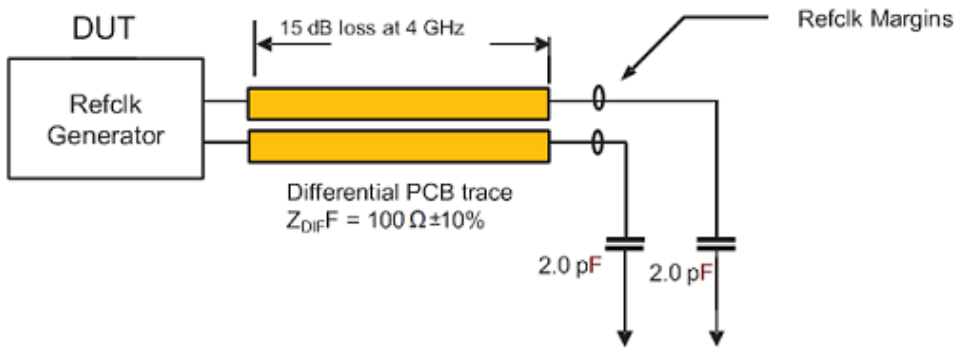


Figure 101 Driver Compliance Test Load

At 32.0 GT/s reference clock jitter is tested with the reference clock terminated directly by 50 Ohm terminations without a channel as mentioned in PCI Express Base Specification, Rev 5.0, Section 8.6.1.

Running Reference Clock Tests

Start the automated testing application as described in "Starting the PCI Express Gen5 Compliance Test Application" on page 25. Then, when selecting tests, navigate to “Reference Clock Tests” in the “PCIE 4.0 Tests” group.

Note that selecting “SSC” or “Clean Clock” under Reference Clock on the Set Up page affects the number of tests that appear on the Select Tests page.

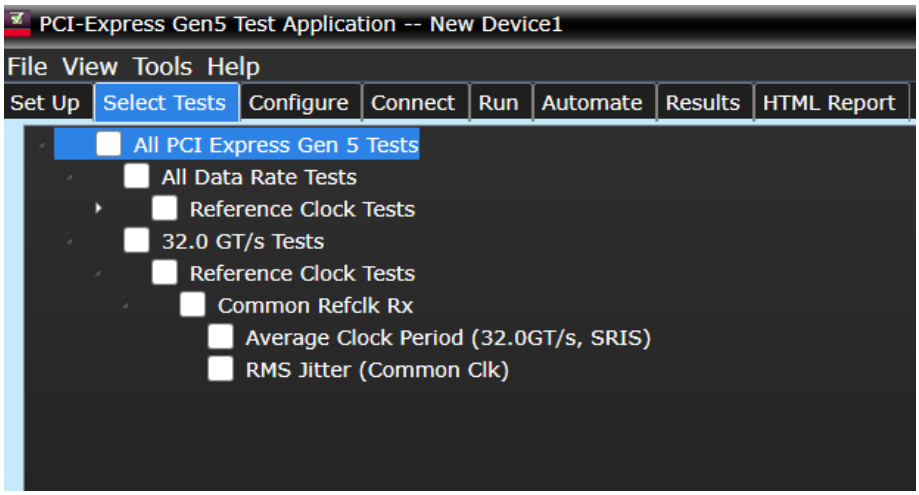


Figure 102 Selecting Reference Clock Tests when SSC or Clean Clock is Selected with SRIS Mode

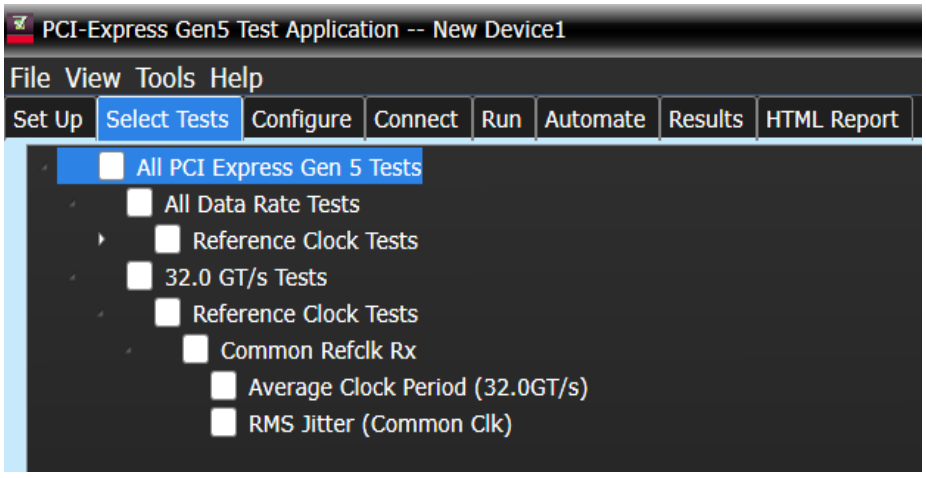


Figure 103 Selecting Reference Clock Tests when SSC or Clean Clock is Selected without SRIS Mode

Average Clock Period Test (32.0 GT/s)

This test verifies that the Refclk Average Clock Period (32 GT/s) is within the conformance limits as specified in PCIE Express Base Specification, Revision 5.0, Section 8.6.2, Table 8-16.

The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100 Hz. A requirement of +/- 300 PPM applies to systems that do not employ SSC or that use a common clock source. For systems employing SSC, there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM. This test is applicable for devices that support 32.0GT/s speed.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.2, Table 8-16 (REFCLK DC Specifications and AC Timing Requirements) is used as reference to check the compliance of the DUT.

Table 119 Average Clock Period Test Details

		100 MHz Input	
Symbol	**Parameter**	**Min**	**Max**
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300 ppm	+2800 ppm
$T_{PERIOD\ AVG\_32G\_CC}$	Average Clock Period Accuracy for devices that support 32.0 GT/s in CC Mode at any speed	-100 ppm	+2600 ppm
$T_{PERIOD\ AVG\_32G\_SRIS}$	Average Clock Period Accuracy for devices that support 32.0 GT/s in SRIS Mode at any speed	-100 ppm	+1600 ppm

Test Definition Notes from the Specification

- Measurement taken from differential waveform.
- PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For example for 300 PPM, then we have an error budget of 100 Hz/ PPM × 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater.

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.

2 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.

3 Configures memory depth and sampling rate as per the data rate.

4 Fits and displays all sample data on screen.

5 Measures the average voltage using **V average** measurement.

6 Configures the **Top Level** threshold to +150 mV and **Base Level** threshold to -150 mV using **Threshold Setup**.

7 Measures the average frequency using **Frequency** measurement of **Clock**.

8 Measures the average period using **Period** measurement of **Clock**.

9 Computes the difference between ideal and actual frequency in terms of parts per million of 100 MHz as follows:

$$\text{Difference between ideal and actual frequency} = [100MHz - AverageFrequency]/100$$

10 Reports the average clock period accuracy and verifies that the value of the parameter is as per the conformance limits specified in the PCI Express Card Electromechanical Specification Rev. 5.0.

For SSC Mode,

$$-300\ ppm \leq Average\ Clock\ Period\ Accuracy \leq +2800\ ppm$$

For Clean Clock,

$$-100\ ppm \leq Average\ Clock\ Period\ Accuracy \leq +2600\ ppm$$

For SRIS Mode,

$$-100\ ppm \leq Average\ Clock\ Period\ Accuracy \leq +1600\ ppm$$

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

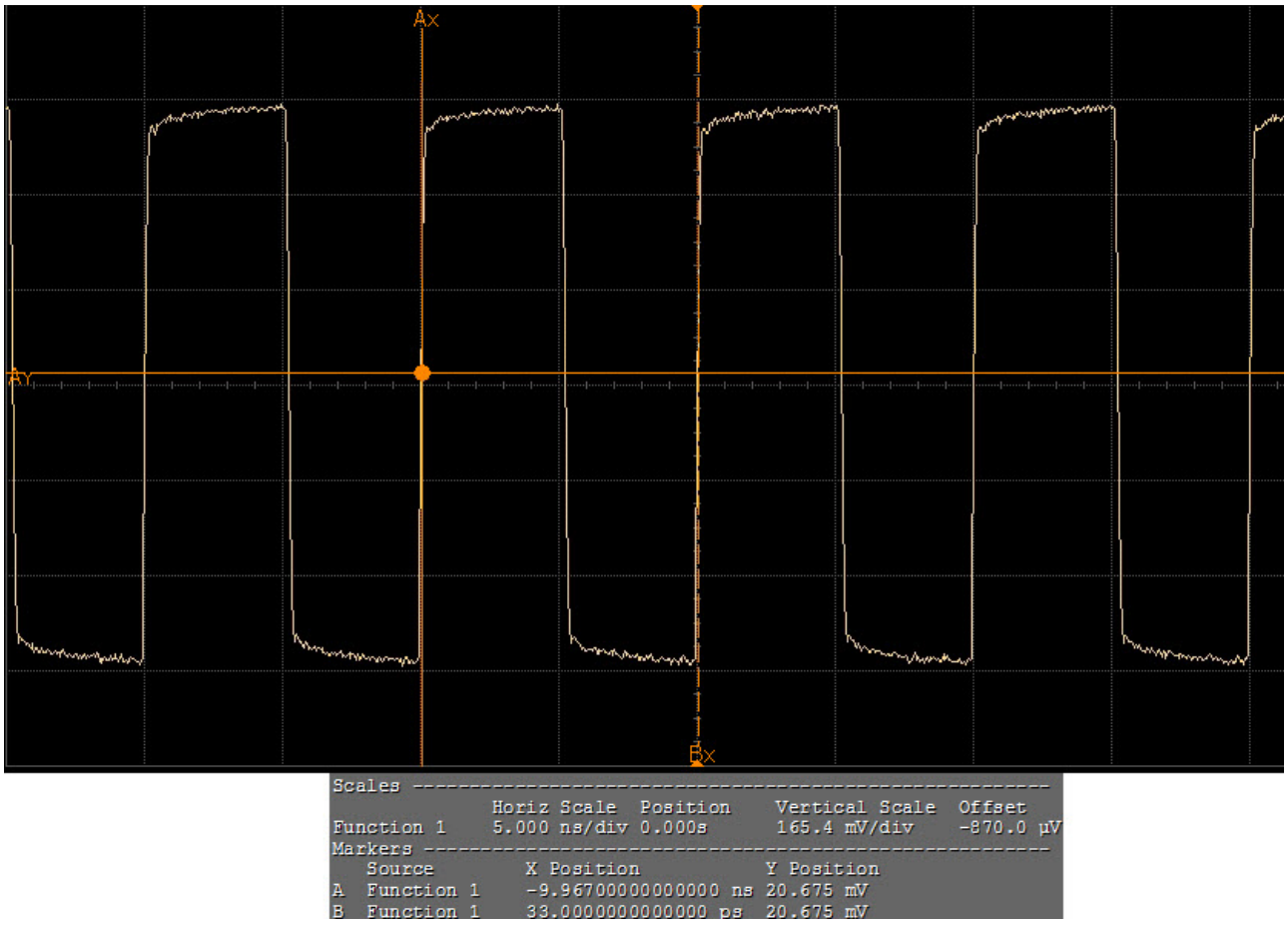


Figure 104 Reference Image for Average Clock Period

RMS Jitter (Common Clk) Test

This test verifies that the measured RMS jitter, $T_{REFCLK-RMS-CC}$, is less than the maximum allowed value.

Test Reference

PCI Express Base Specification, Rev 5.0, Section 8.6.7, Table 8-18 is used as reference to check the compliance of the DUT.

Table 120 RMS Jitter Test Details

Symbol	Description	Max
$T_{REFCLK-RMS-CC}$	RMS Refclk jitter for common Refclk architecture	0.5 ps RMS

Understanding the Test Flow

The PCI Express test application performs the following automated steps for measuring the test results based on the above mentioned references:

1 Gets the reference clock signal.
2 Verifies that the signal period is ~100MHz.
3 Configures optimum values for **Scale** and **Offset** using **Channel Setup**.
4 Configures the value of the test parameters as the values configured for the **Number of UI** and **Sample Rate** configuration parameters using Automated Test Engine.
5 Configures memory depth and sampling rate as per the data rate.
6 Fits and displays all sample data on the screen.
7 Analyzes **Time Interval Error (TIE)** measurements of **Clock** using the **Measurement Analysis (EZJIT)...** option.
8 Analyzes measurements trend using the jitter **Meas Trend** function and acquires data until the minimum number of UIs achieved. For example, at a sample rate of 20 Gsa/s, clock rate 100MHz, each UI takes up 200 points. So for memory depth of 50M, each acquisition yields 250000 UIs. To achieve 1 million UIs, 4 acquisitions are required.
9 Stitches each acquired acquisition to make a continuous TIE data.
10 Analyzes the stitched TIE data using a MATLAB function. The MATLAB function does the following:
   a Converts time domain TIE data to frequency domain.
   b Applies the PLL filter using parameters for common clocked architecture.
   c Converts back the frequency domain TIE data to time domains.
   d Computes the filtered peak-peak jitters and RMS jitter.
11 Reports filtered peak-peak jitter and RMS jitter and verifies that the value of the parameter is as per the conformance limits.

NOTE Base - Reference Clock Tests:
MemoryDepth = SamplingRate/100MHz.

Viewing Test Results

For each test trial, its result is displayed on the **Results** tab. Click the desired test to view its result. Details of the test results are described in the lower pane. A sample reference image based on the measured values is captured by the oscilloscope. You can click the sample reference image to view the details. For information about the test results, refer to **Viewing Results** in the online help.

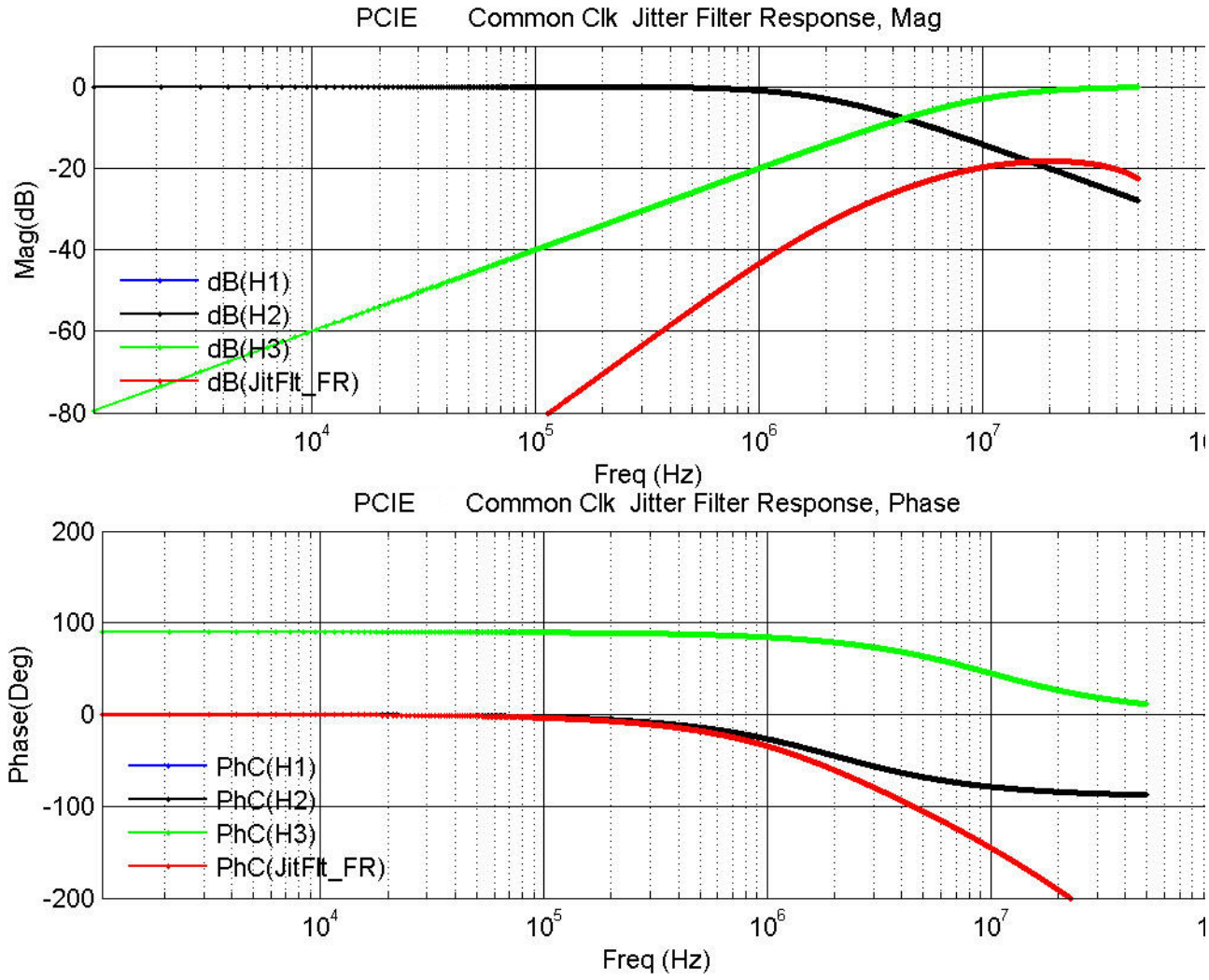


Figure 105 Reference Image for Jitter Filter Response (Common Clock) RMS Jitter Test

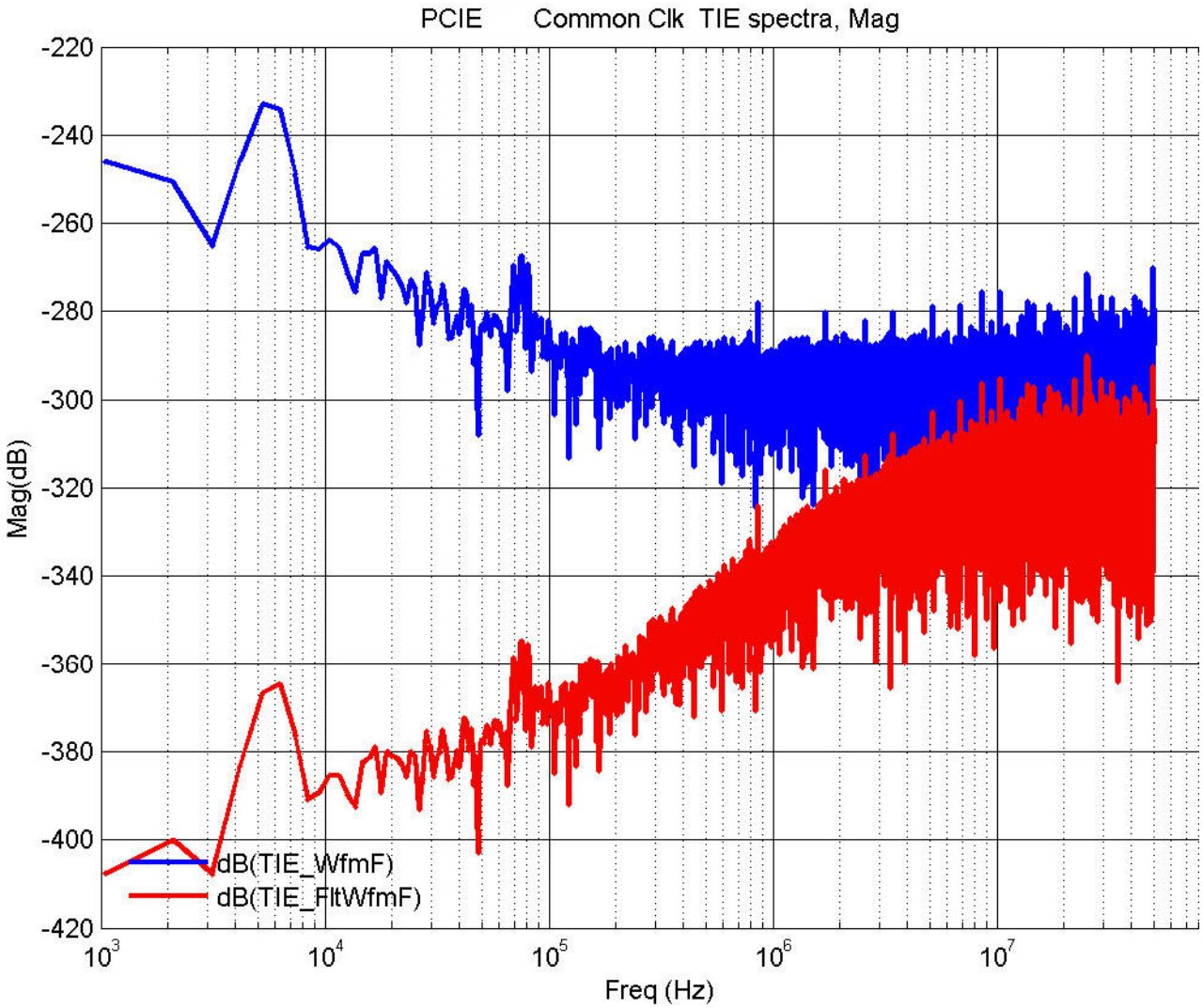


Figure 106 Reference Image for Common Clock TIE Spectra RMS Jitter Test

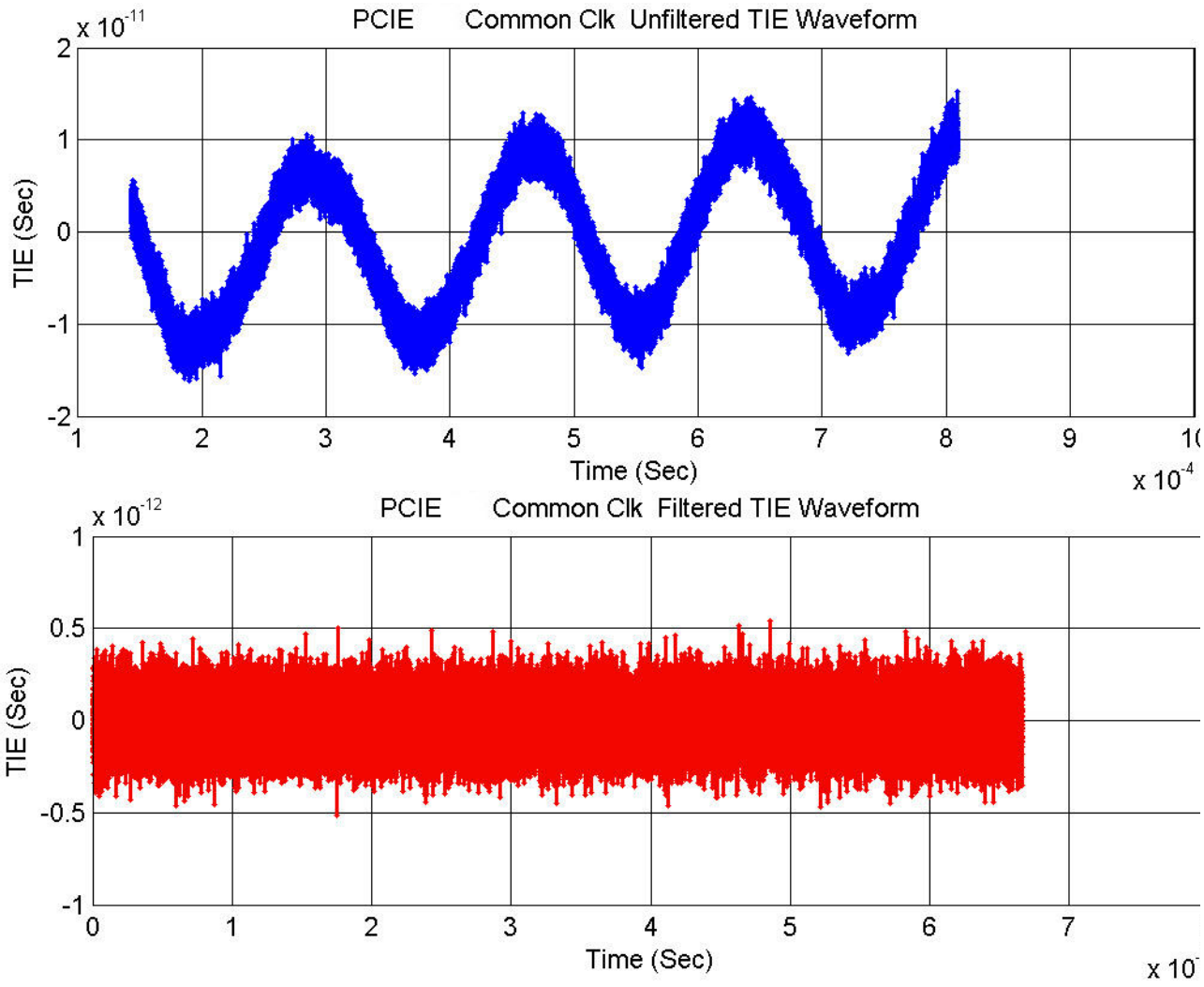


Figure 107 Reference Image for TIE Waveform RMS Jitter Test

Part VIII
Appendices

KEYSIGHT
TECHNOLOGIES

A Calibrating the Digital Storage Oscilloscope

Required Equipment for Calibration / 328
Internal Calibration / 329
Cable and Probe Calibration / 334
Channel-to-Channel De-skew / 343

This appendix describes the Keysight digital storage oscilloscope calibration procedures.

Required Equipment for Calibration

To calibrate the oscilloscope in preparation for running the PCI Express automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, qty = 2, (provided with the Keysight Infiniium oscilloscope).
- Calibration cable.
- BNC shorting cap.

Figure 1 below shows a drawing of the above connector items.

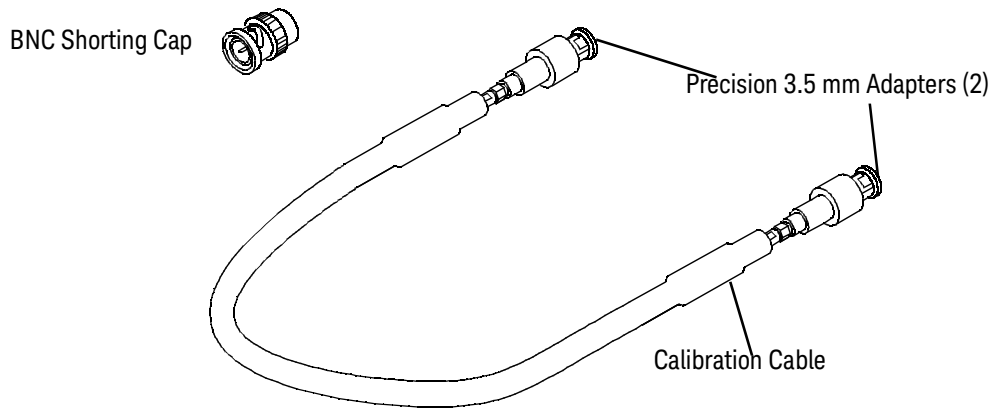


Figure 1 Accessories Provided with the Keysight Oscilloscope

- 50-ohm Coax Cable with SMA Male Connectors – 24-inch or less RG316/U or similar, qty = 2, matched length.
- SMA T-adapter.
- BNC to SMA male adapter, qty = 1.

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Keysight oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:
   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.
   b If SigTest is being used on the oscilloscope, then connect a second monitor to the VGA connector located near the LAN port, on the rear of the oscilloscope.
   c Plug in the power cord.
   d Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.
   e Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:
   a Locate the BNC shorting cap.
   b Locate the calibration cable.
   c Locate the two Keysight precision SMA/BNC adapters.
   d Attach one SMA adapter to one end of the calibration cable - hand tighten snugly.
   e Attach the other SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 2 below, perform the following steps:
   a Click on the Utilities>Calibration menu to open the Calibration window.

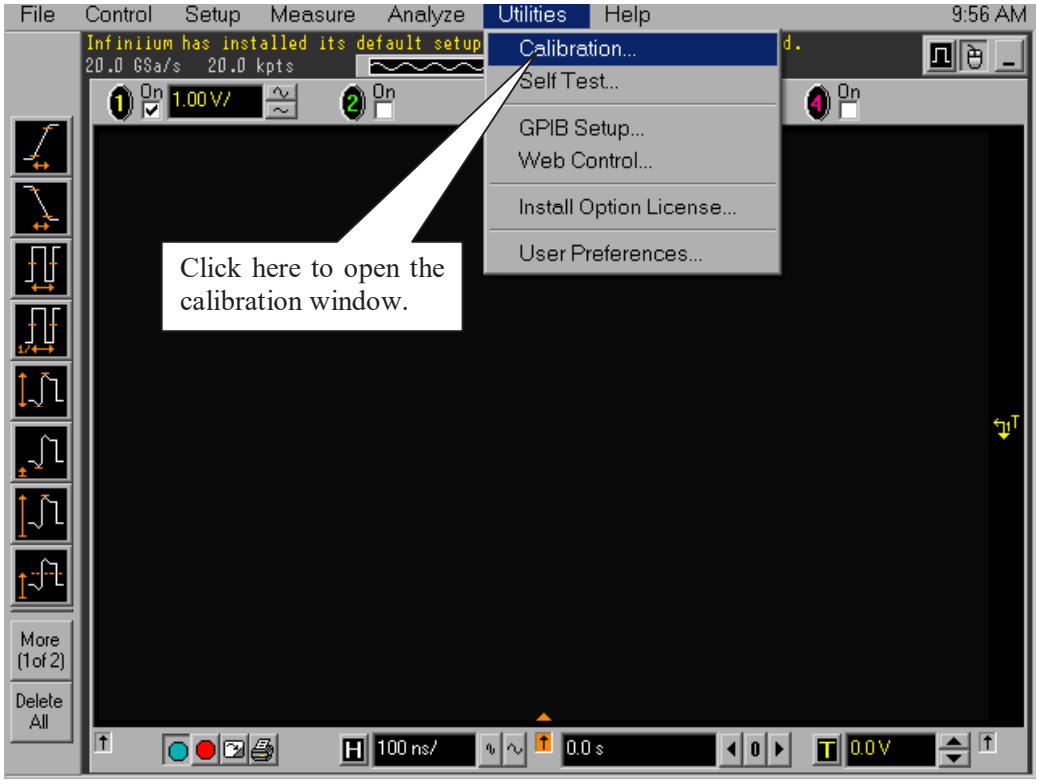


Figure 2 Accessing the Calibration Menu.

4 Referring to Figure 3 below, perform the following steps to start the calibration:

a Uncheck the Cal Memory Protect checkbox.

b Click the Start button to begin the calibration.

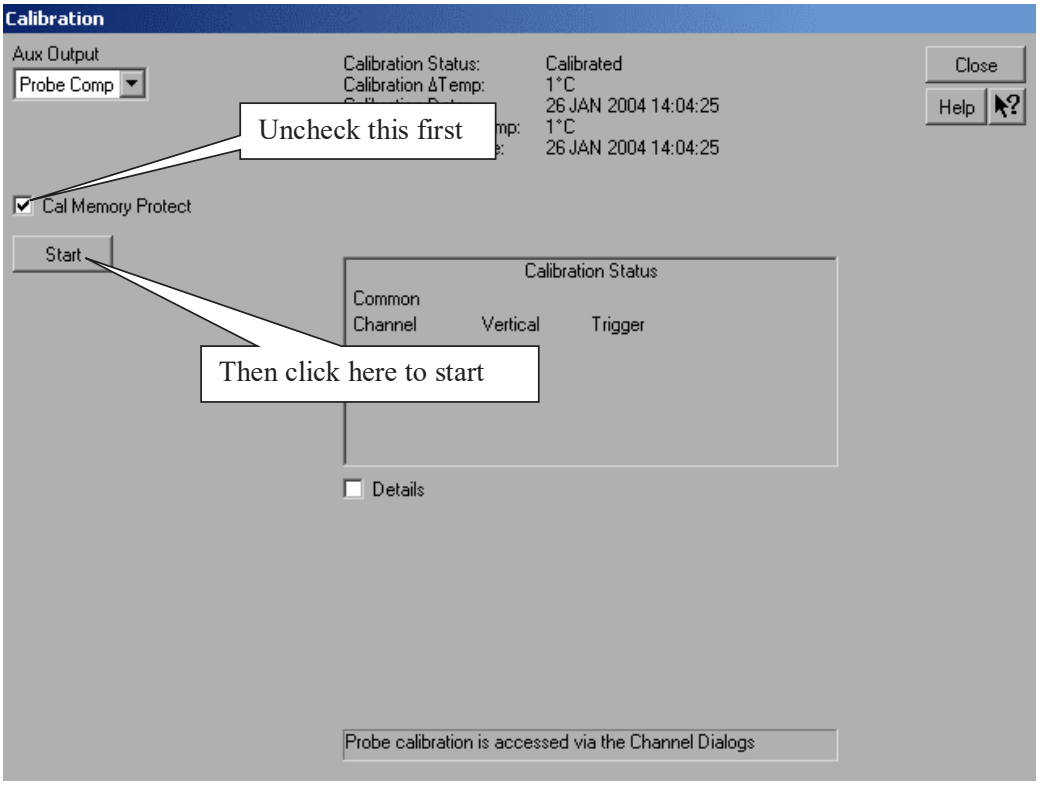


Figure 3 Oscilloscope Calibration Menu.

5 Follow the on-screen instructions:

a You will be prompted to disconnect everything from all the inputs, click the OK button.

b Then, you will be prompted to connect BNC shorting cap to a specified input. Install the BNC shorting cap by pressing it on the specified input BNC, and turning right. Click the OK button after moving the BNC cap to each specified channel.

c Then you will be prompted to connect the calibration cable with SMA adapters between the Aux Out and a specified input, as shown in the example in Figure 4 below. Install the SMA adapter by pressing it on input BNC, and hand tightening the outer ring turning right. Click the OK button after connecting the cable as prompted.

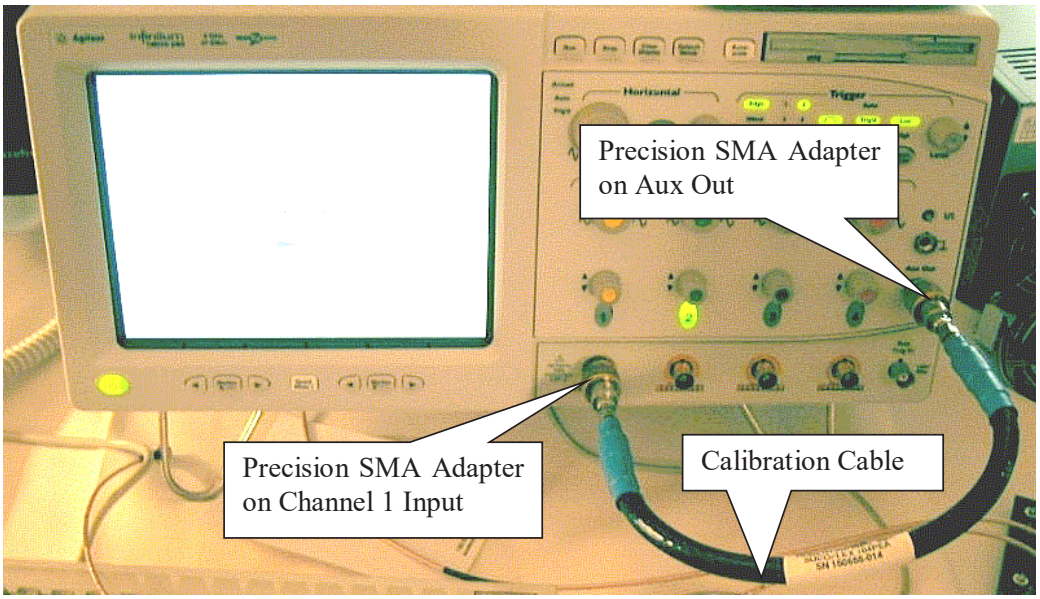


Figure 4 Calibration Cable Connection Example.

d Early during the calibration of channel 1, you will be prompted to perform a Time Scale Calibration, as shown in Figure 5 below.

e Click on the Default button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

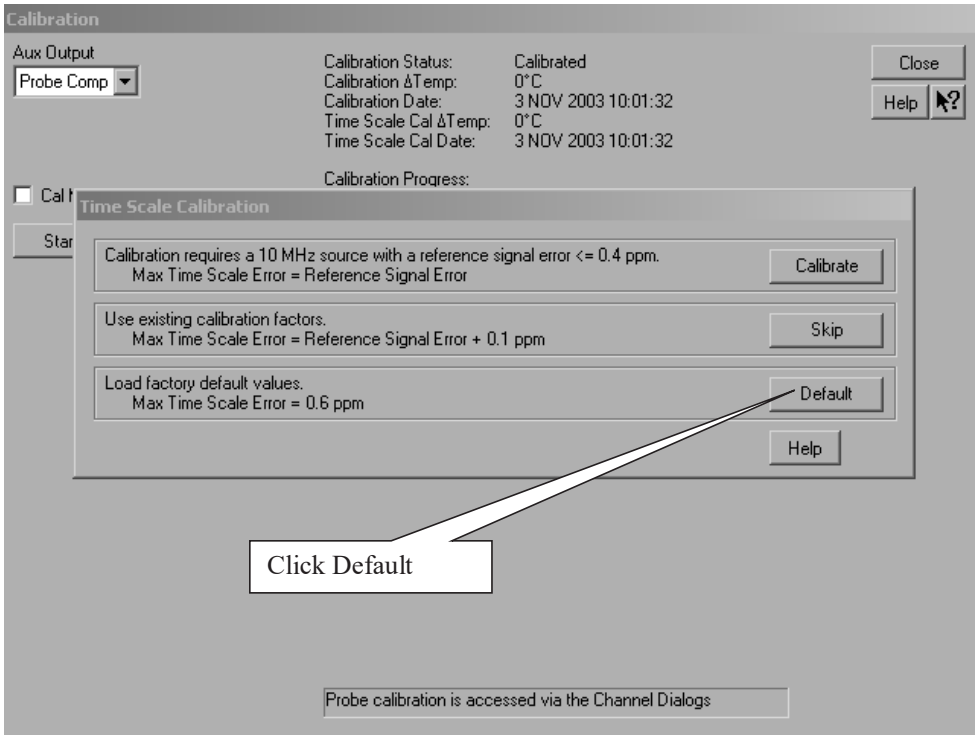


Figure 5 Time Scale Calibration Menu.

6 Referring to Figure 6 below, perform the following steps:

a Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

b Click the Close button to close the calibration window.

c The internal calibration is completed.

d Read NOTE below.

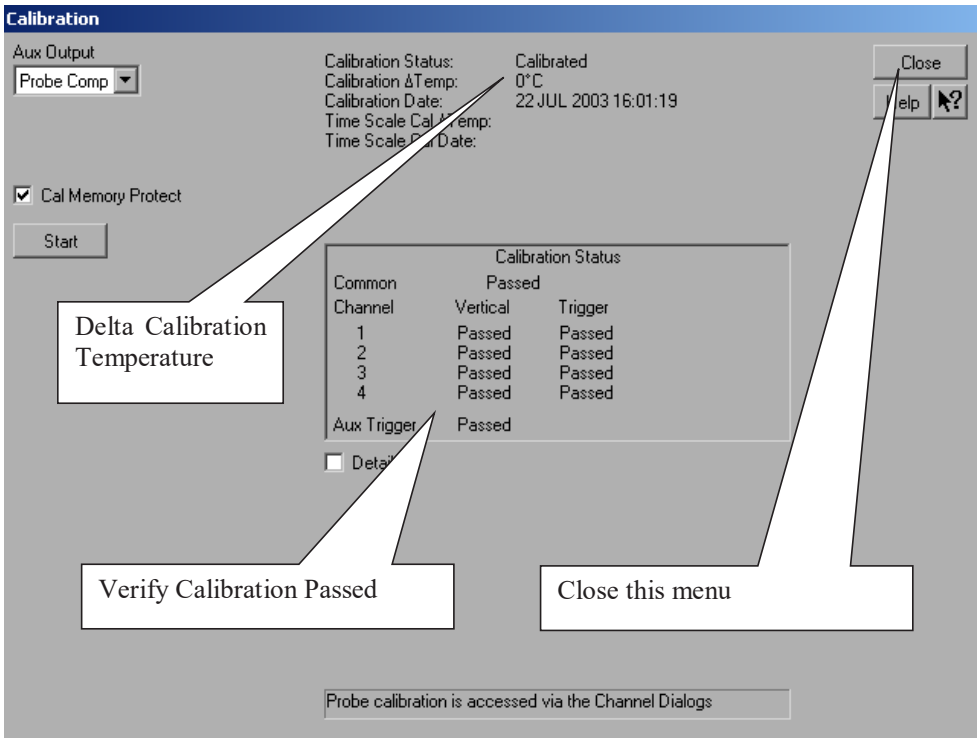


Figure 6 Calibration Status Screen.

NOTE

These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Cable and Probe Calibration

Perform a 50-ohm direct-coupled input calibration for the SMA interface of channel 1 and channel 3. This calibration compensates for gain, offset, and skew errors in cables and probes. Perform the following steps.

1 Referring to the Figure 7 below, perform the following steps:

a Locate and connect one of the Keysight precision SMA adapters to the Channel 1 oscilloscope input.

b Locate and connect the other Keysight precision SMA adapter to the Channel 3 oscilloscope input.

c Locate and connect one end of one of the RG-316 cables to the SMA adapter on Channel 1.

d Locate and connect one end of the other RG-316 cable to the SMA adapter on Channel 3.

e Locate and connect the non-Keysight SMA/BNC adapter to the Aux Out BNC on the oscilloscope.

f Connect the other end of the cable attached to Channel 1 to the SMA adapter on the Aux Out.

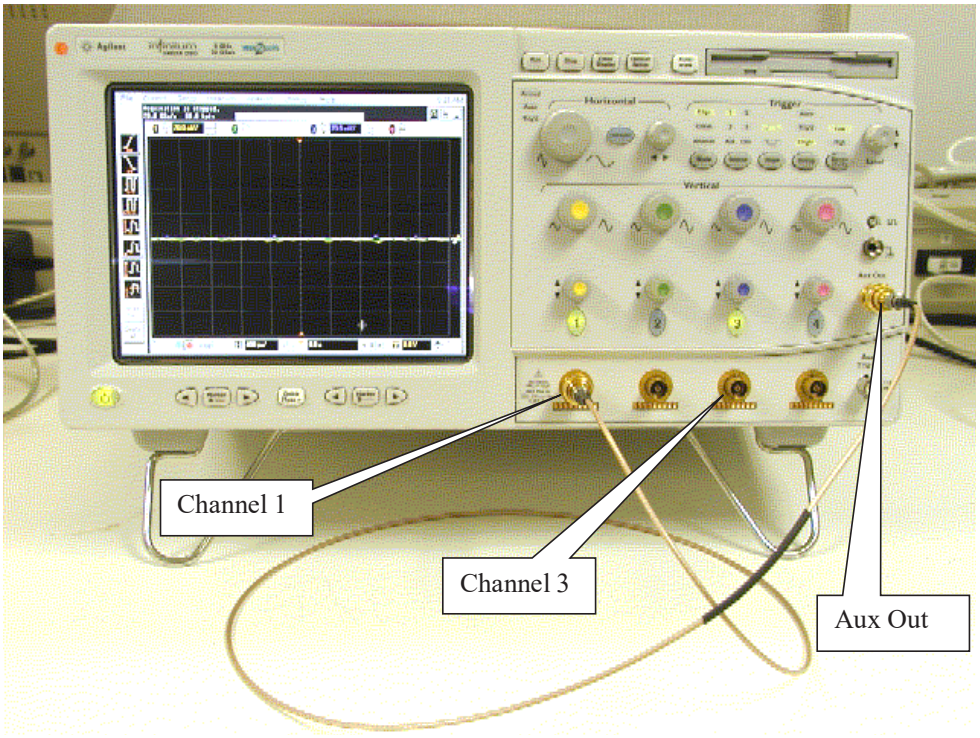


Figure 7 Vertical Input Calibration Connections (Cable on Channel 3 not shown).

2 Referring to Figure 8 below, perform the following steps:

a Click on the Setup>Channel 1 menu to open the Channel Setup window.

b Click the Probes button in the Channel Setup window, to open the Probe Setup window.

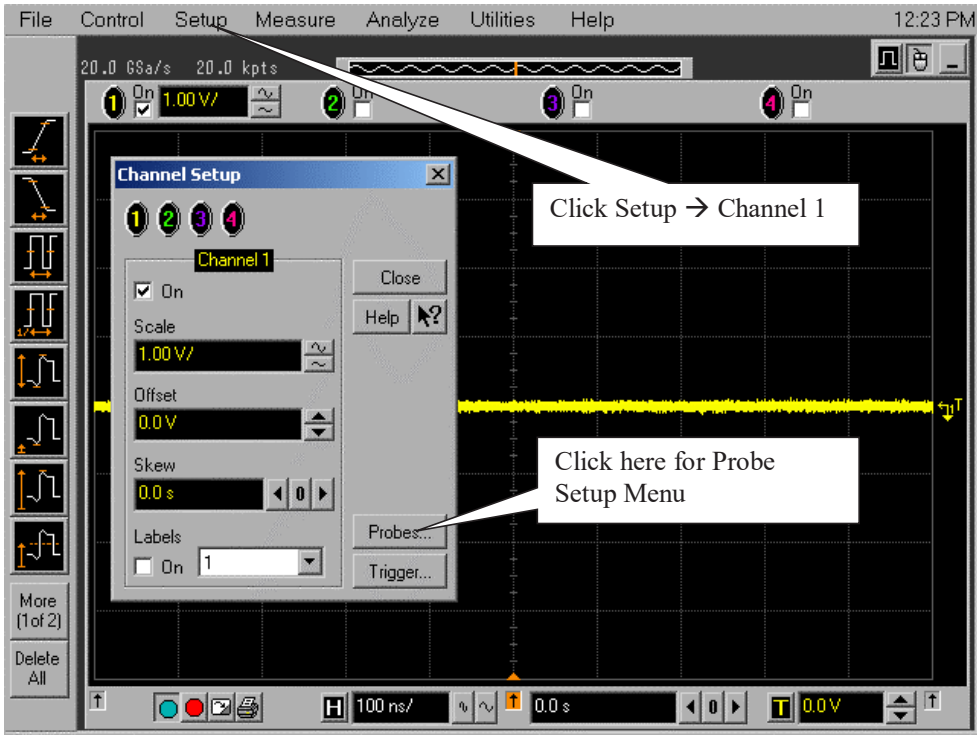


Figure 8 Channel Setup Window.

3 Referring to Figure 9 below, perform the following steps:

a Click the Configure Probing System button, and then click on User Defined Probes.

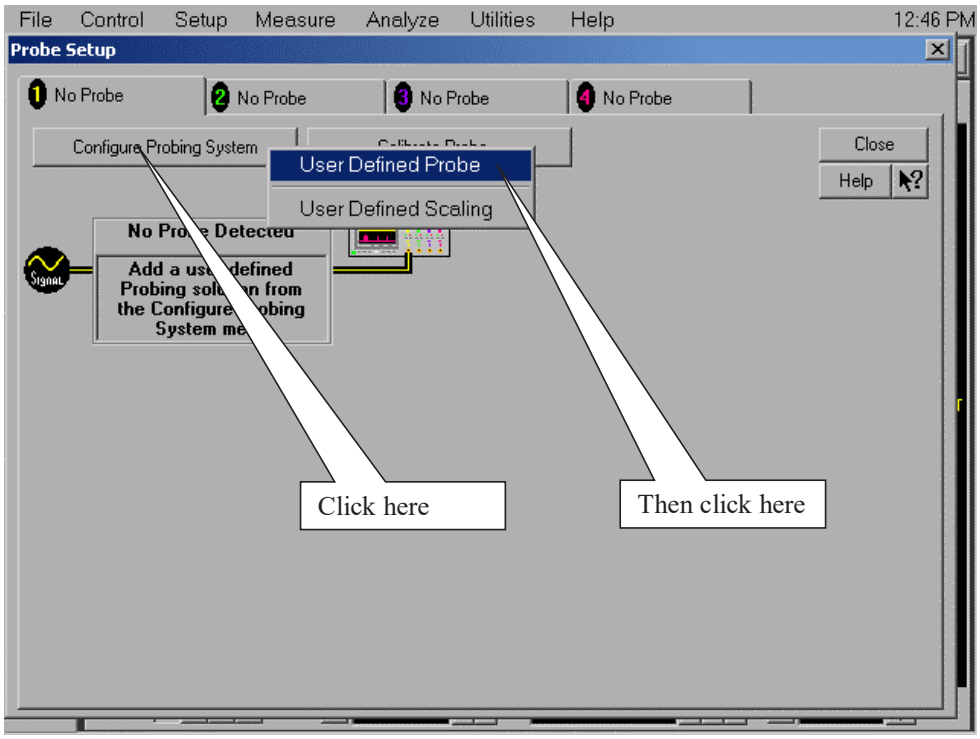


Figure 9 Probe Setup Window.

4 Referring to Figure 10 below, perform the following steps:

a Click on the Calibrate Probe button to open the Probe Calibration window.

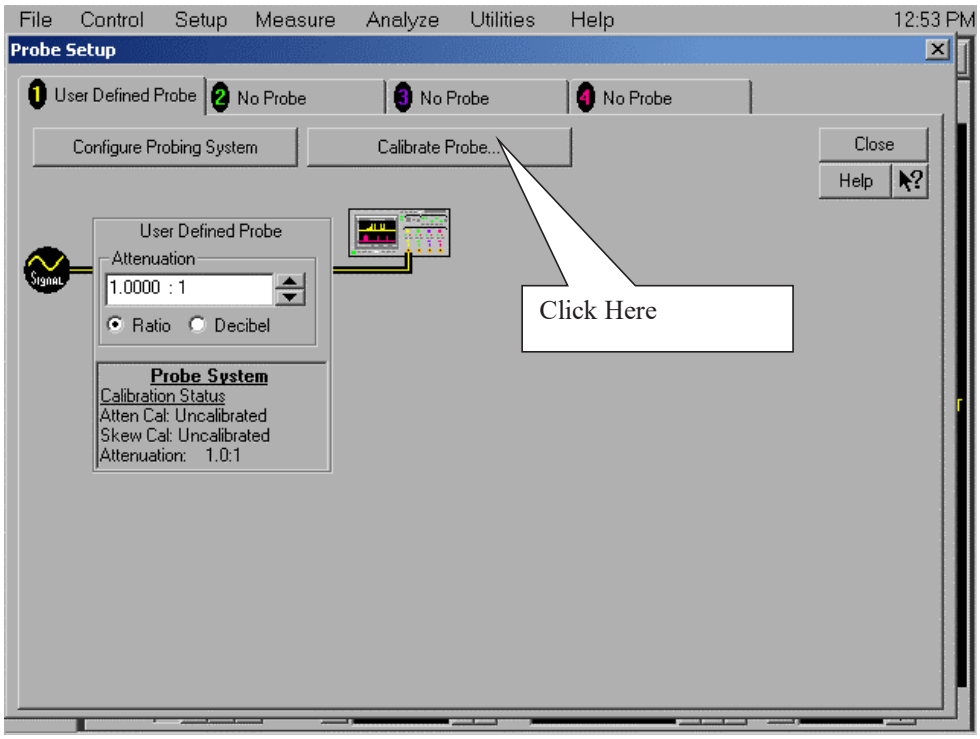


Figure 10 User Defined Probe Window.

5 Referring to Figure 11 below, perform the following steps:

a Select the Calibrated Atten/Offset Radio Button

b Click the Start Atten/Offset Calibration Button to open the Calibration window.

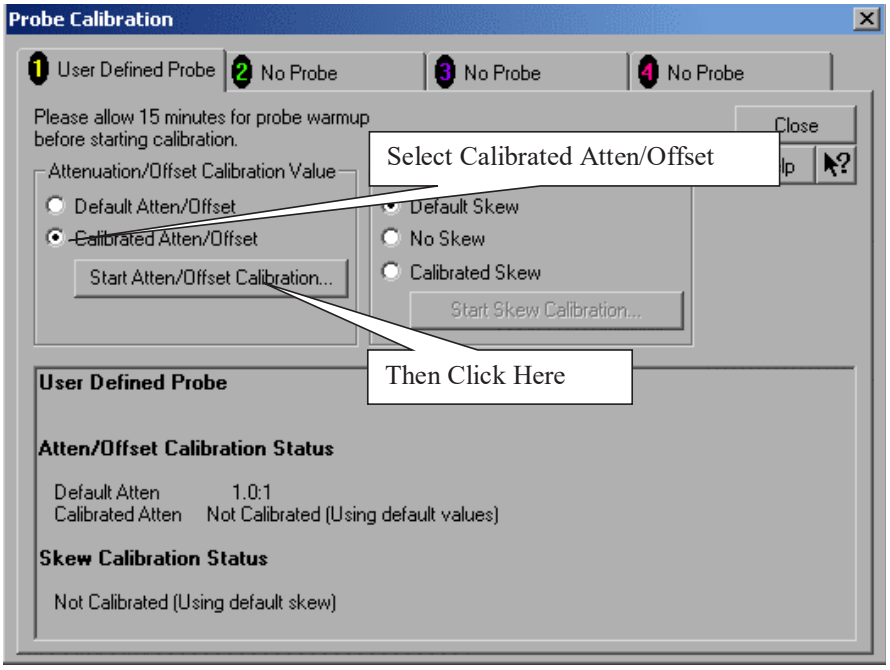


Figure 11 Probe Calibration Window.

6 Referring to Figure 12 shown below, perform the following steps:

a Ignore the instructions shown in the dialog box.

b Click the OK button on the Calibration window.

c The calibration should complete in about 10 seconds.

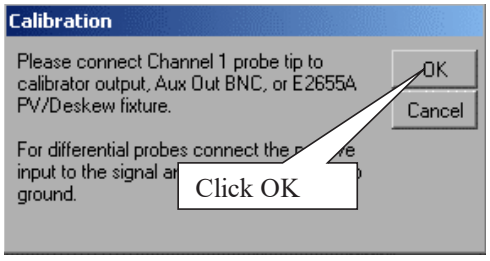


Figure 12 Calibration Window.

7 Referring to Figure 13 below, perform the following steps:

a Click OK to close the Probe Calibration Done window.

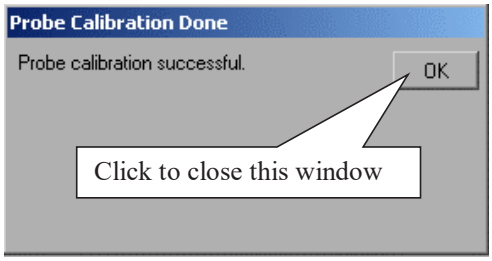


Figure 13 Probe Calibration Done Window.

8 Referring to Figure 14 below, perform the following steps:

a Select the Calibrated Skew Radio button in the Probe Calibration window

b Click the Start Skew Calibration button

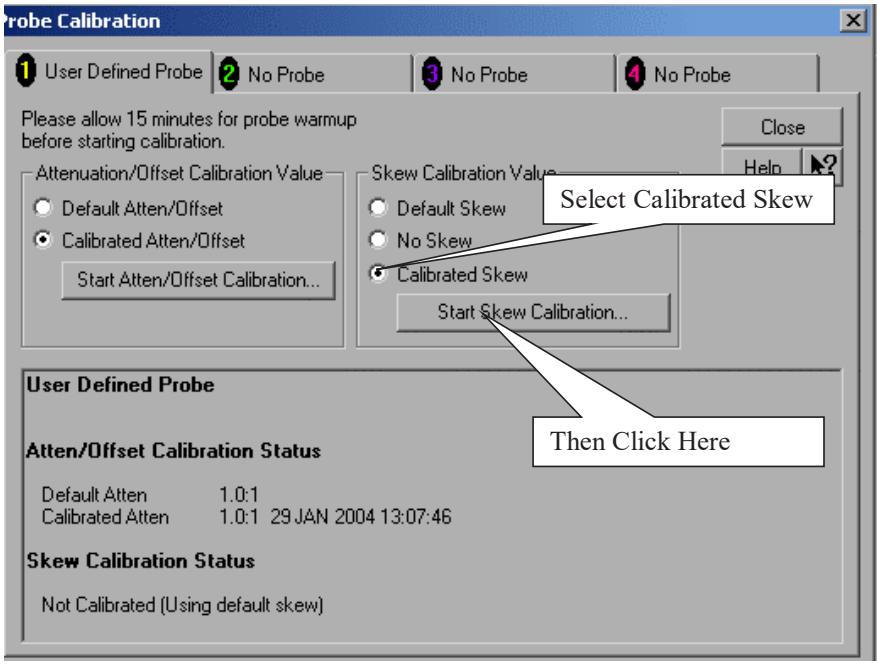


Figure 14 Probe Calibration Window.

9 Referring to Figure 15 shown below, perform the following steps:

a Ignore the instructions shown in the dialog box.

b Click the OK button on the Calibration window.

c The calibration should complete in about 10 seconds.

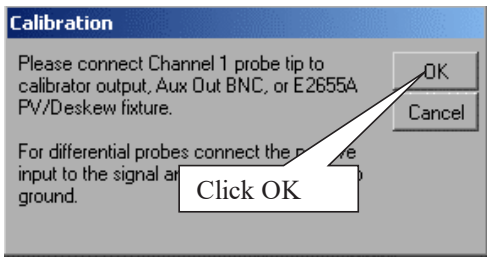


Figure 15 Calibration Window.

10 Referring to Figure 16 below, perform the following steps:

a Click OK to close the Probe Calibration Done window.

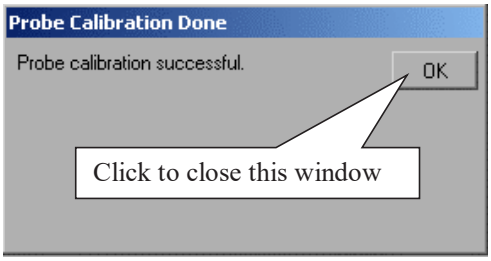


Figure 16 Calibration Window.

11 Referring to Figure 17 below, perform the following steps:

a Click the Close button to close this window.

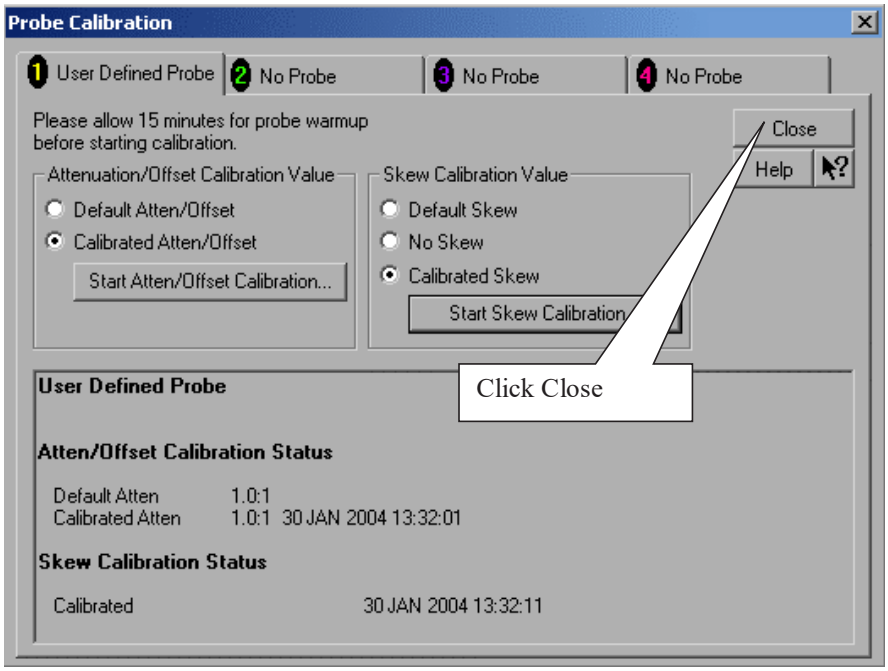


Figure 17 Calibration Window.

12 Referring to Figure 18 below, perform the following steps:

a Click on the Channel 3 tab.

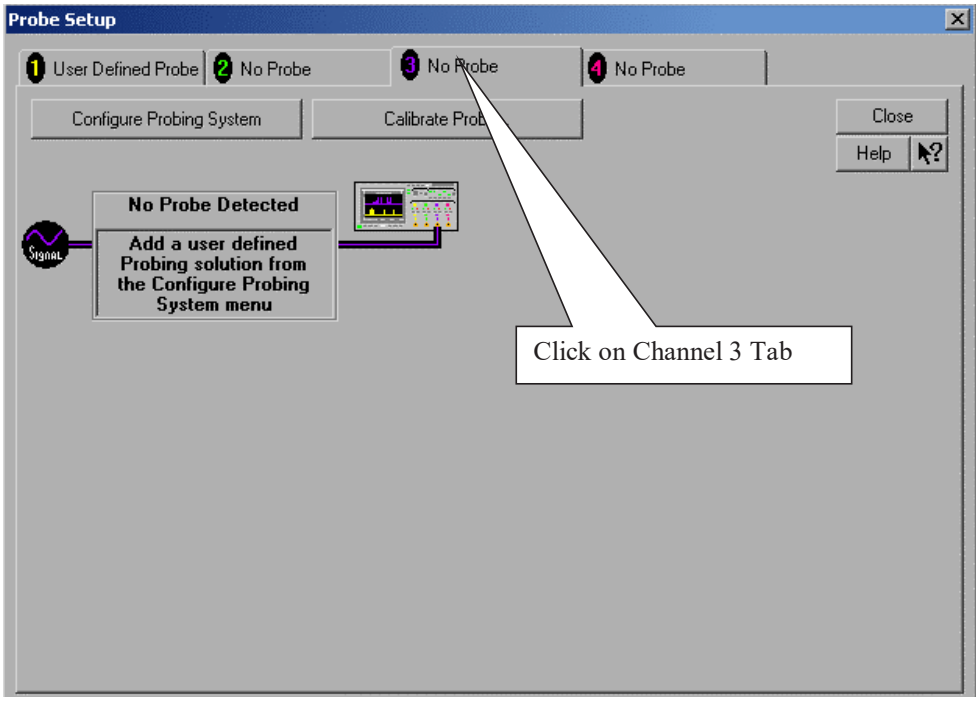


Figure 18 Calibration Window.

13 Referring to Figure 7 on page 334, perform the following steps:

a Disconnect the RG-316 cable connected to the SMA adapter on the Aux Out.

b Connect the other end of the RG-316 cable connected to the SMA adapter on Channel 3, to the SMA adapter on the Aux Out.

14 Repeat steps 3 through 11 of this section to calibrate the cable on Channel 3.

15 Click the Close button on the Probe Setup window (Figure 18) to close this window.

16 Click the Close button on the Channel Setup window (Figure 8 on page 335) to close this window.

17 The Cable and Probe calibration is complete.

18 Read the NOTE below.

NOTE

Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.

Channel-to-Channel De-skew

This procedure ensures that the timing skew errors between channel 1 and channel 3 are minimized. Perform the following steps:

1 Referring to Figure 19 below, perform the following steps:

a Do not disconnect the RG-316 cables from either the Channel 1 or Channel 3 SMA adapters.

b If not already installed, install the non-Keysight SMA adapter on the oscilloscope Aux Out.

c Disconnect any cable connected to the SMA adapter on the Aux Out.

d Locate and connect the middle branch of the SMA Tee to the SMA adapter on the Aux Out BNC.

e Connect the far end of the cable from the Channel 1 SMA adapter, to one branch of the SMA Tee on the Aux Out.

f Connect the far end of the cable from the Channel 3 SMA adapter, to the other branch of the SMA Tee on the Aux Out.

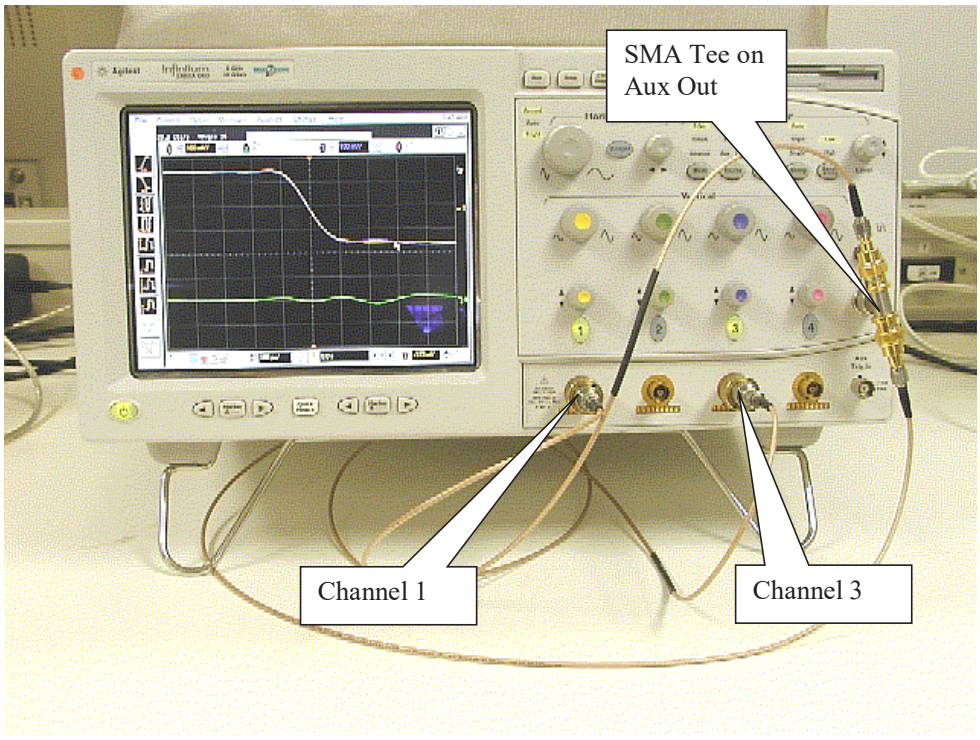


Figure 19 De-skew Connection.

2 Referring to Figure 20 below, perform the following steps:

a Select the File>Load>Setup menu to open the Load Setup window.

b Navigate to the directory location that contains the INF_SMA_Deskew.set setup file. If the setup file is not available, it can be created by following the instructions in Appendix B, “INF_SMA_Deskew.set Setup File Details.

c Select the INF_SMA_Deskew.set setup file by clicking on it.

d Click the Load button to configure the oscilloscope from this setup file.

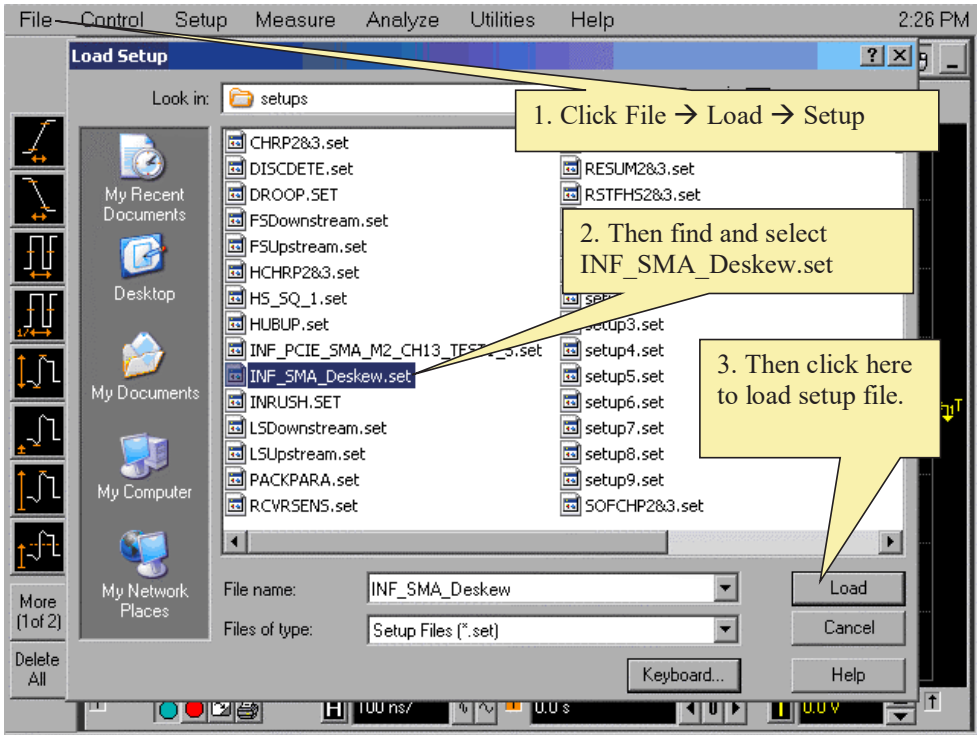


Figure 20 Load De-skew Setup.

The oscilloscope display should look similar to Figure 21 below. A falling edge of the square wave is shown in a 200 ps/div horizontal scale. The upper portion of the screen shows channel 1 (yellow trace) and channel 3 (purple trace) superimposed on one another. The lower portion of the screen is the differential signal (green trace) of channel 1 minus channel 3. The top two traces provide for visual inspection of relative time skew between the two channels. The bottom trace provides for visual presentation of unwanted differential mode signal resulted from relative channel skew (and to a much lesser extent from other inevitable channel mismatch parameters like gain and non-linearity). Figure 21 is an example of exaggerated skew between channel 1 and channel 3, measured to be about 50 ps with the cursor.

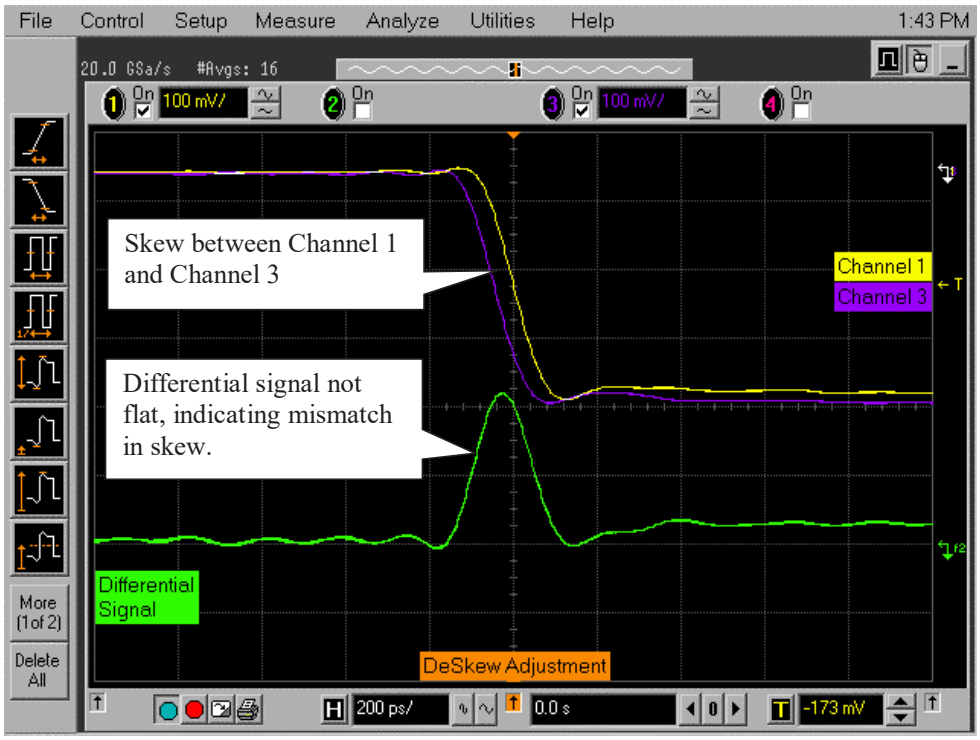


Figure 21 Channel Skew.

Figure 22 below shows the desired effect of no skew between the cables. Note that the channel 1 (yellow trace), channel 3 (purple trace) traces overlap, and the differential signal (green trace) is flat. If this is not the case, then perform the following steps to reduce the skew between channels 1 and 3.

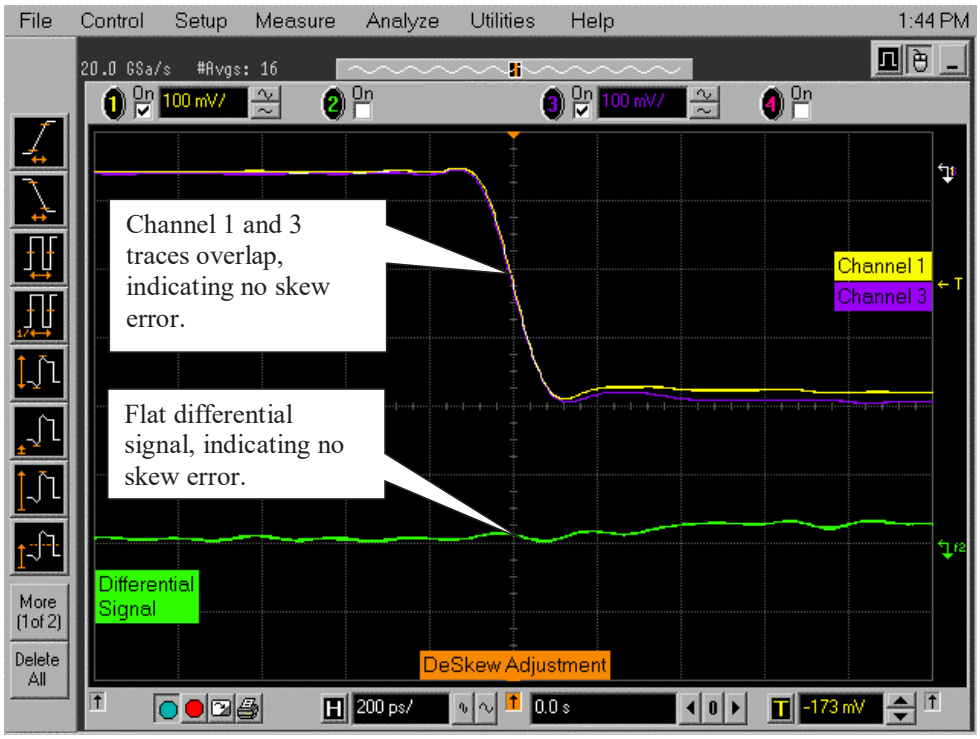


Figure 22 Skew Minimized.

3 Referring to Figure 23, perform the following steps to de-skew the channels:

a Click on the Setup>Channel 1 menu to open the Channel Setup window.

b Move the Channel Setup window to the left so you can see the traces.

c Adjust the Skew by clicking on the < or > arrows, to achieve the flattest response on the differential signal (green trace).

d Click the Close button on the Channel Setup window to close it.

e The de-skew operation is complete.

f Disconnect the cables from the Tee on the Aux Out BNC. Leave the cables connected to the Channel 1 and Channel 3 inputs.

g Read the NOTE below.

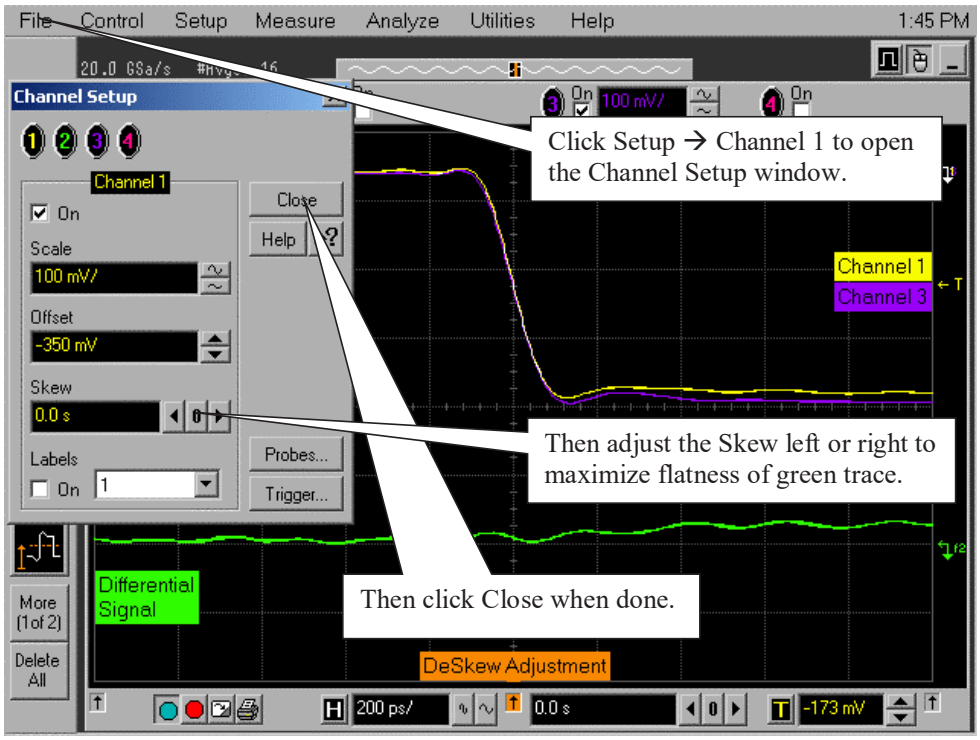


Figure 23 De-skewing Procedure.

NOTE

Each cable is now calibrated for the oscilloscope channel it is connected to. Do not switch cables between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the cables be labeled with the channel they were calibrated for.

B INF_SMA_Deskew.set Setup File Details

If the INF_SMA_Deskew.set file is not available, you can create it by following these instructions.

1 Start from a default setup by pressing the Default Setup key on the front panel. Then configure the following settings:

Acquisition	Averaging on number of averages 16 Interpolation on
Channel 1	Scale 100.0 mV/ Offset –350mV Coupling DC Impedance 50 Ohms
Channel 3	Turn Channel On; Scale 100.0 mV/ Offset –350m V Coupling DC Impedance 50 Ohms
Time base	Scale 200 ps/sec
Trigger	Trigger level –173mV Slope falling
Function 2	Turn on and configure for channel 1 subtract channel 3, Vertical scale 50 mV/ Offset 100.000 mV

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