

Keysight W3301A LPDDR3 BGA Interposers

Installation Guide

Notices

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In This Guide

This guide provides information on how to set up and use the following Keysight products in a LPDDR3 probing setup:

- W3301A LPDDR3 178-ball, BGA Interposer
- E5406A/B Pro Series Soft Touch Connectorless Single-ended Probes
- U4201A 90-pin Cable Connectors (*connects to the E5406A/B probes and Logic analyzer*)

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This chapter introduces the hardware components that are needed for a W3301A LPDDR3 BGA interposer setup. It also lists the software requirements as well as describes the mechanical considerations such as various dimensions and KOV that you should know before you start setting up and using this interposer.

W3301A LPDDR3 BGA Interposers - An Overview

The W3301A LPDDR3 BGA Interposer enables probing of 178-pin JEDEC standard footprint directly at the ball grid array using the Keysight logic analyzers.

This interposer supports:

- probing of all CA and DQ/DQS signals between a single-channel x32 DRAM and a PC board.
- data rates up to 1.6 Gb/s
- smaller KOV

Using this interposer, you can capture LPDDR3 signals up to 1.6 Gb/s for a system under test that can operate under probe load.

A W3301A interposer interposes between the DRAM being probed and the PC board where the DRAM would normally be soldered. The interposer is designed to be soldered to the PCB footprint for the DRAM on top of either the LPDDR riser included with the W3301A interposer or an optional Grypper socket (not included with the interposer) or both. The DRAM being probed is then soldered to the top side of the interposer.

Each LPDDR signal in the common footprint passes directly from the bottom side of the interposer to the top side of the interposer.

NOTE

The W3301A interposer is tested for via connections through the interposer.

The following figure shows a W3301A interposer's top view.

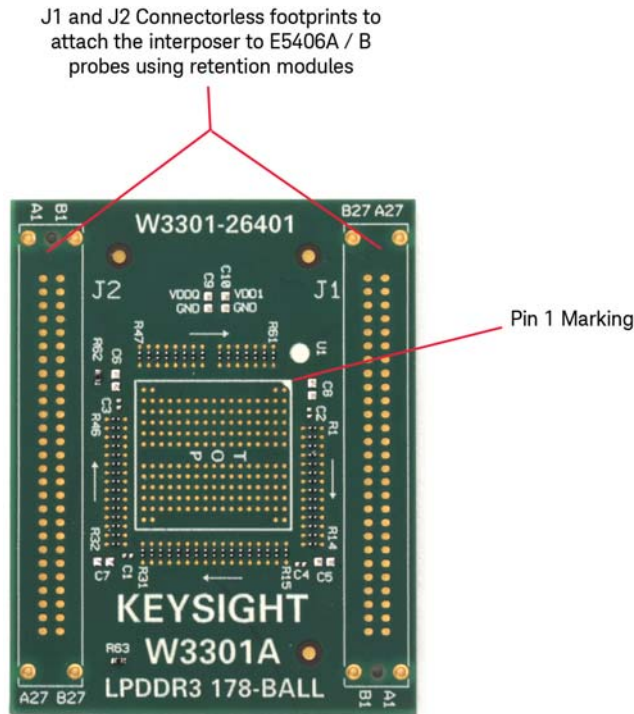


Figure 1 W3301A LPDDR3 Interposer

The W3301A interposer has two connectorless footprints, J1 and J2 on its top side. A retention module (shipped with the E5406A/B Soft Touch Series Connectorless probe) is soldered to each footprint. Each retention module attaches to an E5406A/B probe. These probes are then connected to the U4201A Logic Analyzer 90-pin cable connectors which then connect to the Logic Analyzer module's pods.

Compatibility with Logic Analyzer Modules

The W3301A interposers are compatible with the following Keysight logic analyzer modules.

- U4164A AXIe-based logic analyzer modules
- U4154A/B AXIe-based logic analyzer modules

Software Configuration

The W3301A interposer can be used in the following logic analyzer software configuration:

- State mode under 2500 Mb/s (double edge clocking and dual sampling mode)

You can use the W3301A interposer with the compatible logic analyzer module's dual clock edge clocking and dual sample mode. The U4164A module's dual sampling with dual thresholds allows you to capture separate Read and Write samples per clock edge.

W3301A Technical Features Summary

- Probes a JEDEC LPDDR3 BGA 178 ball standard footprint. Maximum of 11 mm wide X 11.5 mm long LPDDR3 DRAM package can fit on top of the W3301A interposer without an additional riser or a socket to provide clearance for the RC components. A 13 mm wide X 13.5 mm long LPDDR3 DRAM package can also fit without a riser but will cover the silk screen marking and overlap vias slightly.
- Logic analyzer connections are made using E5406A/B Pro Series Soft Touch Connectorless Single-ended probes and U4201A logic analyzer cables. The E5406A/B probes attach to the connectorless footprints on the top of the W3301A interposer using retention modules.
- An isolation Tip Resistor (100 Ohms) for each signal probed by the Logic Analyzer is present on the top of the W3301A interposer. No RC network present on the E5406A/B probes or on the top or bottom of the interposer.

W3301A Riser

An LPDDR3 BGA 178 ball riser is provided with each W3301A interposer to allow the interposer to clear surrounding devices. Optionally, you can use a Grypper socket. It is not provided with the interposer.

The following figure displays the riser that is provided with the W3301A interposer.

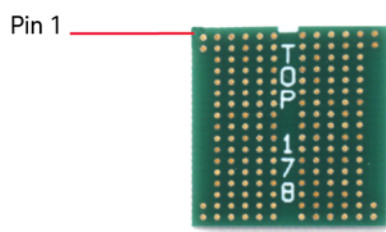


Figure 2 Riser that accompanies the W3301A interposer

NOTE

The LPDDR3 178 ball riser includes ground planes for optimal signal integrity. Due to these ground planes, the riser's alignment with the DRAM should be such that the TOP side of the riser must point towards the DRAM and the Pin 1 indicator on the riser must orient towards the "A1" pin of the DRAM.

To know how to solder the riser to the W3301A interposer and PC board, refer to the chapter "[W3301A Interposer and Riser Soldering Guidelines](#)" on page 19.

E5406A/B Pro Series Soft Touch Connectorless Single-ended Probes

The E5406A/B-pro series soft touch probes are ultra-low-load connector-less probes.

This probe attaches to a connectorless footprint on the top-side of the W3301A interposer using a retention module soldered to this footprint. The retention module ensures pin-to-pad alignment and holds the probe in place. On the other end, the probe connects to a U4201A logic analyzer cable that connects it to a logic analyzer module's pod.

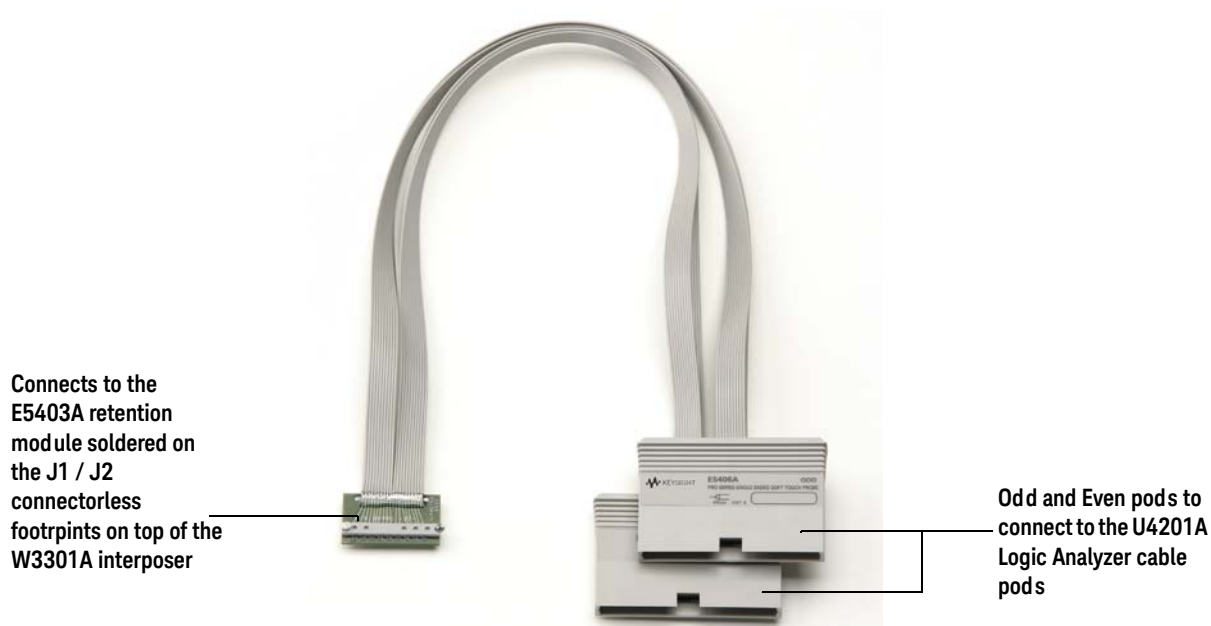
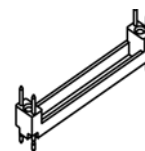


Figure 3 E5406A Probe

NOTE

The probe uses a “top-side” mountable retention module. A kit of five retention modules is shipped with each E5406A/B probe.

You can order additional kits using the Keysight part number - E5403A.



To know how to connect a W3301A interposer to an E5406A/B probe, refer to the following topics in this guide:

- “[Step 2 - Connecting the W3301A Interposer to E5406A/B Probes](#)” on page 28
- “[Step 3 - Connecting the E5408A/B Probe Pods to the U4201A Logic Analyzer Cable Pods](#)” on page 30

To get information such as equivalent probe loads, input impedance, time domain transmission (TDT), step inputs, eye opening, pinout, safety information, and dimensions of the E5406A/B probes, refer to the *E5400-Pro Series Soft Touch Connectorless Probes User's Guide* (part number E5404-97007) available on www.keysight.com.

U4201A 90-pin Logic Analyzer Cable

The U4201A logic analyzer cable connects an E5406A/B probe to a pod of a compatible Keysight AXIe-based logic analyzer module.

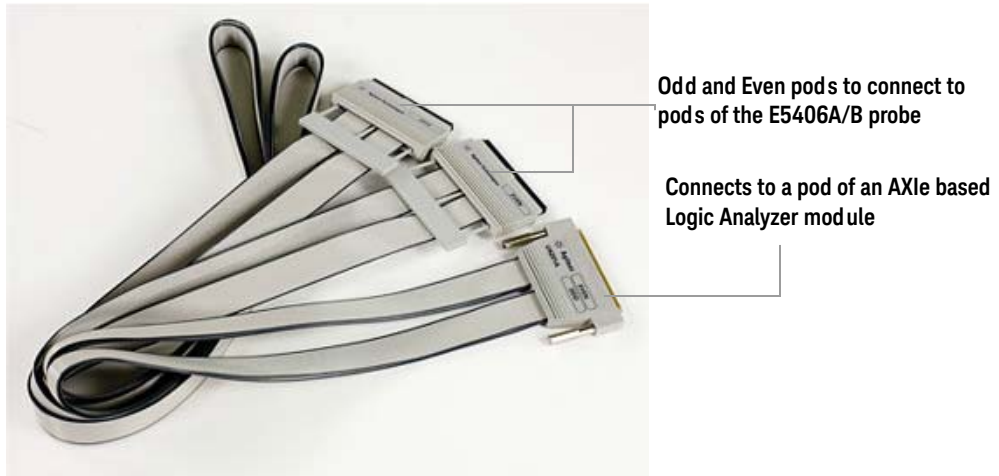


Figure 4 U4201A 90-pin logic analyzer cable

To know how to make connections of this cable with the E5406A/B probe and logic analyzer module, refer to the following topics:

- "Step 3 - Connecting the E5408A/B Probe Pods to the U4201A Logic Analyzer Cable Pods" on page 30
- "Step 4 - Connecting the U4201A Cables to Logic Analyzer Module Pods" on page 31

To get information such as the characteristics, specifications, safety information, and dimensions of the U4201A cable, refer to the *Keysight U4200A-Series Probes and Cables User Guide* (part number U4200-97000) available on www.keysight.com.

Hardware and Software Requirements

Before you start installing the W3301A interposer, ensure that you have the following list of hardware and software components needed for this interposer.

Hardware Requirements
U4164A or U4154A/B AXIe-based Logic Analyzer Module
M9502A 2-slot or M9505A 5-slot AXIe chassis to install the logic analyzer module
M9536A embedded controller or host PC with PCI express adapter card for the chassis
W3301A LPDDR3 Interposer(s)
E5406A/B probes (with retention modules) to connect the interposer to the logic analyzer cables Two probes needed for each interposer. The probes are sold separately from the interposer.
U4201A Logic Analyzer cables to connect the E5406A/B probes to the Logic Analyzer module Two cables needed for each E5406A/B probe.

Software Requirements	Licensing	Description
Logic and Protocol Analyzer software version 6.30 or higher. (Required)	Unlicensed base software with additional licensing options	Base software platform for configuring and using Keysight's logic analyzer modules.
B4661A Memory Analysis Software Tools Package version 6.30.1008 or higher. (Required)	Includes unlicensed as well as licensed features	Base software package that includes configuration files and tools to help you perform DDR/LPDDR post-process as well as real-time protocol compliance violation testing, decode and view memory transactions, and set up your logic analyzer for DDR/LPDDR data capture and analysis.
The below-mentioned licensed/unlicensed software features from the B4661A software package are required for W3301A.		
Default LPDDR configuration files (Required)	Available as an unlicensed standard feature with the B4661A package.	Includes default XML configuration files for use with the W3301A interposer.
DDR Setup Assistant and DDR Eyefinder software (Required)	Available as an unlicensed standard feature with the B4661A package.	A wizard- like application to help you set up your U4164A logic analyzer properly for use with the W3300A interposers.
DDR Custom Configuration Creator Tool (Required)	Available as an unlicensed standard feature with the B4661A package.	Allows you to define the footprint layout as per your custom probing solution used in the DDR/LPDDR setup and then create an XML configuration file based on this footprint information.
B4661A-2FP LPDDR Bus Decoder software (Recommended)	Available as a licensed feature with the B4661A package	Allows you to decode and view transactions, commands, and data from a LPDDR1, LPDDR2, LPDDR3 or LPDDR4 SDRAM memory bus in your device under test.
B4661A-3FP DDR 2/3/4 Protocol Compliance and Analysis toolset (Recommended)	Available as a licensed feature with the B4661A package	A set of tools to: <ul style="list-style-type: none"> ▪ evaluate and analyze the captured LPDDR data. ▪ perform real-time or post process compliance. ▪ set up a trigger on the specified address. ▪ graphically profile the distribution of memory accesses.
B4661A-4FP DDR 2/3/4 Memory Analysis Viewer (Recommended)	Available as a licensed feature with the B4661A package	A viewer installed and displayed within the Logic and Protocol Analyzer GUI to analyze: <ul style="list-style-type: none"> ▪ memory traffic statistics. ▪ refresh rate and self-refresh periods. ▪ distribution of memory accesses. ▪ memory performance measurements.

NOTE

You can install the above-mentioned software components by downloading the required executables from the Keysight web site at: www.keysight.com/find/lpa-sw-download.

The following table displays the number of W3301A interposers and cables required to provide connections to channels of your logic analyzer module.

DRAM	Data Width	Access to	Number of Interposers	Number of Probes	Number of Logic Analyzer cables	Number of Logic Analyzer Modules
LPDDR3 178 ball DRAM used as a single 32-bit channel device	Dual bank 16 bit	<ul style="list-style-type: none"> ▪ Ck_A ▪ All Channel A CA and control signals for Bank 0 and Bank 1 ▪ All DQS and DQ signals from all byte lanes. 	One W3301A	Two E5406A/B, one each for the J1 and J2 connectorless footprints of the interposer	Four cables for a W3301A interposer. (Two cables per E5406A/B probe used in the setup)	One U4164A/U4154A/B module

Mechanical Considerations

W3301A Interposer Dimensions

The following figure shows the dimensions of a W3301A LPDDR3 BGA interposer.

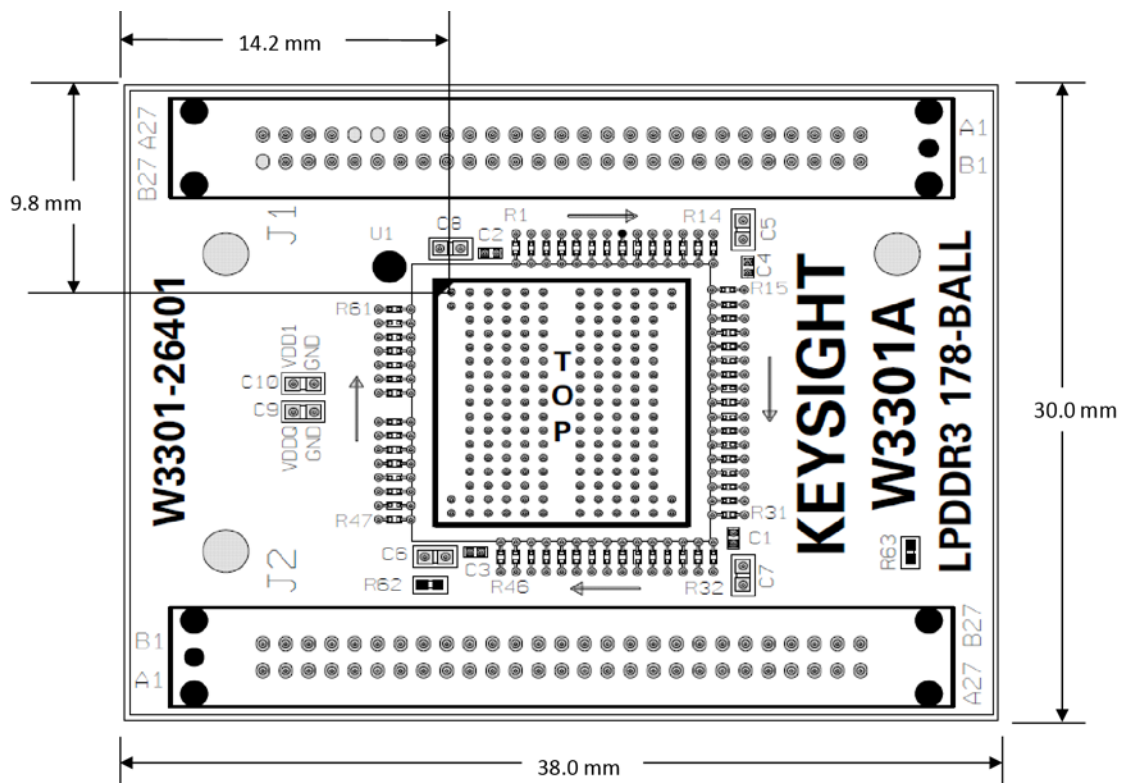
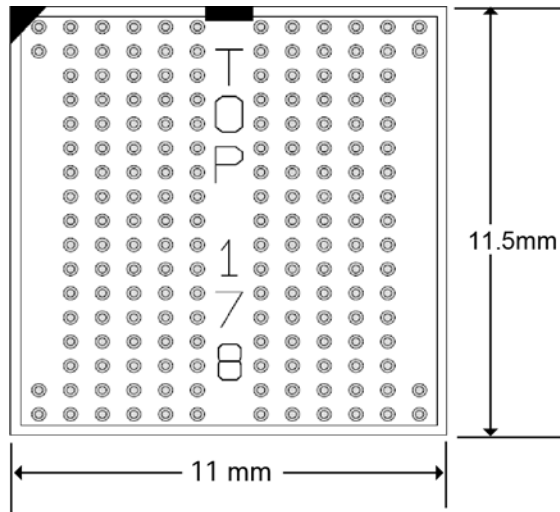


Figure 5 Dimensions of a W3301A interposer (Top View)

W3301A Riser Dimensions



W3301A Keep-Out Volume

NOTE

You must install the W3301A interposer on a riser (shipped with the interposer) or a grypper socket to provide clearance to surrounding DRAM.

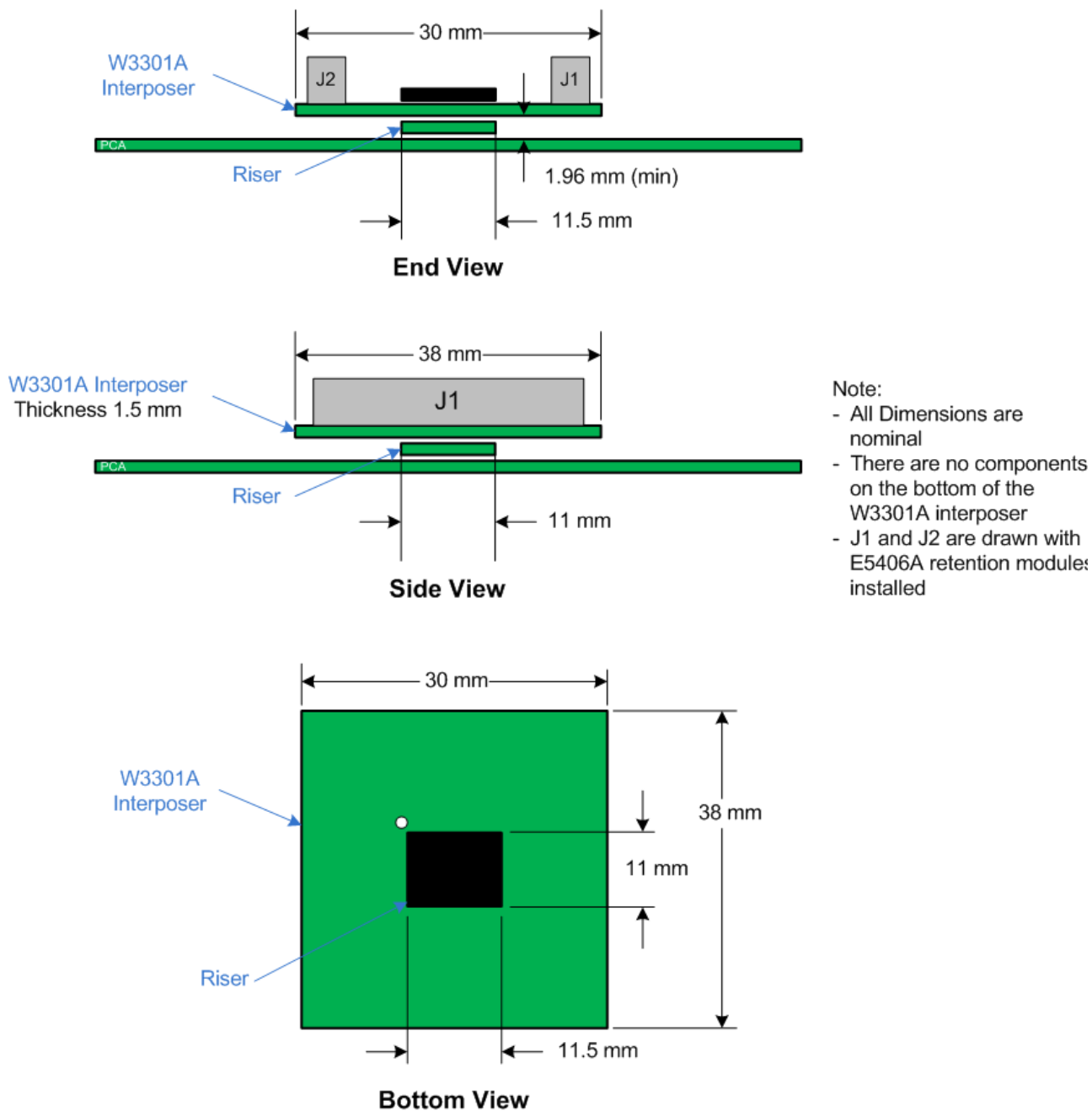


Figure 6 KOV of a W3301A interposer

2 W3301A Interposer and Riser Soldering Guidelines

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In this chapter, Keysight provides the soldering guidelines and information for W3301A interposer installation. However, Keysight cannot guarantee the successful interposer installation due to variations in processes and equipment used at individual BGA rework facilities.

Keysight recommends that interposers be installed by companies with specific expertise in this advanced type of processing.

Keysight does not endorse any specific BGA rework facility but recommends using a reputable and experienced BGA rework facility for the installation of BGA interposers. The following links are provided as a convenience to users investigating BGA rework facilities.

Information on BGA Rework Facilities

Circuit Technology Center
Haverhill, MA
USA

BGA Rework and Repair Services
<http://www.circuitrework.com/services/bga.shtml>

Keysight Technologies Adapter Rework
<http://www.circuitrework.com/features/671.shtml>

eTech
Round Rock, TX
www.eTech-WEB.com

Singularity Electronic Systems
Portsmouth, NH
www.singularitysys.com

Recommended Reading

BGA Component Rework Procedures
<http://www.circuitrework.com/guides/9-0.shtml>

BGA Component Rework Process Flow
<http://www.circuitrework.com/guides/9-1-1.shtml>

BGA Component Rework Inspection
<http://www.circuitrework.com/guides/9-1-2.shtml>

BGA Component Rework Profile Development, Standard Method
<http://www.circuitrework.com/guides/9-2-1.shtml>

Recommended Reading

BGA Component Rework Profile Development, Smart Track Method
<http://www.circuitrework.com/guides/9-2-2.shtml>

BGA Component Rework, Eutectic Solder Ball
<http://www.circuitrework.com/guides/9-3-1.shtml>

BGA Component Reballing, Fixture Method
<http://www.circuitrework.com/guides/9-4-1.shtml>

Recommended Soldering Guidelines

These guidelines are intended for anyone who has decided to install the winged BGA interposers themselves, or would like to provide guidelines to their regular contract manufacturer.

- The W3301A interposers are assembled using lead free or leaded soldering processes.
- Observe standard lead-free rework guidelines and processes when applying LPDDR memory devices and attaching a riser to an interposer and DIMM.
- Typical time-above-liquidus (220°C in the case of SAC305 solder) is 30 to 90 seconds with 60 seconds as the good nominal target.
- The peak temperature at the SAC305 solder joints should be a minimum of 235°C.
- It is best to limit the peak temperature on the package of the IC at a maximum of 245°C.
- To minimize heating effects on components mounted on the interposer assembly, a leaded solder process can be used to attach a riser, when it is compatible with your prototype debug and validation methodologies.
- The maximum processing temperature that the W3301A interposers can withstand is 260 °C for not more than 90 seconds.
- The W3301A interposers are supplied without solder balls. Depending on the exact attachment order, either leaded or lead-free solder may be preferred to attach the interposer to the DUT. The design of the interposer supports either choice.

Soldering Steps

These steps and guidelines apply only to the proper method of attaching BGA interposers to their target host boards. These do not attempt to provide instructions on how to attach BGA balls to the interposer, nor do these attempt to suggest a flux or a solder paste process.

- 1 Profile Development
 - a Profile must conform to the solder paste specification. Use the lowest possible temperatures that will insure reflow.
 - b Profile must also provide a slow ramp up to temperature.
 - c It is recommended that the profile be developed using a non-functional sample interposer in a location on a sample target that is similar to the actual target.
 - d The highest processing temperature must be in the range of 240 °C to 260 °C. The maximum processing time at the highest temperature must not exceed 90 seconds.
- 2 Material Baking
 - a Prior to soldering, bake interposer (to eliminate moisture) for 2-10 hours at 250° F (121° C).
 - b Shield flex areas.
 - c Polyimide films absorb moisture quickly; therefore, soldering and reflow should be done within 30 minutes after baking.
 - d A 7 or 9 zone conventional oven is beneficial. A conventional oven is preferred over infra-red.
 - e Vacuum ovens are also used to remove water. Lower temperatures, such as 150-175 F (65-80 C) can be used. This method also reduces the oxidation of the exposed copper pads.
 - f After baking, if the units are not reflowed within a few hours, these should be re-baked or placed in a desiccant chamber.
- 3 Host assembly components must be shielded using Kapton tape, aluminum heat shield blanket, or plates.
- 4 Site Preparation
 - a If the interposer is being installed onto a new board with gold pads, these pads should be pre-tin to ensure the pads wet properly, and to lower the chance of oxidation.
 - b Add solder paste to the target board using a mini-stencil. This is recommended over using flux only.
- 5 Interposer Reflow
 - a Use the lowest possible temp for reflow - Use a slow ramp up to temperature.
 - b Place the interposer using vision equipped BGA placement/reflow system such as an SRT.
 - c Reflow per the prepared heating profile.
- 6 Memory placement
 - a Add staking epoxy to the four corners of the placed interposer, and cure at 150°C for 2 minutes. This time is defined from the moment the adhesive reaches the cure temperature. As a convenience, the following link has been supplied on a staking adhesive.
[https://tds.us.henkel.com/NA/UT/HNAUTTDS.nsf/web/7DA17BAB270FA76E882571870000D6EE/\\$File/3609-EN.pdf](https://tds.us.henkel.com/NA/UT/HNAUTTDS.nsf/web/7DA17BAB270FA76E882571870000D6EE/$File/3609-EN.pdf)
 - b Apply solder paste to the top-side of interposer.
 - c Position memory using an SRT (or equivalent) with vision system for manual placement.
 - d Reflow per the prepared heating profile.
- 7 Post Processing
 - a Remove flux residue.
 - b Remove any Kapton tape heat shielding and peelable mask material.
 - c Remove heat shielding from the target board.

Interposer Fabrication Notes

Operating Environment

The W3301A interposers are constructed of polyimide material that supports solder attachment of the interposer using the higher temperatures required by a lead-free solder process. The coefficient of thermal expansion for the interposer is 55 ppm/degree C. When operating in a soldered-down environment over a wide range of temperatures, the expansion coefficient of the interposer, DRAM, and system being probed must be matched to avoid stress related failure of the solder connections between the Interposer and attached components. The interposer material allows operation over an industrial temperature range of -40 to +85 degrees Celsius (non-condensing), subject to the above constraint.

Mechanical Dimensions

When a W3301A interposer is soldered to a riser, flatness must be maintained on the order of 3.5 mils or less across the BGA footprint to maximize successful soldering to the interposer.

3 Setting up the W3301A Interposer

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W3301A Interposer Setup - Overview

- 1 Solder the interposer, riser, and memory components. (See [page 27](#))
- 2 Solder the retention modules to the connectorless footprints on top of the W3301A and then attach the E5406A/B probes to these retention modules. (See [page 28](#))
- 3 Connect the E5406A/B probe cables to the U4201A Logic Analyzer cable pods. (See [page 30](#))
- 4 Connect the U4201A Logic Analyzer cable pods to the Logic Analyzer module pods. (See [page 31](#))

CAUTION

Use ESD precautions. Electrostatic discharge can damage components on your board or in the interposer. Use a grounded wrist strap and other ESD control measures as appropriate.

NOTE

Do not open the vacuum sealed packs of the W3301A interposer until you are ready to install the interposer. Discard these packs once the package is opened.

Step 1 - Soldering the W3301A Interposer

The W3301A interposer needs to be attached to the JEDEC LPDDR3 BGA 178 footprint on the design to be probed. The desired DRAM is soldered to the top side of the interposer. This attachment may occur in any order (i.e. first solder the interposer to the DUT, and then solder the DRAM to the interposer, or first solder the DRAM to the interposer, and then solder the DRAM+interposer assembly to the DUT). The interposer is designed to tolerate lead-free soldering temperature profiles. However, it is always recommended to apply the minimum temperature required and the minimum number of heating/cooling cycles to reduce risk of any damage to the interposer.

The stack up of these soldered components is illustrated in the following figure.

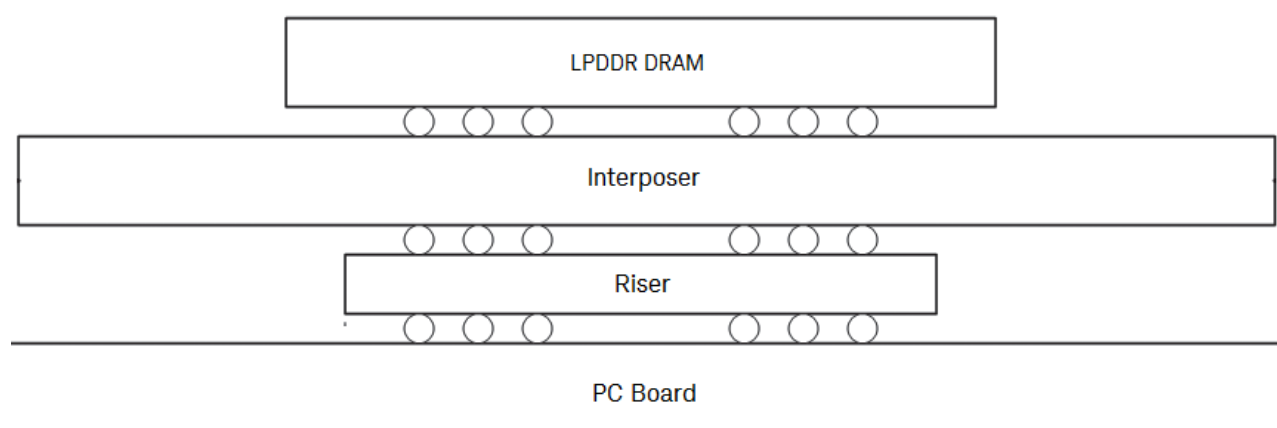


Figure 7 PC board, riser, interposer, and DRAM stack up

NOTE

A maximum of 13 mm wide X 11.5 mm long LPDDR3 DRAM package can fit on top of the W3301A interposer without an additional riser or a socket between the DRAM and interposer to provide clearance for the RC components.

Refer to the chapter "[W3301A Interposer and Riser Soldering Guidelines](#)" on page 19.

Step 2 - Connecting the W3301A Interposer to E5406A/B Probes

After soldering components, you can connect the W3301A interposer to the E5406A/B probes. The E5406A/B probes attach by soldering the E5406A retention modules to the connectorless footprints on top-side of the W3301A interposer.

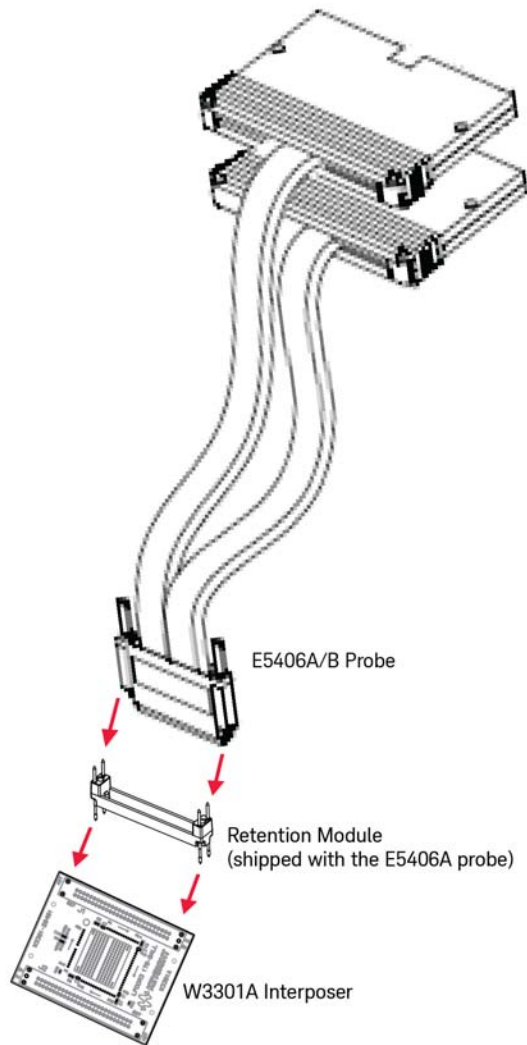


Figure 8 W3301A Interposer connected to an E5406A/B Probe

- 1 Attach the retention module to the interposer from the top.
 - a Insert the retention module into the interposer noting the keying pin.
 - b Solder alignment pins from the top ensuring that solder is added until a fillet is visible on the pin.

- 2 Insert the E5406A/B probe into the retention module.
 - a Ensure proper keying by aligning the Keysight logo on the probe with the one on the retention module and place the probe end into the retention module.
 - b Alternate turning each screw on the probe a little until both screws are finger tight like you would attach a cable to your PC.

Step 3 - Connecting the E5408A/B Probe Pods to the U4201A Logic Analyzer Cable Pods

Two U4201A cables are needed for each E5406A probe used in the setup.

The two pods of the E5406A/B probe and U4201A cable are labeled Odd and Even. Connect these pods as follows:

- Connect the Odd pod of E5406A to the Odd pod of the first U4201A cable.
- Connect the Even pod of E5406A to the Odd pod of the second U4201A cable.
- Do not connect the Even pods of the two U4201A cables used in the setup.

Similarly, connect the other E5406A probe's Odd and Even pods to the third and fourth U4201A cables used in the setup.

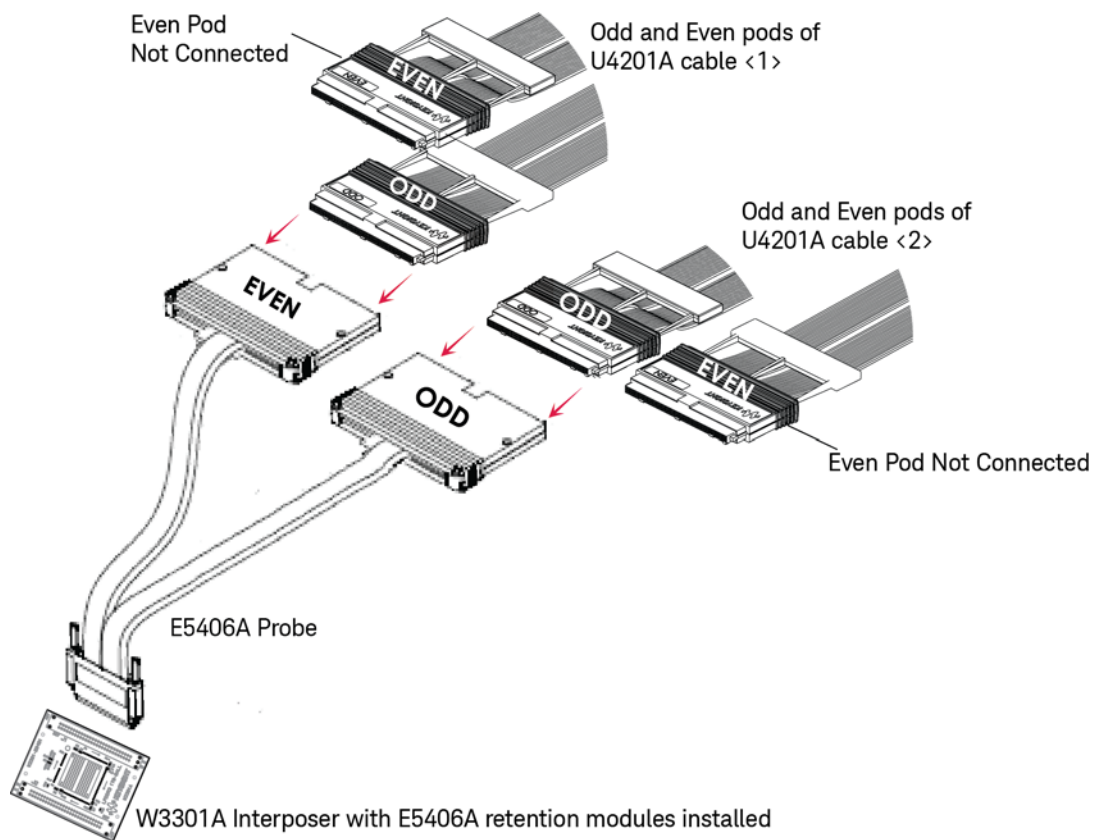


Figure 9 An E5406A/B Probe's pods connected to the Odd pods of two U4201A Cables

Step 4 - Connecting the U4201A Cables to Logic Analyzer Module Pods

Connect the Odd pods of the U4201A cables to the logic analyzer module pods as per the mapping given in the following table. (Even pods of the U4201A cables and logic analyzer module are NOT used.)

E5406A/B Probe Pods	U4201A Cable Pods	Logic Analyzer Module Pods
Even pod of E5406A probe <1> connected to J1 connectorless footprint of interposer	Odd pod of U4201A cable <1>	Pod 1
Odd pod of E5406A probe <1> connected to J1 connectorless footprint of interposer	Odd pod of U4201A cable <2>	Pod 7
Even pod of E5406A probe <2> connected to J2 connectorless footprint of interposer	Odd pod of U4201A cable <3>	Pod 5
Odd pod of E5406A probe <2> connected to J2 connectorless footprint of interposer	Odd pod of U4201A cable <4>	Pod 3

The mapping of the cable pods and logic analyzer pods is also illustrated with the help of the following diagram.

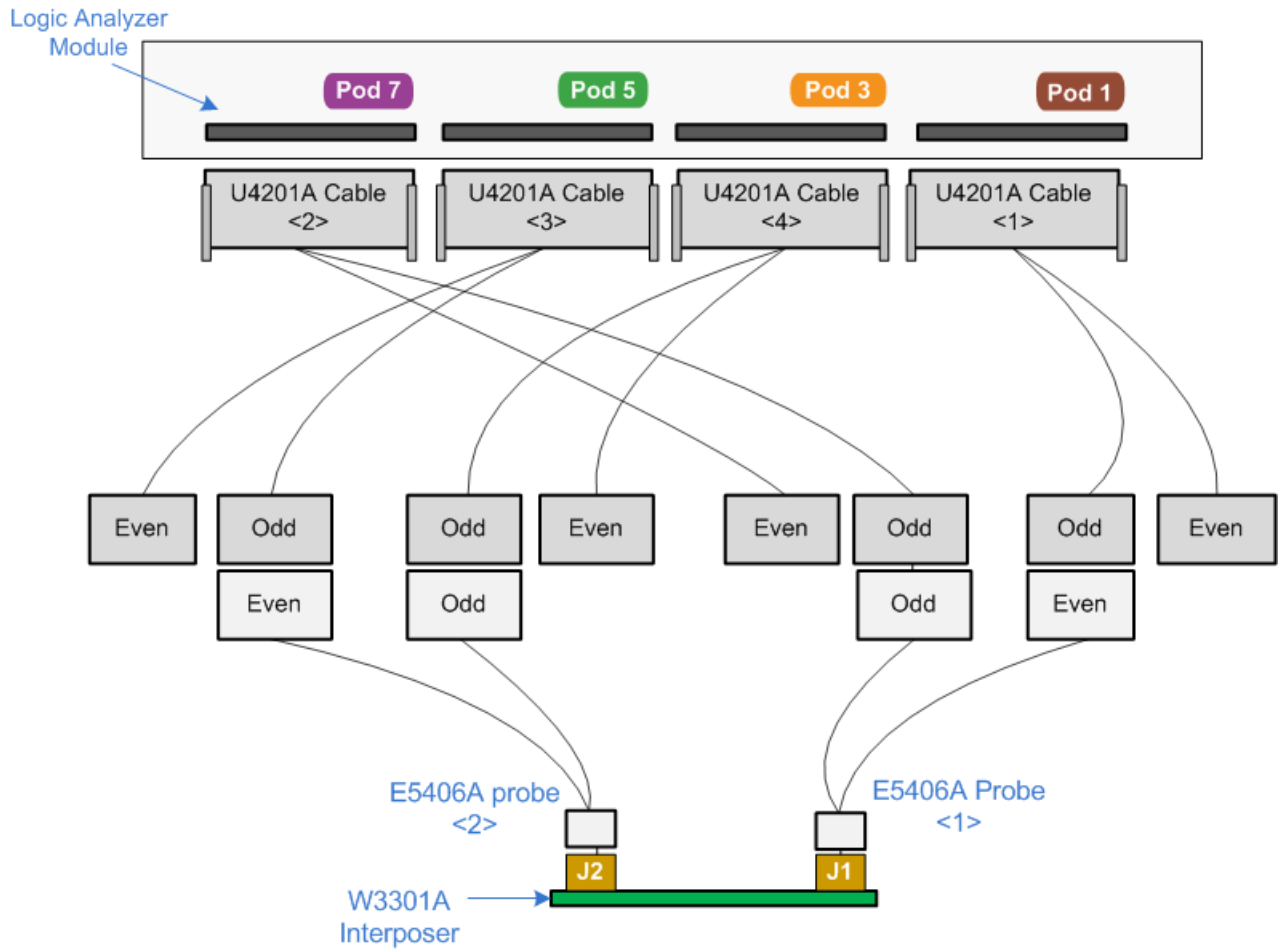


Figure 10 Connections between U4201A cables and Logic Analyzer pods

W3301A Interposer Connectorless Footprints Pinout

The diagram below illustrates the pinout of the two connectorless footprints - J1 and J2 on top of a W3301A interposer.

In the following pinout,

- Clock/Qualifier inputs are highlighted with yellow

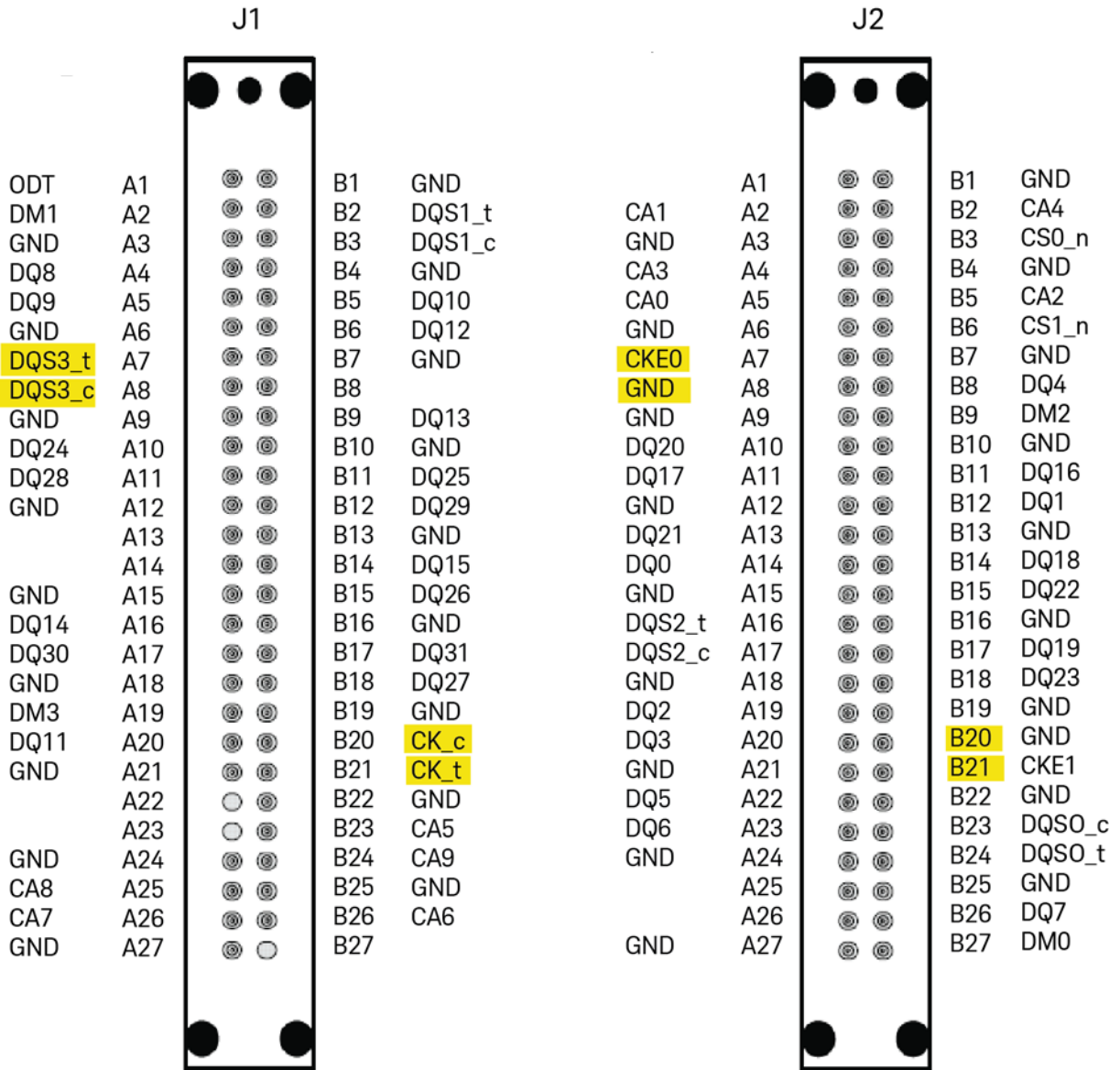


Figure 11 W3301A Interposer Connectorless Footprints Pinout

Logic Analyzer Channels to Signals Mapping

When you connect the U4201A cables to a Logic Analyzer as per the connection diagram in [Figure 10](#), the logic analyzer channels are mapped to LPDDR3 signals as per the table displayed below.

These signals are automatically configured when you load one of the configuration files supplied with the Keysight B4661A LPDDR decoder software.

Note:

- Clock inputs for each logic analyzer pod are highlighted with yellow in this table.

Table 1 Signals and Logic Analyzer Channels Mapping when using the W3301A Interposer

Logic Analyzer Pod and its Channels	Signals on Even pod of E5406A connected to J1	Logic Analyzer Pod and its Channels	Signals on Odd pod of E5406A connected to J1		
Pod 1	0	DQ15	0	ODT	
	1	DQ26	1	DM1	
	2	DQ14	2	DQS1_t	
	3	DQ30	3	DQS1_c	
	4	DQ31	4	DQ8	
	5	DQ27	5	DQ9	
	6	DM3	6	DQ10	
	7	DQ11	Pod 7	7	DQ12
	8		8		
	9		9	DQ13	
	10	CA5	10	DQ24	
	11	CA9	11	DQ28	
	12	CA8	12	DQ25	
	13	CA7	13	DQ29	
	14	CA6	14		
	15		15		
	CLK-	CK_c	CLK+	DQS3_t	
	CLK+	CK_t	CLK-	DQS3_c	

Logic Analyzer Pod and its Channels	Signals on Even pod of E5406A connected to J2	Logic Analyzer Pod and its Channels	Signals on Odd pod of E5406A connected to J2	
Pod 5	0	DQ18	0	
	1	DQ22	1	CA1
	2	DQS2_t	2	CA4
	3	DQS2_c	3	CS0_n
	4	DQ19	4	CA3
	5	DQ23	5	CA0
	6	DQ2	6	CA2
	7	DQ3	7	CS1_n
	8	DQ5	8	DQ4
	9	DQ6	9	DM2
	10	DQS0_c	10	DQ20
	11	DQS0_t	11	DQ17
	12		12	DQ16
	13		13	DQ1
	14	DQ7	14	DQ21
	15	DM0	15	DQ0
	CLK-	GND	CLK+	CKE0
	CLK+	CKE1	CLK-	GND

Signals not probed by the Logic Analyzer

The following signals are omitted from the Logic Analyzer connections for the W3301A interposer.

Interposer	Signal Name
W3301A	DNU
	VDDCA
	VDD1
	ZQ0
	ZQ1
	VDD2
	VrefCA
	VDDQ
	VrefDQ

4 Setting Up the Logic Analyzer for W3301A Interposers

Before You Start / 38
Loading a Configuration File / 39

Before You Start

Ensure that all the software components listed in the topic "[Hardware and Software Requirements](#)" on page 13 are installed on the host computer and the required software licenses are also obtained and installed.

Loading a Configuration File

When you install the Keysight B4661A Memory Analysis software package, a set of XML LPDDR configuration files is installed as a part of the standard unlicensed features of this package. Based on the software configuration (see [page 9](#)) in which you want to use your W3301A interposer with the logic analyzer, you can load an appropriate configuration file from this set in the Logic and Protocol analyzer GUI.

Licensing is not required for obtaining or loading these configuration files.

When you load a configuration file, it will set up the buses and signals, add the LPDDR decoder tool, and add a listing tool in the Logic and Protocol Analyzer GUI. The LPDDR Decoder tool is a licensed feature of the B4661A software package.

To load a provided configuration file:

- 1 Close the logic analyzer GUI window, if it is open.
- 2 Navigate to the following folder that contains all the LPDDR configuration files.
Users/Public/Public Documents/Keysight Technologies/Logic Analyzer/Default Configs/Keysight/LPDDR Bus Decoder
- 3 Select the LPDDR bus type.
- 4 Select the **BGA** and then choose a configuration file corresponding to the bus size and speed.
- 5 Double-click the configuration file to open it.

When you click on a configuration file, the Logic and Protocol Analyzer software will start and configure itself to use the decoder.

The logic analyzer Buses/Signals setup dialog allows you to assign descriptive labels to each analyzer channel that associate each channel with the particular DRAM and DRAM signal being probed.

NOTE

If your unique multi-DRAM configuration is not covered by one of the default configurations, you can use the *DDR Custom Configuration Creator* tool installed with the B4661A Memory Analysis SW package to create your own custom LPDDR BGA configuration.

NOTE

It is recommended that you use the **Advanced Probe Settings (APS)** for all signals on all W3301A interposers. For instructions, refer to the application note "**Capture Highest DDR3 Data rates using Advanced Probe Settings**" available at:

<http://literature.cdn.keysight.com/litweb/pdf/5991-0799EN.pdf?id=2284314>.

To save a configuration file

After you set up the logic analyzer, it is strongly recommended that you save the configuration.

To save your work, select **File>Save As...** and save the configuration as an ALA format file.

ALA format configuration files are more complete and efficient than XML format configuration files. See the Logic and Protocol Analyzer online help for more information on these formats.

5 Characteristics, Regulatory, Safety and Storage Information

Operating Characteristics / 42
Storage, Inspection, and Baking Guidelines / 43
Regulatory Notices / 44

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics.

Characteristics	Description
Temperature	Operating: +5° C to +40° C Non Operating : - 40 ° C to +70° C
Altitude	4,600 m (15,000 ft)
Relative Humidity Range Noncondensing	50% RH Min/80% RH Max at 40° C noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the circuit board. For indoor use only.

Characteristics	Description
To interposer	Memory bus signals from target system
From interposer	High-density connectors for Keysight U4164A AXIe-based logic analyzer module

Storage, Inspection, and Baking Guidelines

The following are some of the guidelines for storing and shelf life of the W3301A interposers.


Guidelines for Shelf Life and Solder-ability of W3301A Interposers

If your Interposer exceeds shelf life (1 year) before solder into application, use the following inspection and baking method.

- Inspect the humidity indicator within moisture proof vacuum sealed bag(s).
- If the humidity indicator shows moisture then bake the board at 120 degrees C for 4 hours and perform the solder-ability test.
- If the test passes, proceed with the assembly (reflow) of interposer.
- If delamination occurs, the interposer cannot be used.

Regulatory Notices

WEEE Compliance

Safety Symbol	Description
	<p>This product complies with the WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/electronic product in domestic household waste.</p> <p><i>Product Category: With reference to the equipment types in the WEEE Directive Annex I, this product is classed as a "Monitoring and Control Instrumentation" product.</i></p> <p>Do not dispose in domestic household waste. To return unwanted products, contact your local Keysight office, or see "www.keysight.com" for more information.</p>

China RoHS

W3301A

E5406B

U4201A



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