Agilent EEsof EDA

Complete Overview on Genesys (V8)

Agilent Technologies

GENESYS V8™

TECHNICAL OVERVIEW

EAGLEWARE

RF and Microwave Design Software

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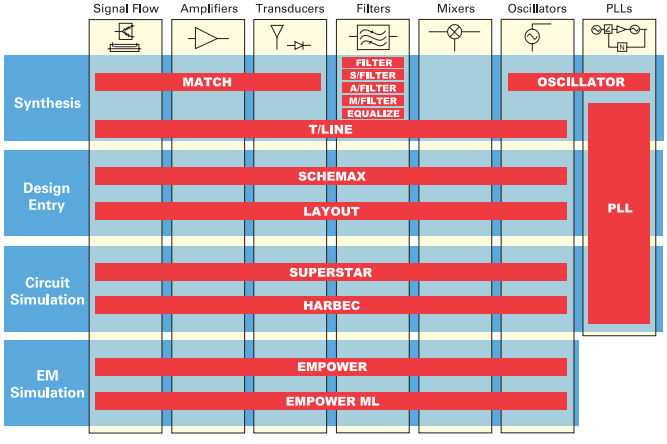
Eagleware is focused on delivering software that is fast, powerful, and accurate. Over the last 15 years, a broad range of synthesis, circuit analysis, and electromagnetic simulation products have developed the GENESYS suite into the most popular software for designing RF and microwave circuits.

This technical overview brochure will give you more insight on the capabilities of the GENESYS V8 software suite. It will discuss each module and how they all work together in the total RF design process.

Using a "keep it simple" philosophy, Eagleware has always focused on delivering practical solutions to everyday design problems faced by RF and microwave designers at affordable prices.

Thousands of seats of Eagleware software are used by engineers in thousands of locations in dozens of countries. Eagleware has grown 30% per year for the last five years, fueled in part by the steady stream of new products. But primarily, Eagleware has grown because of the success of its customers. 99% of surveyed customers would recommend Eagleware to a friend.



The GENESYS design flow is:

- Synthesize the design with synthesis modules: A/FILTER, FILTER, M/FILTER, EQUALIZE, T/LINE, MATCH, OSCILLATOR, and S/FILTER.
- Create a schematic with SCHEMAX.
- Simulate the circuit with SUPERSTAR and HARBEC.
- Layout the circuit with LAYOUT.
- Verify the circuit with EMPOWER.
- Produce your artwork.

As engineers squeeze more and more information into a given bandwidth, the design environment must develop to support sophisticated design. The GENESYS architecture was designed from the bottom up to support multiple simulators. Using object-oriented techniques, elements of the environment operate independently yet communicate through tight channels.

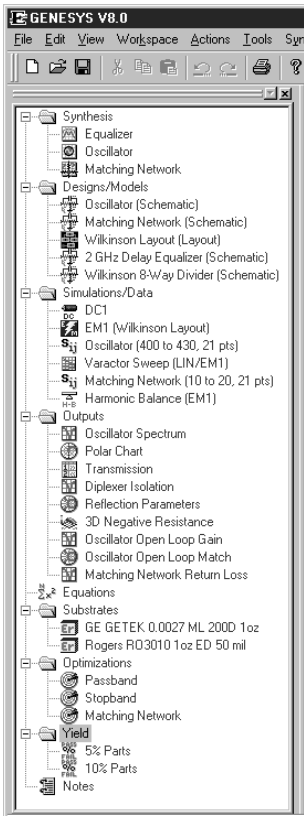
GENESYS integrates synthesis, schematic capture, circuit simulation, layout, and EM simulation into a single environment. It is a platform that enables various modules to work together as one program. Data is stored in a single file using compound storage.

Easy to Learn and Hard to Forget

GENESYS was developed in-house using one interface based on Microsoft Foundation Classes. By adopting Windows standards, Eagleware's software is intuitive, familiar to Windows users, easy to learn, and easy to remember.

Fast Design

Being fast is the leading principle at Eagleware. The design software starts quickly and runs fast. So fast that tuning circuit parameters is truly interactive. Not only is the software fast, so is the support. Call for help and you are connected immediately with an engineer. Engineers respond to your E-mail, web, and fax questions the same or next business day. Even delivery is fast: products ship the same or next business day.



Workspace Manager

RF and microwave designs can grow complex. Circuits may be described in several schematics (or netlists or both), several graphs may be needed to analyze different operating conditions, and multiple simulators may be needed to analyze the design. The Workspace Manager in GENESYS is designed to handle such sophisticated hierarchies. All workspace information is stored in a single compound file, making backup and transfer of simulation information easy.

Powerful Output Graphs and Tables

A powerful set of outputs is built into the GENESYS environment. Data can be displayed from circuit simulation, EM simulation, equation post-processing, or directly from data files. You can plot the data in five different ways:

- Rectangular Graphs (linear, log linear, log-log)
- Smith Chart (impedance, admittance, impedance/admittance)
- Polar Chart (one or two scales)
- Data Tables
- 3D Displays

No Limits

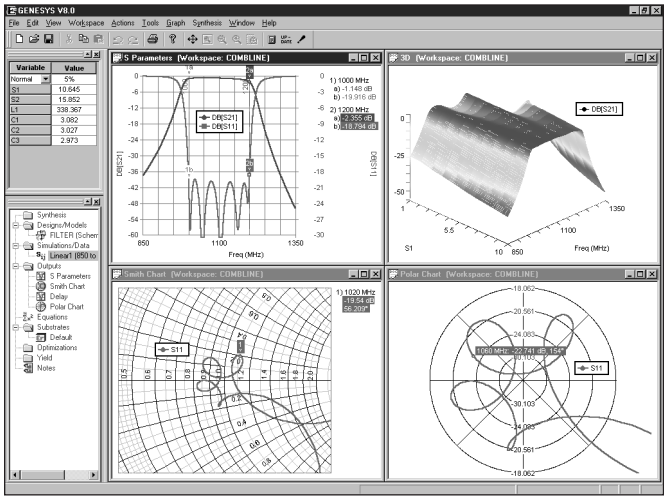
You can add an unlimited number of outputs. An unlimited number of traces can be added to the plots, just as an unlimited number of columns can be added to data tables.

Customize the Look

Graphs and charts are highly customizable, allowing you to see the data just as you want. Titles, arrows, text boxes, and even pictures can be placed on the graphs and charts. You can specify the number of graticule lines on rectangular graphs and zoom in on Smith charts. The graphs have a professional look that can be inserted directly into documentation and presentations. Traces can be customized by selecting colors, changing trace width and type, and selecting marker appearance and size.

Flexible Data Markers

To help you see exact values, markers can be placed on rectangular graphs, Smith charts, and Polar charts. Any number of markers can be placed on traces; only the number of points on the trace limits the number of markers. On rectangular plots, a scalar value of the marker is displayed near the data point

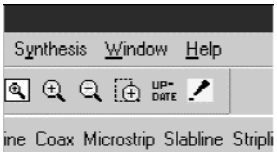


GENESYS V8 offers even more flexibility by introducing network analyzer style markers. Using built-in annotations, you can prepare presentation-quality graphs that can be easily integrated into other applications such as Word or PowerPoint.

while the frequency is shown at the top of the graph; on Smith and polar charts, the magnitude and angle (or the real and imaginary parts) and the frequency are displayed near the data point. Markers can be moved using the keyboard. They can be added or deleted at will.

Status Advisor

GENESYS features a dynamic status advisor. Any time unusual conditions are detected, the advisor toolbar button changes from green to yellow, red, or black. You click on the advisor button and a message is displayed that describes the condition and shows where it occurred. For example, if you have changed a layout and have not re-run an EMPOWER electromagnetic simulation, the indicator turns to yellow. Or, if you have used a variable in an equation that has not been defined, the button turns red and a message is displayed showing the variable name and the location of the variable.



Integration with Documentation and Office Automation Tools

Because GENESYS is based on Microsoft Foundation Classes, it is easy to transfer data to other applications. GENESYS uses standard Windows copy and paste. You can copy schematics, layouts, plots, equations, and notes to the clipboard and paste them into programs such as Word, Quark, Excel, or PowerPoint. This feature makes it easy to generate high-quality proposals, training, and presentation materials. The synthesis programs create bitmap files (.bmp) that can be imported into most desktop publishing programs.

Built-in Help and On-line Manuals

GENESYS includes a help system that incorporates hypertext. Hypertext links to additional help topics from the current help location. When you click on a sample program screen in the help system, help provides additional information about the section in question.

Export and Interfaces

GENESYS provides a wide range of interfaces that allow you to easily transfer information into and out of the software. From netlists to plots to raw data, you can move the data where you need it.

SPICE and Touchstone

SCHEMAX exports both Touchstone and SPICE files including IS-SPICE 4 from Intusoft, P-SPICE from OrCAD/Cadence, Berkeley SPICE 2, and Berkeley SPICE 3. SCHEMAX maintains your inputs for both GENESYS and SPICE models. For instance, a transistor can specify S-Parameters for use in GENESYS while specifying a SPICE model for SPICE translation.

GERBER 274 Files

LAYOUT exports Gerber files for manufacture of your printed circuit boards. Gerber files are written in 274 and 274-X formats. They use Eagleware's SmartScan optimized polygon filling technology to minimize the size of Gerber files. An intelligent etch factor routine accurately compensates for over and under etching of transmission lines and discontinuities. Gerber files can be loaded into most digital layout tools, allowing easy integration of RF circuits into digital boards. GENESYS V8 also features Gerber file importing.

AutoCAD DXF Files

SCHEMAX and LAYOUT write DXF files for AutoCAD from AutoDesk. For years, AutoCAD has been the standard for drawing programs. Any drawing programs that import DXF files can be used to import GENESYS drawings.

HPGL Plotter Files

Another standard for vector based drawings is Hewlett-Packard Graphic Language (HPGL) files. The LAYOUT module exports HPGL files.

PWB Milling Machines

Gerber files generated by LAYOUT are the preferred file format for most PWB milling machines. If necessary, DXF or HPGL files may be used with PWB and artwork devices.

S-Parameter Data Files

GENESYS programs read and write industry standard S-parameter data files. Most RF device manufacturers characterize their devices using S-parameter data and make this data available to their customers. GENESYS includes over 25,000 such data files and adding new ones is easy. Also, these files are easily created by typing data into any ASCII editor such as Notepad that is included with Windows. Z-, Y-, G-, and H-parameter files are supported in a similar fashion.

OSCILLATOR – OSCILLATOR SYNTHESIS

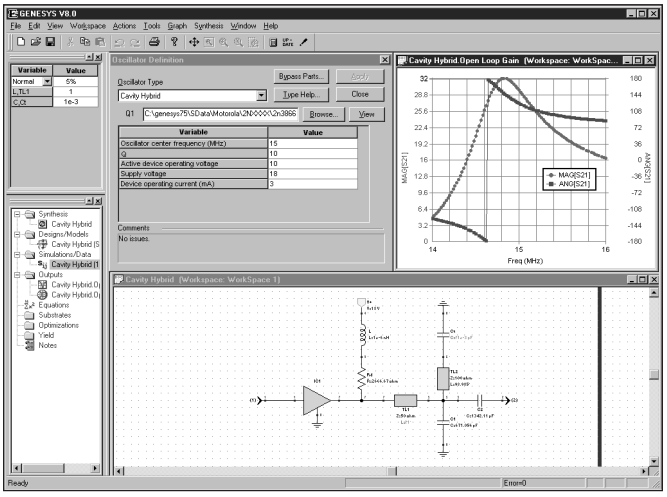
Synthesize L-C, transmission-line, cavity, quartz-crystal, and SAW oscillators with OSCILLATOR. Specify a frequency, a device, and a topology; and OSCILLATOR automatically selects component values to create an oscillator that meets your requirement. Two design methodologies are supported: negative-resistance and open-loop Bode analysis. Fixed and tunable oscillators are covered from sub-megahertz through microwave frequencies. Oscillator phase-noise is also analyzed.

How OSCILLATOR Works

When power is applied to the circuit, a low level oscillation begins and builds until the signal level is sufficient to drive the device into non-linear operation. During the build phase, the signal level is increasing but the circuit is linear and start-up is linear. OSCILLATOR uses linear analysis to establish the correct criteria for oscillation in the circuit.

Two analysis methods are used to establish oscillation criteria: an open-loop Bode analysis to satisfy Barkhousen's criteria and a one-port negative-resistance analysis. These analysis predict the gain and phase margins, loaded Q, loop match, and operating frequency.

If you need to analyze the transient characteristics of the circuit, you do not have to create another circuit description file. GENESYS exports a SPICE file. Alternatively, you can proceed with construction and use the prototype to characterize the output and harmonic levels and the starting performance.



GENESYS screen showing OSCILLATOR synthesis of a cavity hybrid VCO.

Noise Analysis

The OSCILLATOR noise model is based on the work of D.B. Leeson, with the effects of device flicker noise added. The model includes the effects of loaded Q, operating frequency, noise figure, flicker noise, power level, and varactor modulation noise. Varactor modulation noise is independent of the varactor Q and is generally the predominant parameter in the noise of broadband VCOs, particularly at offsets far from the carrier.

Leeson analysis is a sound mathematical relationship between the noise of an amplifier and the action of a resonator on the final oscillator noise performance. It predicts the noise of well-designed oscillators within a few decibels.

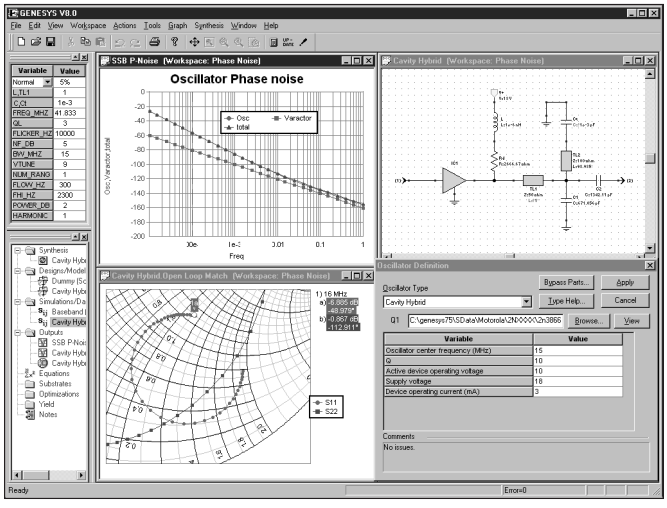
New in GENESYS V8! HARBEC* provides nonlinear noise modeling capability for oscillators. The oscillation spectrum is determined complete with carrier output power and sideband levels for dual sideband noise output.

* See supplemental literature for information on HARBEC.

Oscillator Topologies

The topologies cover a variety of application needs from high-stability and low noise fixed frequency circuits through broad-tuning VCOs. Bipolar, FET, and hybrid amplifier active devices are supported. Topologies include:

- **LC Colpitts** - general purpose JFET VCO up to 50 MHz
- **LC Clapp** - higher Q version of Colpitts
- **LC Bipolar** - shunt-C coupled resonator, higher output
- **LC Hybrid** - simple oscillator uses popular MMIC amps
- **UHF VCO** - wide tuning VCO to 2000 MHz and higher
- **UHF VCO + Transformer** - improved tuning and noise
- **CAVITY Bipolar** - low noise high-Q UHF/microwave
- **CAVITY Hybrid** - MMIC version of bipolar cavity
- **TEM Mode** - high Q design using coaxial resonators
- **SAW 2-Terminal** - low noise, high stability, fixed frequency
- **SAW 2-Port Hybrid** - pullable SAW oscillator
- **SAW MOSFET** - popular circuit for high volume
- **Crystal Pierce** - excellent general purpose fundamental
- **Crystal Colpitts** - popular fundamental mode oscillator
- **Crystal Driscoll** - very high stability and low-noise
- **Crystal Butler Overtone** - high stability to 200 MHz
- **Crystal Butler + Multiplier** - high stability to 1 GHz



GENESYS screen showing SSB phase noise analysis of the cavity hybrid VCO.

MATCH – MATCHING NETWORK SYNTHESIS

Use MATCH to synthesize L-C and distributed impedance matching networks. You specify the basic network topology, frequency range, and arbitrary load and source impedances. MATCH then automatically determines matching network configurations and optimal values for the components. The software can match devices with extreme impedances, multiple-stage amplifiers, and broadband problems.

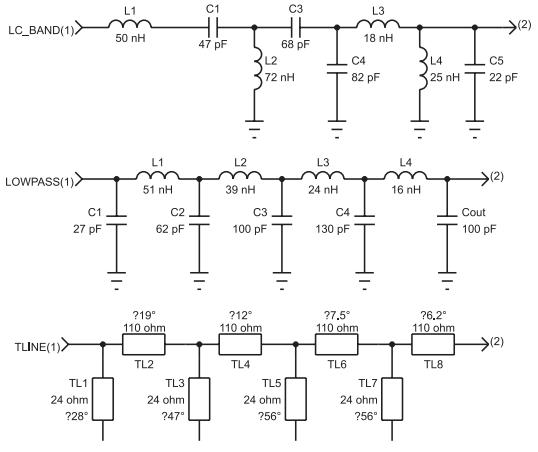
The Matching Problem

At one frequency, an arbitrary source impedance can be matched to an arbitrary load impedance with only two components and the closed-form equations to find the two component values are quite simple. MATCH instantly solves these problems. So why is matching network design often challenging? The primary threat is bandwidth. With increasing bandwidth, a match becomes increasingly difficult and, in fact, a solution is sometimes not possible even using a large number of ideal components. Factors that increase the difficulty are:

- Increasing bandwidth
- Termination reactance higher than termination resistance
- Termination impedances which change significantly with frequency
- Termination resistance not larger than network loss resistance
- Potential instability in active devices being matched

MATCH Algorithms

MATCH includes eight matching network algorithms. The two and three element networks (pi, tee, single/double stub, and TRL ¼ wave) are appropriate for simpler narrowband problems. Challenging problems require the more sophisticated algorithms (L-C bandpass, L-C pseudo lowpass, TRL pseudo lowpass and TRL stepped-impedance). Access to a variety of algorithms is important because no one algorithm is effective for all classes of matching problems. Broadband problems with ill-behaved loads are best handled using the L-C bandpass algorithm.



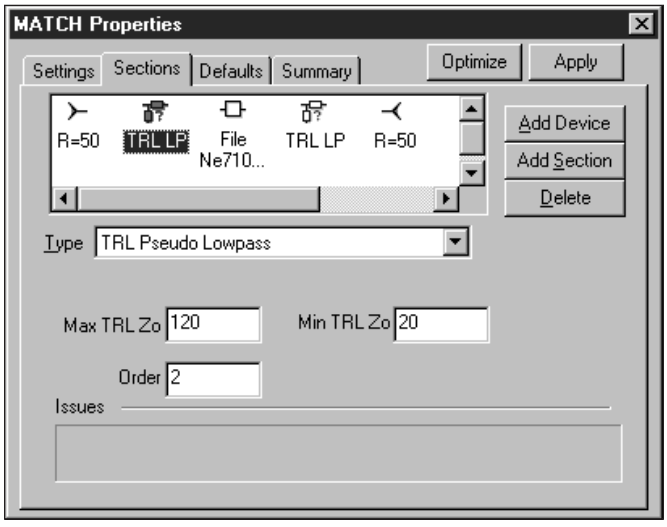
Three of the eight matching network topologies that are available in MATCH.

Arbitrary Terminations and Load Models

The source, load, or both may be resistive, a combination of Rs, Ls, and Cs, or arbitrary R-X data versus frequency. During synthesis, R-X data is automatically modeled as the optimum R-L-C network. Final adjustment of network element values is made using actual R-X data.

Multistage Amplifiers

A MATCH setup consists of a cascade of impedance matching sections and S-parameter data sections. A simple source-load problem uses only one impedance matching section. A two-stage amplifier uses two S-parameter data sections combined with three impedance matching sections for input, output, and inter-stage matching. Up to eleven of these objects may be used in a MATCH problem. Each of the networks may use any of the available algorithms.

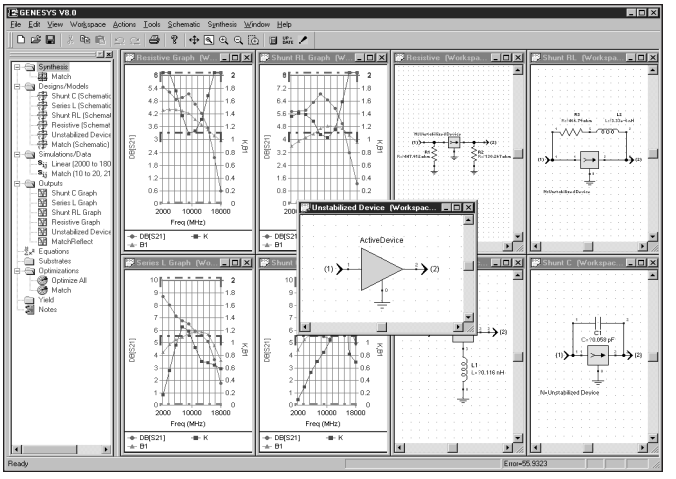


Setting up initial network parameters for a multistage amplifier.

Non-Unilateral Devices

MATCH corrects for non-unilateral devices (S12<>0) using full maximum power transfer equations. This capability, combined with iterative synthesis techniques, designs multistage amplifiers efficiently. All networks are directly synthesized using the maximum power transfer equations to determine optimal impedances. Then, the impedances seen through active devices are used as targets for automatic optimization.

MATCH – MATCHING NETWORK SYNTHESIS

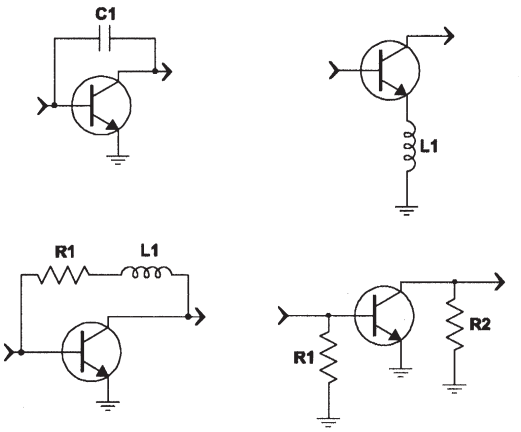


GENESYS automatically designs a variety of stabilization networks. The user then chooses the most suitable solution.

Unstable Devices

GENESYS includes four feedback techniques for automatically stabilizing active devices:

- Shunt Capacitive
- Series Inductive
- Shunt Inductive-Resistance
- Resistive



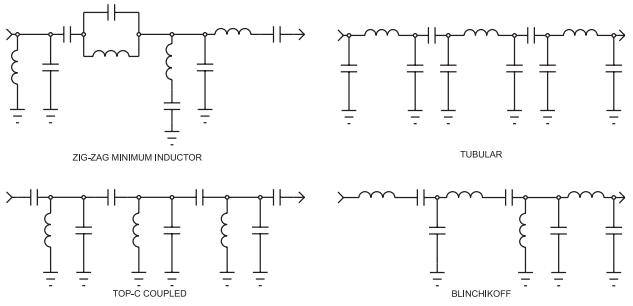
Devices are stabilized by applying any of the built-in templates to optimize feedback element(s) for unconditional stability conditions.

Use FILTER to design a variety of L-C (lumped element) filter topologies with virtually all published transfer function approximations, thus providing you with solutions for a wide range of applications requiring L-C filters.

Topologies

FILTER synthesizes the most complete set of filter topologies available in any program. No one filter topology is well suited for all applications. For example, the conventional "cookbook" bandpass filter works fine for some applications. However, at wide bandwidth, the symmetry of the amplitude and group delay responses is poor. At narrow bandwidths, symmetry is good but element values are unreasonable.

FILTER provides a number of alternative topologies, each of which has desirable characteristics for certain applications. Coupled resonator topologies are suitable when alternating series and shunt resonators are inconvenient. Filters that take advantage of certain technologies, such as coaxial resonators or quartz crystals, require resonators of one form. The symmetry preserving topology is useful when you need symmetry in the amplitude and group delay response. The zig-zag topology is an excellent choice when an elliptic response is required since it reduces the number of inductors required.



Four of the nineteen filter topologies that are available with FILTER.

Realizability and Parasitics

A common filter design problem is unreasonable element values. This issue is even more critical with elliptic transfer functions, controlled phase filters, and narrow bandwidth filters. The conventional bandpass filter uses alternating series and shunt resonators. As the bandwidth is decreased, shunt inductors become small and series inductors become large. With a bandwidth of 10%, the ratio of series to shunt inductor values exceeds 100 to 1 and the ratio worsens with narrower bandwidth.

FILTER helps you overcome this problem by offering a number of topologies which do not use alternating resonators. The top-C coupled, top-L coupled, shunt-C coupled, and tubular topologies have inductors with identical values! Furthermore, you may select the values. Since inductor realization is more critical than capacitor realization, allowing you to select the inductor value also helps control parasitic problems. Every node in the tubular structure has capacitance to ground which helps eliminate stray capacitance problems.

Transfer Approximations

FILTER includes a wide range of transfer approximations (filter shapes) such as Butterworth, Bessel, Chebyshev, transitional Gaussian to 6 dB, transitional Gaussian to 12 dB, linear phase with 0.5° error and 0.05° error, elliptic Cauer-Chebyshev, and elliptic Bessel. Singly terminated Butterworth and Chebyshev and a selected set of singly terminated Cauer-Chebyshev shapes are also supported. FILTER also reads g-values from ASCII files for other filter approximations which may be published in the future.

Symmetry

The conventional bandpass filter topology has less selectivity above the passband than below the passband. This also results in unsymmetrical group delay. Other filter topologies may have less selectivity below the passband. Eagleware has developed a symmetry-preserving transform, based on the work of Blinchikoff and Savetman, that results in bandpass filters with excellent amplitude and group delay symmetry. This is often important in IF filters and filters for data communications systems.

Singly Equalized

The Eagleware proprietary singly equalized transfer approximation is also included in this module. This approximation provides selectivity far superior to Bessel (nearly Butterworth) and is delay equalized to maximum flatness with only one all-pass network. This minimizes filter complexity when flat group delay is needed.

Zig-Zag

The zig-zag, or minimum inductor, elliptic bandpass filter saves one inductor each time the filter order is increased by two. The topology of a zig-zag is shown on the upper left in the figure of sample FILTER topologies. No filter with fewer or an equal number of inductors offers better selectivity than the zig-zag. It would be more common except that computing element values is difficult. With FILTER, you can design this filter with ease. It even has reasonable element values for moderate to wide bandwidth.

M/FILTER – DISTRIBUTED MICROWAVE FILTER SYNTHESIS

The M/FILTER program is the best way to synthesize lowpass, bandpass, highpass, and bandstop (notch) filters with stepped-impedance, end-coupled, edge-coupled, combline, interdigital, and stub topologies. M/FILTER supports microstrip, stripline, coax, slabline, and electrical processes. It displays a physical view that updates as the user modifies input parameters, thus providing direct feedback concerning the size and realization issues. Using LAYOUT, artwork can be printed or exported as a DXF, Gerber, AutoCAD, and HPGL files.

Start-to-Art

Using the GENESYS modules, M/FILTER, LAYOUT, and SUPERSTAR allows you to design distributed filters from Start-to-Art. You start with the initial synthesis with updating physical view, to fast response simulation with tuning and optimization, to the generation of Gerber, AutoCAD DXF, and HPGL files for direct use by board manufacturers and PWB milling machines. The entire process from design concept through PWB measurements is literally hours, not days or weeks!

Accuracy

M/FILTER accuracy is enhanced through 1) absorption of structure discontinuities by adjacent line length compensation, 2) simulator optimization and tuning to correct synthesis assumptions, and 3) verification by independent models in GENESYS. All parasitic and loss effects except radiation and non-direct coupling are considered during the design. These other effects can be handled by our electromagnetic simulator, EMPOWER. See the EMPOWER section for more details.

Comparison of Design Alternatives

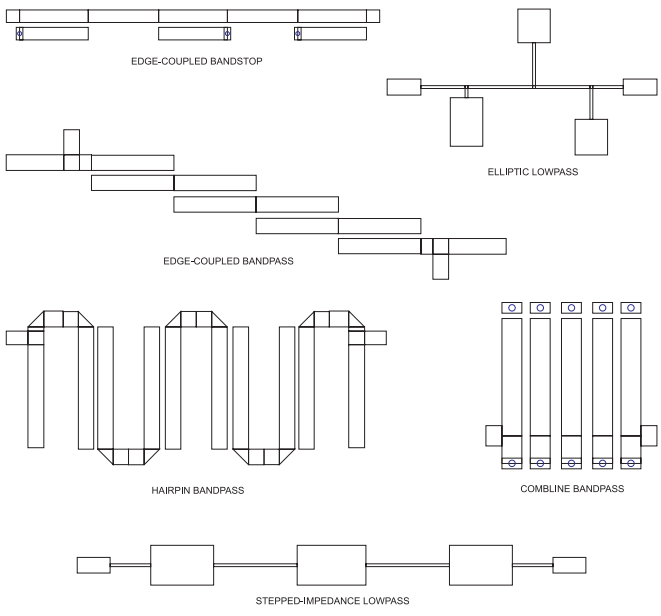
Access to alternative filter topologies is even more important for distributed than with L-C filters because realizable line impedance ratios are small and because of the stopband limitations of distributed filters. These issues are also more critical for bandpass than lowpass or highpass filters, thus the greater variety of bandpass types in both M/FILTER and the L-C synthesis program FILTER. The integrated design environment of M/FILTER, SUPERSTAR, and LAYOUT is a powerful tool for quickly evaluating alternative designs to find the approach best suited for each of your applications.

Processes

All filters are designed for microstrip, stripline, coax, slabline, and electrical processes except when naturally excluded, such as combline in coax. The electrical process is used for designing filters for any process for which the user has model knowledge. Microstrip is normally used for the convenience and economy of printed construction. Although less convenient than microstrip, particularly when lumped or active components are required, stripline can eliminate the microstrip radiation problem. Microstrip and stripline substrates are typically relatively thin and the resulting unloaded Q is lower than larger slabline and coaxial processes. Therefore, slabline and coaxial are more suitable for low loss and narrowband applications. Filters using transmission lines with electrical parameters are also designed. This allows you to design filters using transmission line processes unique to your company's experience.

PWB Milling Machine Interface

By using LAYOUT with the M/FILTER program, you can create printed filter prototypes in hours using PWB milling machines. In fact, you can create PWBs for any of the circuits designed with GENESYS.



Six of the thirteen topologies that are available in the M/FILTER program.

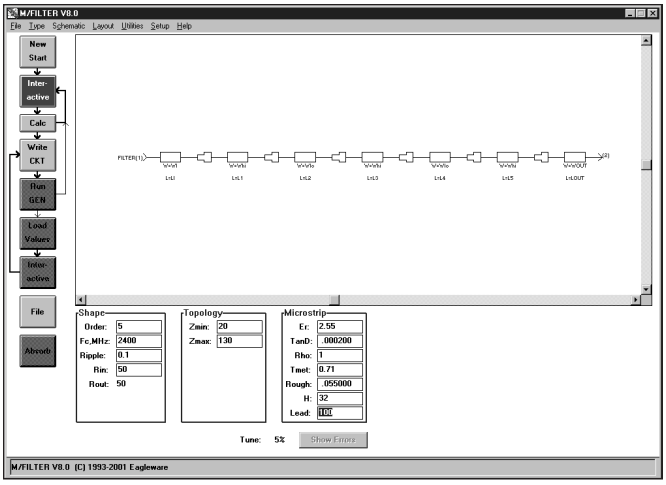
Available Synthesis Topologies in M/FILTER

- STUB LOWPASS - the stub length can be selected so that the response includes transmission zeros
- STEPPED-Z LOWPASS - excellent coaxial filter
- ELLIPTIC LOWPASS - provides a steep transition region; preferred when selectivity is of prime importance
- STUB HIGHPASS - the highpass uses chip capacitors. At microwave frequencies, printed interdigital capacitors can be substituted.
- END-COUPLED BANDPASS - for narrow bandwidth and high microwave frequencies
- EDGE-COUPLED BANDPASS - for lower frequencies and wider bandwidths than end-coupled
- HAIRPIN BANDPASS - for UHF frequencies
- COMBLINE BANDPASS - for compact filters (uses lumped loading capacitors)
- INTERDIGITAL BANDPASS - for compact filters that do not use loading capacitors (narrow and wide bandwidths)

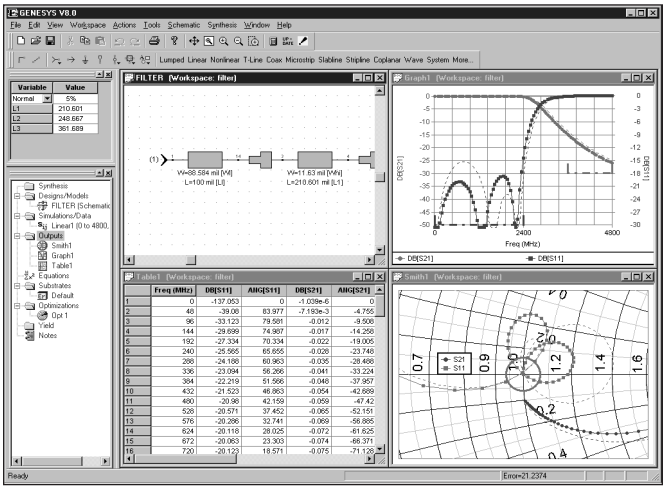
- ELLIPTIC BANDPASS - for elliptic bandpass transfer function; best for moderate to wide bandwidth. It tends to occupy a large area.
- STEPPED-Z BANDPASS - for coaxial bandpass filters
- STUB BANDSTOP - for wide bandwidth bandstop filters (at narrower bandwidths the line impedances become high)
- EDGE-COUPLED BANDSTOP - for narrow stopbands (at wider bandwidths the spacings become too close)

Verification

During the development of M/FILTER, Eagleware built and tested numerous planar and machined filters. Some of the planar filters were etched and some were constructed using the T-Tech PWB milling machine. We also have conducted electromagnetic analysis on many of these filters. When you use M/FILTER, you will definitely see how much easier, faster, and more efficiently you will design filters. The agreement between simulated and actual results depends on many factors. One of the more important factors is substrate thickness. When this dimension becomes significant with respect to a wavelength, evanescent and other modes develop. Not only is simulation less accurate, the actual filter performance is degraded. Narrowband combline and hairpin filters are most susceptible to this problem. Interdigital, end-coupled, and stepped-Z filters are nearly impervious to these effects. Edge-coupled filter simulation is also very accurate when the actual filter is mounted in a housing no wider than necessary. Thinner substrates are the simplest solution to many of these problems. If low loss requirements dictate using thicker substrates, proper topology selection and electromagnetic analysis using EMPOWER are helpful. These issues are discussed further in HF Filter Design and Computer Simulation textbook that is provided with the M/FILTER program.



Synthesizing a Stepped-z lowpass filter in M/FILTER.



M/FILTER design being tuned and optimized in GENESYS.

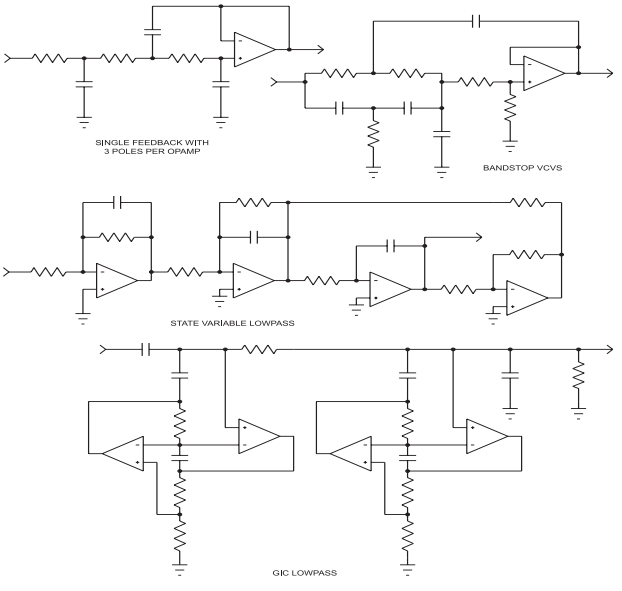
A/FILTER – ACTIVE R-C FILTER SYNTHESIS

The A/FILTER module synthesizes active filters with capacitors, resistors, and operational amplifiers. Both traditional voltage gain filters and resistively terminated filters are designed.

Topologies

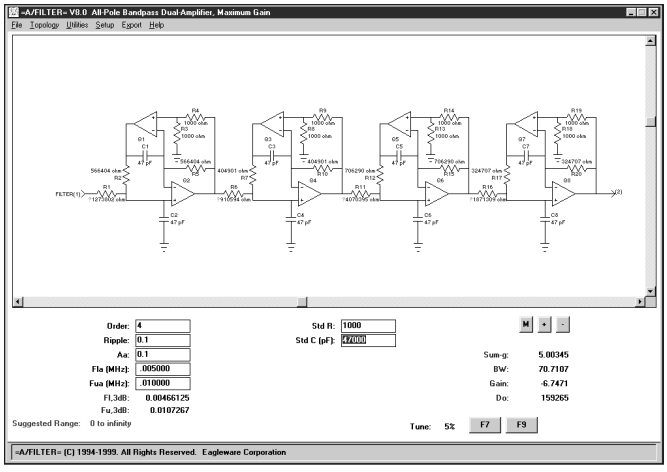
A/FILTER designs a wide variety of structures. Most are available for lowpass, highpass, bandpass, and bandstop. Both all-pole and elliptic transfer functions are supported.

- **GIC MINIMUM INDUCTOR** (All-pole/Elliptic: LP/HP) Good insensitivity and equal valued caps, but 6 dB loss
- **GIC MINIMUM CAPACITOR** (All-pole/Elliptic: LP/HP) Similar to GIC ML. Only one op-amp for 3 poles
- **SINGLE FEEDBACK** (All-pole: LP/HP) Selectable gain and few parts but cap values sometimes unreasonable. High sensitivity.
- **MULTIPLE FEEDBACK** (All-pole: LP/HP/BP) Similar to single feedback. Saves parts when gain is required.
- **LOW SENSITIVITY** (All-pole: LP/HP/BP) Good insensitivity and equal capacitors but requires two op-amps per section
- **VCVS** (All-pole/Elliptic: LP/HP/BP/BS) Equal caps and independent Q and frequency tuning but has more parts
- **STATE VARIABLE** (All-pole/Elliptic: LP/HP/BP/BS) Excellent insensitivity, equal caps, and excellent tuning, lots of parts
- **DUAL AMPLIFIER** (All-pole: BP) Variable gain but high sensitivity
- **TOP-C** (All-pole: BP) Provides power gain and has equal caps but requires more resistors.
- **TOP-L** (All-pole: BP) Similar to Top-C but fewer resistors



Four of the ten topologies that are available in the A/FILTER program.

You select the topology that best fits each application, whether that need is best economy, best insensitivity, specific gain, or easiest production tuning.



Synthesizing a Maximum Gain Dual Amplifier Bandpass Filter in A/FILTER.

Transfer Approximations

These topologies are designed with published all-pole and elliptic transfer approximations: Butterworth, Chebyshev, Bessel, and user-defined.

Gain and Input/Output Buffering

You may specify input and output buffers if desired. Buffers are used to 1) isolate the source or load, 2) allow a voltage gain filter to be added into a 50 ohm system, 3) add gain to the filter without loading op-amps in the filtering sections. If the Gain-Bandwidth product of the op-amps is adequate, then gain can be added to most filter section types. This allows the gain to be distributed among all op-amps in the filter.

Practical Components

Filter design with A/FILTER handles non-ideal parts. You specify operational amplifier parameters, including input and output resistance, open loop gain, and unity gain crossover frequency. In addition, during SUPERSTAR simulation, the operational amplifier model can be replaced with measured S-parameter data provided by device manufacturers. This improves simulation accuracy, particularly at higher frequencies.

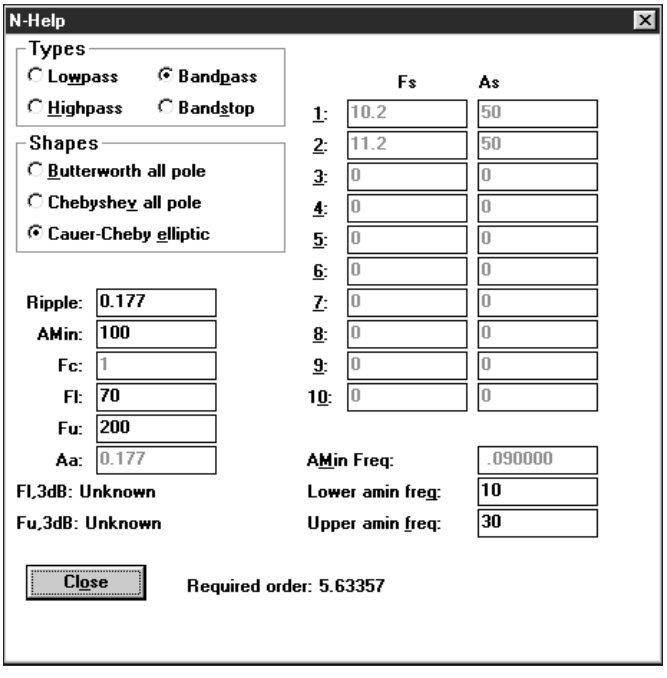
Economy

A/FILTER incorporates unique topologies for improved economy. A 3rd order filter with gain and output isolation is available with only 1 op-amp, 4 resistors, and 3 capacitors! Traditional second-order sections require 2 op-amps and an additional resistor. You can quickly examine various topologies to find the best tradeoff between performance and economy.

Two filter utilities are included with FILTER, M/FILTER, and A/FILTER. N-Help helps you determine the optimal order of a filter and Noise Bandwidth, lets you see the effective noise bandwidth of your filter.

N-Help

The N-Help routines in FILTER, A/FILTER, and M/FILTER estimate the filter order needed to satisfy your selectivity requirements. These routines handle Butterworth, Chebyshev, and elliptic Cauer-Chebyshev transfer approximations. You enter the passband requirements and up to ten stopband attenuation requirements. N-Help then displays the required filter order. The next higher integer order is then used to design the filter. The effects of losses or response variations among



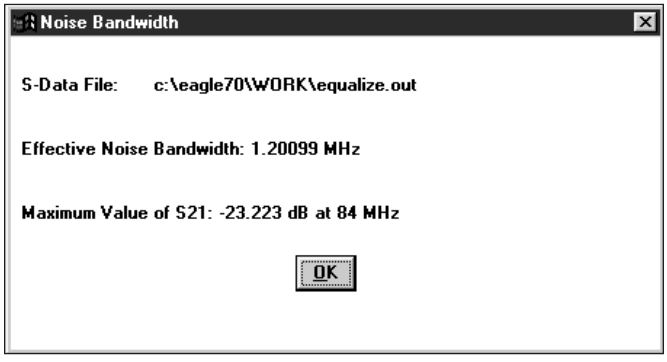
Determining the order of a Cauer-Chebyshev bandpass filter with the desired specifications using N-Help.

different topologies, are accurately predicted by the SUPERSTAR simulator and may identify the need for a higher order filter.

Noise Bandwidth

FILTER and A/FILTER import S-parameter data files to determine the effective noise bandwidth. S-parameter data files are written by GENESYS for any filter that has been analyzed. Using an S-parameter data file allows you to find the effective noise bandwidth whether the filter is ideal or real. The response may include losses and parasitics. The noise bandwidth may even be found for measured filter responses.

This capability offers the advantage of being unrestricted to



theoretical "ideal" response types. Even the effects of finite component Q or approximate bandpass transforms are taken into account.

EQUALIZE – GROUP DELAY EQUALIZATION SYNTHESIS

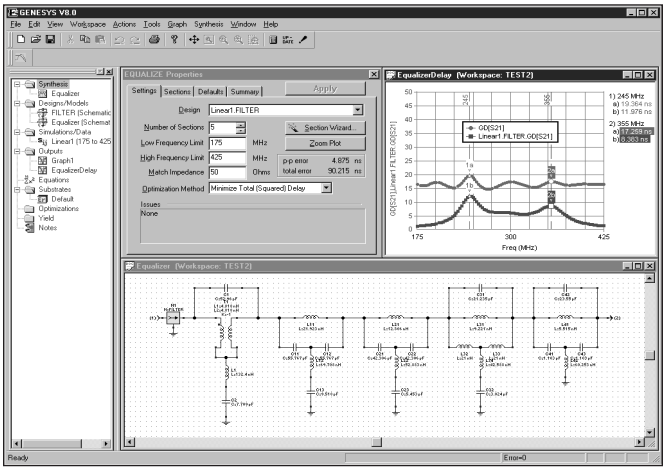
Use EQUALIZE to synthesize all-pass networks that compensate for group delay distortion. Group delay is the rate of change of phase with frequency. When complex signals are transmitted through systems where the group delay versus frequency is not constant, distortion results. The need for flat group delay increases with modern efficient modulation schemes.

All passive ladder networks are minimum phase and the amplitude and group delay characteristics are inseparably related; flay delay and selectivity are not achieved simultaneously.

The group delay flatness of a filter may be improved by cascading the filter with one or more non-ladder all-pass networks. All-pass networks perturb the amplitude response very little and may be used to compensate the delay. The difficulty lies in determining the required number of all-pass networks and finding the parameters for each network to best compensate the group delay. EQUALIZE completely automates this process.

How EQUALIZE Works

Any two port network to be group delay equalized is first created in GENESYS as a netlist, schematic, or layout with EM simulation data. EQUALIZE then applies a sophisticated algorithm to determine the optimum number of all-pass sections which minimize the user-selectable error function. With full integration in the GENESYS simulation environment, EQUALIZE gives the user complete control over response plots, custom schematics, and optimization goals.



Five section group delay equalization of a 300 MHz bandpass filter.

Non-Ideal Filters

Because EQUALIZE determines the group delay to equalize by reading S-parameter data, it is not necessary that the filter being equalized is ideal. Loss and parasitics included in the analysis are considered. In fact, measured S-parameter data of a filter may be substituted for data generated by GENESYS.

2nd Order All-Pass Sections

EQUALIZE designs 9 types of 2nd order all-pass sections including discrete inductor, coupled inductor, operational amplifier forms, and all-pass sections with Qs less than 1 which are often required to equalize lowpass filters.

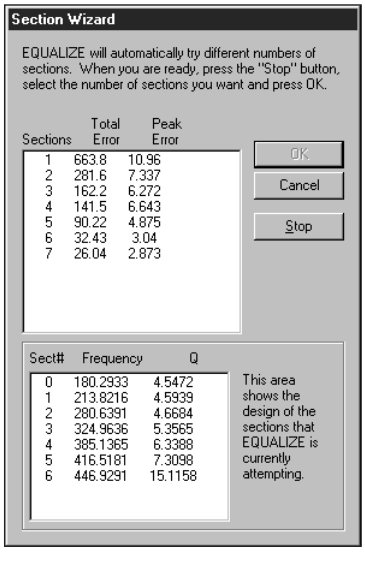
Partial Passband Equalization

Because the user specifies the frequency range to equalize, you can equalize only a portion of the passband. This also allows equalization of highpass filters up to a user specified frequency limit. It is even possible to equalize into the transition region.

Other Phase and Delay Controls

Selectivity is uncompromised when group delay is equalized using all-pass networks and the number of networks can be increased until the necessary group delay flatness is achieved. Unfortunately, manufacturing and tuning is difficult when several all-pass networks are required.

The GENESYS suite of tools offers alternative methods of controlling the phase and group-delay characteristics for filters. In addition to the popular Bessel transfer approximation, the transitional Gaussian, equi-ripple linear phase, and elliptic Bessel transfer approximations are supported. Also, two Eagleware proprietary techniques are available for phase sensitive applications; the singly-equalized transfer approximation and the symmetry-preserving transform. No other software package provides this range of solutions for phase-sensitive applications.



New Section Wizard automatically finds minimum all-pass section solution.

Section Wizard

GENESYS V8 introduces the EQUALIZE Section Wizard for automatic determination of the optimum number of all-pass sections. Often, engineers must iteratively try a different number of sections to determine the flattest group delay possible in a particular configuration. The Section Wizard uses iterative algorithms coupled with section optimization to quickly determine the best delay possible with the minimum number of sections.

T/LINE – TRANSMISSION LINE SYNTHESIS

The T/LINE program computes transmission line performance parameters from physical descriptions (analysis) or determines dimensions from the required line impedance (synthesis).

Structures

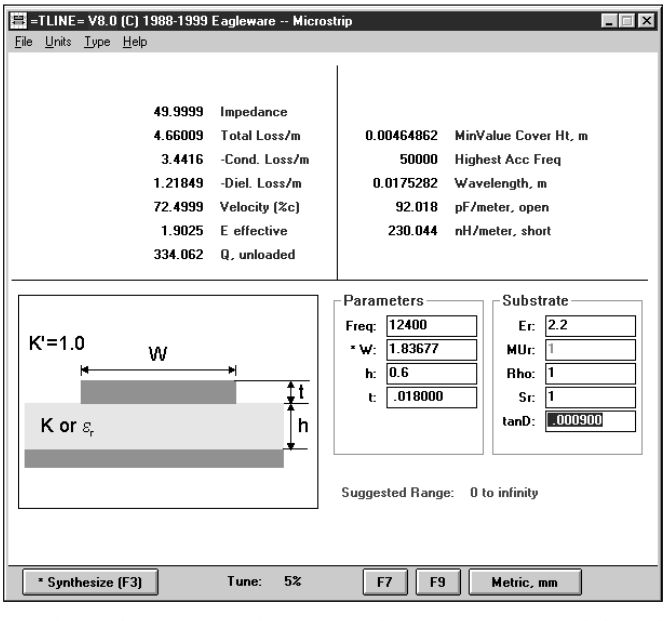
T/LINE Topologies

RECTANGULAR	CIRCULAR
Microstrip	Coaxial
Suspended Microstrip	Eccentric Coaxial
Inverted Microstrip	Partially Filled Coaxial
Stripline	Round Edge Stripline
Coaxial Stripline	Twin Wire
Coplanar	Wire Over Ground
Grounded Coplanar	Round Microstrip
Square Coaxial	Trough Line
Equal Gap Rectangular	Slabline
	Square Slabline

COUPLED
Microstrip
Stripline
Broadside Horizontal Stripline
Broadside Vertical Stripline
Slabline

Graphic Display

The line structure is graphically displayed. This makes it easier for you to identify requested parameters.



Synthesis of a microstrip line given substrate properties and desired impedance.

T/LINE Models And References

Exact or nearly exact solutions are known for the impedance of many of the structures such as coaxial and stripline. Only approximate solutions are known for other structures such as microstrip and slabline. In each case, the references are given from which the models were derived. The range of parameters, such as strip width or dielectric constant, for which the models are valid are also given.

Microstrip Model Derivations

The most suitable algorithms for fast circuit simulation are closed form equations. Much of the last decade's work was developing closed form equations to fit the older and accurate, but slower, electromagnetic simulation results.

No single reference gives all the equations required to compute parameters when loss, metalization thickness, and roughness are considered. The resulting equations are sufficiently accurate to strain verification efforts. The primary reference for the microstrip models in T/LINE is the work of Jansen and Kirschning. Dispersion is considered and the results are generally within 1% over a wide range of parameters.

Output Data

T/LINE provides a rich set of output parameter data including impedance, total loss, separate losses for conductors and the dielectric, the effective dielectric constant, the propagation velocity, and the unloaded Q of lines used as resonators. It also determines the physical length for a one-wavelength line, the recommended cover clearance, the highest frequency for accurate results, and the effective line capacitance and inductance. For coupled lines, T/LINE calculates the quarter-wave coupling and coupler impedance.

Synthesis and Analysis

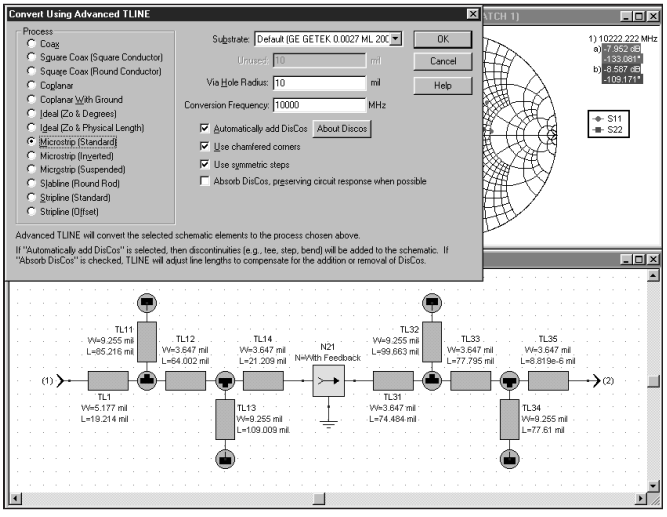
T/LINE supports both analysis and synthesis. Analysis computes electrical parameters from physical dimensions. For synthesis, T/LINE iterates line width or diameter to realize the user specified impedance. For coupled lines, the line width and spacing are adjusted to realize the even and odd mode impedances or the desired coupling and impedance. T/LINE synthesis iterates analysis routines so that both obtain identically accurate results.

Exciting New Features in T/LINE V8

- Advanced mode integration within the GENESYS simulation environment (Advanced T/LINE)
- Automatic conversion of electrical schematics to physical (e.g. microstrip, stripline, coplanar waveguide)
- Automatic conversion of physical schematics to electrical
- Automatic insertion of DisCos™ elements (Eagleware's new discontinuity models)

T/LINE – TRANSMISSION LINE SYNTHESIS

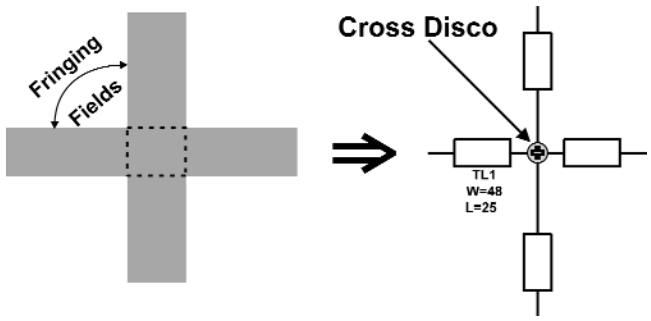
Entire schematics (or portions of schematics) are converted between electrical and physical models by using the new Convert function from the schematic menu.



Advanced T/LINE setup dialog and matching circuit converted to microstrip.

The Convert option allows any schematic using any of the supported processes to be converted to any other process, including electrical descriptions. This is a powerful tool for engineers involved in the design of distributed circuits, as it allows quick and easy translation between processes and different substrate materials for response comparison.

GENESYS V8 introduces DisCos, the automatic discontinuity model. Discontinuities exist in any distributed circuit where a discontinuous metal pattern exists, as in a bend or step in width. These discontinuities are important because they nearly always perturb the desired response in some way. However, they are purely a modeling issue since they do not have physical footprints in the layout. Engineers often spend lots of time inserting these models in schematics simply out of necessity for accurate simulations. Advanced T/LINE automatically places these models, and automatically "absorbs" them into the adjacent lines to preserve the response.



Physical and schematic representation of two crossed microstrip lines. Fringing fields exist at all four corners of the intersection, and are only modeled when using discontinuity models. Advanced T/LINE automatically inserts these models as needed.

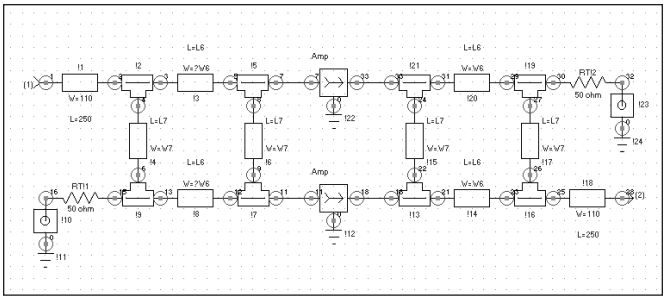
Generally, two overlapping lines are assumed to join at the exact center of the intersection. However, the cross discontinuity model uses the reference planes shown with dashed lines in the cross figure. The cross models the metal portion indicated by the dashed square. Since this metal is modeled by the cross, it should not be included in the length of the lines connected to the cross model. This reference plane shift makes it necessary to "absorb" discontinuities into connected lines to preserve the desired response. Advanced T/LINE automatically places DisCos, fills in the required parameters based on the surrounding line connections, and absorbs the DisCos by adjusting connected line parameters.

SCHEMAX – SCHEMATIC CAPTURE

The SCHEMAX schematic capture module helps you quickly and easily create circuit descriptions. These descriptions are used to drive the simulators and layout. Once entered, you can print high quality output or copy the image to office automation tools for documentation.

How SCHEMAX Works

GENESYS includes a built-in text editor for creating and modifying a netlist to describe your circuits. With SCHEMAX, instead of typing a netlist, you simply draw a schematic to describe a circuit. Components are selected from the toolbar windows; several component groups may be displayed simultaneously. You lay down parts by clicking on a component icon, dragging the part to the desired place, and releasing the button. Double click on the component to set its parameter. Parts are arranged, rotated as desired, then interconnected using lines. When the inputs and outputs are added, the circuit is ready to simulate or layout.



Schematic of a Balanced Amplifier.

Fully Integrated

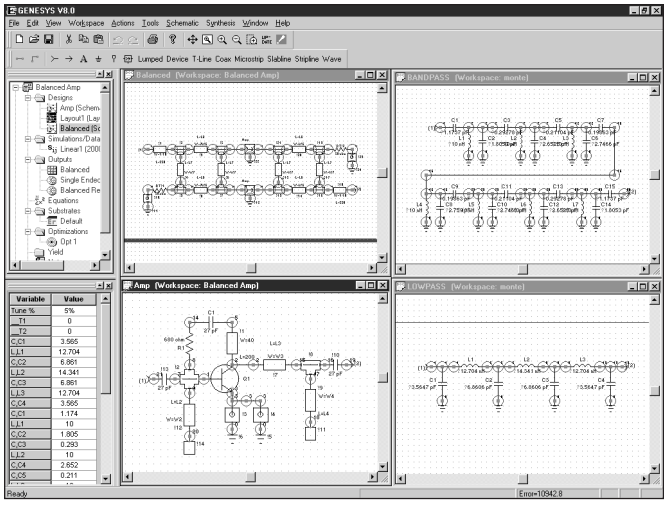
You may have a schematic program so why use SCHEMAX? The reason is speed and convenience. SUPERSTAR, SCHEMAX, and LAYOUT are actually one program. With this powerful combination, you can instantly compute and display the response, tune and optimize values, and produce your artwork. There is no need to transfer files from one program to another.

Editing

SCHEMAX includes a rich feature set for convenient schematic creation and editing such as node snapping, rotate, mirror, block controls, page set-up, and mouse set-up. Several sizing buttons allow you to quickly adjust the view. Real-time panning lets you view the schematic as you move around a zoomed-in design.

Hierarchical Design

You can define and simulate networks with any number of ports. Full hierarchy is supported meaning that you can split your design into logical blocks. Each block has its own schematic and a master schematic is used to interconnect the blocks. Networks can be simulated and graphed together or separately. Also, you can optimize multiple networks simultaneously. These networks may share common components or may be independent.



You can display multiple schematics within the same window.

Links to SPICE Simulators

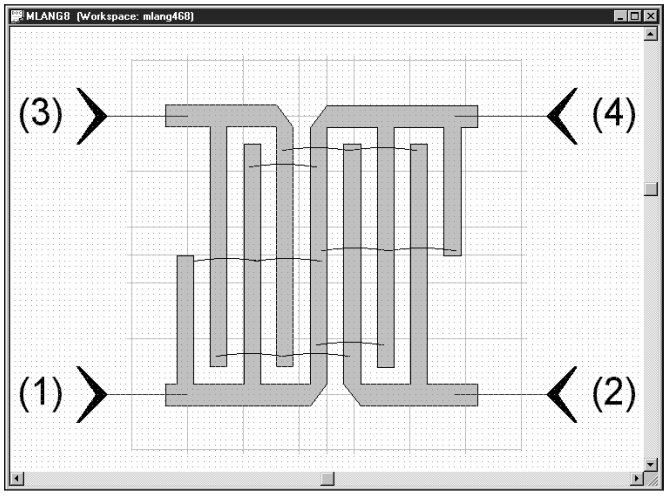
SCHEMAX writes files which are ready to run in IS-SPICE 4 from Intusoft, P-SPICE from OrCAD/Cadence, Berkeley SPICE 2, and Berkeley SPICE 3. After completing the interactive design in GENESYS, you can run a SPICE analysis without creating a new netlist.

Interface with Other Drawing Programs

Schematics in SCHEMAX can be copied onto the Windows clipboard and pasted into other applications. As with all GENESYS modules, it also prints using standard Windows drivers.

Symbol Editor

Create your own schematic symbols in GENESYS V8 with the new symbol editor. Add unique symbols, or symbols for unsupported components such as digital ICs for complete project documentation. Any existing symbol is easily loaded and modified. Lines, polygons, circles, and arcs are supported.



New editor makes it easy to create custom schematic symbols.

LAYOUT – RF/MICROWAVE PHYSICAL DESIGN

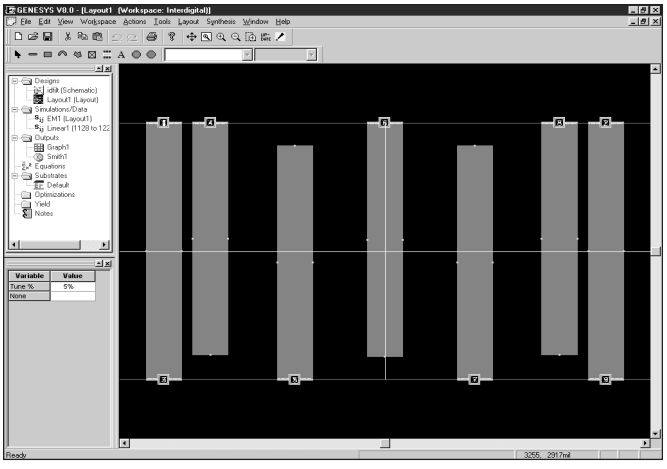
Producing a circuit board or hybrid ready for fabrication is quick and easy when you use our LAYOUT program. It handles the unique needs of RF and microwave circuits.

How LAYOUT Works

You can automatically create the layout from the schematic or manually create it through interactive design. Either way, complete layouts are created on up to 128 layers including metalization, silk screen, solder mask, solder paste, and assembly layers.

In schematic-driven layout, each component has a corresponding footprint. The footprints are placed into the layout window, connected by rubber-band lines. Components are arranged, metal traces are placed to interconnect lumped components, and targets are added to complete the layout.

When designed manually, the layout is created using lines, arcs, and polygons. Predefined layout footprints can be inserted as well as free-form text.



The layout of an interdigital filter. You can export a DXF or Gerber file that is sent to the PCB/PWB manufacturer or you can use with your own PWB milling machine.

Select an output format, either Gerber or DXF, generate a file, and send it to the PCB/PWB manufacturer for fabrication. You can also make fast prototypes with the PWB milling machine of your choice.

IPC SM-782 Library

LAYOUT includes a large library of footprints (land patterns) for active and passive components based on IPC SM-782. This library includes footprints for chip resistors, capacitors, and inductors plus SOT, SOIC, SSOIC, SOPIC, SOJ, CFP and DIP transistors, ICs, and other devices.

Also included are libraries derived from published manufacturer's data such as RF/microwave transistor footprints, samples of other objects such as wagon-wheel grounds, and footprints for a variety of leaded devices.

Footprint Editor

The built-in LAYOUT editor lets you modify existing footprints and create new footprints. You may use the footprint editor to simply add a few objects or to develop a complete library of components.

Association List

When launched, LAYOUT selects a footprint to associate with each object in the schematic. The user controls the association list. Also, components in the layout are easily changed to any library footprint.

Layers

LAYOUT is configurable with up to 128 layers including metalization, silk screen, solder mask, solder paste, substrate, and assembly layers. Any layers associated with the backside can be mirrored. Layer management handles blind and buried vias, multi-layer footprints, dielectric cutouts for power and other devices, and multiple ground planes.

Special RF and Microwave Features

In addition to features that are required in any layout program, LAYOUT has features that specifically address the needs of RF and microwave designers. For example, you can design circuits with multiple ground plane layers, arbitrary metal shapes, automatically dimensioned transmission lines and discontinuities, and pouring for both coplanar and conventional ground planes.

Gerber 274X and Excellon Drill Lists

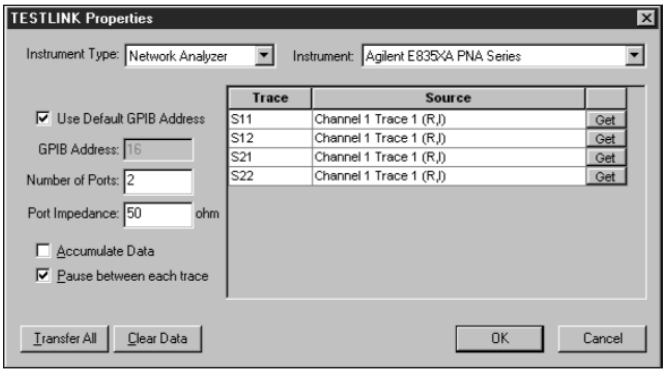
LAYOUT creates Gerber 274X and D files and an Excellon drill list for use by PWB manufacturers. These files are the standard for printed circuit board manufacturing. Files are optimized using the LAYOUT program's SmartScan technology which minimizes the size of the Gerber file, critical for high-precision microwave boards. LAYOUT also exports AutoCAD DXF files and HPGL files.

The Gerber files are ready for use with PWB milling machines. Eagleware uses the Quick Circuit 5000 machine from T-Tech, Inc.

LAYOUT also reads standard 274X Gerber files, allowing layouts to be imported for modification and EMPOWER simulation.

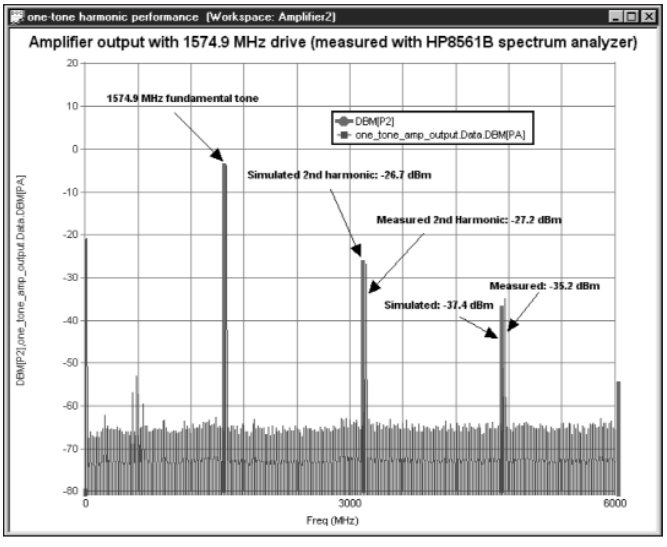
TEST LINK – AUTOMATIC DATA GATHERING

Engineers using test equipment know how difficult it can be to get measured data into PCs. Measurements end up as hard copy clipped into folders and if a plot is needed for documentation, it's normally scanned in. Measurement data for use in CAD software or spreadsheets is often typed in. Newly introduced in version 8.0, TEST LINK acquires data files at the click of a button. Simply hook up a Network Analyzer, Spectrum Analyzer or Oscilloscope to a PC using a GPIB card or RS-232 port, and have instant access to trace data.



The TEST LINK setup dialog.

TEST LINK supports many GPIB-capable instruments, and allows multiple, real-time data connections to bench measurements. This is a powerful tool for comparing measured and simulated waveforms, or for completely new characterization of devices and networks.



Measured and simulated single tone excitation of a 1.5 GHz GPS LNA. The measurement data was acquired with TEST LINK.

Instrument Interface Software

To use TEST LINK, configure the instrument's controls for your desired measurement. Then insert a TEST LINK icon on the design manager tree and transfer the data into the GENESYS workspace. There, you can compare simulated versus measured or use the data as models in larger simulations.

Hardware Requirements

Minimum System Requirement:
Same as GENESYS plus:

GPIB Card:
National Instruments: PC-IIA, PC-AT, PC-PCMCIA, PC-USB
Agilent/Hewlett-Packard: HP82335, HP82340, HP82341, HP82350
ComputerBoards, Inc.:ISA-GPIB, ISA-GPIB/LC, ISA-GPIB-PC2A, PCI-GPIB, PCM-GPIB

Note: TEST LINK can also use RS-232 port if the instrument supports it.

Instruments Supported

Network Analyzers:
Agilent: E835XA PNA Series
Anritsu Wiltron: 360, 371xx/372xx/373xx, MS462XX
Hewlett-Packard: HP8510, HP8711-14B/C, HP8751/52/53, HP8700 Series, HP4195, HP4396A Network/Spectrum Analyzer, HP3561A, HP35660 Dynamic Signal Analyzer, HP4291A Impedance Analyzer, HP8757 Scalar Analyzer
Marconi Instruments/IFR: 6210 Reflection Analyzer, 6200, 6800 Series Microwave Test Sets
Rohde & Schwartz: ZVR/ZVC/ZVM Series

Spectrum Analyzers:
Agilent/HP: E44XXA/B, ESA-E, -L, PSA Series
Advantest: R3261/3361, R3265/3271, R3267/3273 Series
Anritsu: MS2602, MS2650/60, MS612A, MT8801B Radio Comms Analyzer
Hewlett-Packard: HP8590 Series, HP8560/1/2/3, HP8566B, HP8568A/B, HP3585, HP4195, HP8542E/HP8546A EMI Receiver
IFR: AN940 Series, IFR 2398/2399
LG Precision: SA-9270/SA-7270
Marconi Instruments: 2380 and 2390 Series, 2945 Series (spectrum analyzer display only), 2965 Series (graphical displays only)
Rohde & Schwartz: ESMI, FSA/B/M, FSE, FSP, FSIQ Series, CMS50 Series (spectrum analyzer display only), CMD55/65, CMU200 Radio Test Sets
Tektronix: 2711/2712

Oscilloscopes:
Fluke/Philips: PM3350/55/65/75 Series, PM338XA/PM339XA Series
Hewlett-Packard: HP54120, HP54200A, HP54502A, HP54520C, HP54540C, HP54600 A Series, HP54645 A/D, HP54750, HP548XXA Infiniium Series, HP83480
LeCroy: LC300/LC500/9300/WaveRunner Series
Tektronix: TDS 200 to 800 Series, 2432A, 7D20 Digitizer
Yokogawa: DL1520/DL1540 Series

SUPERSTAR – CIRCUIT SIMULATOR

The SUPERSTAR simulator sets the standard for RF and microwave circuit simulation software. Easy operation, accuracy, a rich feature set, fast execution, and "when you call" factory support define that standard. Even if you use another simulator, unique SUPERSTAR features help you solve new problems or old problems in new ways.

Accuracy

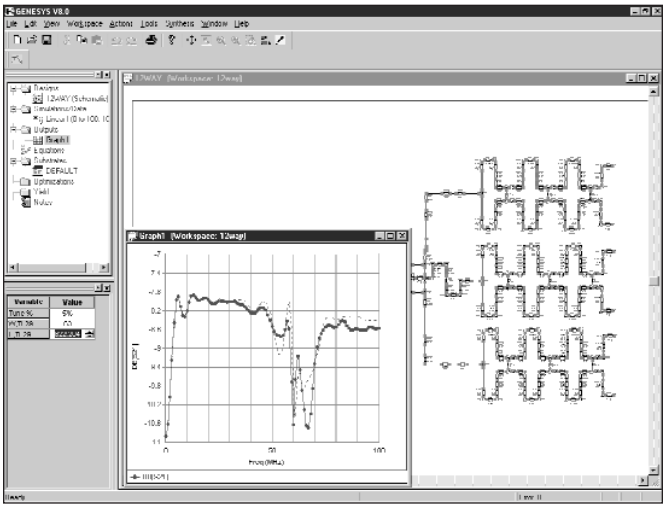
SUPERSTAR model development involved painstaking cross-referencing and verification with measured and published data, electromagnetic simulation, and comparison with other simulators. Eagleware has a fully equipped RF lab where networks are built and tested regularly. We accept selected design contracts when that work expands our test database.

Active devices are characterized in SUPERSTAR using S-parameter data files. This process is inherently more precise than the procedures required for Spice simulation.

All circuit simulators use symbolic expressions to define microstrip lines and discontinuities. For lines, most simulators use expressions based on the work of Jansen and Kirschning, which are regarded as the most accurate available.

Eagleware customers successfully use our software up to 40 GHz. As the operating frequency increases, improved circuit performance and simulator accuracy is achieved with thinner substrates. Good results are achieved through 40 GHz on 5 mil board, 18 GHz on 10 mil board, and 4 GHz on 1/16" board.

If you need to push accuracy limits or if you work with unusual geometries, you should consider augmenting circuit simulation with electromagnetic simulation such as the GENESYS EMPOWER module.



This 400 element power splitter simulates 101 points in less than 2 seconds, tunes 101 points in less than ¼ second on a 366 K6 PC.

The Fastest Simulator You Can Fly!

One of the most exciting features of SUPERSTAR is the execution speed. You tune by tapping a cursor key and watching results update on screen. Tuning is just like being at the bench. Fast execution also results in amazing optimization speed and statistical analysis. Execution time on Pentium machines for typical circuits is less than 100 microseconds per frequency! This speed is achieved using unique Eagleware algorithms based on diakoptic technology. Specific techniques include node elimination, closed form equations, element and output classes, and model caching.

Simulation Parameters

A full set of simulation parameters are built into SUPERSTAR. In addition to these parameters shown in the table below, you can use post-processing to calculate any other parameters you desire.

Network Parameters	**Noise Parameters**
S-parameters	Noise correlation matrix
H-parameters	Noise figure
Y-parameters	Noise measure
Z-parameters	Noise resistance (normalized)
	Noise temperature (effective)
	Noise circles
	Minimum noise figure
	Optimum noise match impedance
	Optimum noise match admittance
	Optimum noise match gamma
Stabilty Parameters	**Impedance Parameters**
Stability factor	Input impedance
Stability measure	Input admittance
Stability circles, input plane	VSWR
Stability circles, output plane	
Gain Parameters	**Match Parameters**
Maximum available gain	Simultaneous match impedance
Gain circles, available	Simultaneous match admittance
Gain circles, power	Simultaneous match gamma
Gain circles, unilateral	
Voltage gain	

Unrestricted Global Noise Analysis

SUPERSTAR uses the noise correlation matrix technique to compute the noise figure and noise parameters of general topology networks. Unlike many circuit simulators, there is no special noise block to write nor does the circuit have to conform to specific topologies. This allows the computation of noise figure for unusual circuits such as transformer feedback amplifiers. The noise correlation matrix is global and active cascades are automatically handled.

Optimization

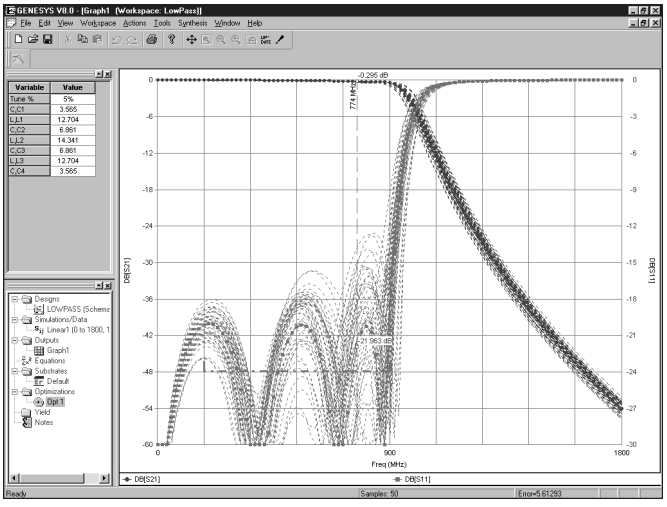
A powerful performance optimizer is part of SUPERSTAR. The simulator will adjust component parameters to improve performance. You select which component to optimize and specify your performance objectives. SUPERSTAR then uses gradient, pattern search, or automatic modes to search for better

values. Gradient optimization finds a local performance peak quickly, but is susceptible to being caught in local performance maximums. Using Newton's Method, derivatives of the performance specification with respect to component values are calculated and values are determined by projecting the derivative. The pattern search optimizer jumps to new values in an effort to find a better set of values. It is slower but less susceptible to getting stuck in local maximums. The automatic method switches between gradient and pattern search to take advantage of both techniques.

Statistical Analysis and Yield Optimization

SUPERSTAR supports a full range of statistical analysis and optimization tools including:

- **MONTE CARLO ANALYSIS**:
  Estimates the impact of the tolerance of multiple components on the output parameters. Monte Carlo analysis helps determine which specifications are at risk for high volume manufacturing. A Monte Carlo display for an elliptic bandpass filter is shown in the captured screen below.



A sample Monte Carlo analysis of a lowpass filter, simulating 50 samples using a Gaussian distribution and tolerances of 5%.

- **SENSITIVITY ANALYSIS**:
  Identifies components that are most responsible for performance degradation. You quickly discover which parts must have a tight tolerance and which can be less expensive.

- **YIELD OPTIMIZATION**:
  Selects element values that result in the greatest yield. Different from optimizing to a particular response, yield optimization is useful when designing for high volume, low cost applications. Two methods are included: Design Centering and Yield Optimization.

Each component has a unique tolerance and distribution. You can specify Gaussian or uniform distribution, either symmetric or skewed.

Simulation Models

A rich set of simulation models are built into SUPERSTAR. All models have been verified by measurement, EM simulation, or comparison with published material. Moreover, the models have been verified by the thousands of customer-designed circuits using SUPERSTAR over the last 15 years.

Lumped Component	Microstrip	Transmission Lines
Resistor	Coplanar waveguide	Coaxial line
Capacitor	Coplanar waveguide with ground	Coaxial gap
Inductor	Line	Coaxial end
Mutually coupled Ls	Tapered Line	Coaxial with square conductor
Transformer	Curved line	Four terminal coaxial line
Tapped transformer	Exponential line	Electrical transmission line
Parallel L-C	Interdigital capacitor	4-terminal electrical t-line
Parallel resonator-L	Round spiral	Physical transmission line
Parallel resonator-C	Rectangular spiral	4-terminal physical t-line coupled lines
Parallel R-C	Thin film capacitor	N-coupled lines
Parallel L-C	Thin film resistor	Ruthroff transformer
Parallel R-L-C	N-coupled lines	Wire
Series resonator-L	Cross	R-C line
Series resonator-C	Bend	Distortionless TEM line
Series L-C	Open-end	Uniform TEM line
Series R-C	Gap	Exponential TEM line
Series R-L	Radial stub	Single mode transmission line
Series R-L-C	Step	Multimode transmission line
	Tee	
	Via hole	

Stripline & Slabline	Ideal Elements	Interconnects
Broadside coupled stripline	Gain block	Bond wire
Offset stripline	Constant delay	Flat wire
Line	Constant phase shift	
Bend	Gyrator	
2 Coupled lines	V-controlled V-source	
N-coupled lines	V-controlled C-source	
Open-end	C-controlled V-source	
Gap	C-controlled C-source	
Step		
Tee		

Other Models	Slabline & Waveguide	Device & Data Models
Circulators	Slabline	ABCD parameters
Isolators	Coupled slabline	Bipolar transistor
Couplers	N-coupled slabline	FET transistor
Splitters/Combiners	Rectangular waveguide	PIN diode
Switches Monopole	Waveguide adapter	Varactor
Dipole		1-, 2-,3-,4- port S, Y, Z, H data
Circulator		N-port S, Y, Z, H data
Isolator		
Piezoelectric resonator		
Air-core solenoid		
Toriodal inductor		

Device Data

SUPERSTAR includes over 25,000 device data models from 14 vendors. Device data is available for a variety of transistors (BJTs, FETs, MESFETS, MOSFETS), diodes, ICs, capacitors, and inductors.

Alpha	Mitsubishi
CoilCraft	Motorola
Fujitsu	NEC
HP	Philips
Johanson Technology	Polyfet
Microwave Technology	Siemens
MiniCircuits	Stanford Microdevices

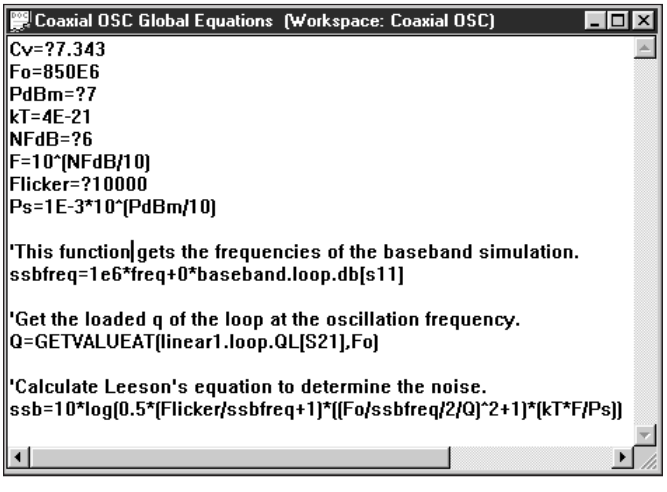
User Models

You can easily create your own models. These models can be used to add parasitics to components, to create new models, and to characterize unique components. Element values are passed to the model and GENESYS's built-in equation features may be used to calculate values based on the input parameters.

User models are automatically registered with the SCHEMAX program and are available for use within schematics. They are also integrated into the layout environment where a default footprint is registered with the model.

Equations, Functions, and Post Processing

Equations may be used throughout GENESYS. You can compute element values or post-process results. For example, Ct=32/(1+0.7/Vt)^1.5 could be entered. You could then tune the voltage Vt and watch the circuit response as the capacitance changes. Or, you could determine power splitter flatness by dividing S21 by S31.



Using post-processing equations, you can calculate phase noise from loaded Q.

Full complex math with string, vector, and matrix operators are available. Flow control is available with IF/THEN and GOTO constructs. A wide range of transcendental functions and logic operators are built in. In addition, you can combine the built-in operators and develop your own functions. These functions can be stored with a particular design file or stored in a library to become just like a built-in operator.

Built-in Functions and Operators available in GENESYS

Trigonometric Functions
ARCCOS - inverse cosine
ARCSIN - inverse sine
ARCTAN - inverse tangent
COS - cosine
SIN - sine
TAN - tangent

Hyperbolic Functions
ARCCOSH - inverse H cosine
ARCSINH - inverse H sine
ARCTANH - inverse H tangent
COSH - hyperbolic cosine
SINH - hyperbolic sine
TANH - hyperbolic tangent

Logs and Exponents
DB10 - returns 10*log(x)
DB20 - returns 20*log(x)
EXP - "e" raised to x
LOG - base 10 logarithm
LN - natural logarithm
SQR - square root

Number Conversion
ABS - Absolute value
MAG - Magnitude
ANG- Phase ± 180 deg
ANG360 - Phase 0 - 360 deg
COMPLEX- Converts real to complex
REAL - Real part
IMAG - Imaginary part
FIX - Truncates numbers
INT - Integer part

Vector and Matrix Functions
VECTOR - Defines a vector
MATRIX- Defines a matrix
COUNT - Size of an array

Operators
Array Index ([])
Exponentiation (^)
Multiplication (*)
Division (/)
Integer division (\)
Modulo (%)
Addition (+)
Subtraction (-)
Equality (=)
Less Than (<)
Greater Than (>)
Greater Than or Equal to(>=)
Less Than or Equal to (<=)
NOT (!)
AND (&)
Exclusive-Or (@)
Equivalence (#)
Logical Implication ($)

Post Processing
GET - access simulation data
GETVALUE - value of a post-processed expression
GETVALUEAT - value at a given independent value
GETINDEPVALUE - Independent value of an array
MIN - Minimum of an array
MAX - Maximum of an array

Conditionals and Flow
IF/THEN
IFF-returns x if true, y if false
IFTRUE- returns x if true, zero if false
GOTO-Jump to new line
FUNCTION-Begin a function
RETURN-Ends a function

Other
BESSELJ0 - Bessel function J
FN_E - Elliptic integral of the second kind
FN_K - Elliptic integral of the first kind
RND - Pseudo-random number

The electromagnetic simulator, EMPOWER, analyzes planar circuits such as microstrip, stripline, coplanar, slotline, finline, and suspended/inverted substrates (often called a 2½D or planar 3D simulator). EMPOWER analyzes circuits with a single level of metal while EMPOWER ML analyzes an unlimited number of metal levels. Both support an unlimited number of substrate layers.

Historical Background

The root of EMPOWER is work that began in 1987 at the Novosibirsk Electrical Engineering Institute and leading to the commercial development of TAMIC in 1991 in Moscow. TAMIC saw commercial use in the Soviet Union and elsewhere. In late 1996, Eagleware acquired TAMIC and the principle author joined the Eagleware team to begin significant improvements. The code was integrated into GENESYS 6.5 in 1998.

Method Of Lines

EM simulation is numerically expensive and execution is slower than circuit theory simulation. EMPOWER is based on the Method of Lines, a technique that simulates MIC and MMIC structures with better accuracy. It is a type of integral method that is particularly well behaved numerically because it has superior convergence and numeric conditioning properties when compared to other integral methods. It solves for 3D currents present in a defined layout and calculates S-parameters from the current structure. The implementation is highly optimized which results in fast analysis.

Benchmarked Accuracy

You can use two different forms of benchmarking the accuracy of simulations; compare measured data to computed results or compare results to theoretical problems that have a known exact solution. The first one is the most widely used form of benchmarking and we have several examples in the Examples manual. However, it is often difficult to separate simulation error from measurement error. Port discontinuities are examples of phenomena that make direct comparison difficult.

Advanced Features

EMPOWER includes many features not available in many expensive EM simulators. Some examples include circuit-EM co-simulation, automatic symmetry detection, and multi-mode decomposition.

Real Time Tuning Techniques

Automatic lumped element configuration and solution with symmetry and multimode decomposition make optimization and tuning faster and more convenient. For example, a simple and powerful technique available for filter structures with vias is to run EMPOWER without the vias. The filter structure is non-resonant and only a few frequencies are run. Vias are replaced by GENESYS and hundreds of frequency points may be displayed resulting in fine sweep detail. Decomposition may be used to optimize and tune spiral inductors and meander lines as fast as circuit theory simulators.

Circuit-EM Co-Simulation

When simulation begins, EMPOWER places internal ports at the location of each lumped element in the circuit and computes S-parameters for the n-port. Then, SUPERSTAR computes the response with lumped elements reinstalled. The GENESYS environment handles the entire process automatically. Accuracy is maintained because all signal metal segments are present in the enclosure and their coupling is simulated. Since many circuits contain lumped elements, this capability saves effort without compromising accuracy.

Automatic Detection of and Solution with Symmetry

Halving the size of a problem reduces the execution time and memory requirements by a factor of four. With most EM simulators you may divide some symmetrical circuits into two sections, simulate, and combine the networks back together. EMPOWER automatically detects symmetry and solves all symmetrical circuits. It even detects 2-mirror and 180° rotational symmetry with memory savings of 16X and 8X, respectively. No special steps are required: the entire process is automatic.

Generalized S-Parameters

S-parameters are typically normalized to a constant impedance such as 50 or 75 ohms. You have the option of normalizing S-parameters to the simulated line impedance with EMPOWER. This technique reduces much of the error associated with assuming a limited number of simulation cells across the width of transmission lines. GENESYS automatically reads and creates generalized S-parameters, resulting in high accuracy.

Multimode Transmission Line Models

Coupled lines have multiple propagation modes. For example, two coupled lines have an even and odd propagation mode. There are N modes for N coupled lines. EMPOWER creates a multimode transmission line model that can be used for a simulation. This coupled line model considers non-adjacent line coupling and the length of this line may be tuned and optimized in GENESYS in real time.

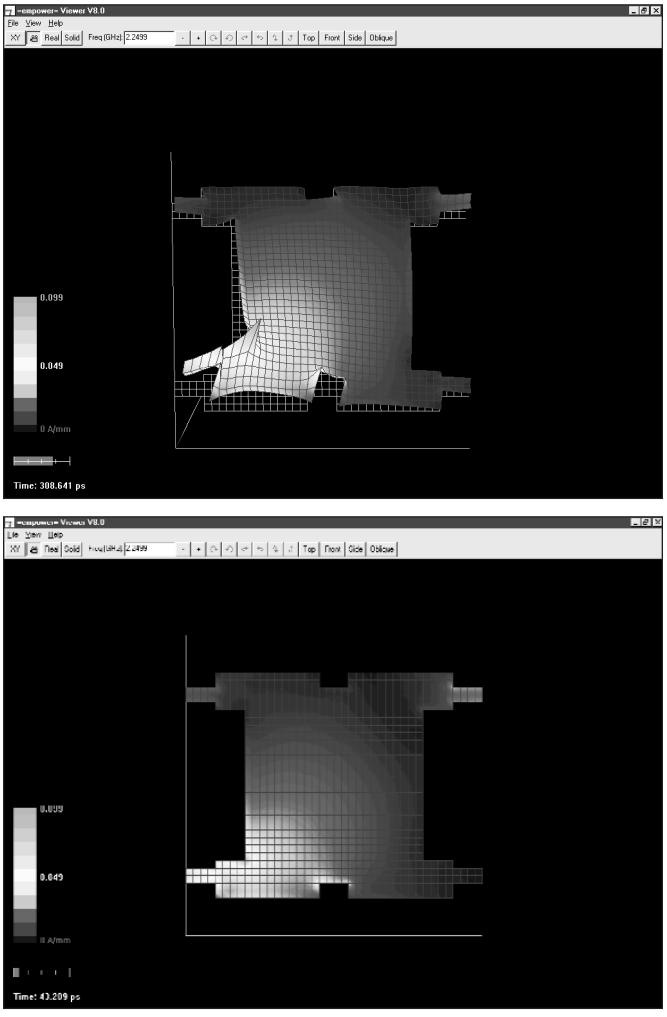
Large Problems And Decomposition

With multimode line models and generalized S-parameters it is often possible to break large circuits into smaller sections, thus making EM simulation feasible for circuits that would otherwise be too large. This can be done while retaining non-adjacent line coupling for circuits such as filters, spiral inductors, and meander lines.

3D Viewer With Dynamic Phase Rotation Plots

EMPOWER includes a 3D color viewer that helps you visualize current density (voltage in slotline mode) in your circuit. The viewer processes both the magnitude and angle of currents and

displays them as static and dynamic plots. These plots provide insight and help you discover modifications for improved performance. Most EM simulators offer a viewer but the EMPOWER viewer provides dynamic views with precise phase information. The magnitude, real, or angle components of the current are selectable. You may select x, y, z, or xy currents and the view may be rotated in all three planes. Visit our website at www.eagleware.com to see a demonstration.



A dualmode coupler in the EMPOWER viewer. An oblique view and a top view of the XY current magnitude. The port on the lower left is driven.

Accurate Loss Computation

EMPOWER computes metal, dielectric, and radiation loss with high accuracy. Circuit simulators do not predict radiation loss and some EM simulators are not well behaved in the prediction of loss with respect to the number of simulation cells across the transmission line. With EMPOWER, the loss of structures is accurately predicted for both enclosed circuits and boxes with open or lossy covers.

Slot Mode For Slot And Coplanar Circuits

Typical circuits are sparse in circuit metal and are best simulated by solving for current in the metal. Other circuits, such as slotline and coplanar, have significant metal coverage and are more efficiently solved using the slotline mode in EMPOWER. Rather than solving for current in the metal region, EMPOWER solves for voltage in the non-metal regions. This mode saves significant computational effort and reduces the required time and memory.

Port De-embedding And Reference Planes

When a line approaches the box sidewall, there is additional reactance from the line to "ground." EMPOWER automatically removes this effect for normal ports. This is called de-embedding and is done because the simulated object may be used as a part of another circuit and the wall is not present. If you want to move the reference planes for the EMPOWER run, you may simply drag them to the desired location using the mouse. EMPOWER also lets you turn off de-embedding to analyze a circuit in a box with sidewalls.

Box Modes And Package Effects

Have you ever designed an amplifier, paying careful attention to the stability factor, only to have it oscillate despite all your precautions? Have you fought poor ultimate rejection in filter stopbands? Have you fought spurious signals that aren't reduced by filtering? A common cause of these problems is box modes.

An enclosed box acts like a cavity resonator. This can have a profound influence on the circuit behavior. While some EM simulators assume an "open" environment, EMPOWER inherently predicts these effects.

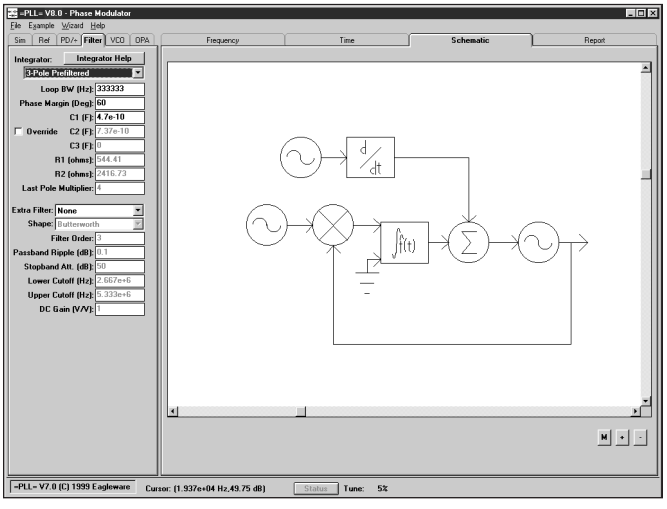
At frequencies near each resonance, signal metal radiates efficiently into the cavity. Because this radiation is reciprocal, coupling occurs between metal segments in the signal path. If the circuit is run with an open or lossy cover, then resonance effects are reduced. In this case, EMPOWER accurately predicts surface modes which limit the ultimate rejection in the circuit.

PLL – PHASE-LOCKED LOOP SYNTHESIS AND SIMULATION

The PLL module includes all of the features you will need to design PLL phase and frequency modulators, phase and frequency demodulators, and synthesizers. Conventional frequency domain analysis is included for quick and simple stability assessment. Sophisticated routines model single sideband phase noise down to the resistor level and a built-in time domain simulator characterizes true non-linear loop locking and transient behavior. PLL integrates a number of techniques within one complete design package including:

- Synthesis of loop filter element values
- Loop analysis in the frequency domain
- Loop analysis in the time domain
- Noise estimation down to the resistor level

The PLL module surpasses the capabilities of simpler programs that model the behavior of phase-locked loops in the frequency domain. These techniques, which are included in our software, are convenient for quick loop bandwidth and stability analysis. However, PLL also incorporates sophisticated techniques for the time domain analysis of the loop.



Schematic of a PLL used as a phase modulator.

PLL Topologies

The PLL locks a VCO to a multiple of the reference frequency. This basic PLL is called a synthesizer. PLL includes set-ups for other PLL applications such as phase and frequency modulators and demodulators.

Synthesis

PLL calculates the loop filter element values. You specify parameters for the loop components such as the VCO tuning characteristics and the phase detector output current. You control the impedance level of the integrator values by choosing C1 in the loop filter. Letting you choose C1 helps maintain practical values for both narrow and wide bandwidth loops and it is also critical for controlling the PLL phase noise. Then, PLL calculates the remaining component values for the filter.

Phase Detector Types

XOR, mixer, phase-frequency detector (PFD), and the newer PFD with charge pumps are supported. The PFD and charge pump phase-frequency detectors have improved locking and tracking performance. When properly designed, loops with the charge pump PFDs offer improved phase noise performance.

Active and Passive Filters to 4th Order

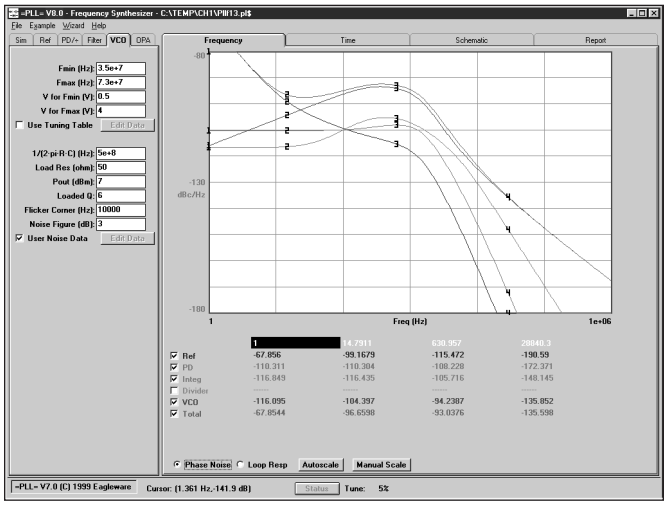
PLL synthesizes both active and passive loop filters. Active filters for loops up to 4th order and passive filters for loops up to 3rd order are synthesized. While 2nd order loops are more common, higher order loops offer significantly improved reference sideband rejection and require only a few additional components. The charge pump PFDs typically use passive loop filters which eliminate the often significant noise from the operational amplifier.

Pre-Filtered Loops

PFDs have pulse rise-times and pulse widths beyond the capabilities of common op-amps. Some of the loop filters in PLL implement the first pole as an R-C network preceding the op-amp, thus limiting the bandwidth of signals presented to the op-amp. This implementation allows you to use common op-amps.

Noise Analysis

PLL accurately models the contribution of each loop component and the action of the loop on the PLL output single-sideband phase noise (SSB n). Noise in the phase detector, dividers, VCO, op-amp, and even resistors in the loop filter are considered.



A PLL single side-band noise output window with a sweep from 1 Hz to 1 MHz carrier offset. The top trace is the total SSB noise at the output of the PLL. The remaining traces are the contributions to this total noise from the various loop components. These curves consider the action of the PLL on the original spectral noise plots of the offending components.

Residual FM and PM Noise

PLL integrates the single side-band noise over the baseband frequencies you specify to determine the residual FM and PM noise modulation. Residual FM and PM relate directly to the S/N performance of communications systems and are an alternative method to specify noise.

VCO Noise

The VCO is often the major source of noise at offsets greater than the loop bandwidth. Characterization of VCO noise and realizing the lowest possible noise are therefore critical aspects of VCO design. PLL estimates VCO noise using D.B. Leeson's equation with an additional term for active device flicker noise. The required input parameters for Leeson's equation are determined using the GENESYS modules SUPERSTAR, OSCILLATOR, and the documentation that is included with them. Alternatively, you may enter measured VCO noise data point by point versus carrier offset frequency.

VCO Tuning Characteristics

Unfortunately, real VCOs do not have a linear frequency versus applied voltage curve. Typically, the tuning sensitivity is greatest at low frequencies. The programmable divider N is lowest at the same time and both effects increase the PLL gain at low frequencies. This places stress on loop stability, particularly in wide tuning PLLs. PLL allows you to specify the VCO frequency at multiple voltage points, thus providing accurate stability analysis at all PLL output frequencies.

VCO R-C Filter

A bypass capacitor at the VCO input, or even the varactor capacitance, introduces an R-C time constant that is included in the loop analysis.

Extra Loop Filters

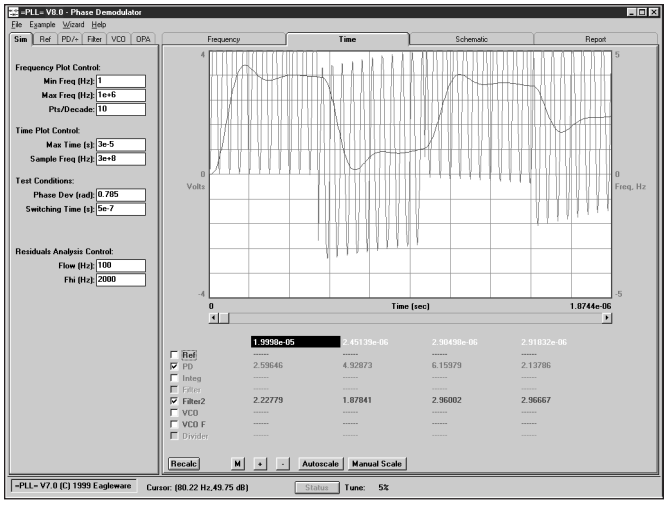
You may cascade an extra lowpass or bandstop filter after the loop integrator. PLL computes the transfer function for Butterworth, Chebyshev, and elliptic Cauer- Chebyshev filters of any practical order and considers the effects of this extra filter on the frequency, noise, and time domain responses.

Non-Linear Analysis

Predicting lock times and transient behavior of PLLs by the transform of classic frequency domain behavior is not accurate enough. PLL accurately predicts the behavior of such systems at the functional bit level.

High Speed Time Domain Analysis

The time domain responses of a linear PLL could be found by transforming the frequency domain response. However, PLL includes sophisticated time domain analysis using a built-in time domain simulation engine.



Time-domain responses of a 10.7 MHz phase demodulator.

The engine starts with initial voltages of zero. For each time step, the inputs are used to calculate outputs that serve as future inputs. This process ripples through the network developing a "time picture" of voltages at each node.

Because PFD pulse widths are much less than the reference period, a short time step is required. Low loop bandwidth requires significant time to lock. This combination dictates a large number of sample points. PLL uses a number of techniques to speed execution and to support over 500,000 time steps.

Wizard

The number of required input parameters to design a PLL is intimidating. The Wizard in PLL helps you set-up the loop by providing suggestions at each prompt and by automatically entering responses to other prompts. The Wizard then launches the interactive mode where you may change any parameters selected by the Wizard.

Computer Requirements

- Pentium-class CPU
- 32 MB of RAM minimum, 64 MB of RAM typical, and 256 MB of RAM for large electromagnetic simulations
- Windows 95/98/NT/2000
- VGA or higher video mode (Super VGA video mode for the EMPOWER viewer)
- Hard drive (30 MB minimum installation, 100 MB typical installation including manuals and on-line help, 200+ MB with uncompressed library data files)
- Parallel Port
- Mouse or compatible pointing device

Network Licenses

GENESYS Premier and GENESYS Designer are available as floating network licenses. Using the industry standard FLexLM license manager, a license can float among a network of computers in a 10-mile (16 km) radius. No more searching for a key that is shared among a group...the license is always on the network and the server can tell you where the keys are being used. If you already own standalone licenses, you will receive a full trade-in credit towards your purchase.

Subscription Service

Eagleware's subscription service provides you with automatic updates to your GENESYS software. Several times per year you will receive a new CD containing new features, modules, and enhancements.

Part of the Eagleware philosophy is to deliver solutions to make the engineer's job easier, and automatically delivering the products you need will make your job easier. Our new subscription service is the perfect complement to our winning design suite GENESYS. The speed, power and accuracy of GENESYS are proven. And the value and convenience of our subscription service will be a real benefit to you.

What Do You Get?

In the course of supplying the RF and microwave community with a steady stream of new products, Eagleware often releases software updates. Our subscription service will automatically ship these upgrades directly to you.

- CDs for all major and minor releases
- New set of manuals with up-to-date application examples for major version releases (e.g. 7.0, 8.0) of GENESYS.

Technical Support

Technical support is free from Eagleware. However, the software is so easy to learn and use, you probably will not need it. Call, e-mail, fax, or use the web to get answers to your questions. You will get a quick response and your question is answered completely and to your satisfaction.

Training and Reference Materials

All GENESYS modules were developed in-house using one interface that is based on the latest Windows standards. This makes our software intuitive, familiar to Windows users, and easy to learn and use. Eagleware documentation and technical support are all you will need to effectively use our software. However, Eagleware regularly conducts workshops and training sessions on RF/microwave design at technical meetings, at customer sites, and in-house. Please contact us to schedule training sessions or visit our website for dates and locations of workshops and technical meetings.

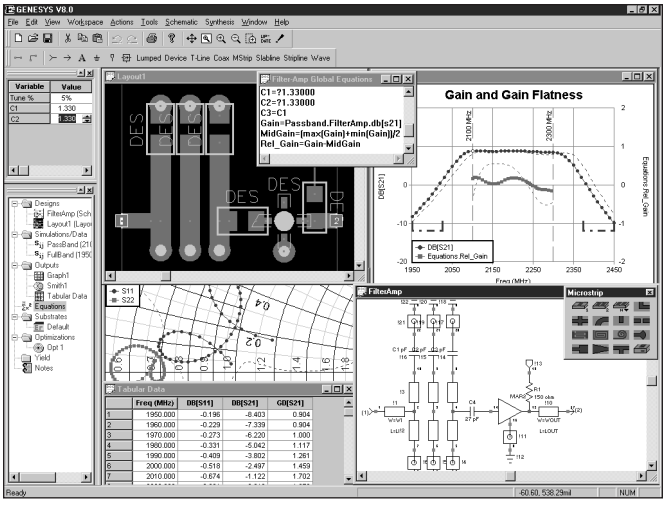
Absolute Satisfaction Guaranteed

Try GENESYS or any Eagleware module and you'll be more than satisfied: you'll be amazed. If not, return GENESYS within 30 days for a full refund.

The GENESYS Design Package

Eagleware offers power, speed and accuracy for RF and microwave design engineers. Synthesis, design entry, and simulation software are integrated into a single design environment called GENESYS.

GENESYS sets the standard for RF and microwave design software. Accuracy, a convenient interface, a rich feature set, fast execution, and "when you call" direct factory support define that standard. GENESYS is available in five design suites and fifteen individual modules.



Synthesis, schematic capture, circuit simulation, layout, and electromagnetic simulation are all integrated in the GENESYS environment.

GENESYS Design Suites

- **GENESYS Premier** . . . . Complete design suite featuring all modules.
- **GENESYS/EM** . . . . . Design suite featuring GENESYS Basic and EMPOWER ML.
- **GENESYS Designer** . . . Includes all modules except HARBEC, EMPOWER and EMPOWER ML.
- **GENESYS/NL** . . . . . Complete circuit simulation and layout suite featuring SUPERSTAR, HARBEC, SCHEMAX, and LAYOUT.
- **GENESYS Basic** . . . . . Circuit simulation and layout suite featuring SUPERSTAR, SCHEMAX, and LAYOUT.

GENESYS Modules

Synthesis

- **OSCILLATOR** . . . . . L-C, SAW, line and crystal oscillator synthesis
- **MATCH** . . . . . Active and passive matching network synthesis
- **FILTER** . . . . . L-C filter synthesis
- **M/FILTER** . . . . . Distributed printed and machined filter synthesis
- **A/FILTER** . . . . . Active R-C filter synthesis
- **EQUALIZE** . . . . . Group delay equalization synthesis
- **T/LINE** . . . . . Transmission line synthesis
- **S/FILTER** . . . . . Advanced direct filter synthesis

Design Environment

- **SCHEMAX** . . . . . Schematic entry for simulation and layout
- **LAYOUT** . . . . . RF/microwave circuit board design
- **TEST LINK** . . . . . Automatic data gathering from measurement equipment

Circuit Simulation

- **SUPERSTAR** . . . . . High-speed linear circuit simulation
- **HARBEC** . . . . . Harmonic balance nonlinear circuit simulation

Electromagnetic Simulation

- **EMPOWER ML** . . . . . Multi-level planar 3D electromagnetic simulation
- **EMPOWER** . . . . . Single-level planar 3D electromagnetic simulation

Phase-Locked Loop Design

- PLL . . . . . PLL synthesis and simulation

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