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Non-Destructive Analysis and EM Model Tuning of PCB Signal Traces using the Beatty Standard

White Paper from DesignCon 2017

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Abstract

The Beatty standard has been gaining attention from the high-speed digital printed circuit board (PCB) community as an approach to obtain PCB signal trace and dielectric material parameters for PCB manufacturing verification and measurement based modeling [1,2]. This is especially critical for test and measurement applications where only a single PCB might be manufactured and destructive physical analysis like cross sectioning is not possible. The simple resonant Beatty test structure can be easily placed anywhere on the PCB and together with an additional structure for connector de-embedding provides non-destructive analysis of the PCB fabrication.

In this paper we will introduce the different Beatty standard implementation topologies including single ended and differential series resonant structures. Measured results from the Beatty test structures can then be used to run a model optimization procedure that tunes for as-fabricated material properties to match with measured results. The significance of PCB test fixture de-embedding will also be addressed for accurate high frequency material properties. The end result of the paper is to provide a step-by-step procedure for a PCB designer wishing to use and implement the Beatty standard on his next board turn.

The step-by-step procedure will then be applied to three different Beatty PCB test structures: stripline, microstrip, and differential microstrip. Each implementation will be evaluated by comparing measurement with the design data sheet simulation, and the optimized as-fabricated measurement-based-model simulation. Cross sections of the PCB test coupons containing the structures were also performed for further comparison of the obtained results.

KEYSIGHT TECHNOLOGIES

DesignCon 2017

Non-Destructive Analysis and EM Model Tuning of PCB Signal Traces using the Beatty Standard

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Authors' Biographies

Heidi Barnes is a Senior Application Engineer for High Speed Digital applications in the EEsof EDA Group of Agilent Technologies. Past experience includes over 6 years in signal integrity for ATE test fixtures for Verigy, an Advantest Group, and 6 years in RF/Microwave microcircuit packaging for Agilent Technologies. She rejoined Agilent Technologies in 2012, and holds a Bachelor of Science degree in electrical engineering from the California Institute of Technology.

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Manuel Walz is a hardware design engineer at Advantest (former Verigy) in Böblingen and joined the company in 2010 after receiving his B.Eng. degree in mechatronics from the DHBW Stuttgart. He is involved in the development of the high-speed interfaces between the components of Advantest's IC testers. Since 2016 he also holds a M.S. degree in electrical engineering from the University of Applied Sciences Darmstadt.

Introduction

Printed circuit boards (PCBs) are ubiquitous in all but the simplest electronic products. As the complexity of those products has increased, so has the complexity of the PCBs. PCBs can represent a significant share in the overall cost of complex electronic products/equipment. Examples of interest in this paper include large backplanes, prototype PCBs manufactured in a fast track process and automated test equipment (ATE) test fixture PCBs.

During the design and prototype phases of a new piece of equipment, it is often necessary to extract certain as-fabricated parameters from a PCB for further use in the development process like simulations to tune manufacturing tolerances and evaluate design cost trade-offs. Traditional destructive methods such as making cross-sections to measure as fabricated dimensions require additional expensive PCBs to be ordered. In addition, many companies will not have the required capabilities in-house and the added time and expense of an external laboratory must be included.

Figure 1 shows a picture of a test fixture PCB example used with in an ATE system. Due to the large size, high layer count and advanced manufacturing techniques used, these boards have a significant cost. Furthermore, they are typically used for only one specific device under test (DUT) resulting in extremely low volumes. Volumes can even go as low as only one single PCB.

In this ATE example the DUT high-speed digital outputs are routed to coaxial connectors allowing either to be measured with external instrumentation or to create a loopback path back to a DUT input [3]. The challenge is that for high-speed digital or high-frequency applications, the DUT test fixture signal traces have a significant impact on the measured DUT signal and this impact needs to be evaluated and in most cases de-embedded from time domain measurements.

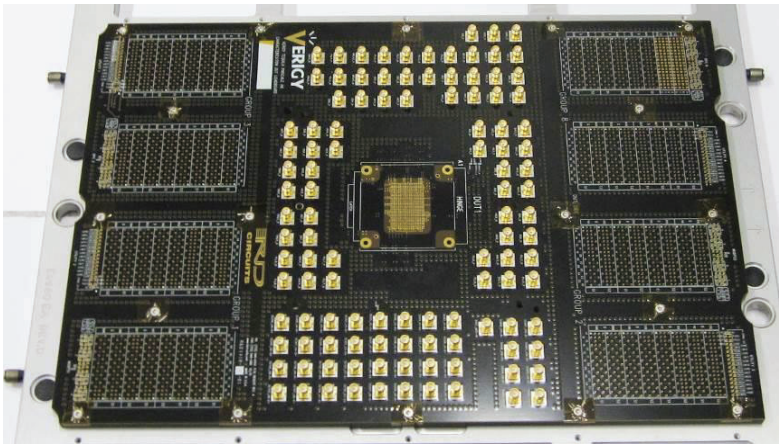

Figure 1: Example of an ATE PCB test fixture

Early in the design cycle of the PCB, it is good practice to use electromagnetic (EM) simulations of the high speed PCB signal traces. The EM simulation is used to evaluate the signal trace loss, crosstalk, and optimize transitional structures such as vias. The simulated data can also be used for de-embedding of the test fixture from the measured data. The challenge is how to guarantee that the simulation model is a true representation of the as-manufactured PCB test fixture performance. When there is no prior measurement data the only option is to use the manufacturer's data sheet values for the different design parameters, or best estimates. Even after the test fixture is manufactured and a measurement made, it is still unclear what the real values of the relevant parameters are for the manufactured board especially if we see a significant discrepancy between the simulated and measured results.

A possible approach to address this challenge is to include a test structure on the PCB that can easily be measured using a vector network analyzer (VNA). This structure is simulated before manufacturing and added to the PCB. Typically there is a connectorized fixture to go between the VNA and the planar PCB test structure, but if this poses a problem due to the connector size or height, it is possible to use micro-coaxial probes or removable compression contact connectors. A calibration fixture de-embedding structure is also added to the PCB so that the connectors can be removed from the full-path measurement and only the raw performance of the PCB structure is used for simulation comparison. It is this de-embedded raw performance of the PCB structure with the connectors removed that can then be used to verify the pre-fabrication design simulation. If there is a discrepancy between measurement and simulation, then the measurement is used to tune the simulation model. Utilizing a simple test structure greatly reduces the simulation time and provides for fast tuning of the as-fabricated parameters. This process is shown in Figure 2.

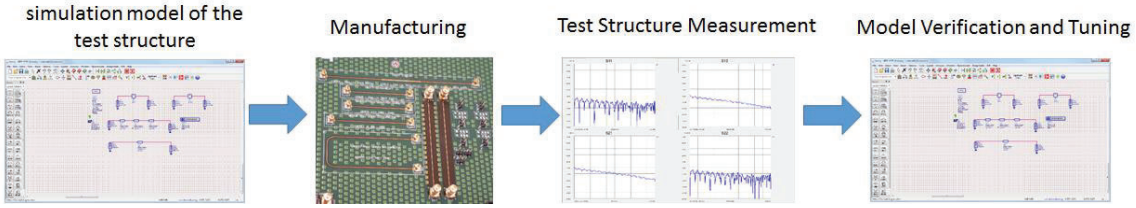

Figure 2: Using a test structure on the DUT PCB test fixture for checking pre-layout simulation accuracy and tuning simulation parameters to manufactured PCB measurements.

In this paper we propose that a series resonant Beatty standard [4] be used as the test structure in the above methodology. We will show that it is a better fit for parameter identification and simulation model tuning than other test structures like a simple microstrip or stripline lossy transmission line. The next sections will discuss the measurement based model tuning methodology in detail, the proposed Beatty standard, and the required connector fixture de-embedding from the measurement. Finally we will present example results using three different implementations of a Beatty standard: stripline, microstrip, and differential microstrip.

Measurement Based Simulation Tuning

To tune the simulation model based on the measured S-parameters of the test structure it is necessary to compare the simulated data with the measured data. There are three groups of parameters that may deviate from the expectations based on the material specifications and PCB artwork.

- Materials
  - Dielectric constant ε_r
  - Loss tangent $\tan\delta$
  - Surface roughness *Rq* or *Rz*
- Substrate variations
  - Overall Height of the dielectric material *H*
  - Height of the core dielectric material H_{core} in stripline case
- Etching and plating variations
  - Trace width *W*
  - Trace height *T*

A structure selected for measurement based simulation tuning should be sensitive to all the above mentioned deviations of the material properties and the manufacturing variations. Furthermore, each of the deviations should leave a unique signature in the parameters used for tuning. The goal of the tuning process is to identify the geometrical and material's deviations of the manufactured PCB by comparing the electrical parameters of the model to those of the measured test structure.

Figure 3 shows four typical parameters that characterize a test structure electrically and can be used for simulation tuning. In this case insertion loss, return loss, time domain reflectometry (TDR) and the transmitted phase.

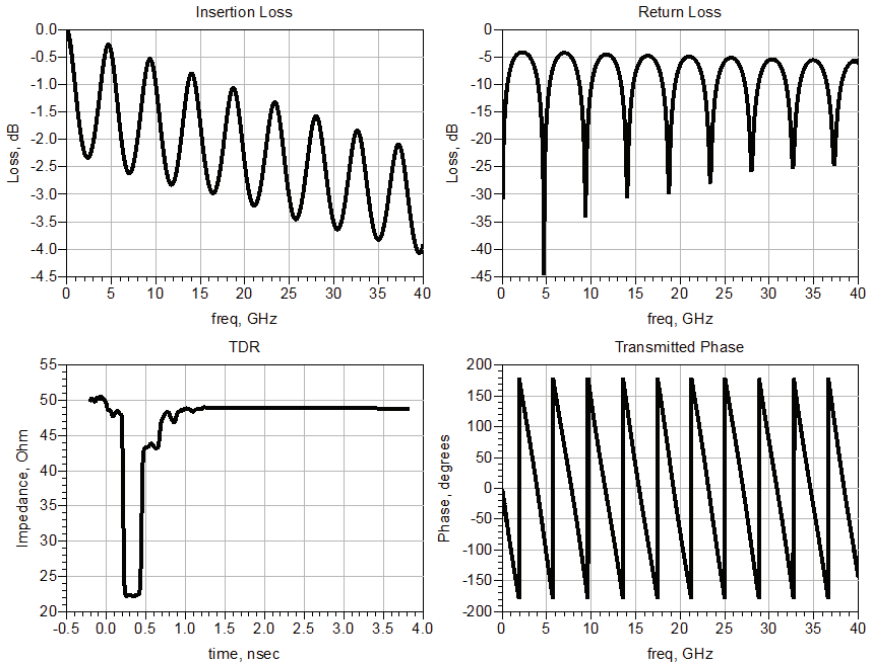

Figure 3: Example of the typical parameters used for measurement based simulation tuning.

This paper assumes that the test structure is made from segments of transmission line. Geometrically, a transmission line in a PCB is characterized by its cross section and length *L*. Figure 4 shows the two most commonly used transmission line types in high-speed digital PCBs: microstrip and stripline.

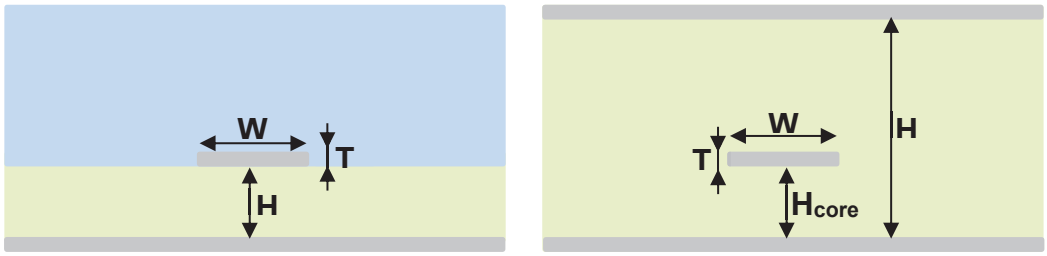

Figure 4: Cross-section of microstrip (left) and stripline (right).

It is desirable to take a look at some basic equations that define the electric behavior of a transmission line. The dielectric material surrounding the conductors can be characterized by the complex dielectric constant ε_r [5], where:

$$\boldsymbol{\varepsilon_r = \varepsilon' - j\varepsilon'' = \varepsilon'(1 - jtan\delta)} \quad (1)$$

ε' is commonly referred to as the dielectric constant (*Dk*) and *tanδ* describes the dielectric loss. As this paper is interested in the wideband material properties, $\varepsilon'$and *tanδ* cannot be represented as constants, but are frequency dependent. Note that ε' and ε'' are not independent, but both related by the causality enforcing Kramers-Kronig relation [5].

The propagation delay for a signal traveling along a transmission line of length *L* in a uniform dielectric is given in equation (2).

$$\boldsymbol{t_{pd} = \frac{L}{c_0}\sqrt{\varepsilon'}} \quad (2)$$

It is important to note that whatever the cross-section of the line looks like, its propagation delay is constant if the dielectric is uniform. This means that time or frequency information can easily be related to ε' if the length *L* of the line segment is known.

A microstrip trace is a typical example for a transmission line surrounded by two different dielectrics. In the case of the second *Dk* being air, then t_{pd} can be calculated using (2) by inserting the effective dielectric constant ε'_{eff} instead of ε'.

$$\varepsilon'_{eff} = \frac{\varepsilon'+1}{2} + \frac{\varepsilon'-1}{2}\frac{1}{\sqrt{1+12\left(\frac{H}{W}\right)}} \quad (3)$$

Equation (3) can be used when $\left(\frac{W}{H} \geq 1\right)$ and is presented in [6].

The impedance of a line is governed by its cross-section and the dielectric constant. Equations (3) and (4) are approximations for the impedance of symmetrical stripline [7] and microstrip [6] traces.

$$Z_{0,stripline} = \frac{60\Omega}{\sqrt{\varepsilon'}} \ln\left(\frac{2H+T}{0.8W+T}\right)\Omega \quad (4)$$

$$Z_{0,microstrip} = \frac{120\pi}{\sqrt{\varepsilon'_{eff}}\left(\frac{W}{H}+1.393+\frac{2}{3}\ln\left(\frac{W}{H}+1.444\right)\right)}\ \Omega \quad (5)$$

For a given ε, assuming the trace thickness T is negligible, the ratio of W and H determines the impedance of a line, and therefore the reflections in the time domain and resonances in the frequency domain. Having in mind that it is the ratio of W and H that determines the impedance, it becomes clear that an approach that uses two uniform lines with different lengths but identical cross sections can be used to find the dielectric constant and loss, but it will not be enough for verifying the dimensions of the cross-section. A simple solution is to combine two trace widths in one structure for extracting the additional cross section dimensions that are needed for EM simulation and for exploring as-fabricated manufacturing tolerances.

The Beatty Standard

The Beatty test structure is a simple option for meeting the challenge of correlating the simulation model parameters to the as-manufactured PCB test fixture parameters. The Beatty structure is sometimes referred to as a standard since it is often used to verify a measurement calibration by providing a known mismatch [2,4]. In the case of simulation it is used to verify the accuracy of the simulator. The idea is to create one or multiple impedance discontinuities that generate resonances in the insertion and return loss. Figure 5 shows a possible example of a Beatty structure.

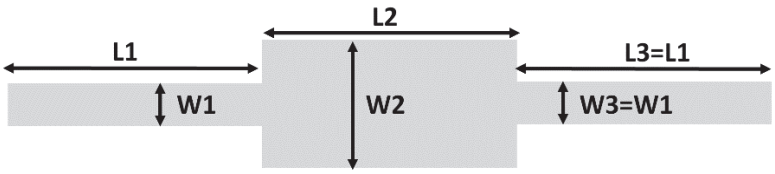

Figure 5: Possible implementation of a series resonance Beatty structure.

The critical feature of the Beatty standard shown in Figure 5 is the trace width transition. It needs to be as sharp as possible without any rounding. Figure 6 shows a microscope picture of a real implementation of a Beatty standard structure for a single-ended and differential application, showing the trace width transition. It is very hard to get a perfect corner but a very good approximation is possible with proper control of the PCB manufacturing process.

A typical implementation of the resonator would be symmetrical, so that $W1=W3$ and $L1=L3$. The left and right line segments are designed to match the system's characteristic impedance Z_0, the impedance of the middle segment is determined by selecting the trace width $W2=3\times W1$. The choice of $W2=3\times W1$ simplifies the layout, provides roughly a 50% step change in impedance for Z_0=50 Ω, and minimizes the edge effects of the Beatty section.

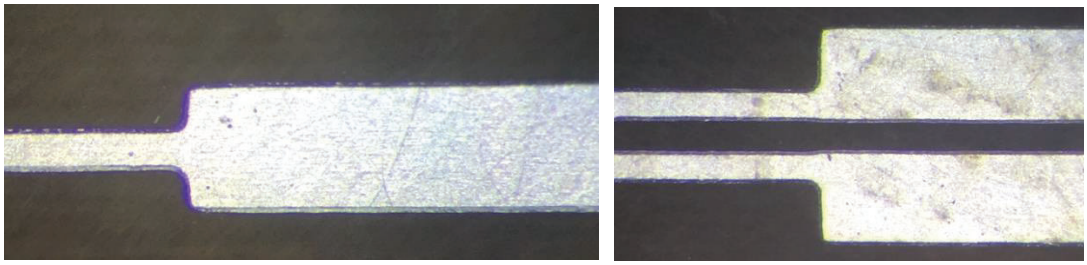

Figure 6: Picture of a Beatty standard single-ended and differential microstrip implementation with silver plating.

Figure 7 shows a comparison of the simulation results of a stripline trace and a Beatty standard. The design parameters are given in Table 1. The stripline trace used for comparison is modeled with the same substrate parameters, a width $W=W1=150$ µm and a length of 55 mm. The impedance variation of the Beatty standard clearly shows up as a resonance in the frequency domain and a step change in the time domain. In the case of the phase vs. frequency they are almost the same for these equal length structures. To emphasize these small differences the phase plot in Figure 7 uses the difference in the unwrapped phase.

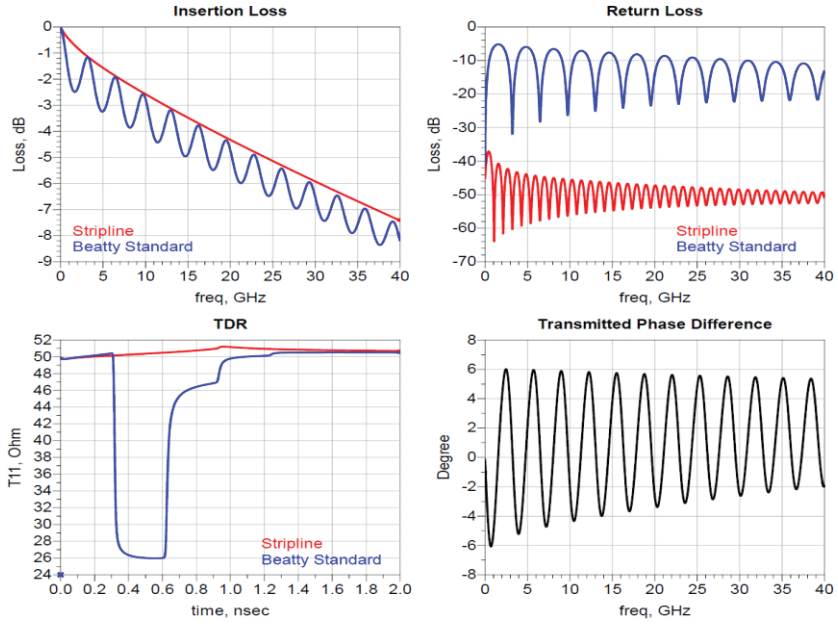

Figure 7: Comparison of four characteristic plots for a 55 mm long 50 Ω stripline trace (blue) and a stripline Beatty resonator (red). Insertion loss, return loss and TDR of the Beatty resonator show much more distinctive features then those of the simple stripline. The phase of both is almost the same.

Table 1: Stripline Beatty standard design parameters

$W1=W3$	$W2$	$L1=L3$	$L2$	H_{core}	H	ε'	$tan\delta$	T
150 µm	450 µm	15 mm	25mm	127 µm	353 µm	3.41	0.008	17 µm

One can derive a number of interesting properties of the Beatty standard from the comparison of the two plots. Looking at the magnitude plots, both insertion loss and return loss show resonance patterns, caused by multiple reflections at the discontinuities. The distance Δf between two neighboring minima or maxima can be calculated by

$$\Delta f = \frac{1}{2t_{pd2}} \quad (6)$$

Where t_{pd2} is the propagation delay of the middle segment. A quick initial estimation of ε' is also possible:

$$\varepsilon' = \left(\frac{c_0}{2\Delta f L_2} \right)^2 \quad (7)$$

The phase of a simple line grows almost linear as frequency increases (the decrease of ε' towards higher frequencies in lossy materials makes the phase change slightly slower as frequency increases). Seen over the whole frequency range, the insertion phase of the Beatty standard behaves the same as that of a uniform line, however, there is a slight ripple superimposed on the phase.

In the insertion loss plot, the curve of the stripline seems to define the upper boundary for the insertion loss of the Beatty standard. However, the maxima in the insertion loss of the Beatty standard never touch the curve of the stripline. This is because some of the energy rattles around between the discontinuities until it is completely dissipated, never making it out through one of the ports again. The height of the initial step in the TDR gives an indication about the relation of *W2* and *W1*.

In the example given above, the impedance of the narrow line segments is very well matched to the port impedance Z_0 of 50 Ω. In this case, there are almost no reflections at the ports and the characteristic patterns are well developed. If for example the line width was manufactured smaller than desired, causing the narrow sections' impedance to be significantly different from 50 Ω, additional reflections occur and disturb the classic series Beatty ¼ wavelength resonance pattern. This is shown in Figure 8, where the impedance of the narrow trace (*W1* and *W3*) was changed to 55 Ω.

The effect is likely to be encountered with measured S-Parameter data. There is nothing wrong with the measured data, but the additional resonances can make it harder to understand what is going on. Simply adjusting the port impedance to equal that of the Fixture Zo calibration reference plane at the W1 input and output line segments removes the effect, without changing the measured data, making it easier to interpret.

This example also shows one important property of the stripline Beatty standard: As the propagation delay in stripline only depends on ε'. The additional resonances cause some local ripple in the phase difference plot. This makes the base material properties unique in that they are the only parameters that affect the overall or integrated phase difference in case of a perfect stripline implementation.

Microstrip Beatty resonators lack this property, because the propagation delay in microstrip is determined by the effective dielectric constant ε'_{eff}, which is a function of the microstrip's geometry. The effect is demonstrated in Figure 9, where the width of the middle segment of a microstrip Beatty standard is changed by +/-10% causing a delta change in the phase.

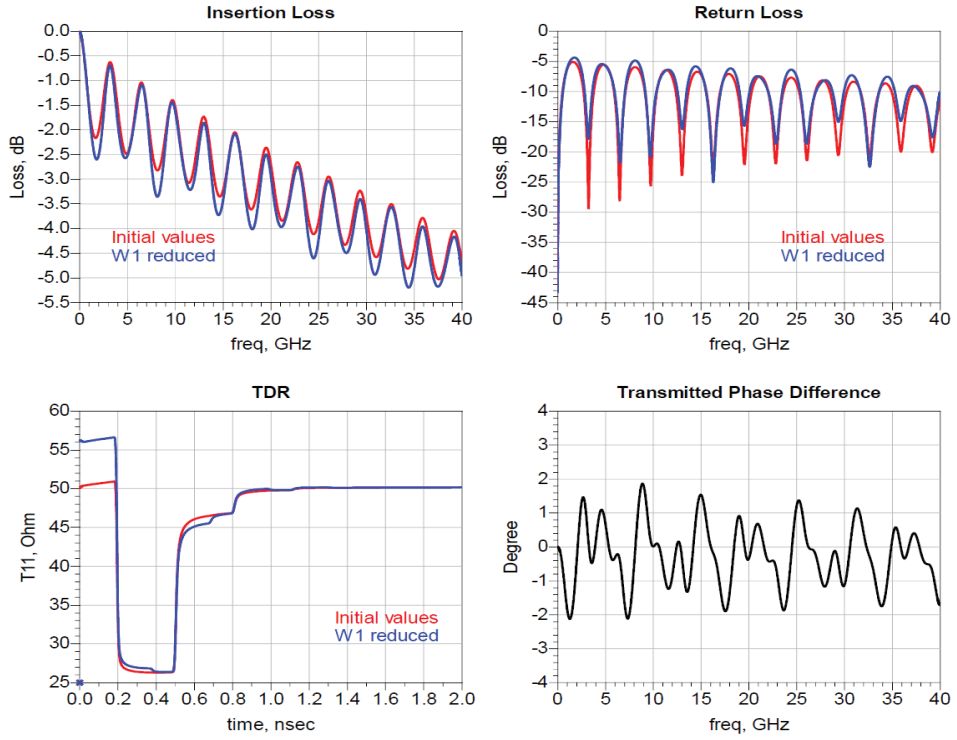

Figure 8: Simulated Beatty resonator with mismatched narrow trace segments (blue). The Beatty standard with matched launch traces from Figure 7 is added in red for comparison.

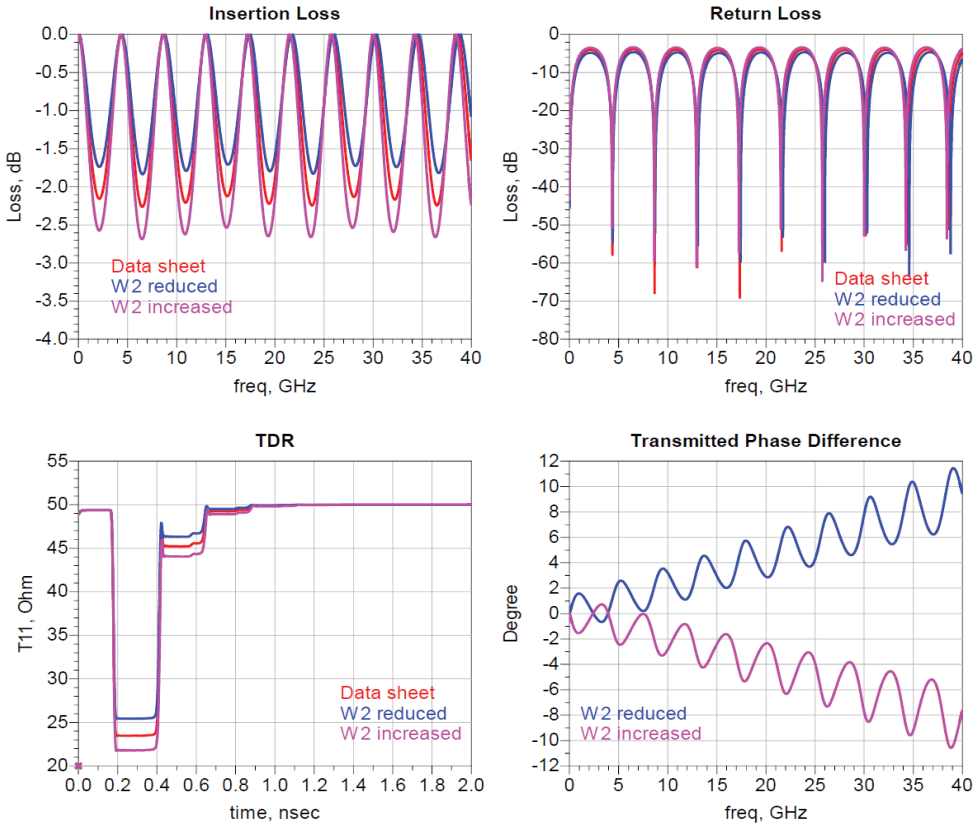

Figure 9: Changing cross-section dimensions in a microstrip Beatty standard will also cause the effective dielectric constant to change slightly. The effects are moving minima and maxima in the insertion and return loss and a change of the overall phase. A loss free model is used here to make it easier to see the effect.

Connector De-Embedding

For accurate measurement of a Beatty standard structure it is critical to de-embed the coaxial connector to planar PCB fixture used to measure the test structure.

Among the different available techniques, the simple twice the test fixture through path, aka 2x-Thru, method is rapidly replacing the traditional TRL method for PCB structures. This is because of the accurate results that can be obtained with this 2-Tier calibration method [9,10] despite the simplicity. There are multiple software packages available in the market, and in the case of this paper we used Keysight's Physical Layer Test Sytem (PLTS) Automatic Fixture Removal (AFR).

As shown in Figure 10, in addition to the resonant Beatty test structure itself, only one additional 2x-Thru calibration structure is required on the PCB.

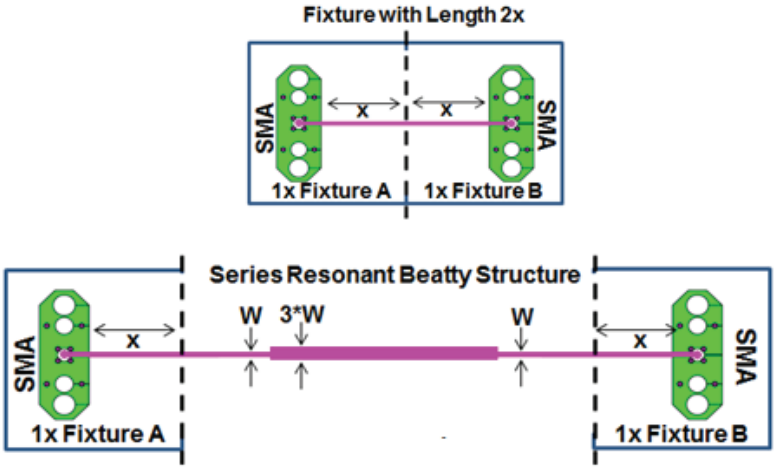

Figure 10: Connector de-embedding from a Beatty structure using a 2x-Thru de-embedding structure.

For a successful de-embedding it is critical that the variations in the connector transition and trace impedance between the 2x-Thru structure and the Beatty standard be kept to the minimum. This is especially important if the Beatty standard is manufactured in stripline technology where the transition to an inner layer adds manufacturing variations. The connector breakout may use backdrilled vias to avoid via stub resonances and extend the usable bandwidth of the structure. The 2x-Thru method assumes the fixture launch towards the resonator is identical to one half of the 2x-Thru structure. Therefore before the de-embedding, it is recommended to check that the impedance of the signal trace and connector transitions including any backdrilled vias are sufficiently similar. This can be easily performed with a TDR using a fast rise time or by translating the measured S-parameters into the time domain.

A Step-by-Step Simulation Model Tuning Process

In the previous Measurement Based Simulation Tuning section, three classes of parameters were identified for adjustment. These are material properties, substrate dimensions, and conductor dimensions. The large number of tuning variables requires a systematic step by step approach to narrow down the measurement based model to those parameter values that fit with in manufacturing tolerances and provide a realistic model for predicting the performance of the PCB. Appendix A provides a reference set of plots that show in detail the relative sensitivities that each of these parameters have on the time and frequency domain performance plots of the Beatty standard for stripline and microstrip designs.

The material parameters influence all of the important performance characteristics of the Beatty standard. They affect the propagation delay, impedance and loss in the structure. Substrate dimensions affect the impedance of the trace segments and will also influence ε'_{eff} in the case of microstrip. The conductor dimensions mainly contribute to the impedance of a line segment. In addition, there is a small effect on the loss (narrower conductors cause higher copper loss) and in the ε'_{eff} case of microstrip routing.

The optimization strategy presented here makes three assumptions:

- The dielectric constant ε' has a major effect on all characteristic plots. A good estimate for ε' should be obtained before attempting to tune any of the other parameters. In the case of stripline, a simple hand calculation can be done with Equation 2.
- Etching process variations affect both wide and narrow trace segments the same way. If the fabricated *W1* is 20 µm smaller than expected, it is assumed that *W2* will be smaller by the same amount.
- The signature of an etch width change is substantially different from that of a change in the dielectric height, so that both effects can be separated.

Tuning the design parameters of the Beatty standard model is a three step process as described in Figure 11. For the work presented in this paper, we used the optimizer contained in Keysight Technologies ADS software package to implement the optimization process. Figure 12 shows a picture of the tuning setup for one of the examples shown later in this paper. In each step one or more goal equations are given to the optimizer to determine the matching between measurement and model. Depending on the properties we try to match, different design parameters are varied. A random optimization algorithm is used to prevent the optimizer from getting trapped by local minima.

Based on our finding that the structure is most sensitive to ε' changes, we propose to tune this base material parameter first. The first step is also used to make slight adjustments to the launch trace lengths to compensate for small errors from manufacturing and fixture removal. The length of the middle W2 segment is assumed fixed by design, so care must be taken that there are no deviations of the intended length during the board layout.

The second step is used to adjust the dimensions of the trace cross-section. Optimizing in the time domain using the TDR (T_{11}) allows one to tune on both the narrow input trace impedance and the wider Beatty section. Adjusting the cross section parameters to get the correct impedance variations vs. time.

In a final step, the transmitted time domain T_{21} signals are compared to make sure a good correlation with the measured data was obtained. If the correlation is not good enough, then it is necessary to go back to the start of the tuning process and modify for example the initial conditions or the allowed tuning range. Although T_{21} it is relatively insensitive to design parameter changes, the major interest in high-speed digital design is in the time domain transmitted waveforms.

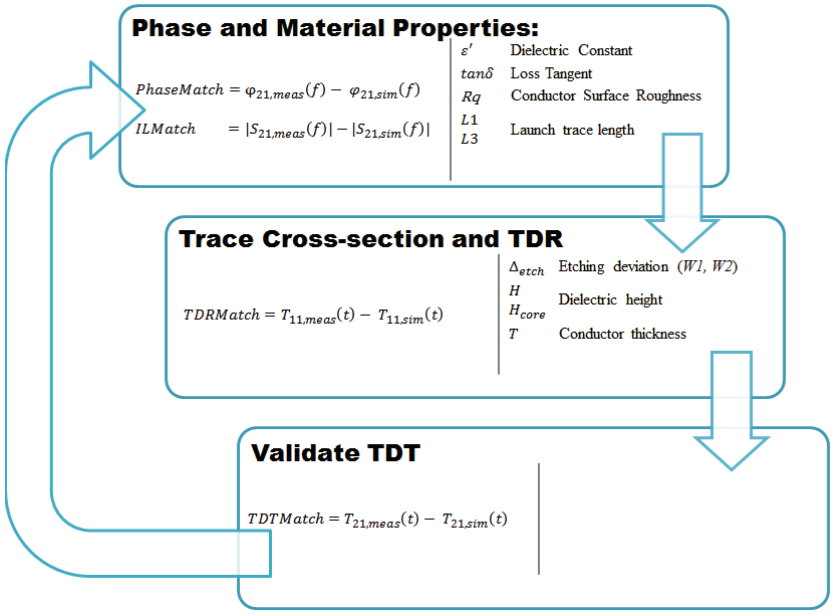

Figure 11: Optimization process to match the simulation model to the Beatty standard measurement results. The left side of the boxes contain the tuning goals, the right side variables that are adjusted in each step.

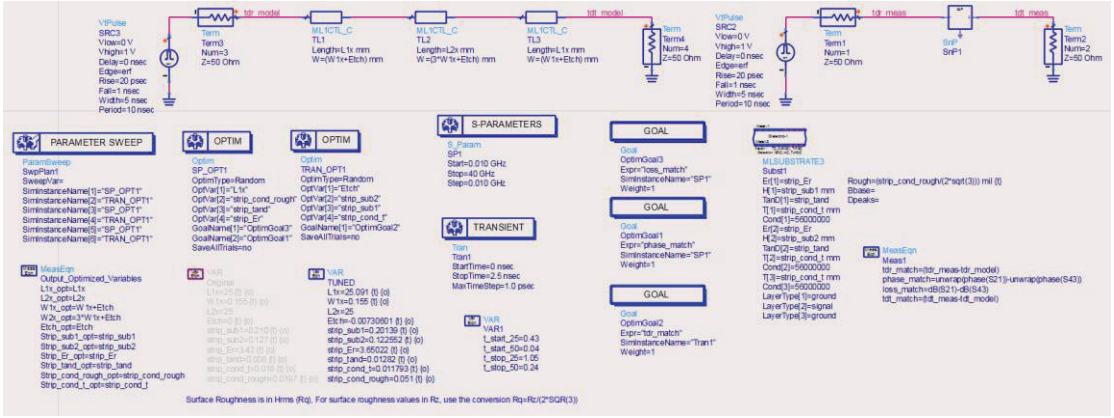

Figure 12: Example of the tuning process implementation in Keysight Technologies ADS.

It is important to note that depending on the simulation tools or the simulation models, additonal parameters might be available for tuning (e.g. bulk conductivity), but our approach was to concentrate on the critical parameters. This keeps the tuning

methodology as simple and generic as possible. Another important simplification on the proposed simulation model is that a rectangular shape is used for the signal trace. We know that manufactured PCB signal traces have a trapezoidal shape but this additional complexity can significantly slow down a 3D-EM simulator vs a simple rectangular shape, and some models may not include this feature.

After de-embedding and before starting the optimization procedure, the quality of the measured S-parameters should be checked. If necessary, the simulation bandwidth should be limited to not include de-embedding artifacts. One can adjust the port impedance used in the simulation to prevent additional resonances in the plot. Equation (7) may be helpful to set a start value for ε' .

Once the tuning process is completed, it is necessary to compare the new design parameters against the tolerances specified by the PCB manufacturer and base material vendor. There is no guarantee that the random optimizer process finishes with realistic results and some manual adjustments or modification to realistic min/max values may be necessary.

Examples

The following sections present different examples of the implementation and usage of the Beatty standard for EM model tuning in the cases of a stripline, microstrip and differential microstrip. In all examples the connector de-embedding was done using the 2x-Thru approach described in the previous section using the AFR de-embedding software that is part of the Keysight Technologies PLTS software package. For the EM tuning we used the Keysight Technologies ADS simulation software.

We also performed cross-sections of the test-coupon PCBs used in the examples. Unfortunately due to time constrains it was not always possible to do the cross-sections on the exact test coupon PCBs used for the measurements but rather on an identical test coupon that was manufactured on the exact same panel. This of course does not guarantee the measured parameters will be identical but they should be closer than if PCBs from different panels and/or lots were used.

Stripline Single-Ended Beatty Standard

Figure 13 shows a picture of a printed circuit board that contains a single-ended stripline Beatty structure and a 2x-Thru calibration structure. The stripline was designed with a width of 155 µm in an Elite Materials EM-828 dielectric. Both prepreg and core have quite high resin content (70%) so the provided dielectric constant value was 3.41 and the loss tangent was 0.008. Surface roughness (*Rz*) was specified at 1.5 µm for the shiny side and 2.5 µm for the rough side, we used an average of 2 µm for our simulations and converted to *Rq* [8]. The stripline design geometry is shown in Figure 14. The 2x-Thru de-embedding structure had a total length of 1.6 cm while the Beatty standard had a geometry composed of 3.4 cm with the standard trace width on both sides and 2.5 cm with 3x trace width. This means that the de-embedded Beatty standard is composed of a standard trace width length of 2.5 cm on both sides and a 3x trace width length of 2.5 cm as shown in Figure 14.

Figure 13: Stripline Beatty standard example test PCB.

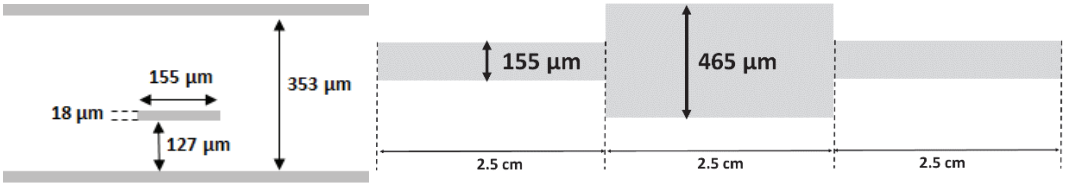

Figure 14: Stripline cross section design geometry (left) and de-embedded single-ended stripline Beatty standard structure (right).

Figure 15 shows the measured insertion and return loss for the 2x-Thru test coupon and the Beatty standard test coupon. Figure 15 also shows the computed impedance profile for the 2x-Thru and Beatty structures showing that the Beatty standard impedance error is below 5% for the input W1 segment. It also shows that the connector transition (which includes a backdrilled via) is practically identical between the 2x-Thru and Beatty structures as required for a successful de-embedding. Figure 16 shows the measured and de-embedded insertion and return loss from the Beatty standard.

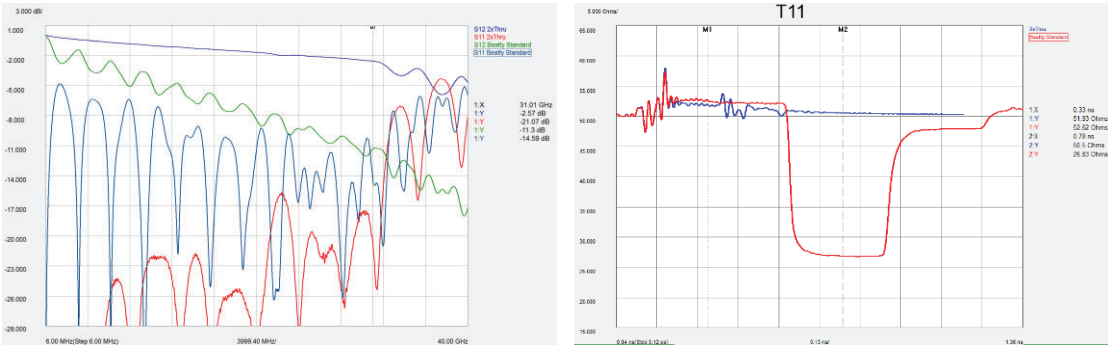

Figure 15: Measured insertion and return loss of the 2x-Thru and Beatty test structures and computed TDR of the 2x-Thru and Beatty test structures.

Figure 17 shows a comparison of the de-embedded measured data and the results from a simulation model using the design and material specification parameters performed in EESoft ADS. As expected the simulation results differ from the measurement data requiring tuning of the simulation model.

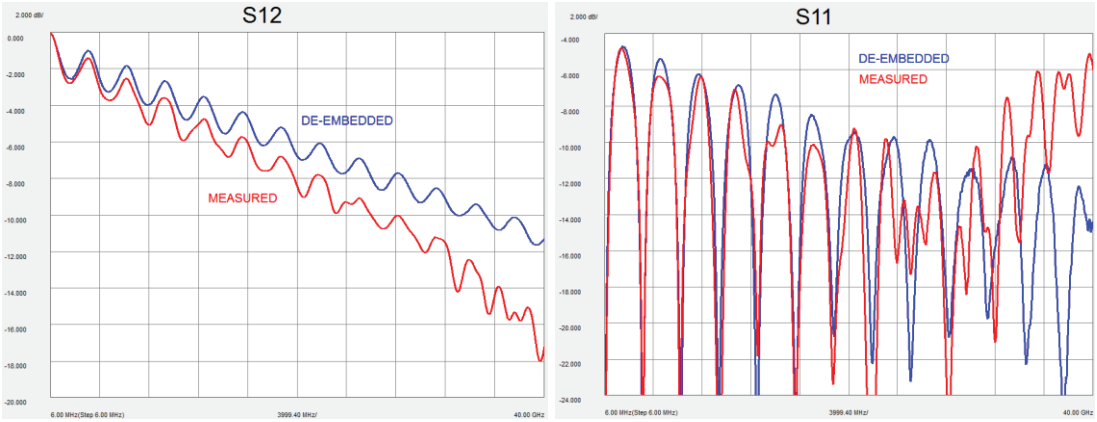

Figure 16: Measured and de-embedded insertion and return loss of the single-ended stripline Beatty standard.

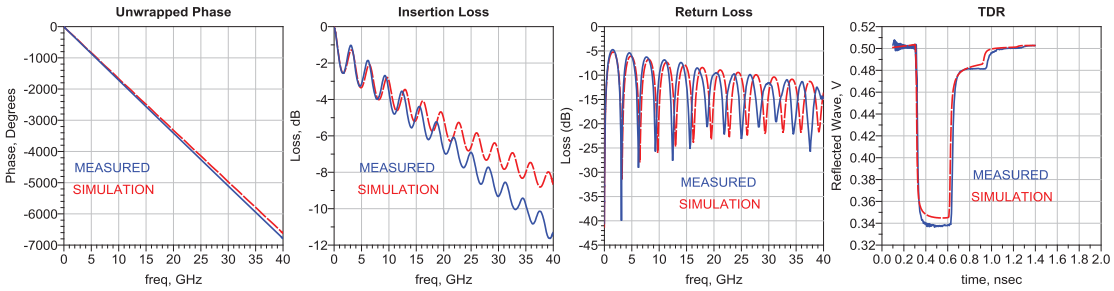

Figure 17: Comparison between the de-embedded measured data and a simulation model based on the design parameters and material specifications.

The simulation tuning procedure described in the previous section was applied to the measured data resulting in the optimized parameters shown in Figure 18 and Figure 19.

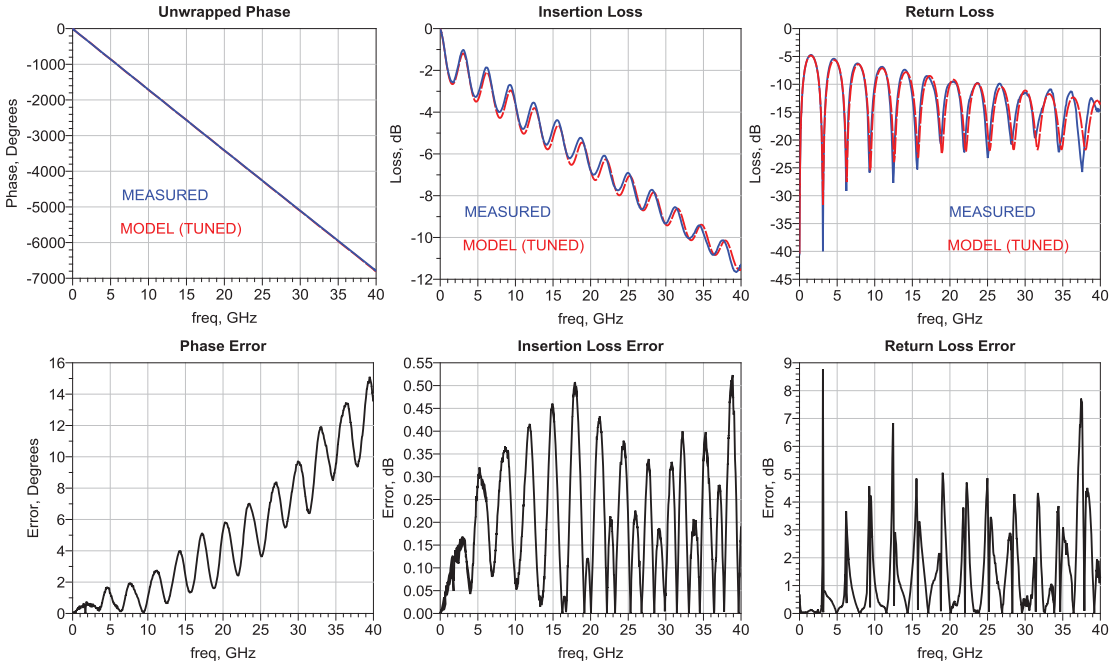

Figure 18: Comparison of the tuning results with the measured data for the unwrapped phase, insertion loss and return loss.

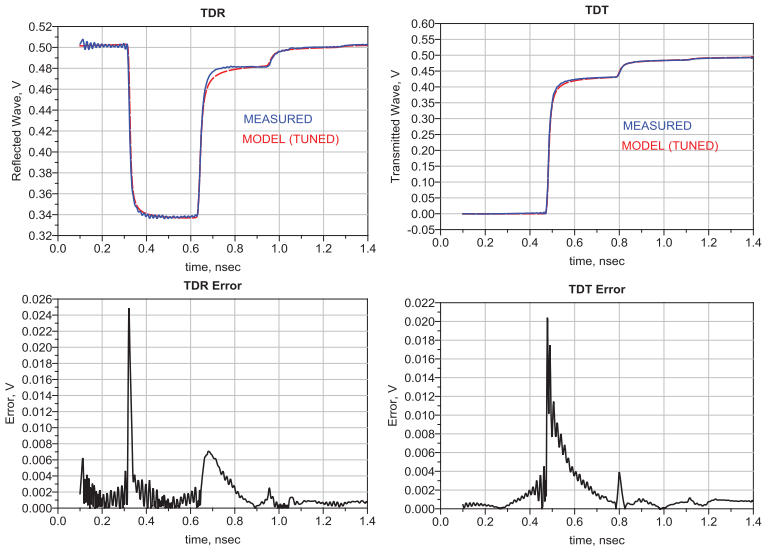

Figure 19: Comparison of the tuning results with the measured data for the TDR and TDT.

Table 2 shows a comparison of the original design parameters, the parameters obtained from the model tuning process. It also includes the cross-section results shown in Figure 20 for the Beatty standard using a similar structure manufactured on the same PCB panel.

Table 2: Original design parameters and tuning results for the stripline example (variables described in Figure 4 and Figure 5). Surface roughness (Rz) was converted to RMS (Rq) using Rq=Rz/3.4.

Parameter	Design	Model Tuning	Cross-Section Coupon
W1	155 µm	141 µm	147 top, 157 µm bottom
W2	465 µm	451 µm	472 top, 483 µm bottom
W3	155 µm	141 µm	
L1,L3	2.5 cm	2.4943 cm	
L2	2.5 cm	2.5 cm	
Dielectric Constant	3.42	3.688	
Loss Tangent (1 GHz)	0.008	0.014	
Surface Roughness (*Rq*)	0.588 µm	0.305 µm	
H	353 µm	345 µm	362 µm
H_{core}	127 µm	126 µm	131 µm
T	18 µm	16 µm	17 µm

Two parameters that are difficult to directly correlate to their "real" values are the loss tangent and surface roughness. Surface roughness is especially problematic since a multitude of models are available to describe its influence [11]. The proposed tuning process in its current form does not include special measures to accurately separate conductor and dielectric loss. A procedure to do this has been presented in [12] and could be added to a more advanced tuning process. In this case it is best to look at the loss tangent and surface roughness as a parameter pair that is tuned based on the EM simulator model but the individual values might not necessarily represent "real" material values.

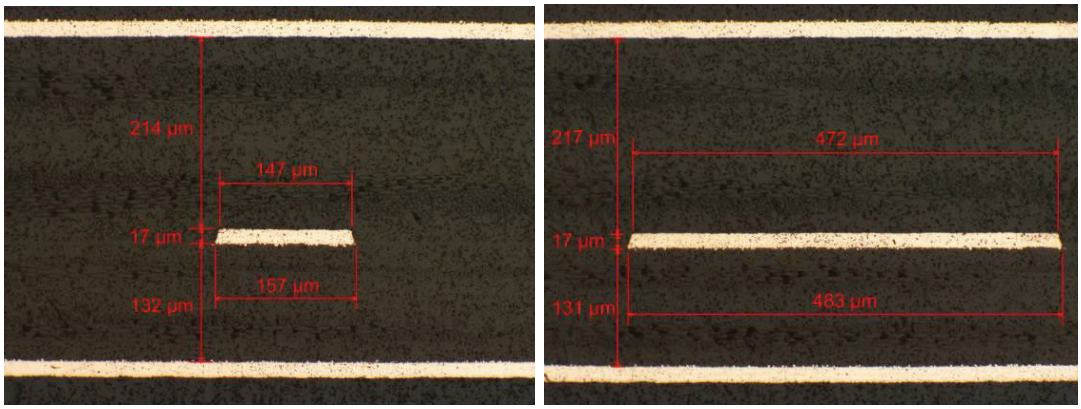

Figure 20: Cross-sections of the stripline Beatty standard PCB test board (different PCB from the one used for the measurements).

Microstrip Single-Ended Beatty Standard

Figure 21 shows a picture of a single-ended Beatty structure and the corresponding 2x-Thru connector de-embedding structure. The microstrip was designed with a width of 11.6 mil in a Nelco 4000-13 SI dielectric with a silver plating. The surface roughness specification of the used copper foil is 4.44 µm (Rz) on the matte side which we converted to Rq. The design dielectric constant was 3.2 and the loss tangent from the spec sheet is 0.008. Figure 22 shows the microstrip design geometry. The 2x-Thru de-embedding structure had a total length of 6 cm while the Beatty standard structure has a geometry composed of 4.5 cm using the standard trace width on each side and 2 cm with 3x trace width. This means that the de-embedded Beatty standard is composed of a standard trace width length of 1.5 cm and a 3x trace width length of 2 cm as shown in Figure 22.

Figure 23 shows the measured insertion and return loss for the 2xThru test coupon and the Beatty standard test coupon. Figure 23 also shows the computed impedance profile showing that the Beatty standard impedance is slightly offset by 2 ohms and also that there is a very good correlation on the impedance and connector transition between the 2x-Thru and the Beatty structure. Figure 24 shows the de-embedded insertion and return loss from the Beatty standard.

Figure 21: Single-ended microstrip Beatty standard example.

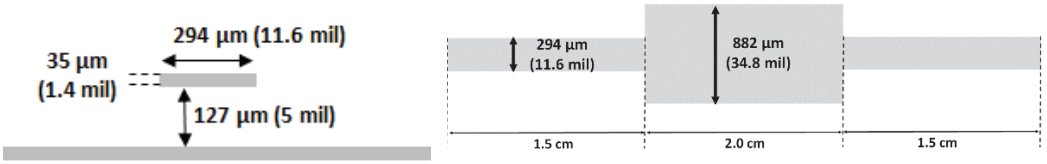

Figure 22: Microstrip design geometry (left) and de-embedded single-ended microstrip Beatty standard structure (right).

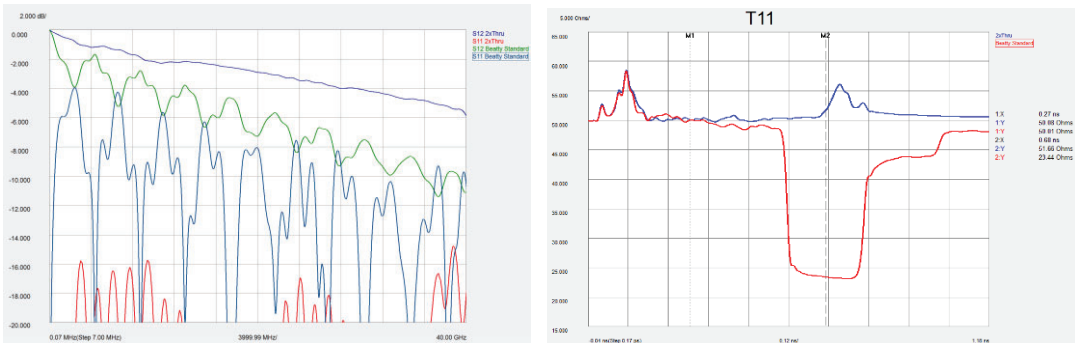

Figure 23: Measured insertion loss and return loss of the 2x-Thru and Beatty test structures and computed TDR of the single-ended microstrip 2x-Thru and Beatty test coupon.

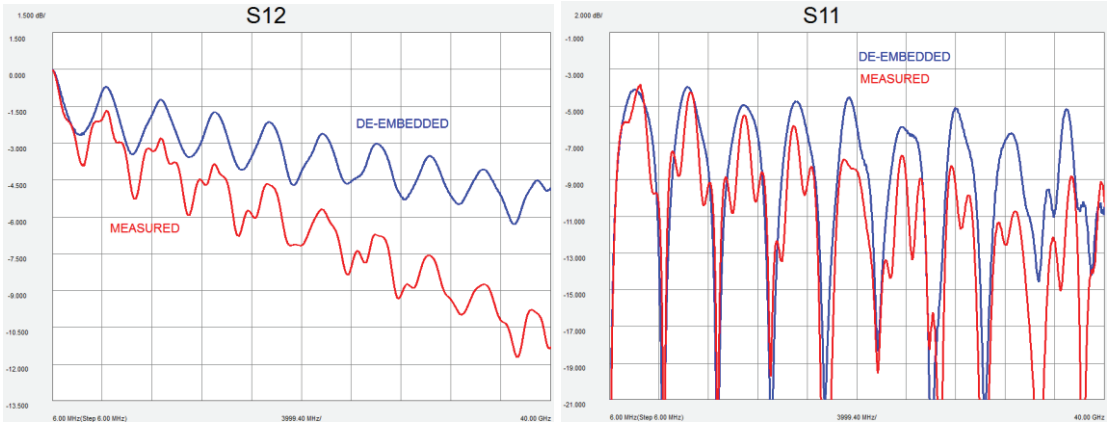

Figure 24: Measured and de-embedded insertion and return loss of the single-ended microstrip Beatty standard.

Figure 25 shows a comparison of the de-embedded measured data and the results from a simulation model using the design and material specification parameters performed in EESoft ADS. As expected the simulation results differ from the measurement data requiring tuning of the simulation model.

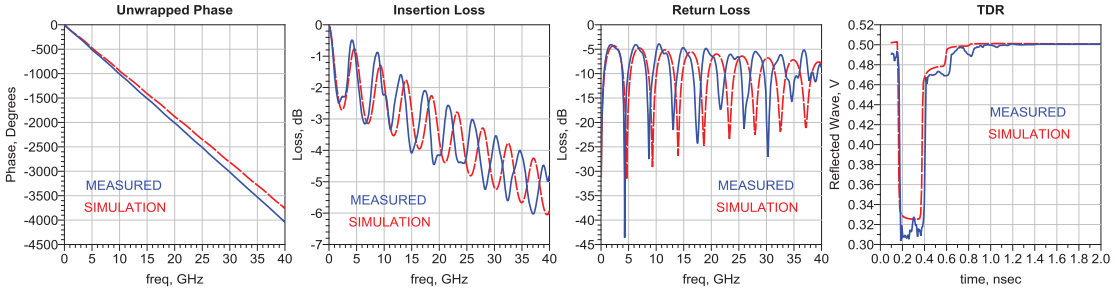

Figure 25: Comparison between the de-embedded measured data and a simulation model based on the design parameters and material specifications.

The simulation tuning procedure described in the previous section was applied to the measured data resulting in the optimized parameters shown in Figure 26 and Figure 27.

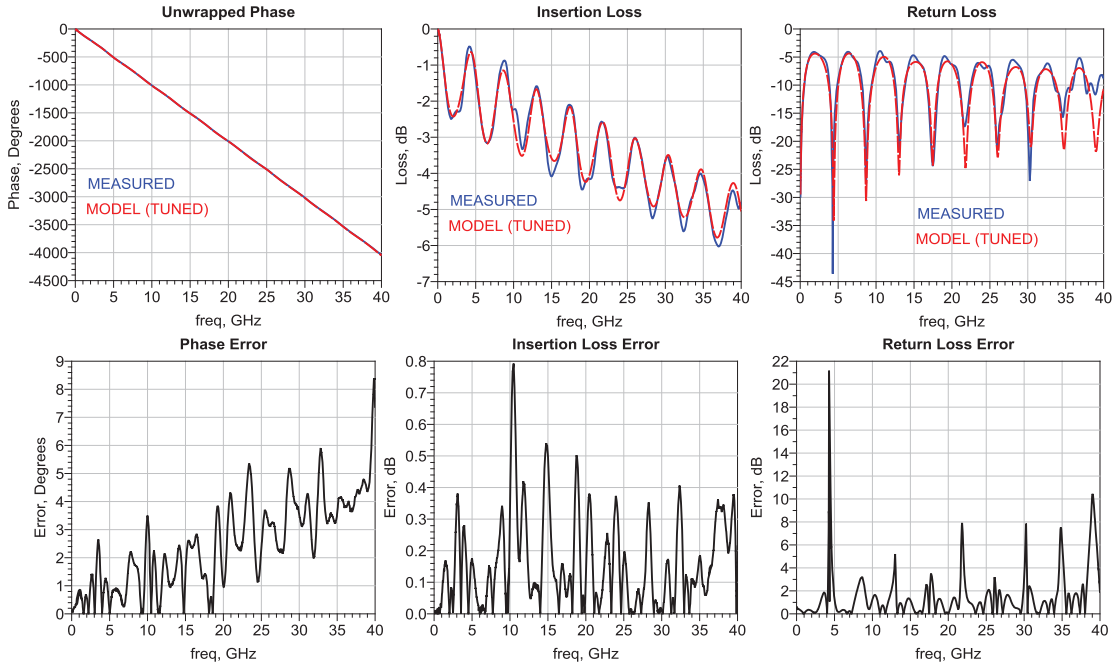

Figure 26: Comparison of the tuning results with the measured data for the unwrapped phase, insertion loss and return loss.

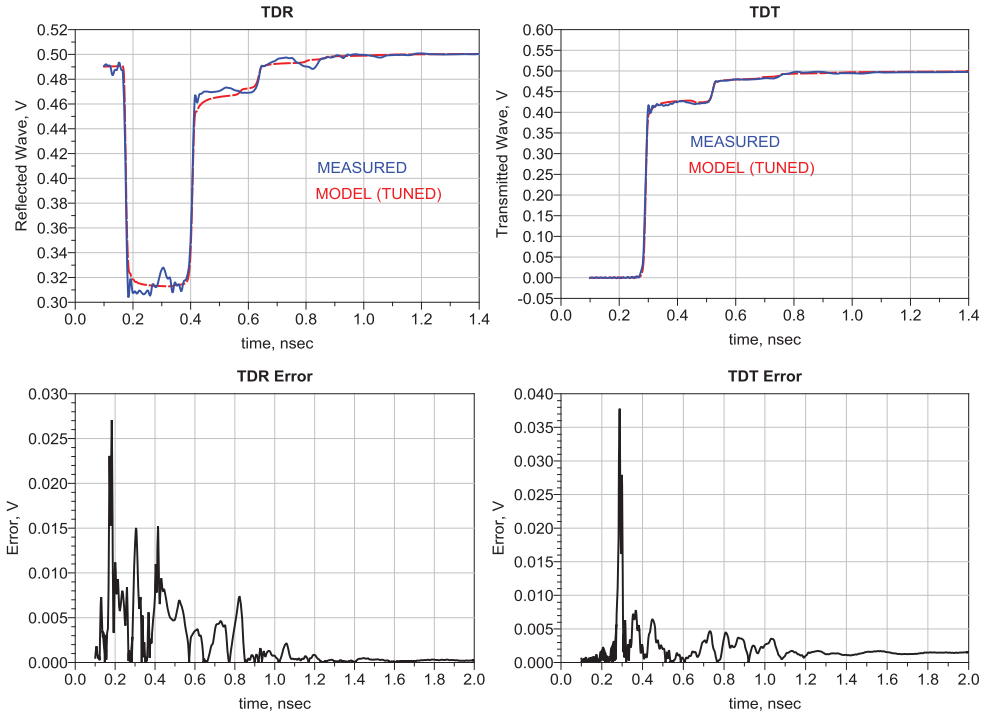

Figure 27: Comparison of the tuning results with the measured data for the TDR and TDT.

Table 3 shows a comparison of the original design parameters and the parameters obtained from the model tuning process. It also includes the cross-section results shown in Figure 28 for the Beatty standard but in a different PCB structure manufactured on the same panel. Only the trace width corresponding to a 50 Ohm trace is shown.

Table 3: Original design parameters and tuning results for the microstrip example (variables described in Figure 4 and Figure 5).

Parameter	Design	Model Tuning	Cross-Section Coupon
W1	294 µm	301 µm	268.85 µm (top), 308.86 µm (bottom)
W2	882 µm	889 µm	
W3	294 µm	300 µm	
L1,L3	1.5 cm	1.5152 cm	
L2	2 cm	2.0 cm	
Dielectric Constant	3.2	3.495	
Loss Tangent (10 GHz)	0.008	0.010	
Surface Roughness (*Rq*)	1.3 µm	0.6858 µm	
H	127 µm	133 µm	129.48 µm
T	35 µm	27 µm	25.98 µm

Figure 28 shows the cross-section from a different board in the same panel as the measured Beatty standard test coupon. Only the trace width corresponding to a 50 Ohm trace is shown.

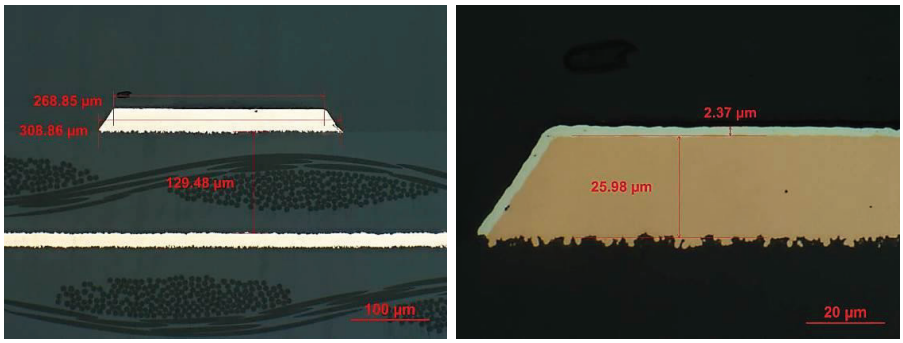

Figure 28: Cross-sections of the microstrip Beatty standard PCB test board (different PCB from the one used for the measurements).

Microstrip Differential Beatty Standard

Figure 29 shows a picture of a differential Beatty structure and the corresponding 2x-Thru connector de-embedding structure. The differential microstrip was designed with a trace width of 10 mil and a 10 mil separation between both traces to achieve a 100 Ohm differential impedance. The dielectric material was Nelco 4000-13 SI and silver plating was used on the microstrip. The surface roughness specification of the used copper foil is 4.44 µm (Rz) on the PCB side which we converted to Rq. The design dielectric constant was 3.2 and the loss tangent from the spec sheet is 0.008. Figure 30 shows the differential microstrip design geometry. The 2x-Thru de-embedding structure has a total length of 6 cm while the Beatty standard had a geometry composed of 4.5 cm with the standard trace width on each side and 2 cm with 3x trace width. This means that the de-embedded Beatty standard is compose of a standard trace width length of 1.5 cm on each side and a 3x trace width length of 2 cm as shown in Figure 30.

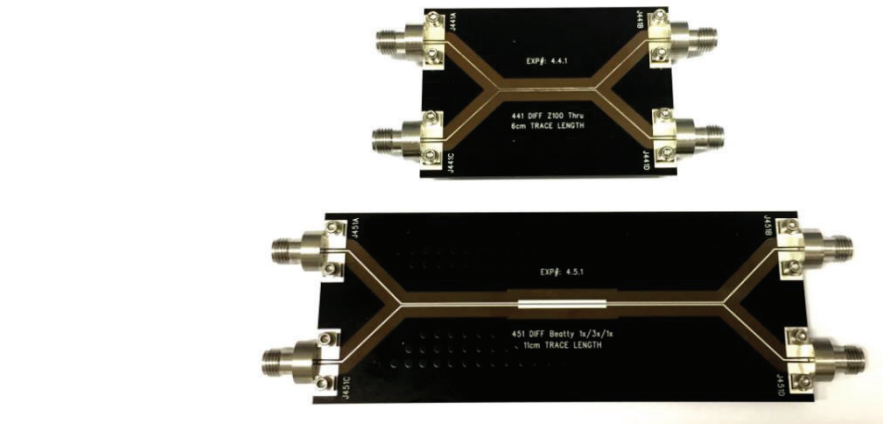

Figure 29: Differential Beatty standard example.

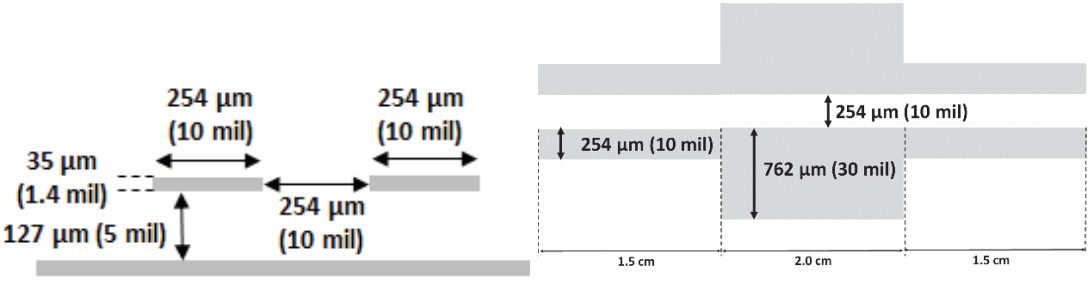

Figure 30: Differential microstrip cross section design geometry (left) and de-embedded differential microstrip Beatty standard structure (right).

Figure 31 shows the measured differential insertion and return loss. Figure 31 also shows the computed impedance profile of the differential 2x-Thru and Beatty structures showing not only that the Beatty standard impedance is as expected but also that there is an excellent correlation on the impedance and connector transition between the 2 structures.

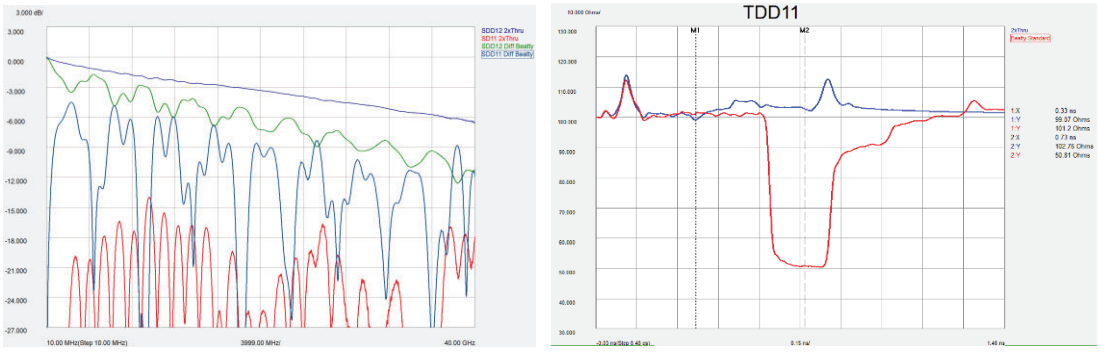

Figure 31: Measured insertion and return loss of the 2x-Thru and Beatty test structures and computed differential TDR of the 2x-Thru and Beatty test coupon.

Figure 32 shows the measured and de-embedded insertion and return loss from the microstrip differential Beatty standard. Figure 33 shows a comparison of the de-embedded measured data and the results from a simulation model using the design and material specification parameters performed in EESoft ADS. As expected the simulation results differ from the measurement data requiring tuning of the simulation model.

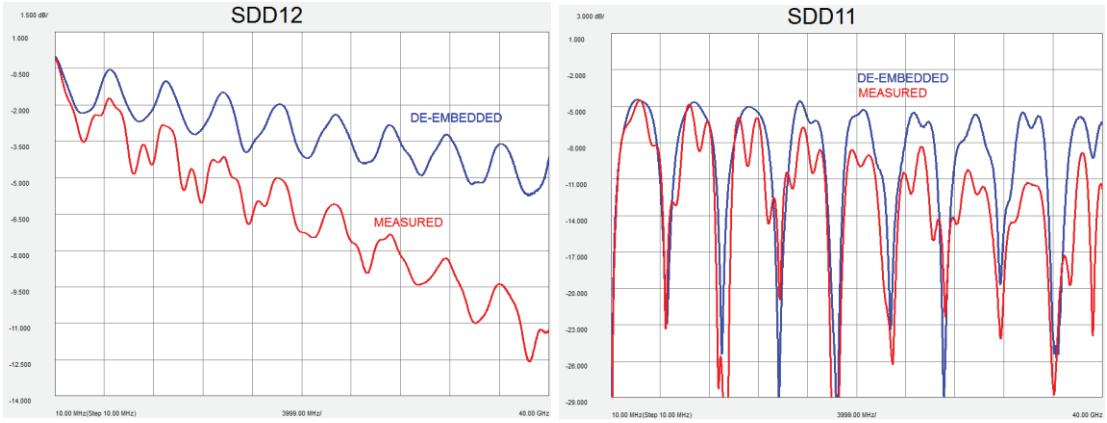

Figure 32: Measured and de-embedded insertion and return loss of the differential microstrip Beatty test structure.

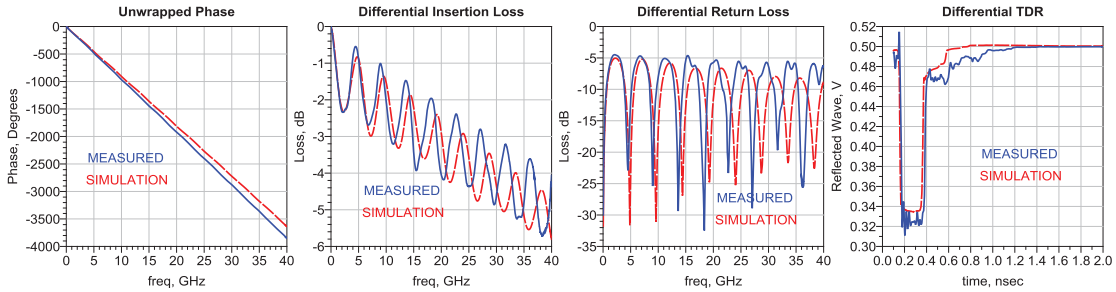

Figure 33: Comparison between the de-embedded measured data and a simulation model based on the design parameters and material specifications.

The simulation tuning procedure described in the previous section was applied to the measured data resulting in the optimized parameters shown in Figure 34 and Figure 35.

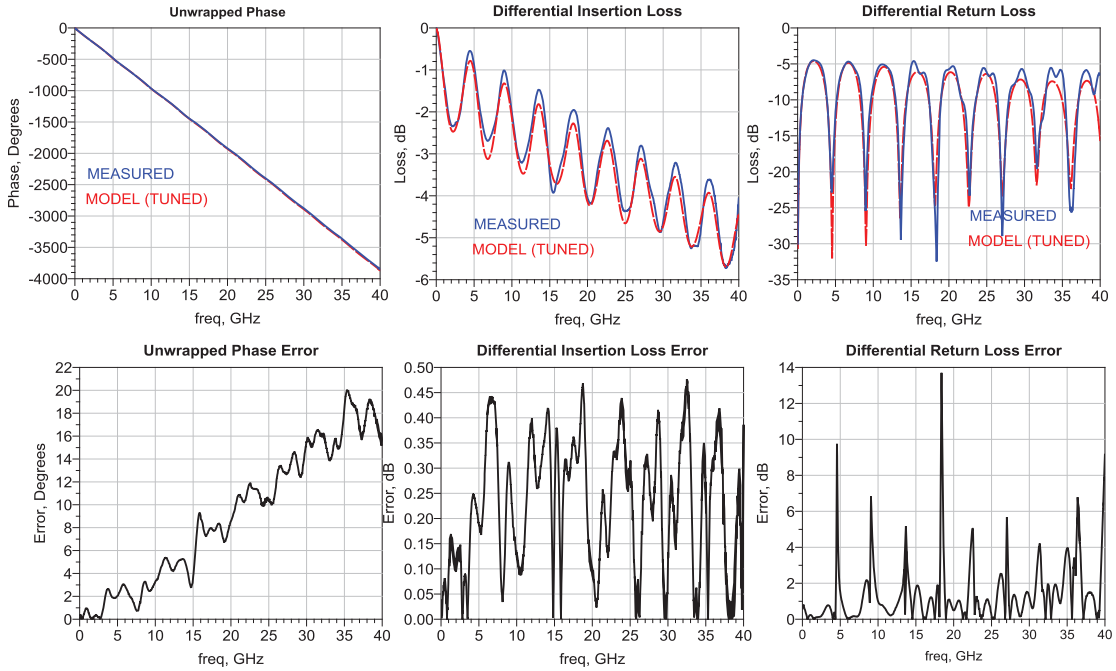

Figure 34: Comparison of the tuning results with the measured data for the unwrapped phase, insertion loss and return loss.

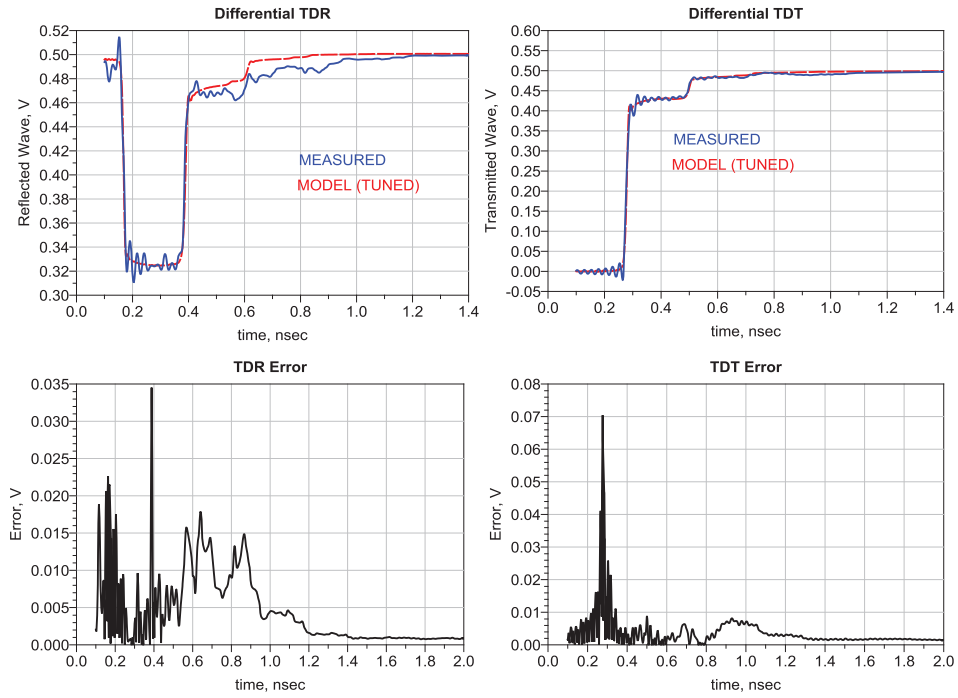

Figure 35: Comparison of the tuning results with the measured data for the TDR and TDT.

Table 4 shows a comparison of the original design parameters and the obtained parameters from the model tuning process. Figure 36 shows some cross-sections of the PCB test coupon.

Table 4: Original design parameters and tuning results for the differential microstrip example (variables described in Figure 30).

Parameter	**Design**	**Model Tuning**	**Cross-Section**
W1	254 µm	244 µm	264 top, 192 µm bottom
W2	508 µm	752 µm	795 top, 732 µm bottom
W3	254 µm	244 µm	264 top, 192 µm bottom
Gap	254 µm	303 µm	244 top, 318 µm bottom
L1,L3	1.5 cm	1.5101 cm	
L2	2 cm	2 cm	
Dielectric Constant	3.2	3.4	
Loss Tangent (10 GHz)	0.008	0.009	
Surface Roughness (Rq)	1.3 µm	1.143 µm	
H	127 µm	125 µm	
T	35 µm	25 µm	27.3 µm

One important discussion is if a differential Beatty standard structure provides additional information or accuracy compared to a single-ended Beatty structure for model tuning. We do not have a conclusion since the answer might be dependent of the PCB design strategy (e.g. is a tightly or weakly coupled differential line used). This is a topic that requires more future work.

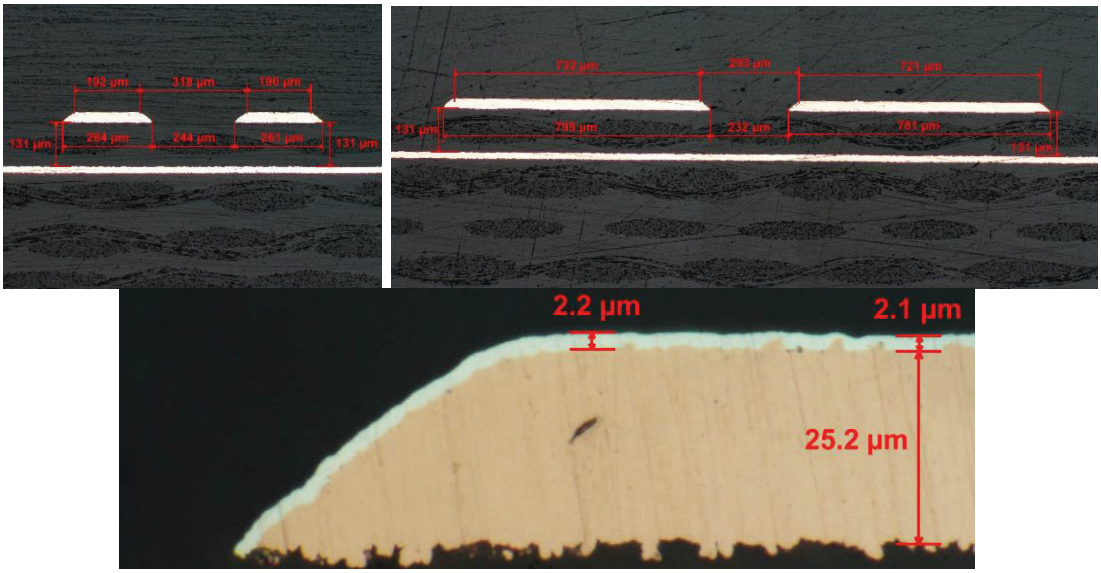

Figure 36: Cross-sections of the differential microstrip Beatty standard PCB test board.

Conclusions

This paper has shown that by using a simple resonant test structure like the Beatty standard on a PCB it is possible to use it to verify the as-manufactured parameters and tune the PCB simulation model. We also have shown that using a non-resonant structure like a simple microstrip or stripline trace does not provide a measurement result that is rich enough to allow for a good model tuning.

Since a simulation model is used to tune the manufacturing parameters and given that the simulation model itself has a certain degree of error it is not possible to guarantee that the tuned parameters correspond exactly to the manufactured parameters. In fact if these tuned parameters are used on a different simulation tool, the obtained results might be slightly different because different simulation tools might use different models. Figure 37 shows a comparison of the results obtained from four different EM simulators using the same parameters. As expected the results are slightly different for each simulator. But assuming that the simulation tool uses a reasonably accurate model one will be able to identify significant delta variations of a parameter after manufacturing. The differences between the results presented in Figure 37 originate at least partially from different features and models used by the simulators. ADS and Hyperlynx include surface roughness in their calculations, but do not use the same model. The models in AWR and CST MWS did not account for surface roughness at all.

From an engineering point of view, the most critical point is to make sure our simulation model correlates to the manufactured PCB. In this context even if the model tuning was done in a different simulation tool it is still beneficial to use those tuned values rather than the data sheet design parameters as shown in Figure 38, especially if one understands the differences between the tools.

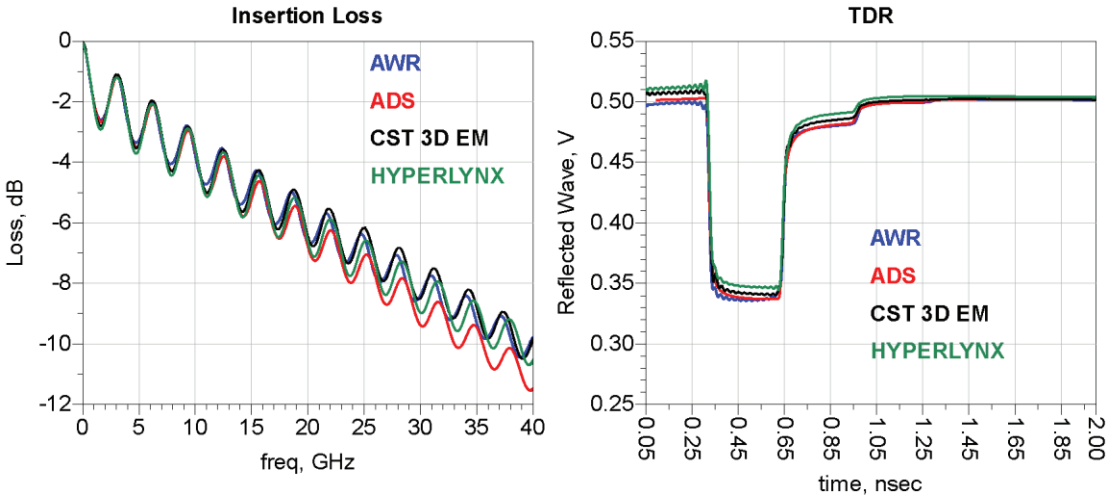

Figure 37: Simulation the stripline example Beatty standard with the same design parameters in different simulators: ADS, NI AWR, CST 3D EM and Hyperlynx.

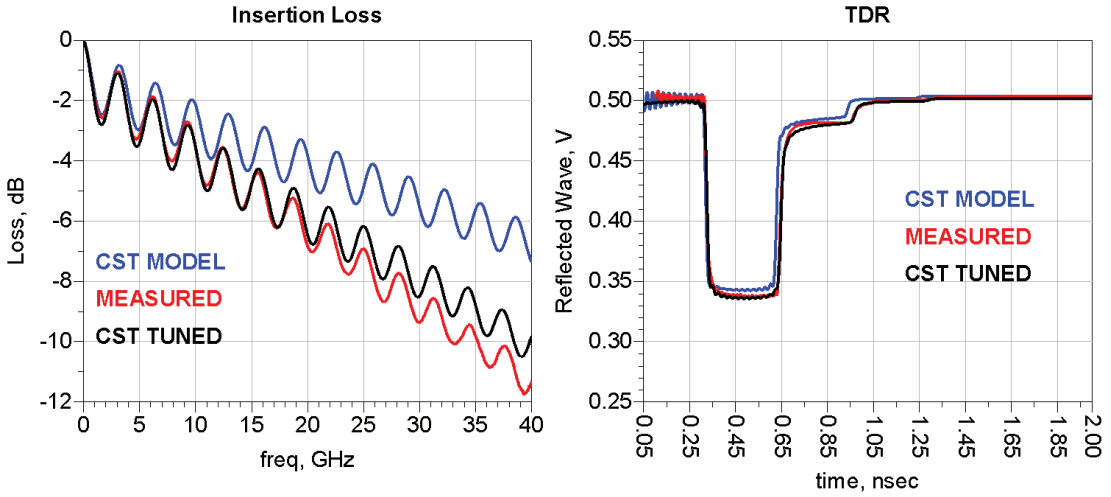

Figure 38: Comparison of measured data with a CST 3D EM simulation using the design parameters (Model) and a simulation using the tuned parameters obtained with Keysight Technologies ADS (Tuned).

The results show that the simple to fabricate Beatty structure can provide the necessary as-fabricated manufacturing details of the PCB cross section to significantly improve the correlation of a simulation model with measurement. This allows improved accuracy of EM based simulations to determine the desired nominal performance and explore manufacturing tolerances. The traditional 2-line method can provide a quality verification of the PCB losses, but does not have the complexity to enable accurate simulation to measurement correlation with modern EM tools. The Beatty structure along with the 2x-Thru requires no more space or measurement effort then the 2-line method and is highly recommended for implementing on your next high speed digital PCB.

Acknowledgments

We would like to thank the Satoshi Sekiguchi and Toshiyuki Ihara from the Advantest FA team in Gunma Japan for the PCB cross-sections, Giovanni Bianchi for the microstrip filter design in Appendix C and also to Evan Green and Sharon Trueman from R&D Altanova for their work on the microstrip test coupons.

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Appendix A

As we have been writing this paper, a large number of swept simulations were used to gain a better understanding of the effects that parameter changes have on the characteristic plots we can obtain from the Beatty standard as also shown in [2] for the stripline case. This appendix presents some of these sweep simulation results using two examples, one for a stripline and one for a microstip implementation of the Beatty standard. The design parameters used for both models are shown in Table 5.

Table 5: Design parameters for stripline and microstip Beatty standard models

	W1	*W2*	*L1*	*L2*	H_{core}	*H*	ε'	*tanδ*	*T*
Stripline	150 µm	450 µm	15 mm	25 mm	127 µm	353 µm	3.41	0.008 (1 Ghz)	17 µm
Microstrip	270 µm	810 µm	15 mm	20 mm	-	130 µm	3.54	0.008 (10 Ghz)	33 µm

The stripline implementation of the Beatty standard is the one that is easier to understand, because there is no ε'_{eff} which is dependent on the resonators dimensions. Because of that, we will begin with the stripline example.

Varying the width of the middle section of the Beatty standard produces effects that are easily explained. Figure 39 shows what happens if the width *W2* is changed by +/- 45 µm (+/- 10%). The results of the simulation with the nominal width are shown in red, the results after reduction of the width in blue and the results after a width increase in pink. This color scheme will be used in all subsequent plots.

The most obvious effect of changing *W2* can be seen in the TDR. Here the height of the impedance steps change according to the change of *W2*. There is also a change in the insertion loss and the return loss. A decrease of the impedance of the middle segment leads to deeper minima in the insertion loss and larger maxima in the return loss. The maxima in the insertion loss remain almost unaffected. Constructive interference exists at the frequency of the maxima, making the impedance discontinuity 'invisible'. It is important to note that there are only local changes of the phase difference centered around the x axis, but there is no integral change over the whole frequency range, as varying the impedance in a stripline trace does not affect the propagation delay.

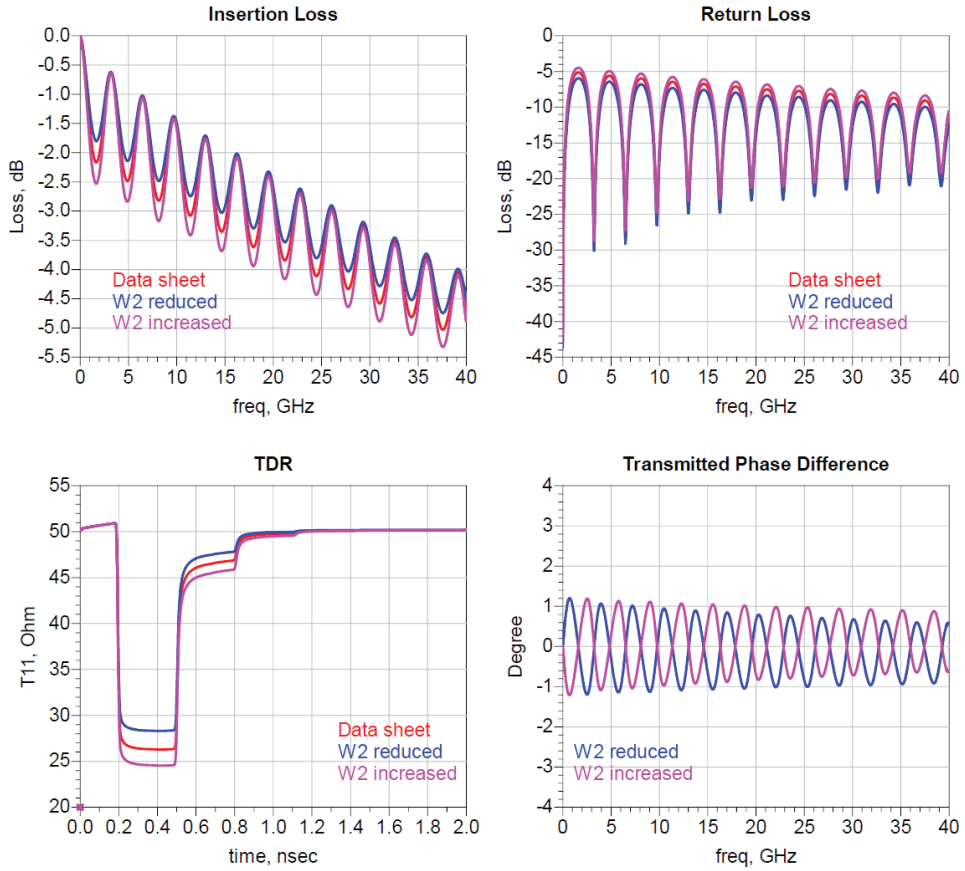

Figure 39: Varying the width *W2* of middle segment of a stripline Beatty standard. Nominal width shown in red, width reduced by 45 µm in blue, width extended by 45 µm in pink.

Modifying ε' has a major impact on the characteristic plots of the Beatty standard. As the dielectric constant does not only affect the impedance but also the phase, the minima and maxima in the insertion loss and return loss plots will shift not only in the loss but also in the frequency. Looking at this set of simulations, one finds that there is now also a deviation of the phase difference from the x-axis, or in other words a change in the integrated phase difference. The overall attenuation increases with an increase of ε' as the real and imaginary part of the dielectric constant are related by Equation (1). For this sweep, ε' has been changed by roughly +/- 6%, the relative changes in all other experiments are much larger. Note how this relatively small change has a huge impact on all the characteristics of the model. The high sensitivity and the fact that the dielectric properties are the only properties that have a major effect on the phase let us to conclude that it is important to find good estimates for ε' and *tanδ* before trying to tune the other parameters. The sweep results are shown in Figure 40.

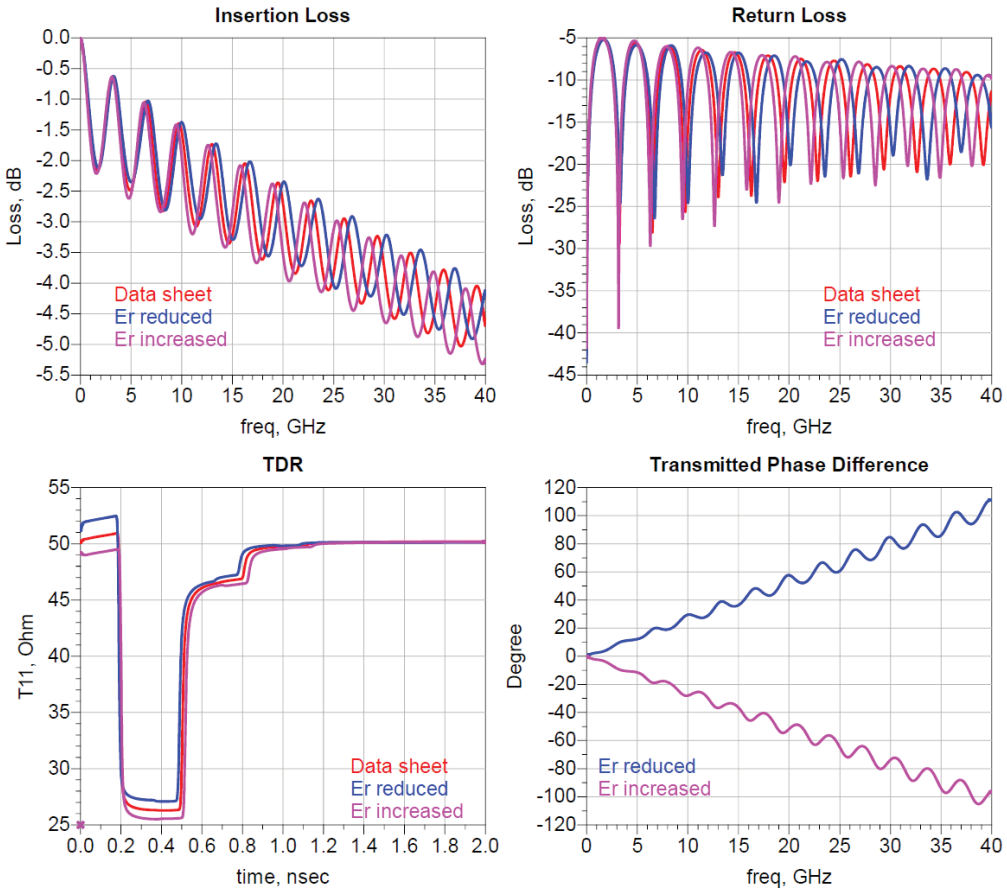

Figure 40: Varying the ε' of a stripline Beatty standard. Nominal ε' is shown in red, ε' reduced by 0.2 in blue and ε' increased by 0.2 in pink.

The next experiment is to vary the narrow trace's width *W1* by +/- 10%. The experiment results are shown in Figure 41. Changing the width *W1*, and therefore the impedance of the launch traces of the Beatty standard causes additional reflections at the ports, if the port impedance Z_0 is kept at 50 Ω. The additional resonances interfere with the characteristic patterns caused by the two intended discontinuities in the Beatty standard. These effects can make it harder to intuitively interpret the effects of other parameter variations. To deal with this problem, one can adjust the port impedance to match the impedance of the narrow line sections. This does not cause any change of the information content of the modeled or measured S-Parameters, but may make intuitive understanding easier.

A change of the dielectric height *H* will affect the impedance of both the narrow and the wide trace. The behavior of the characteristic plots when the height *H* is changed by +/- 10% is shown in Figure 42. In this simulation, the height of the core changes proportionally with the change of the dielectric height *H*. The most obvious effect can be seen again in the TDR. As expected, increasing the vertical separation between trace and reference plane increases the impedance of the line segments. Because of the changing impedance of the narrow trace, some extra ripple occurs in the insertion loss and the return loss.

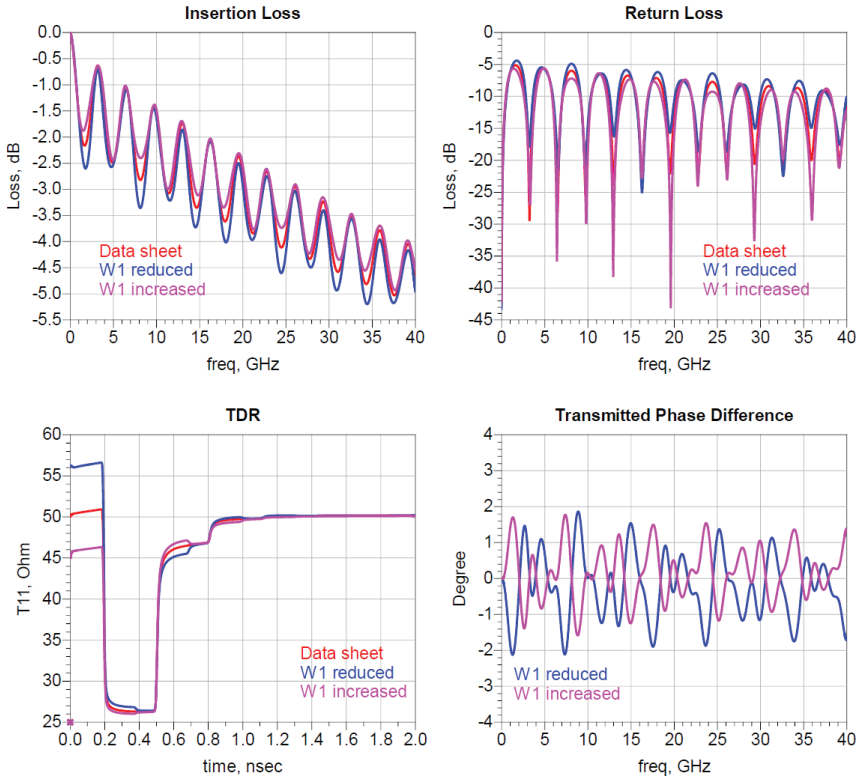

Figure 41: Varying the width *W1* of left and right segments of a stripline Beatty standard. Nominal width shown in red, width reduced by 30 µm in blue, width extended by 30 µm in pink.

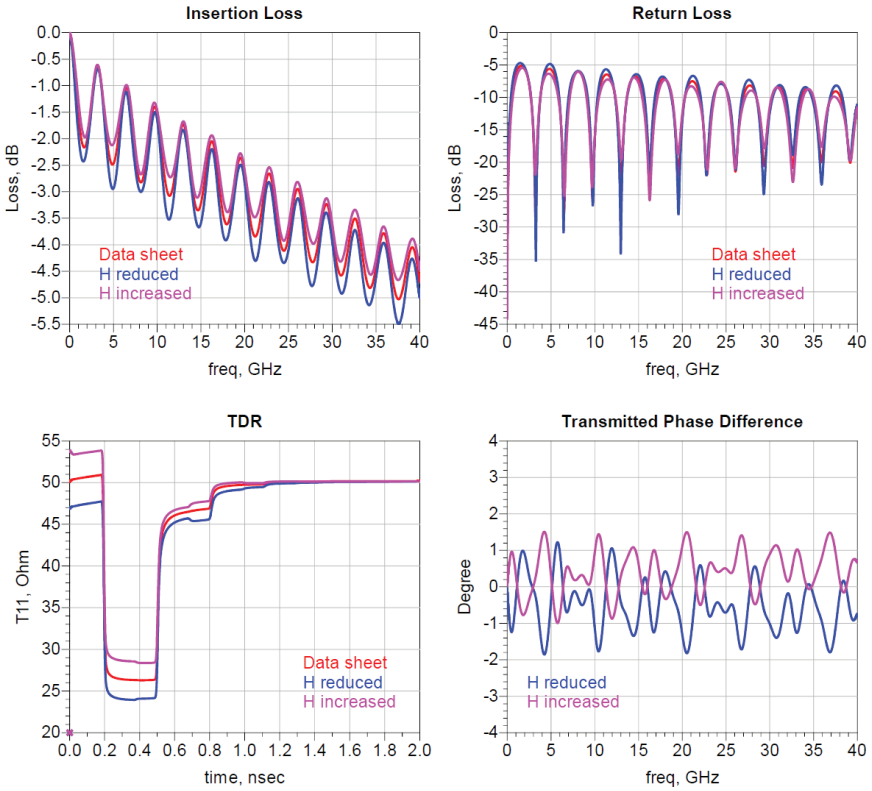

Figure 42: Varying the dielectric height *H* of a stripline Beatty standard. Nominal dielectric height is shown in red, dielectric height reduced by 35 µm in blue and dielectric height increased by 35 µm in pink.

The next experiment peformed with the stripline Beatty standard was to change the widths of the line segments by the same amount together, as it would happen because of under-etching or during a plating process. The results are shown in Figure 43. It is especially interesting to look at the TDR in this case and compare it to the TDR presented in Figure 44. As already mentioned in [2], the impact on the impedance is much larger on the narrow trace segments than on the wide middle segment. Contrary to that, changing the dielectric height *H* will affect the impedance of all trace segments about the same. This different behavior makes it possible to separate the effects of width and height variations during the optimization process. This is not possible if a simple stripline trace is used for the simulation tuning process.

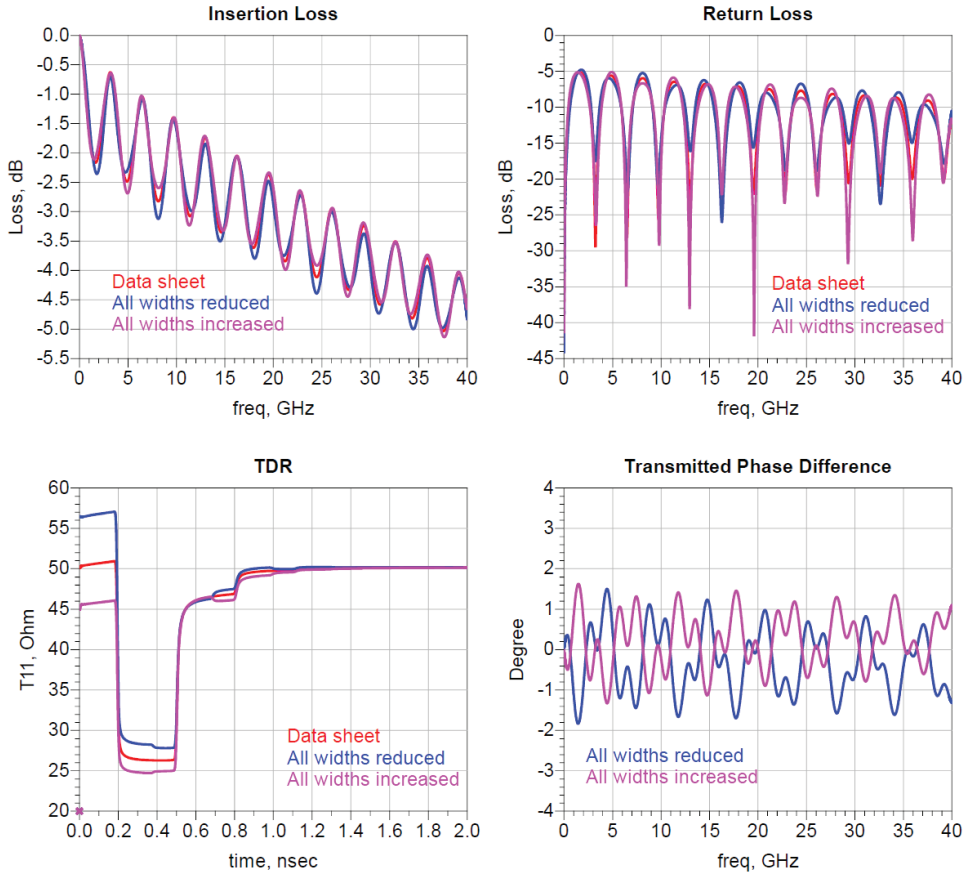

Figure 43: Varying the conductor width for all line segments in a stripline Beatty standard by the same amount, as it would happen because of under-etching, for example. Simulation results with the nominal design parameters are shown in red, all widths reduced by 15 µm in blue and all widths increased by 15 µm in pink.

Both effects are compared in Figure 44. If one reduces the conductor width or increases the dielectric height, it is expected that both modifications cause the characteristic plots to change in the same direction. Two comparisons are made, the first for a wider trace and reduced dielectric height, the second one for an increased dielectric height and narrower traces.

Another geometrical parameter is the conductor thickness. It has some impact on the impedance of narrow traces because of the additional fringe fields that occur when the thickness of the conductor is increased. However, the effects in the characteristic plots

are relatively small. To achieve visible changes in the plots, the trace thickness is varied from 12 µm to 22 µm, or roughly +/- 30% of the nominal value. It is very unlikely to encounter such large variations in practical PCBs. The resulting plots are presented in Figure 45. Change of the conductor thickness causes a change of about 1 Ω in the impedance of the narrow trace sections, and the effect is even smaller on the wide 25 Ω section. From these results it can be concluded that the trace thickness *T* is a minor factor if *W1/T* is large.

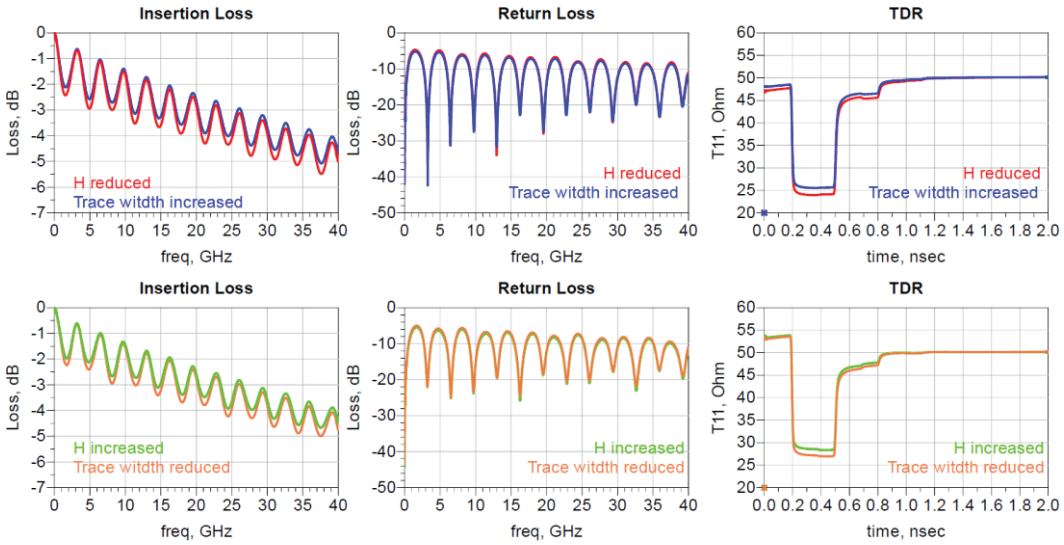

Figure 44: Stripline Beatty standard, differences between etch and substrate variation. Only one dimension was changed per curve. Upper row: *H* -10% (red) and trace width on all segments +15 µm (blue). Lower row: *H* +10% (green) and trace width on all segments -15 µm (orange).

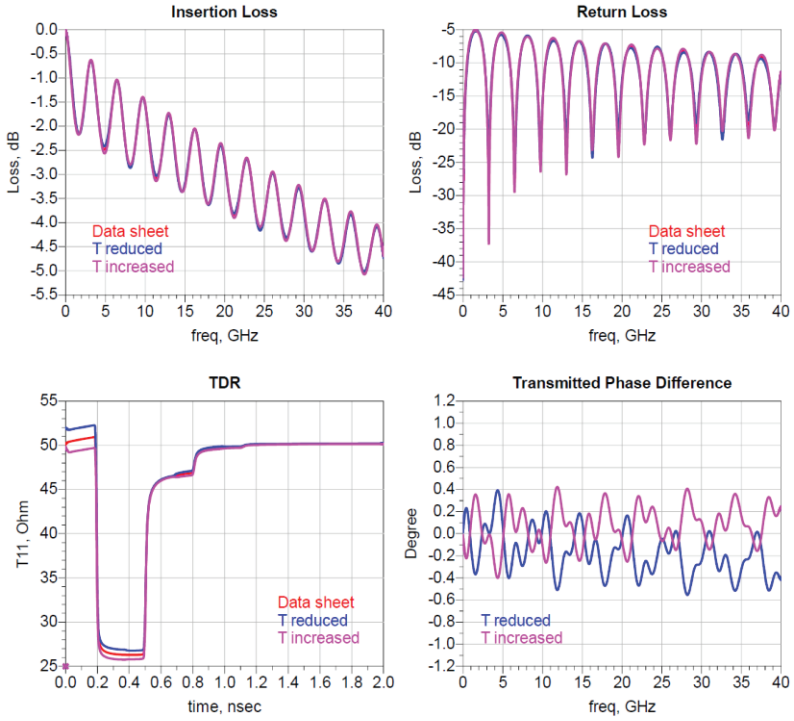

Figure 45: Varying the conductor thickness *T* of a stripline Beatty standard. *T's* nominal value is 17 µm and shown in red, *T* reduced by 5 µm in blue and T increased by 5 µm in pink.

The impact of a change to the loss tangent $tan\delta$ is shown in Figure 46. As expected the insertion loss falls faster towards higher frequencies and in the time domain the edges of the TDR get more rounded as $tan\delta$ increases.

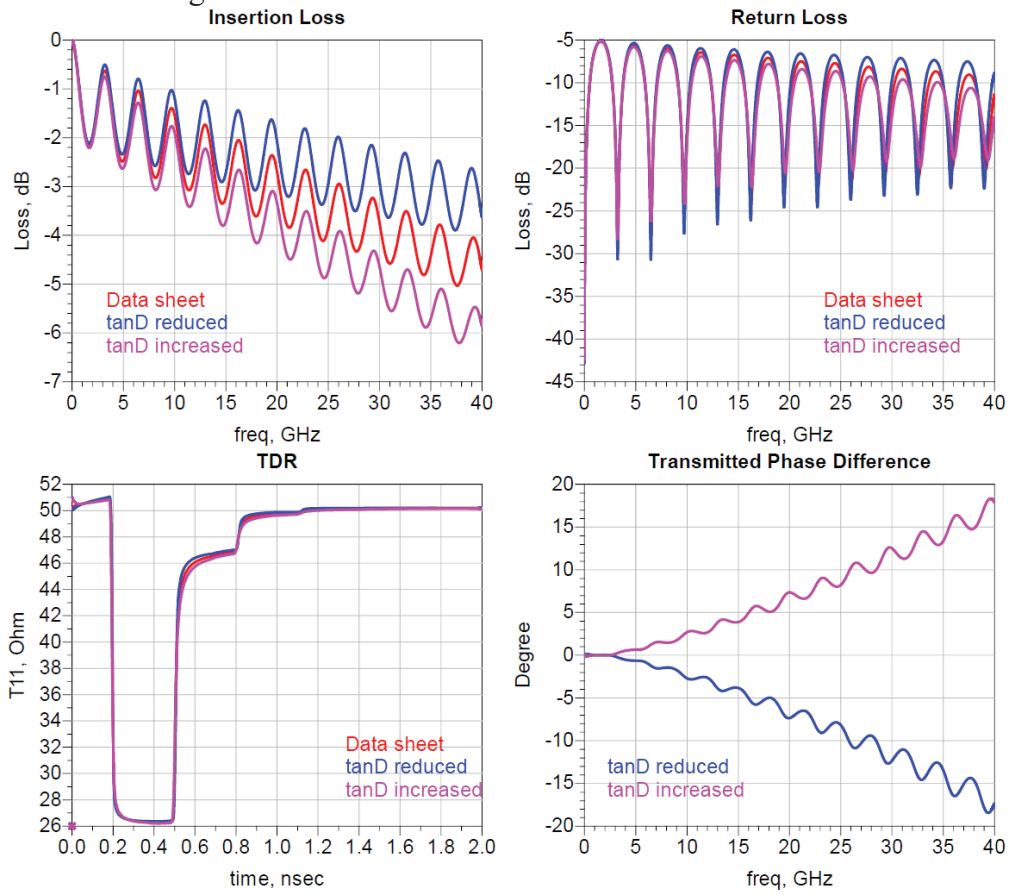

Figure 46: Varying loss tangent *tanδ* of a stripline Beatty standard. The nominal value of *tanδ* is 0.008 and shown in red, *tanδ* reduced by 0.005 in blue and *tanδ* increased by 0.005 in pink.

More energy is dissipated as traveling waves move back and forth between the discontinuities, which leads also to a decrease in the return loss towards the higher frequencies with higher $tan\delta$. Due to the causal nature of the material model used, losses will cause a decrease in group delay towards higher frequencies. This can be seen in the delta-phase plot, where the phase changes slower if the losses are higher.

The second section of the appendix will show some examples for a Beatty standard implemented in microstrip technology. Table 5 shows the design parameters for this example, too. We will point out the differences between the microstip and stripline Beatty standard. The first experiment is to change the dielectric constant ε'_{eff} for the microstrip Beatty standard. The characteristic plots obtained are shown in Figure 47.

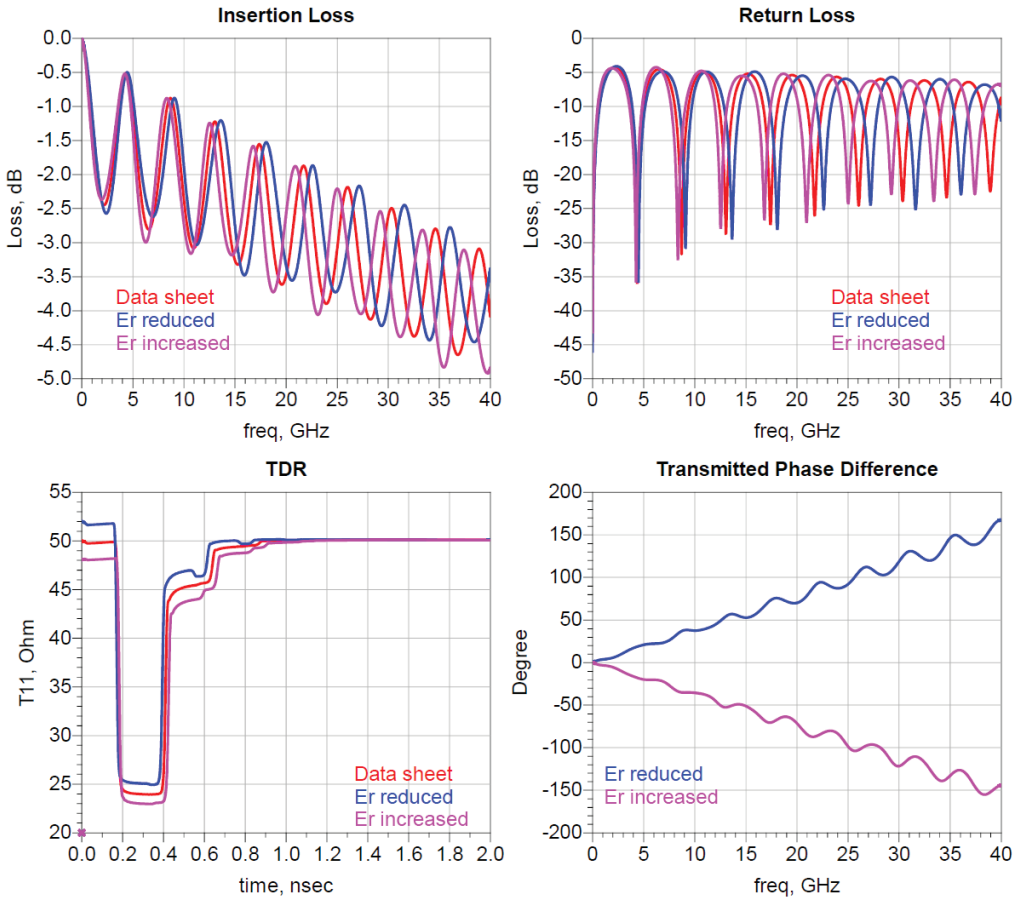

Figure 47: Varying the ε' of a microstrip Beatty standard. Nominal ε' is shown in red, ε' reduced by 0.3 in blue and ε' increased by 0.3 in pink.

Similar effects as in Figure 44 can be observed. Variations of ε' have a major impact on all four plots, most notably on the frequency axis. The change of the phase is obvious. Minima and maxima in the loss plots will shift horizontally. Higher ε' causes the impedance of all line segments to drop.

Figure 48 and Figure 49 show the effects of changing the dielectric *H* and the conductor width *W*. The width change is the same for all three trace segments again. The most interesting insight can be gained from comparing the two TDR plots. As already demonstrated with the stripline Beatty standard, the impedance of both narrow and wide trace segments change by about the same amount if the dielectric height *H* is changed. In comparison, the variation of the conductor width affects the narrow line segment much more than the wide one. As the ε'_{eff} changes in all cases due to the changes in the cross section geometry, there is some variation in the integrated phase difference in both cases.

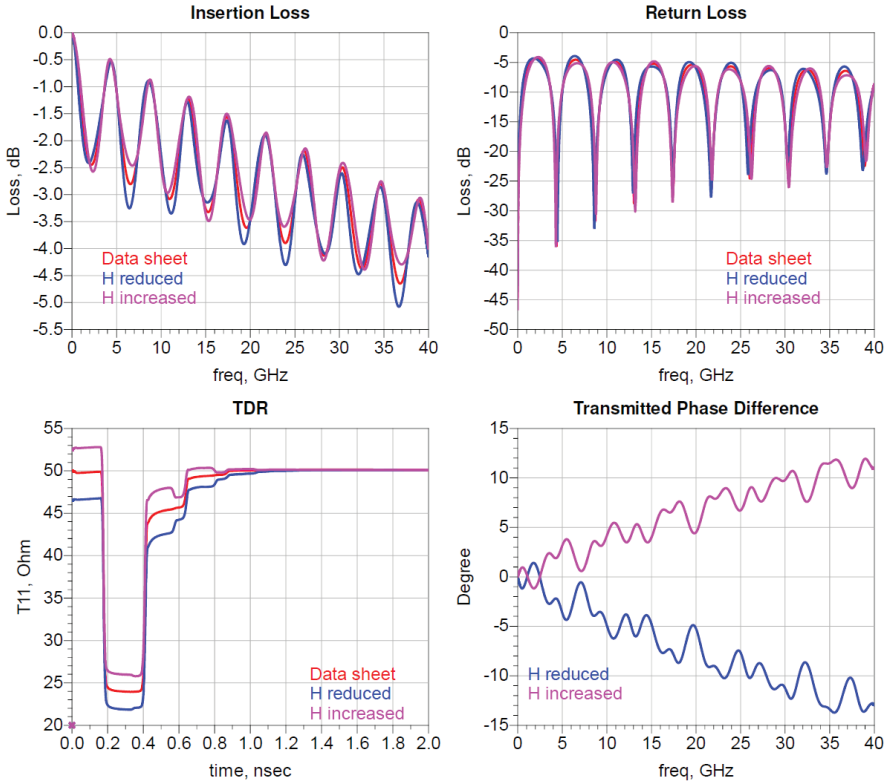

Figure 48: Varying the dielectric height *H* of a microstrip Beatty standard. Nominal dielectric height is shown in red, dielectric height reduced by 13 µm in blue and dielectric height increased by 13 µm in pink.

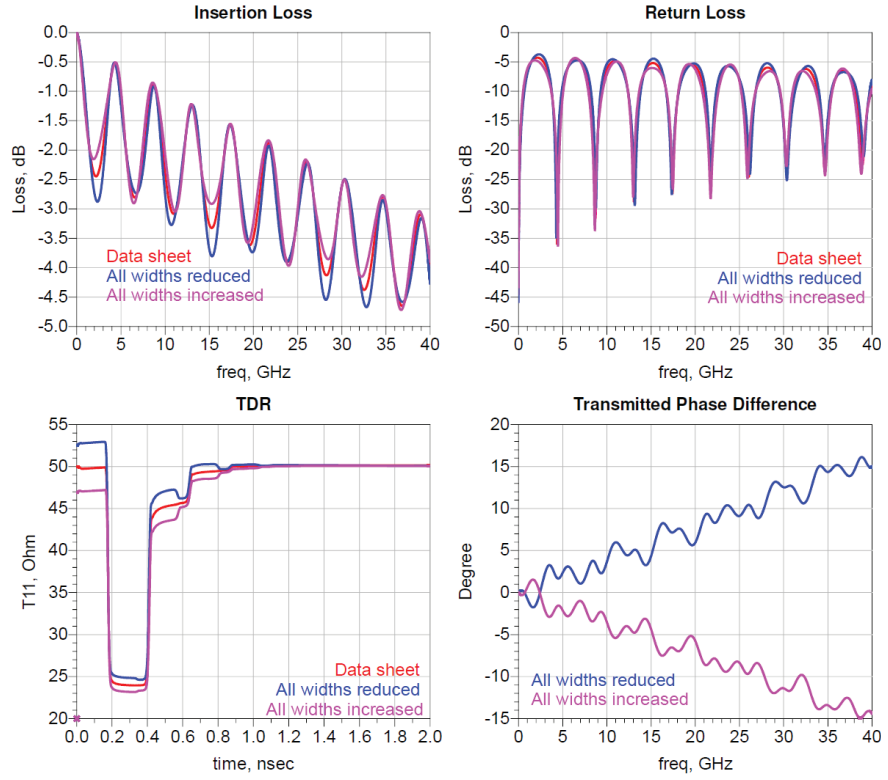

Figure 49: Varying the conductor width for all line segments by the same amount, as it would happen because of under-etching, for example. Simulation results with the nominal design parameters are shown in red, all widths reduced by 27 µm in blue and all widths increased by 27 µm in pink.

Varying the conductor thickness T has only little effect on all four plots as can be seen in Figure 50. This is easily explained by the large ratio of W/T in this example.

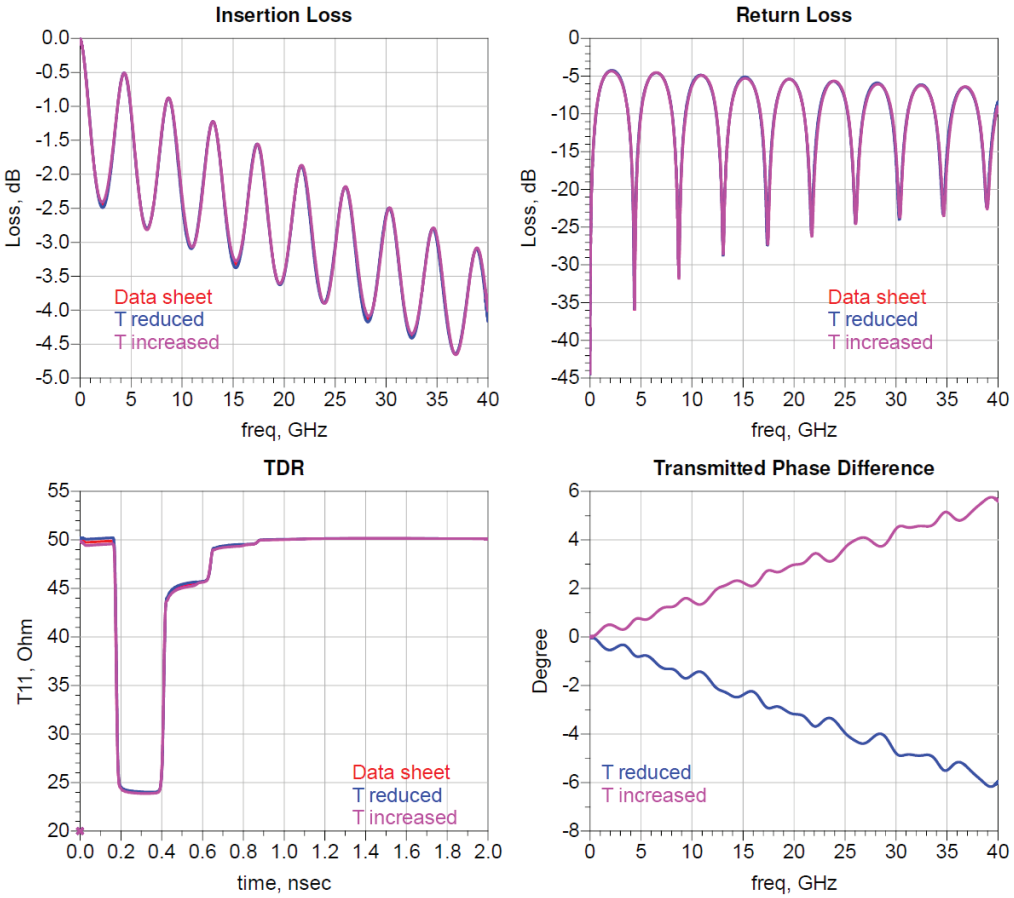

Figure 50: Varying the conductor thickness *T* of a microstrip Beatty standard. *T's* nominal value is 33 µm and shown in red, *T* reduced by 5 µm in blue and *T* increased by 5 µm in pink.

Appendix B

Another type of test structure for EM model tuning is the parallel resonator [2]. In this appendix we apply the parameters identified using the single-ended microstrip Beatty standard that are described in Table 3 to the two test coupons shown in Figure 51. These test coupons were manufactured on the same panel as the microstrip Beatty standard so the tuned values should apply also to these test coupons.

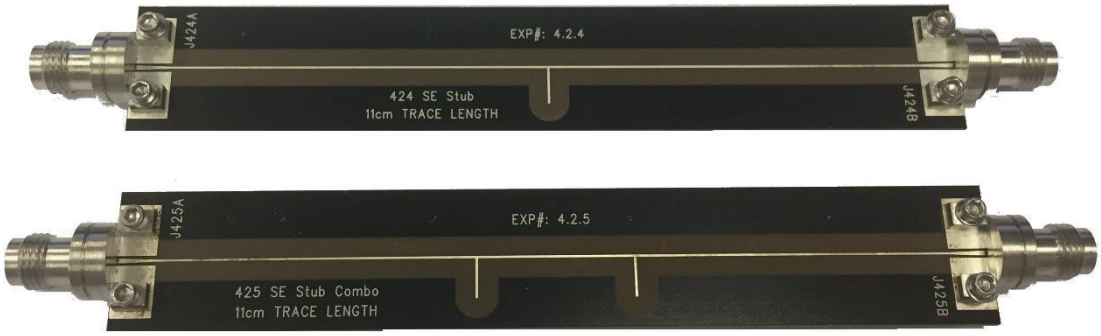

Figure 51: Pictures of the two test boards with a single stub and a combo of two stubs.

Figure 52 shows the model in Keysight Technologies ADS for the two stubs test coupon. Figure 53 shows the results for the single stub test coupon and Figure 54 for the two stubs test coupon. The connectors were de-embedded using the 2x-Thru test coupon shown in Figure 21. The results show as expected that the tuned values significantly improved the simulation to measurement correlation.

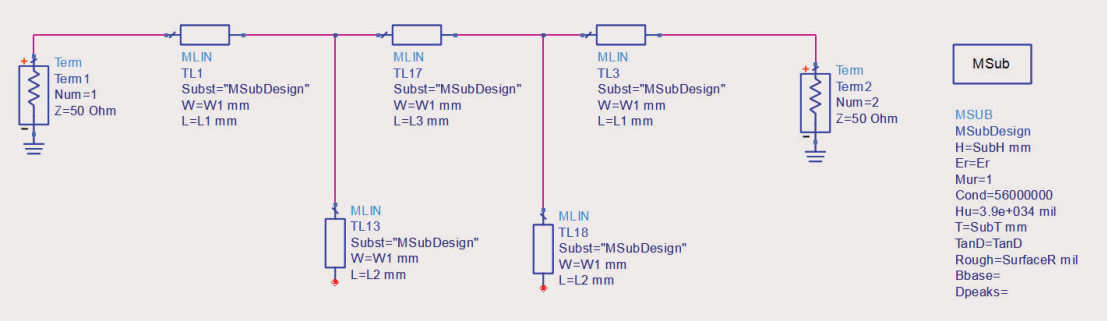

Figure 52: Model in Keysight Technologies ADS of the two stubs combo.

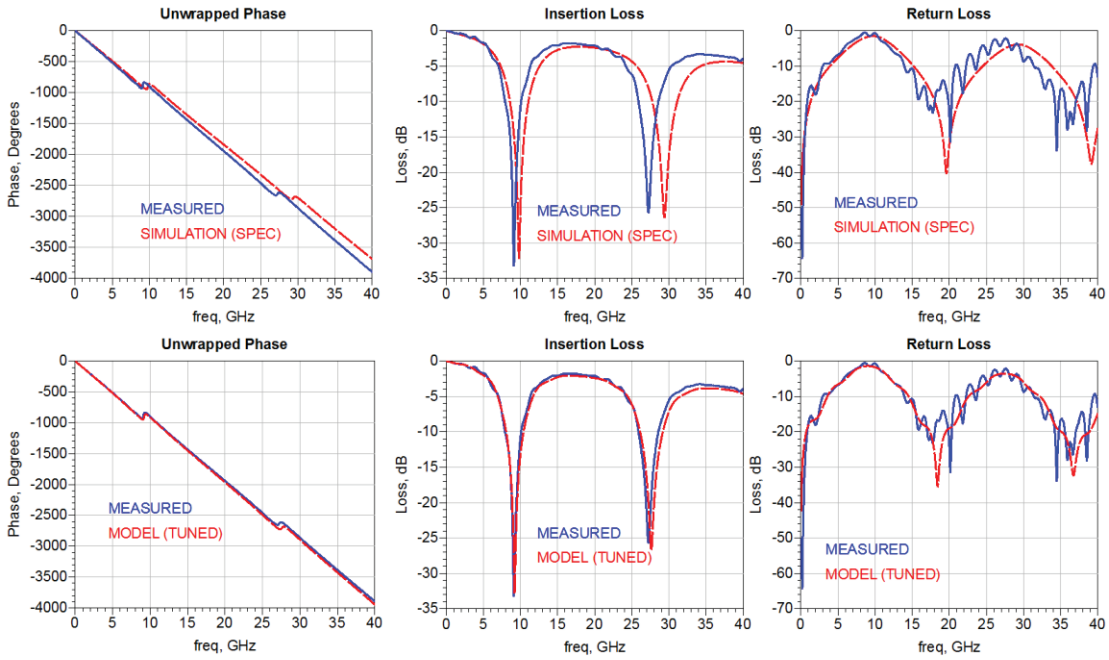

Figure 53: Comparison of the measured and simulation results using the design and material specifications and the tuned values using the Beatty standard for the single stub test coupon.

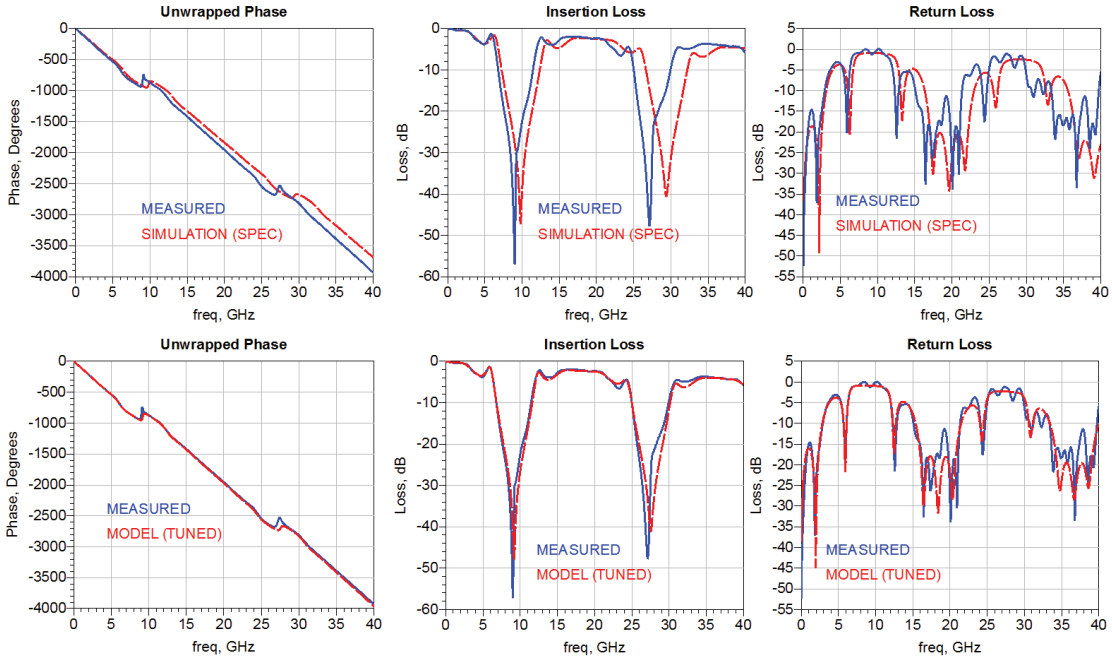

Figure 54: Comparison of the measured and simulation results using the design and material specifications and the tuned values using the Beatty standard for the double stub test coupon.

Appendix C

In this appendix we present one more example of applying the tuned parameters presented in Table 3 to another structure built on the same PCB panel: a bandpass filter shown in Figure 55. No sufficient 2x-Thru coupon was available to de-embed the connectors, so we show the raw measured data here. Figure 56 shows the ADS model of the filter. Figure 57 shows a comparison of the filter simulated frequency response with the measured data for the cases where the design values and the model tuned values were used. The results show that by using the tuned values (in this case the dielectric constant, loss tangent and surface roughness), a better fitting between simulation and measurement is achieved.

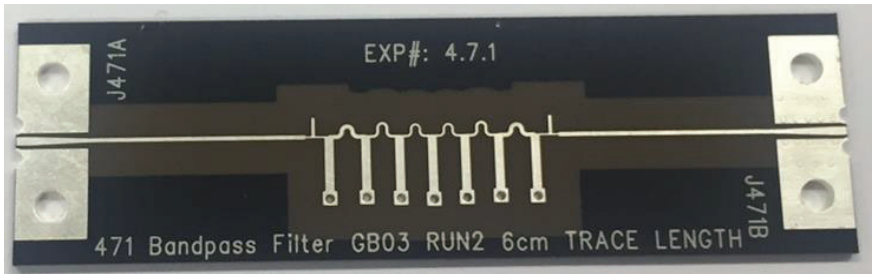

Figure 55: Bandpass filter test coupon.

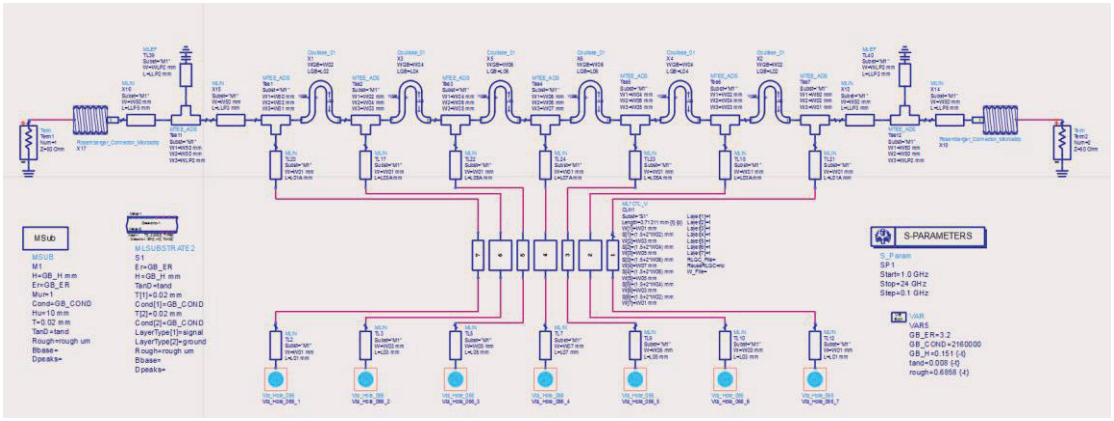

Figure 56: ADS model of the microstrip based bandpass filter.

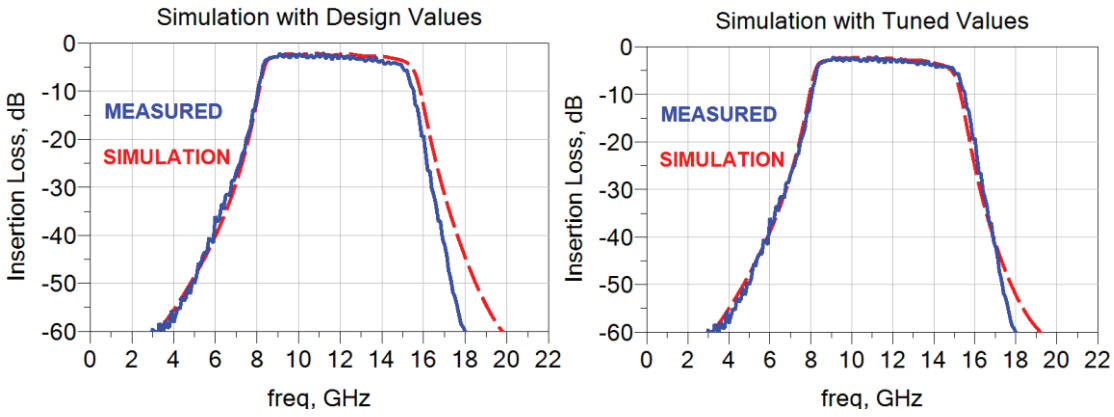

Figure 57: Comparison of the measured results with the simulation results using the initial design values (left) and using the tuned values (right).

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