400GE FEC Encode/Decode Processing



The IEEE 802.3bs Task Group defines specifications for 400 Gigabit per second (Gb/s) Ethernet, where forward error correction (FEC) is mandatory. See how a 400GBASE-R Reed-Solomon RS-544 (KP4 FEC) encode/decode works in operation. Note that FEC encoding/decoding takes place at the binary level before the physical layer.

TRANSMIT PATH **KP4 FEC** Encoder **FEC Codeword** Encoding Pre-FEC Interleaving **Symbol Distributor Transmit Transcoder** & Distribution 8 PAM4 Lanes FEC a at 53 Gb/s Scrambler to PHY **Alignment Marker Transmitter Group Insertion** FEC b LEARN MORE >> 64/66 bit Codewords Transm 256b/257b Reduces line Self-synchronizes, Gearboxing facilitates 30 check symbols Different markers IEEE 802.3bs specifies 16 PCS are calculated & inserted are created for each FEC symbol encoding ensures no long lanes across both 400GAUI-16 of the 16 PCS lanes per FEC codeword overhead runs of 1s & 0s boundaries & 400GAUI-8 electrical interfaces

RECEIVE PATH

