

TECHNICAL OVERVIEW

Chapter 9

Microwave Amplifier Design and Smith Chart Utility for Matching Networks

PathWave Advanced Design System (ADS)



Background

The purpose of this lab is to provide designers with a simple method of developing and designing amplifiers. There are many textbooks available on amplifier theory and design, but they often leave a gap between theory and practical considerations necessary to produce good amplifiers. A good circuit will compare well with simulated data so that minimal post-production fine-tuning is required. This lab combines basic amplifier design theory with practical procedures that are needed to make the design right the first time, minimizing time and effort.

Amplifiers are an integral part of any communication system. The purpose of having an amplifier in a system is to boost the signal to the desired level. They also help in keeping the signal well above any present noise so that it can be analyzed easily and accurately. The choice of amplifier topology is dependent upon the individual system requirements and can be designed for low frequency applications, medium to high frequency applications, mm-wave applications, and many more.

Amplifiers can also adopt many design topologies and can be used at different stages of the system. They are classified as Low Noise Amplifiers, Medium Power Amplifiers, and Power Amplifiers. The most common structure tends to be a Hybrid MIC amplifier. The main design concepts for amplifiers, regardless of frequency and system, remain the same and need to be understood very clearly by designers. Specific frequency ranges pose their own unique design challenges and must be handled appropriately. This paper focuses on the design of small signal C- band Hybrid MIC Amplifiers.



This methodology is equally applicable for other amplifiers operating in other frequency ranges, requiring only minor changes to the design procedure.

Create Amplifier Workspace

- 1. In the main ADS window, click on New Workspace, and when the wizard opens, name your new workspace: **Lab9_Amp_wrk**.
- 2. Click on Change Libraries. Ensure that both **Analog/RF** and **DemoKit_Non_Linear** are selected. Click OK and **Create Workspace**. The workspace and library windows are shown in Figure 1.

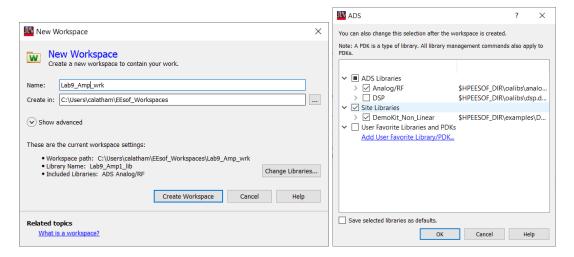


Figure 1. New workspace and library selection windows

DC - FET Curve Tracer Template

This step uses a built-in DC simulation template that sweeps drain-source voltage at different steps of gate- source voltage (also called a nested sweep). The resulting IDS or bias characteristics are plotted automatically using a built-in data display template. This FET will be used for the amplifier.

- Create a new schematic named FET_curves. Click Show Advanced. Under Insert Template, select ads_templates:FET_curve-tracer.
- In the new schematic, select the DemoKit_Non_Linear palette and insert the DEMO FET 1 and the DEMO KIT TECH INCLUDE component, as shown in the bottom of Figure 2.
- The FET text may overlap other text, components, or wires. Move the component text using the F5
 keyboard key or the move handle (blue diamond near component text when component is selected).
 This keeps schematics easy to read.
- 4. Save the schematic and run the simulation. If a window pops up and warns that the nodes are not named, select Run Anyway.

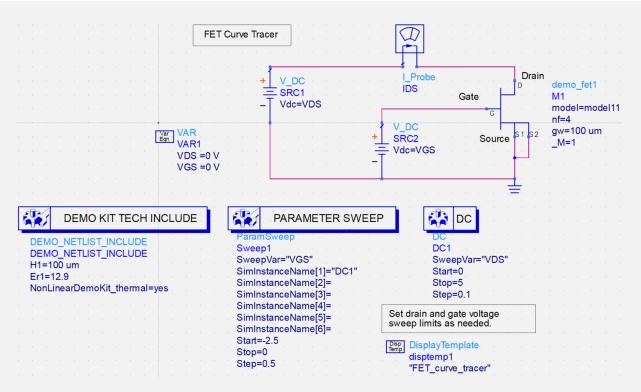


Figure 2. FET schematic, including the Demo Kit Tech Include block and sweeps

Notice the status window and the data display will pop up. Scroll through the status summary and notice that for each value of VGS and VDS is swept from 0 to 5 volts. This is shown in Figure 3.

```
        Status/Summary

        CT Sweep1[1] < Lab9_Amp_lib:FET_curves:schematic>
        VGS=(-2.5->0)

        DC Sweep1[1].DC1[1/6] < Lab9_Amp_lib:FET_curves:schematic>
        VGS=-2.5 VDS=(0->5)

        DC Sweep1[1].DC1[2/6] < Lab9_Amp_lib:FET_curves:schematic>
        VGS=-2 VDS=(0->5)

        DC Sweep1[1].DC1[3/6] < Lab9_Amp_lib:FET_curves:schematic>
        VGS=-1.5 VDS=(0->5)

        DC Sweep1[1].DC1[4/6] < Lab9_Amp_lib:FET_curves:schematic>
        VGS=-1 VDS=(0->5)
```

Figure 3. Status / Summary window of the sweep

Compare the status information to the Parameter Sweep and DC Simulation blocks in the schematic to understand how a nested sweep is done in ADS. In this case, the Parameter Sweep is the outer sweep, and the DC Sweep is the inner sweep. Notice that the variables must first be declared in the VAR block before they are used. The initial value is not used for the sweep, as they are automatically overridden with the swept values. The setup for these sweeps is shown back in Figure 2, at the bottom of the schematic view.

In the Data Display plot, the marker value should appear at VDS = 3 V and VGS = -0.5 V with IDS = 75 mA. Select the marker with your cursor and then use the marker arrow icons to move to different values. These bias characteristics are shown in Figure 4.

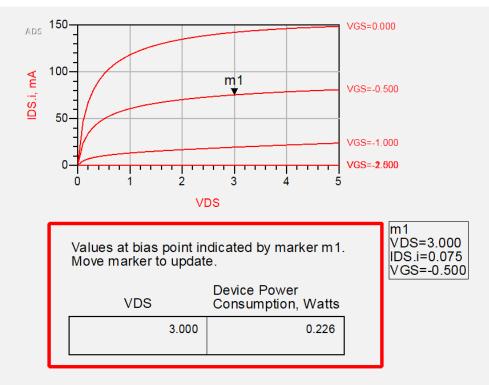


Figure 4. Bias characteristics for the sweeps

- 5. Use your cursor again to select and drag the marker to another trace and try using your keyboard arrow keys to move the marker. Try inserting your cursor in the marker readout and type in a different VDS to move the marker.
- 6. Move the marker to various traces and values of VDS and notice that the marker (m1) readout and the computed power changes as the marker position changes.
- 7. Save and close the Data Display, Status, and Schematic windows.

Now that you know how this FET performs under bias conditions, it's time to build an amplifier and test its performance.

Build the FET Amplifier Schematic and Symbol

- 1. Build the amplifier shown in Figure 5. The basic steps are shown below:
 - a. Create a new schematic and name the cell AMP 7GHz.
 - b. Insert **FET 1** from the DemoKit_Non_Linear palette. Additionally, insert the **DEMOKIT TECH INCLUDE**, which is required for the demo components.
 - From the Lumped-Components palette, insert inductors (L) and capacitors (C). From the Sources-Freq Domain palette, insert V_DC sources.
 - d. From the toolbar, insert pins on the input and output, grounds, and wires.
 - e. Save the design.

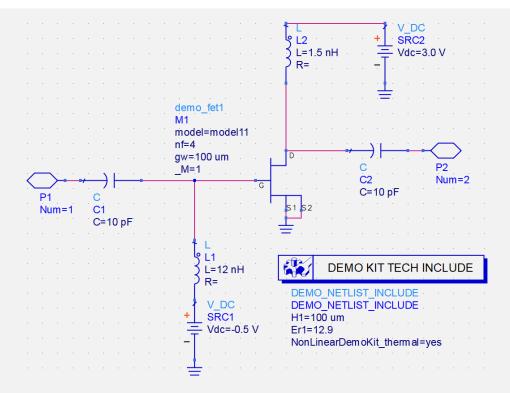


Figure 5. FET amplifier schematic

Because ADS supports hierarchical designs, a schematic created as a sub-circuit can be placed inside another schematic. The pins were added to establish connectivity for the sub-circuit schematic.

- 2. In the Main window, click the **Symbol** icon.
- In the dialog box, browse to the cell AMP 7GHz and click Create Symbol.

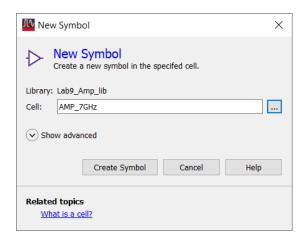


Figure 6. New Symbol window

4. In the Symbol Generator window, go to the **Copy/Modify** tab and find the tab marked **System-Amps Mixers** and select the **Amp** symbol. Click **OK**. Save and close the symbol window.

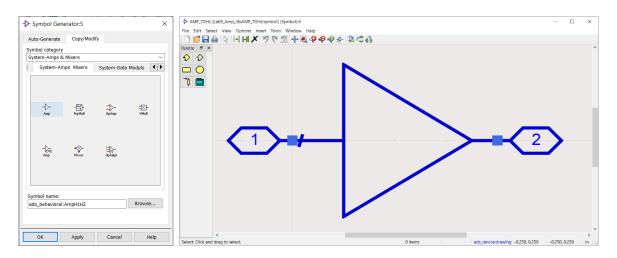


Figure 7. Create the symbol for the sub-circuit

ADS cell AMP_7GHz is now setup to be used on another schematic since the symbol and the ports establish the connectivity to the corresponding design. In other words, this design can be used in a hierarchical design flow.

Amplifier DC and AC Simulation

Creating the Schematic with Sub-Circuit

- 1. Create a new schematic and name the cell AMP test DC AC.
- 2. In the new schematic, drag and drop the amplifier symbol from the main window.
- From the Source-Freq Domain palette, connect a V_AC source to the input of the amplifier. On the
 output of the amplifier, connect a resistor from the Lumped-Components palette. Ground both the
 input and output.
- 4. For DC and AC simulation to work, you must have either node labels, current probes, or power probes in the circuit. Place a wire label by clicking the Wire/Pin Label icon, which says 'NAME' on the icon (or Insert > Wire/Pin Label). Name the input wire Vin and the output wire Vout. The completed circuit is shown in Figure 8.

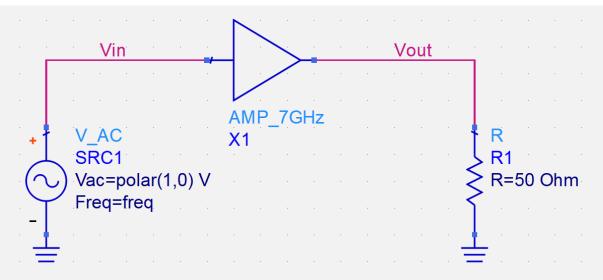


Figure 8. Schematic showing the sub-circuit placement

Simulation Setup

1. Insert the AC and DC simulation controllers. These can be found in the Simulation-AC and Simulation-DC palettes, respectively.

All ADS simulation controllers have default setup values, but we will need to change the values for the AC simulation. You can have multiple simulation controllers in one schematic, as long as the sources and circuits are value for all the controllers.

- 2. Edit the **AC** controller by double clicking on it. In the **Frequency** tab, change the **Sweep type** to **Single point** and set it to **7 GHz**.
- 3. Under the **Noise** tab, check the **Calculate noise** box. In the **Edit** dropdown menu, select **Vin** and click **Add**. Repeat for **Vout**.
- 4. Under the **Display** tab, scroll down, uncheck the **Start, Stop, and Step** boxes and check the **CalcNoise** and **Freq** boxes. If you display the parameters that are being used in the simulation, you can edit them from the schematic without having to open the dialog box.
- 5. Click **OK** to close the AC controller dialog.

The AC simulation should now be setup as shown in Figure 9.



Figure 9. AC simulation setup

DC Simulation and Annotations

The next step is to analyze the DC voltage and current throughout the circuit.

- 1. Click Simulate.
- 2. In the schematic window, go to Simulate > DC Annotation > Annotate Voltage. This will label each of the nodes with their DC voltage.
- 3. Select the **Push Into Hierarchy** tool (icon with the down arrow) and select the AMP_7GHz symbol. This will take you down a level into the schematic for the AMP_7GHz circuit.
- 4. Examine the schematic for the DC voltage values. If you want to view the current values, go to Simulate > DC Annotation > Annotate Pin Current. The minus sign for the current indicates the direction (into or out of a node). The DC annotations for the schematic are shown in Figure 10.

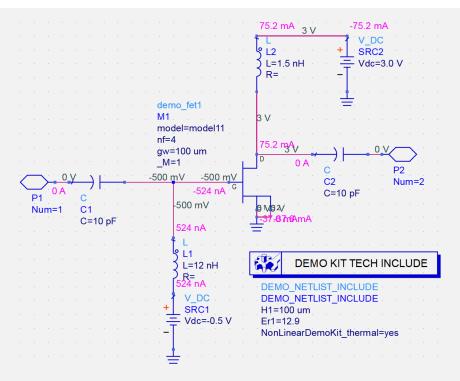


Figure 10. DC simulation annotation

- 5. To clear the annotation, go to **Simulate > DC Annotation** and uncheck Annotate Voltage and Annotate Pin Current.
- 6-. To go to the original schematic (one level up), click on the **Pop Up** icon, which is right next to the Push Into Hierarchy tool.

AC and Noise Data

The next step is to list the noise data.

- 1. Return to the Data Display window. If you closed the window, select the icon to the right of the Simulate button or go to Window > New Data Display.
- 2. Add a list from the palette. In the Plot Traces and Attributes dialog, select **Vin.noise** and **Vout.noise**. The results are shown in Figure 11. The list shows that the noise level at the output pin is about 1.8 nV (rms). This will be different at other points in the circuit.

freq	Vin.noise	Vout.noise	
7.000 GHz	0.0000 V	1.782 nV	

Figure 11. Noise results

3. In the same data display, insert another list. Select both **AC.Vin** and **AC.Vout**, and click **OK**. The results are shown in Figure 12. The AC results are in magnitude/phase format.

freq	AC.Vin	AC.Vout
7.000 GHz	1.000 / 0.000	4.486 / -165.113

Figure 12. AC voltage results

Parametric Simulation

- 1. In the schematic, deactivate the DC simulation controller. Since the DC simulation isn't needed for the rest of this section, we can deactivate the simulation controller.
- 2. Insert a **VAR** (Variable Equation) block. Change the name of the variable to **L_val**. This can be done by clicking on the default variable or by double clicking on the block.
- 3. **Push into** the amplifier sub-circuit. Change the drain inductor to **L_val** nH, as shown in Figure 13. It is important to keep the units as nH. Otherwise, the unit would default to Henrys. Using the L_val variable, the inductor initial value will be 1.0 nH, but this will change as we sweep. **Pop out** to the top-level schematic.

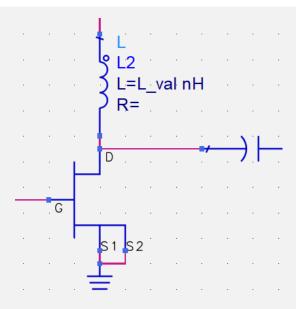


Figure 13. Value of inductor defined as L_val

- 4. To sweep a variable for AC analysis, insert a **Parameter Sweep** component from any of the simulation palettes.
- 5. Edit (double click) the Parameter Sweep component. In the Sweep tab, set the parameters to the following quantities:

Parameters to Sweep = L_val

Start = 1.5

Stop = 4.5

Step-size = 1.5

6. In the Simulations tab, set Simulation 1 to the name of the AC controller, which should be AC1. Click OK. This is shown in Figure 14. Notice that on the schematic, the Parameter Sweep block contains quotes around the variable to sweep and the simulation instance name. If the names were typed on the screen directly into the block, quotes would need to be added.

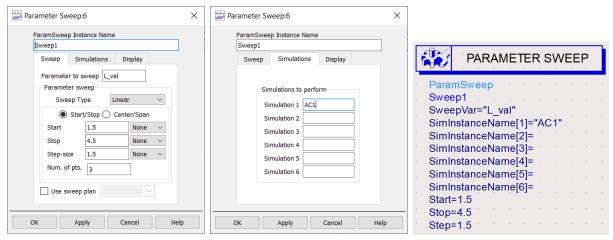


Figure 14. Setup of the Parameter Sweep

- 7. Run the simulation. Look at the data display to see the results of the sweep. You might have to expand the lists to show all the sweep values. The results are shown in Figure 15.
- 8. Save and close the schematic and data display.

frog	Vin.noise		Vout.noise			
freq	L_val=1.500	L_val=3.000	L_val=4.500	L_val=1.500	L_val=3.000	L_val=4.500
7.000 GHz	0.0000 V	0.0000 V	0.0000 V	1.782 nV	1.869 nV	1.866 nV

frog	AC.Vin		AC.Vout			
freq	L_val=1.500	L_val=3.000	L_val=4.500	L_val=1.500	L_val=3.000	L_val=4.500
7.000 GHz	1.000 / 0.000	1.000 / 0.000	1.000 / 0.000	4.486 / -165.113	4.693 / 178.950	4.681 / 173.469

Figure 15. Results of the noise and AC voltage simulations

Creating a Matching Network

Determining Amplifier's Initial Input Impedance

- 1. Create a new schematic and name the cell **SP_amp**. This will be used to determine this input impedance (Zin).
- 2. In the new schematic, drag and drop the symbol for the amplifier.
- 3. From the **Simulation-S_Param** palette, insert the **S-parameter controller** and **port terminations**. Set the parameters for the S-Parameter block as follows:

Start = 4 GHz Stop = 10 GHz Step = 0.1 GHz

4. Add a VAR block and set L_val = 3.0. The finished schematic is shown in Figure 16.

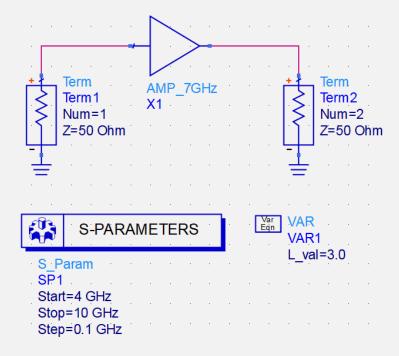


Figure 16. Schematic used for determining initial input impedance

- 5. Push into the **AMP_7GHz** amplifier sub-circuit and change the value of the capacitor connected to the drain, C2, to **1.5 pF**. Save the changes.
- 6. Pop out of the schematic to go back to the top-level schematic. Run the simulation.
- 7. In the new Data Display, insert a **Smith Chart** and add **S(1,1).**
- 8. Put a marker on the trace at 7 GHz. Double click on the marker to edit the properties. Under the Format tab, set **Z0** to **50**. Click **OK**. The marker impedance should show about 13.1-j62.8 at 7 GHz. This is shown in Figure 17. This value will be used for the match at the amplifier input next.
- 9. Save and close the schematic and data display.

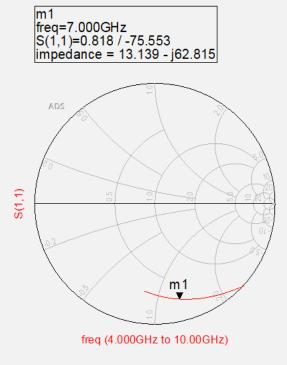


Figure 17. Smith Chart showing S(1,1)

Using Smith Chart Utility for Matching Network

The next step is to use the Smith Chart Utility to create a matching network for the amplifier.

- 1. Create a new schematic and name the cell **Z match**.
- 2. Open the Smith Chart Utility, which can be found under **Tools > Smith Chart**. The utility is shown in Figure 18.

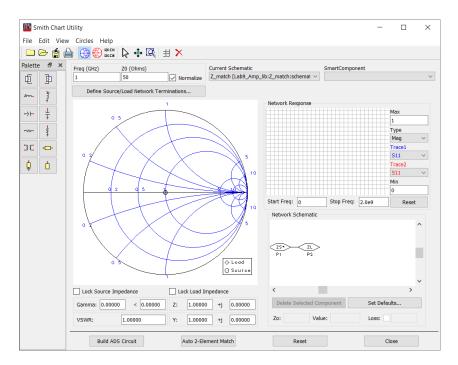


Figure 18. Smith Cshart Utility

- 3. At the top of the Smith Chart Utility window, click the **Palette** icon. It is the grid icon to the left of the red **X**. This will open the appropriate palette in the schematic.
- 4. Go back to the schematic window. From the palette, insert the **Smith Chart Matching Network** component, as shown in Figure 19. Click **OK** when a message dialog appears you can ignore it. This component is needed in order to use the Smith Chart Utility.

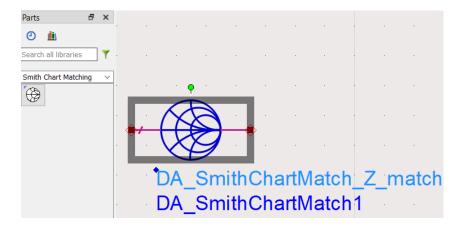


Figure 19. Smith Chart Matching Network component

5. Switch back to the Smith Chart Utility. Change the frequency **7.0 GHz**. When prompted, **select Update SmartComponent** from Smith Chart Utility, and click **OK**. This is shown in Figure 20.

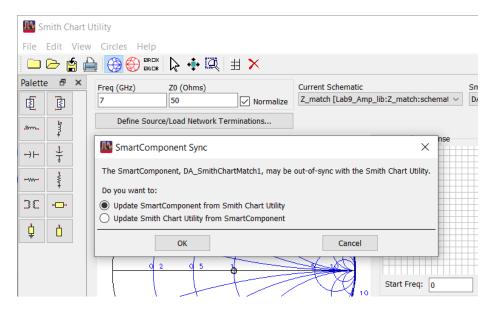


Figure 20. SmartComponent Sync message

6. In the lower right corner, select the ZL component in the Network Schematic section. Under Value, enter the approximate impedance looking into the amplifier from the load, which was found during the last section. For this lab, the value is 13.1-j*62.8. Press tab to accept the value. This is shown in Figure 21. Notice that the load symbol (diamond) on the Smith chart has relocated to the lower right of the Smith Chart.

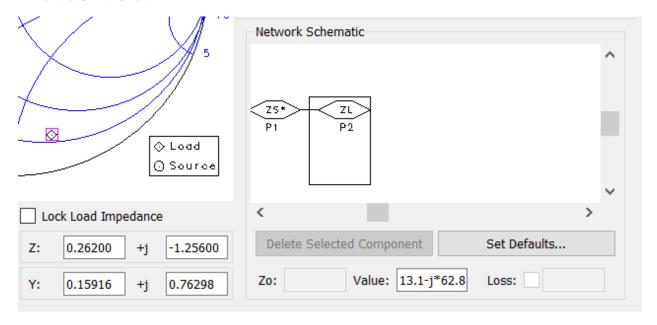


Figure 21. Changing the ZL value

7. To build the matching network, select the **shunt inductor** from the Smith Chart Utility palette. Move the cursor on the Smith chart to the 50 Ω circle of constant resistance. Left click on the Smith Chart to 'place' the shunt inductor, as shown in Figure 22. The placement does not have to be exact.

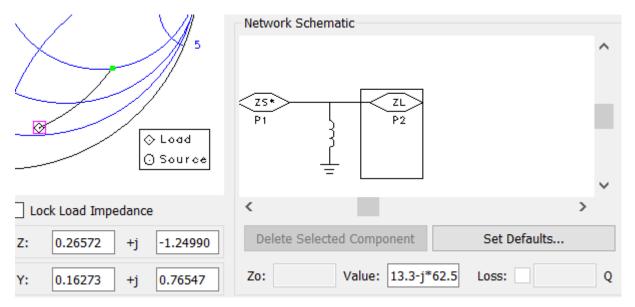


Figure 22. Placing the shunt inductor

8. Select the **series inductor** from the palette. Move the marker along the circle to the center of the Smith chart. Again, left click to place the series inductor, as shown in Figure 23.

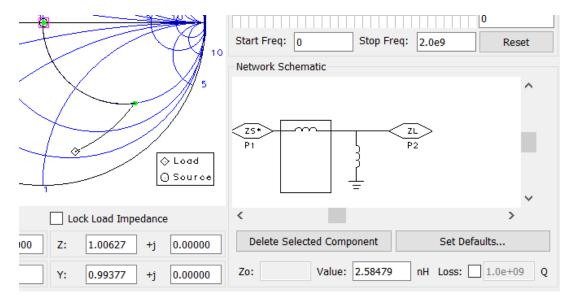


Figure 23. Placing the series resistor

- 9. In the Network Schematic section, select either shunt or series inductor to see the value.
- 10. To create the matching network, click the **Build ADS Circuit** button at the bottom of the Smith Chart Utility window. Close the Smith Chart Utility window.
- 11. In the Z_match schematic, push into the Smith Chart symbol to see the matching network, which is shown in Figure 24. Take note of the values and the topography. These will be used in the next section.

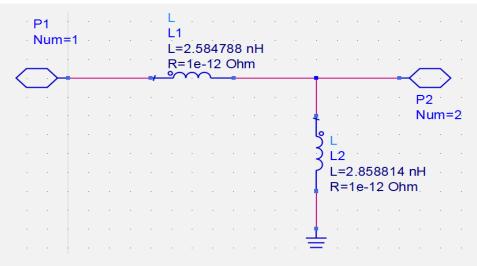


Figure 24. Matching network schematic

12. You can close any files used for the Smith chart matching – you don't need them. You only used the utility to design the matching network topology.

Analyzing the Impedance and Gain with a Matching Network

Using the matching network from the Smith Chart Utility, the next step is to incorporate the design to improve the results.

1. Go back to the **SP_amp** schematic. Add the series and shunt inductors to this schematic, as shown in Figure 25. Use the rounded values that you calculated.

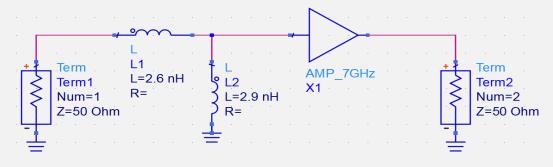


Figure 25. Amplifier schematic with matching network

- 2. When we simulate using this new circuit, all existing data will be overwritten. In order to preserve the old data, we will create a new dataset. To do this, go to Simulate > Simulation Settings. Under Output Setup, change the Dataset name (you may have to uncheck Use cell name) to SP_amp_matched. Press Simulate. If prompted, do not change the default dataset.
- 3. When the simulation finishes, go to your SP_amp Data Display. Edit (double-click) the Smith Chart. Under the dropdown, select the **SP_amp_matched dataset** and add the S(1,1) trace, as shown in Figure 26.

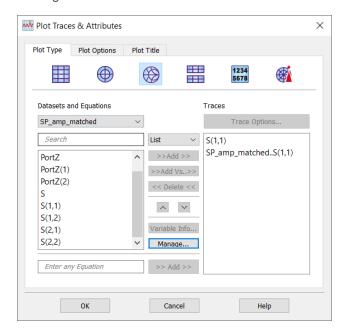


Figure 26. Adding S(1,1) from the matching network dataset

4. Place a marker on the new trace at 7 GHz. As shown in Figure 27, the amplifier input is now matched to 50 Ω. As with before, double click on the marker to change **Z0** to **50**, which can be found under the Format tab. Click **OK**. If you wanted to further optimize, you can create an output matching network.

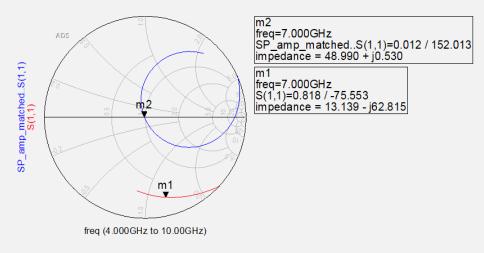


Figure 27. Smith Chart comparing S(1,1)

5. Insert a rectangular plot. Add S(2,1) from the **SP_amp** dataset and compare to the S(2,1) from the **SP_amp_matched** dataset. Figure 28 shows about a significant improvement in the gain by adding a matching network.



Figure 28. Plot comparing S(2,1)

6. Save and close the schematic and data display windows.

Amplifier Stability Analysis

Setup and Simulation of Unstable Amplifier

This part of the lab focuses on small signal stability analysis. A built-in ADS template is used for this lab.

- From the ADS Main window, open the My_Sys_AMP.7zads example. This can be found under File >
 Open > Example. Save the example in your preferred directory.
- 2. Open the schematic view for **a1_stability**. The schematic is shown in Figure 29. Notice that this circuit is very similar to the FET amplifier from the previous sections.

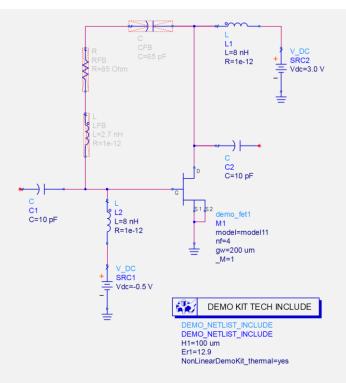


Figure 29. Amplifier Stability Template

3. In the schematic window, select **Insert > Template**. Scroll down and select **ads_templates:S_Params_DC**. This is shown in Figure 30.

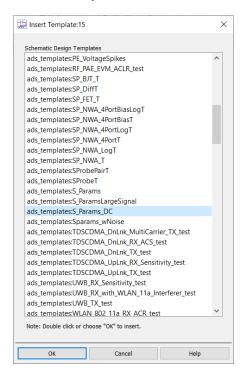


Figure 30. Insert Template Window

4. Clicking OK will load a ghost image, which is a collection of components and controllers. This is shown in Figure 31. Place these components on your schematic, so that it does not overlap the amplifier design.

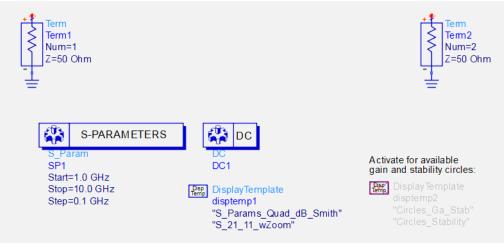


Figure 31. Template components

5. The template that you added has everything needed for analysis. Connect the two terminations to your design. Make sure to place Term1 on the input and Term2 on the output. The final schematic is shown in Figure 32.

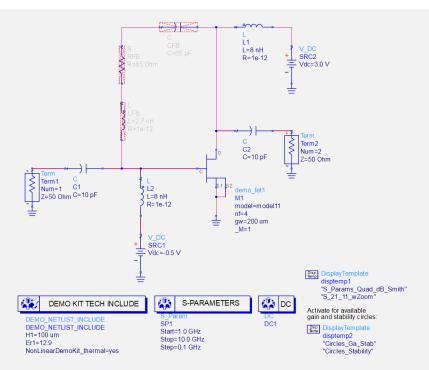


Figure 32. Final schematic with template added

- 6. Activate the **disptemp2** DisplayTemplate object.
- 7. Run the simulation. If you get an error stating there are no named nodes, select Run Anyway.
- 8. Once the Data Display window opens, you will see there are several tabs already configured. This was done by the DisplayTemplate object that was added to the schematic. Experiment with the frequency settings to see how the different parameters change.
- 9. In the third tab ("Circles_Ga_Stab"), move the RF Frequency Selector slider to **7 GHz**. Note that the Stability Factor is less than 1, indicating that it is potentially unstable.
- 10. In the fourth tab ("Circles_Stability"), observe the source and load stability circles and plot. Since mu_source and mu_load are both < 1, the circuit is potentially unstable.

Simulation of Stable Amplifier

From the previous analysis, it's clear that the amplifier is potentially unstable. In this section, the necessary stability circuit components will be added and their impact on results will be analyzed.

- 1. In the schematic window, activate the feedback components on the gate. All components should now be enabled.
- 2. Run the simulation.
- 3. In the Circles Ga Stab tab, notice that the Stability Factor is 1.105 at 7 GHz.
- 4. In the Circles_Stability tab, notice that both mu_source and mu_load are greater than 1 from 1 GHz to 10 GHz. This is shown in Figure 33. This is a sufficient condition for an unconditionally stable amplifier.

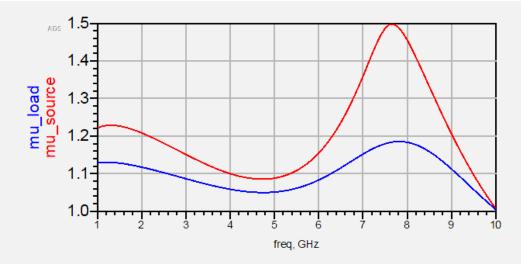


Figure 33. Graph of amplifier stability

5. Save and close the schematic and data display windows.

Running Optimizations

Set Up an Optimization Controller and Goals

In the remainder of this lab, you will perform an optimization for matching a FET amplifier to 50 Ω . This lab will cover the basics of using the optimizer and goals.

- 1. Open the schematic view for **a2_match_opt**. This is the same stable amplifier from the previous section with an added output match circuit formed by L3 and C3. The input match is formed by C1 and L2.
- 2. In this schematic, the optimization controller and the goals have been set up to save time. These components are located on the Optim/Stat/DOE palette.
- 3. Open the **OptimGoal1** setup window by double clicking on it. Notice that in the **Expression** field, the value **dB(S11)** means that when the simulation is performed, S(1,1) will be calculated in dB. This quantity will be used as our goal for the optimization. The analysis is set to **SP1**, which is the name of the S Parameter block. Frequency will be the swept variable, which means that the goals will be analyzed over the range of frequencies. This is shown in Figure 34.

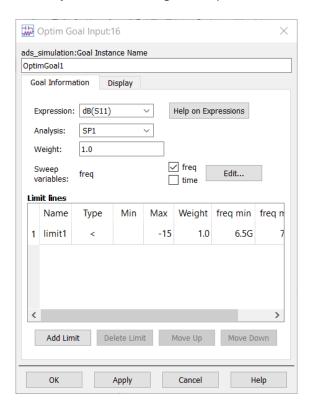


Figure 34. Optim Goal Input window

In the limit lines, the operator type has been set to < (less than). This tells the optimizer that this goal must be **below -15 dB** (max value) for a successful optimization. The minimum and maximum frequency are set to **6.5 GHz** and **7.5 GHz**, which establishes a 1 GHz frequency sweep centered around 7.0 GHz. Note that in the frequency fields, G is used in place of e9, as the default unit is Hertz.

Open the Optimization controller, **optim1**. The optimization type is currently set to gradient. For this example, a gradient search is more efficient. At the bottom of the screen, the maximum number of iterations is set to 50. If the optimization does not meet the goals within the maximum number of iterations, the optimization will stop.

NOTE: The 'Save' parameters on the Optim controller that are set to 'no', means that those values will not be written into the dataset.

Setting Up Parameters to be Optimized

Now that the optimization has been set up, it is time to select the components whose values are to be optimized.

- 1. Edit (double click) the input capacitor (C1). Click the **Tune/Opt/Stat/DOE Setup** button. This window is shown in Figure 35.
- 2. In the Optimization tab, set the **Optimization Status** to **Enabled**. Make sure the **type** is set to **Continuous**. Define the range as **0.5 pF** to **20 pF**. Click **OK** twice to return to the schematic. You will see that the capacitor value is set to **10 pF {o}**. The {o} means that the value is being optimized.

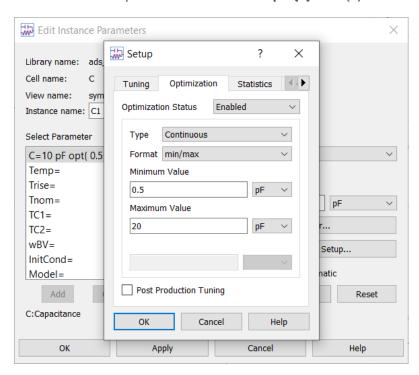


Figure 35. Optimization Setup window

This same process can be used on any optimization. However, there is another way to control variables for optimization, which is especially helpful if multiple variables are to be tuned, optimized, or used for statistical analysis.

- Go to Simulate > Simulation Variables Setup. Select the Optimization tab and notice that your enabled capacitor and values appear. This setup makes it easy to set multiple parameters or variables.
- 4. Set capacitor **C3** and inductors **L2** and **L3** to be optimized (check box) with the values shown in Figure 36. Press **OK** when complete.

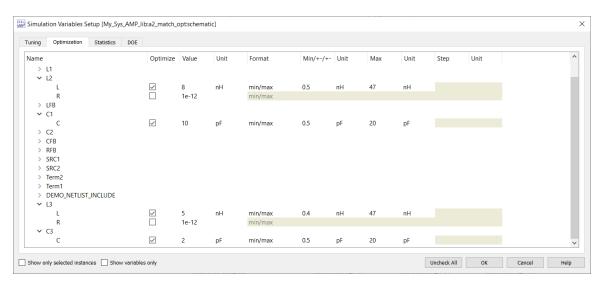


Figure 36. Simulation Variable Setup window

Running the Optimization

- 1. Press **Optimize** to run the optimization. The Optimize icon is the green and red arrow. It can also be found under **Simulate > Optimize**.
- 2. The Optimization Cockpit and Data Display will open. When the optimization is completed successfully, the optimization will pause. This is shown in Figure 37.

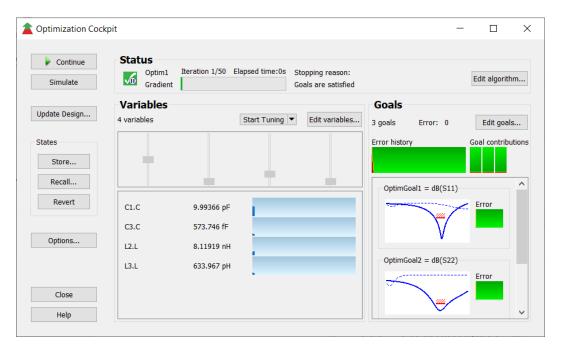


Figure 37. Optimization Cockpit window

- 3. After the optimization is complete, switch to the Data Display (a2_match_opt). On the rectangular plot, move the line markers to 6.5 GHz and 7.5 GHz. On the Smith chart, set the markers to 7 GHz. Notice that all the goals were met, meaning S11 < -15 dB, S22 < -15 dB and S21 > 15 dB. The plots are shown in Figure 38.
- 4. Close out of the Optimization Cockpit. In the window that opens, select **Don't Update the Design**. The optimization will not change the component values. If you wanted to change the component values to match the optimization, simply select **Update the Design**.
- 5. Save and close the schematic and the data display.

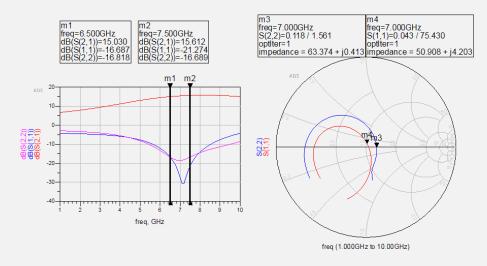


Figure 38. Rectangular and Smith Chart plots of S(1,1), S(2,1), and S(2,2)

Conclusion

Congratulations! You have completed Microwave Amplifier Design and Smith Chart Utility for Matching Networks. Check out more examples at www.Keysight.com/find/eesof-ads-rfmw-examples.

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at: www.keysight.com/find/contactus

