

Keysight Technologies

B4621B Bus Decoder for DDR2, DDR3, or DDR4 Debug and Validation

Data Sheet

Physical Address	DDR Bus Decode	Cycle Type
Click here for trigger menu		
21F4 3140	Write CS-0 BA-2	Write Command
	Row Address = 0x0fa1	*
	Col Address = 0x228	*
	Burst Type = Sequential (0, 1, 2, 3, 4, 5.	*
21F4 3140	mem write 0x196c4d0d dbffb1aaa	*
21F4 3148	mem write 0x46b093d1 f6167656	*
21F4 3150	mem write 0x877dd63d 6d75accf	*
21F4 3158	mem write 0xd14b042a 5fe89e29	*
21F4 3160	mem write 0x1dc85d8b faf17a8b	*
21F4 3168	mem write 0x10524112 0b388b63	*
21F4 3170	mem write 0x3cfd79bd 2833e9c2	*
21F4 3178	mem write 0x6ecfbbae 4451c4db	*
	Deselect	Data Read
	Deselect	Data Read
	Deselect	Data Read
	Deselect	Data Read
	Deselect	Idle
	Deselect	Idle
	Activate CS-0 BA-6	Activate Command
	Row Address = 0x0091	*



Unlocking Measurement Insights



Introduction

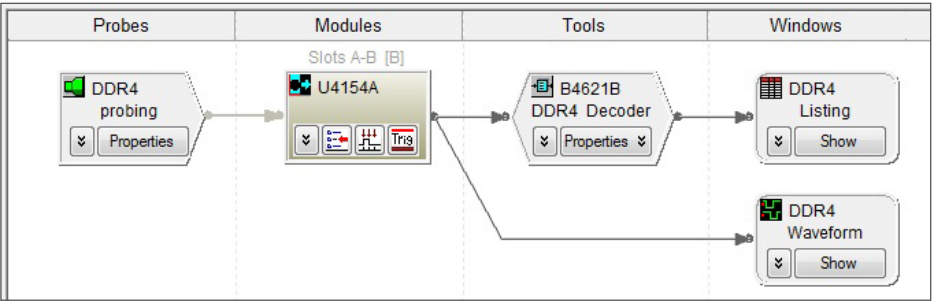
Accelerate your time to insight using the B4621B bus decoder for DDR2, DDR3, or DDR4 debug and validation. The B4621B provides complete protocol decode of memory transactions using a Keysight Technologies, Inc. logic analyzer as the analysis execution engine. (Select your logic analyzer module depending on your system data rate.)

The B4621B protocol-decode software translates acquired signals into easily understood, colorized, bus transactions showing associated data bursts for double-edge data-rate captures up to 2.5 Gb/s.

Valid read and write commands are decoded to include row and column addresses and the complete data burst associated with the command. The B4621B bus decode software anticipates key system attribute inputs (burst length, CAS latency and CAS write latency, chip selects) from default DDR2, DDR3, or DDR4 probing configurations and/or DDR Setup Assistant tool to accelerate decode of DDR2, DDR3, or DDR4 bus signals.

Description

After installing the logic analyzer software and the B4621B software and loading the default configuration for your DDR memory, the B4621B icon will show up in the Keysight logic analyzer overview window between the logic analyzer module and the listing.



DDR4 example showing B4621B icon in Keysight logic analyzer overview window, between logic analyzer module and listing.

The properties button on the B4621B icon allows the selection of memory variables. Typically, preferences are filled out for you in default configurations for specific DDR probes and by the DDR Setup Assistant software tool ¹, which walks you through state mode setups.

The screenshot shows the 'DDR System Configuration' window. It has two main sections: 'Chip Selects' and 'Memory Configuration'. The 'Chip Selects' section lists 16 chip selects (0-15), each with a checkbox and a dropdown menu set to 'CKE0'. The 'Memory Configuration' section includes: 'Memory Type' (DDR4), 'Memory Width' (64), 'Row Bits' (15), 'Column Bits' (10), 'Bank Group Bits' (2), 'CAS Latency' (11.0), 'CAS Write Latency' (10.0), 'Burst Type' (Sequential), 'Burst Length' (8), and a 'DM Enable' checkbox. Below these is the 'Physical Address Construction' section with three radio buttons: 'BA Row Address Column Address' (selected), 'Row Address BA Column Address', and 'User supplied .NET assembly'. A 'Browse...' button is next to the 'User supplied .NET assembly' option. At the bottom, there is a 'Physical Address Summary' section showing a 32-bit address (39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0) with corresponding colored boxes (grey, cyan, red, yellow, green) and a '000' value for the last three bits. At the bottom are 'OK', 'Cancel', and 'Help' buttons.

B4621B window with DDR4 setting example.

Key features and benefits

- Decodes DDR2, DDR3, or DDR4 acquired traces on Keysight logic analyzer or off-line
- Displays commands, protocol transaction type, physical/ row/column/bank addresses, and data in the listing viewer
- Data is displayed at any level of detail from protocol to binary
- Anticipates key system attribute inputs from default probing configurations and/or DDR Setup Assistant tool
- Allows user input to customize system attributes

1. DDR Setup Assistant and Eyefinder software is available free of charge. DDR Setup Assistant provides a series of semi-automated steps to simplify state mode measurements for DDR2, DDR3, DDR4, LPDDR2, and LPDDR3 with U4154A or 16962A logic analyzer modules. The DDR Setup Assistant and Eyefinder software also provides a DDR Eyefinder tool specifically for the 16962A module using the read and write data valid windows for accurate sampling of data.

Keysight's 4.0 GB/s U4154A logic analysis module is recommended for all DDR2, DDR3, and DDR4 configurations.

The B4621B bus decoder for DDR2, DDR3, or DDR4 debug and validation operates with the following Logic Analyzers from Keysight Technologies. Logic analyzer selection criteria includes: logic analyzer specifications and characteristics, maximum DDR technology data rate, and minimum data valid windows of the data eyes at the logic analyzer probe point.

Logic analyzer recommendations

Keysight logic analysis module recommendations for DDR2/3/4 memory technologies	DDR2	DDR3	DDR4
U4154/B	Yes	Yes	Yes
16962A	Yes	Yes, up to DDR3 1867	No
16950B	Yes, up to DDR2 667	No	No
16951B	Yes, up to DDR2 667	No	No
16910A/11A with option 500	No	No	No
16800A series with option 500	No	No	No

Refer to www.keysight.com/find/logic for a comparison view of Keysight logic analyzer modules.

Refer to your logic analyzer module data sheet or specific DDR2/3/4 probing solution for logic analyzer module configurations.

Default configurations for the B4621B bus decoder for DDR2, DDR3 or DDR4 debug and validation are loaded for standard BGA (ball grid array), DIMM and SODIMM interposers with the B4621B software.

Default configurations speed setup and are easily modified

For custom embedded DDR technology applications, refer to on-line help in the logic analyzer software application for details on the B4621B bus decoder label requirements. For new embedded application configurations, Keysight recommends loading one of the existing default configurations that most closely matches your application and modifying that configuration for your unique embedded system.

Related literature

Publication title	Pub number
<i>U4154B Logic Analyzer Module - Data Sheet</i>	5992-0108EN
<i>U4154A AXIe-Based Logic Analyzer Module - Data Sheet</i>	5990-7513EN
<i>Keysight 16900 Series Logic Analysis Systems - Brochure</i>	5989-0420EN
<i>W3630A Series DDR3 BGA Probes for Logic Analyzers and Oscilloscopes - Data Sheet</i>	5990-3179EN
<i>B4623B Bus Decoder for LPDDR, LPDDR2, or LPDDR3 Debug and Validation - Data Sheet</i>	5991-1064EN

Ordering information

Required/recommended software	
Logic and protocol analyzer software (required)	
B4621B (required)	Bus decoder for DDR2, DDR3, or DDR4 debug and validation
DDR Setup Assistant and DDR Eyefinder (recommended)	
Related software	
B4621U	Upgrade from B4621A to B4621B Bus decoder for DDR2, DDR3, DDR4 (requires a prior license for the B4621A)
B4622B	Protocol Compliance and Analysis toolset for DDR2/3/4 and LPDDR/2/3
B4623B	Bus decoder for LPDDR, LPDDR2, LPDDR3 Debug and Validation

For software downloads refer to www.keysight.com/find/la-sw-download.

For additional analysis software, refer to www.keysight.com/find/logic-sw-apps

Related products	
U4154A	Logic analyzer module
16962A	Logic analyzer module
16950B	Logic analyzer module

For DDR/2/3/4 memory probing options, refer to:

U4154B logic analyzer data sheet, 5992-0108EN.

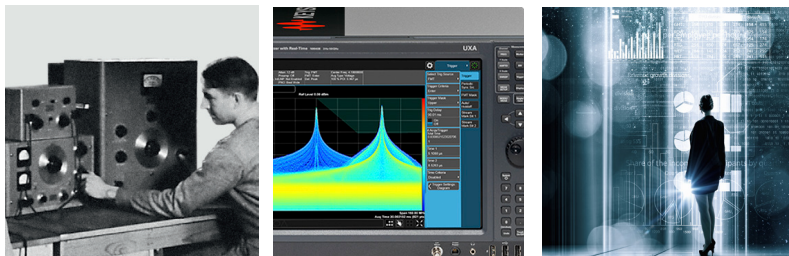
Information on FuturePlus DIMM and SODIMM interposers for DDR2, DDR3, and DDR4. is available at: <http://www.futureplus.com>.

For additional DDR/2/3/4 probing options, contact your local Keysight representative www.keysight.com/find/contactus.

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