

Keysight Technologies

N4968A Clock and Data Demultiplexer 44 Gb/s

Data Sheet



Features

- Clock and data demultiplexer for lower-rate BER measurements
- 3.5 to 44 Gb/s operation
- Demux-by-2 or demux-by-4
- Integrated phase shifter for highspeed clock and data alignment
- Differential or single-ended input
- Adjustable sub-rate clock output

Description

The Keysight N4968A clock and data demultiplexer 44 Gb/s is a small highperformance 3.5 to 44 Gb/s clock and data demultiplexer, designed to simplify the process of making highbitrate BER measurements at half-or quarter-rate speeds. The N4968A clock and data demultiplexer 44 Gb/s is capable of operating in demux-by-4 up to 44 Gb/s data rate or in demuxby- 2 up to 22 Gb/s data rate with an adjustable sub-rate clock output for triggering BER testers, oscilloscopes, logic analyzers, or other instruments.

N4968A Clock and Data Demultiplexer specifications

Data Input	
Data rate	3.5 to 44 Gb/s
Data amplitude	150 to 1000 mV p-p single-ended. Maximum DC voltage ± 0.5 V
Interface	Differential. DC coupled, 50 Ω nominal, 1.85 mm female connectors. Can be used single-ended if unused input is terminated with 50 ohm load
Data Output	
Data rate	0.875 to 11 Gb/s
Data amplitude	> 210 mV p-p typical
Interface	Single-ended outputs. AC coupled, 50 Ω nominal, 2.92 mm female connectors
Clock Input	
Type	Half-rate clock for demux-by-4 mode. Full-rate clock for demux-by-2 mode.
Frequency	1.75 to 22 GHz for demux-by-4 mode ¹ 3.5 to 22 GHz for demux-by-2 mode ²
Clock amplitude	+2 to +10 dBm (0.8 to 2 V p-p)
Interface	Single-ended input. AC coupled, 50 Ω nominal, 2.92 mm female connector
Divided Clock Outputs	
Division ratios	1, 2, 4, 8, 16, 32, and 64
Clock amplitude	> -5 dBm (355 mV p-p) typical
Interface	Differential outputs. AC coupled, 50 Ω nominal, SMA mm female connectors. Can be used single-ended if unused input is terminated with 50 ohm load

1. Demux-by-4 mode data rate is 3.5 to 44 Gb/s

2. Demux-by-2 mode data rate is 3.5 to 22 Gb/s

N4968A Clock and Data Demultiplexer

Block diagram

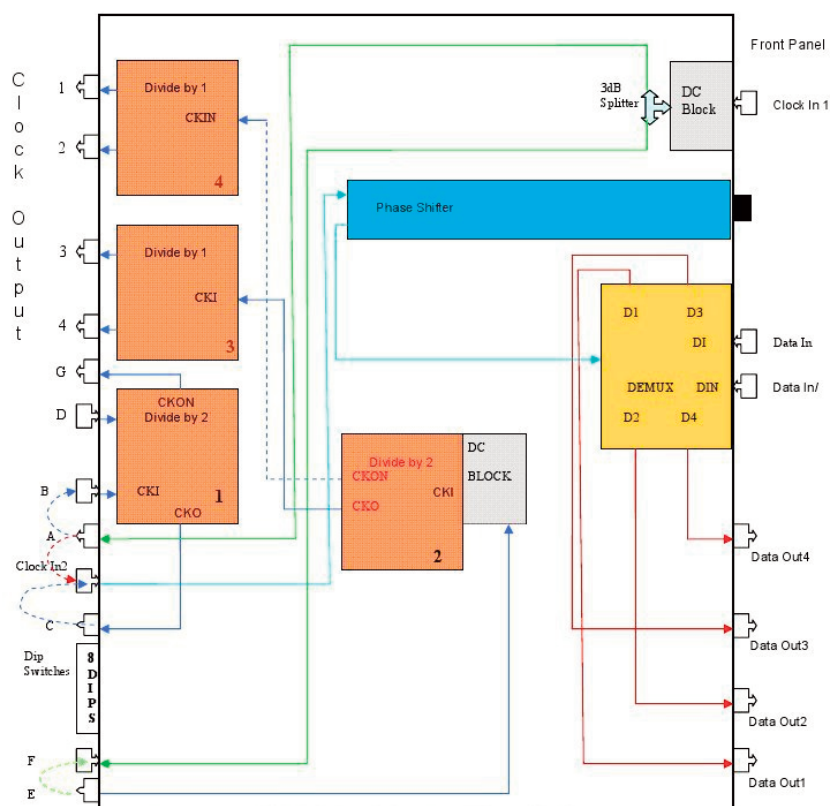


Figure 1. N4968A clock and data demultiplexer 44 Gb/s

Figure 1. N4968A clock and data demultiplier 44 Gb/s

Demux-by-4 Example with 40 Gb/s Data Input

- Configuration:
 - Data input = 40 Gb/s
 - Clock input = 20 GHz
 - Data output = 4 x 10 Gb/s
 - Clock output = 10 GHz
- Loop A to Clk2 (provide 20 GHz half-rate clock to Demux).
- Loop E to F.
- Set Divider 2 to $\frac{1}{2}$.
- Set Divider 3 and 4 to 1 (provides 10 GHz clock output).

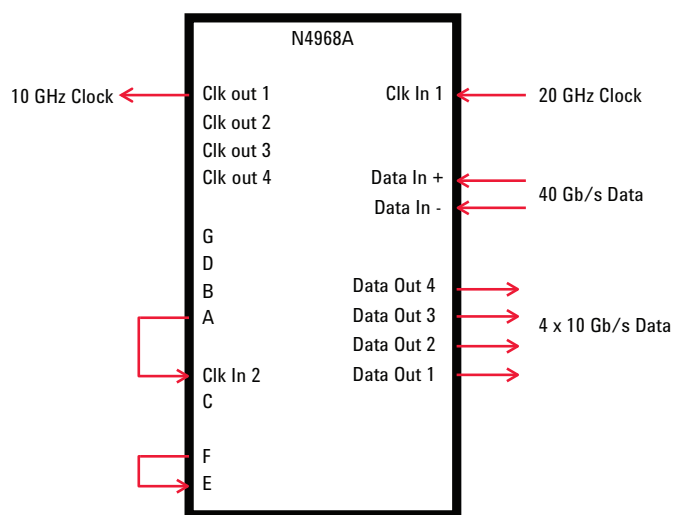


Figure 2. Demux-by-4 with 40 Gb/s data input

Demux-by-2 Example with 20 Gb/s Data Input with Full Rate Clock

- 1. Configuration:
 - Data input = 20 Gb/s
 - Clock input = 20 GHz
 - Data output = 2 x 10 Gb/s
 - Clock output = 10 GHz
- 2. Loop A to Clk2 (provide 20 GHz full-rate clock to Demux).
- 3. Loop E to F.
- 4. Set Divider 2 to 1/2.
- 5. Set Divider 3 and 4 to 1 (provides 10 GHz clock output).

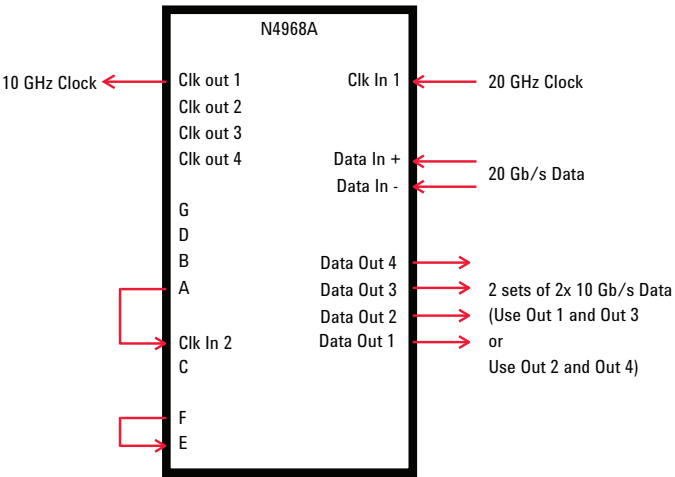


Figure 3. Demux-by-2 with 20 Gb/s data input

Specifications

General and Mechanical Parameters	
Operating temperature	+10 to +40 °C
Storage temperature	-40 to +70 °C
Power requirements	42 W External AC Adaptor (included) – 100 to 240 V AC, 47 to 63 Hz, 1.35 A
Physical dimensions (W x H x D)	25.4 x 6.35 x 25.4 cm (7 x 2.5 x 10 inches)
Weight	3.2 kg (7 lbs)

Regulatory standards

EMC

Complies with European EMC Directive 2004/108/EC

- IEC/EN 61326-1
- CISPR Pub 11 Group 1, class A
- AS/NZS CISPR 11
- ICES/NMB-001

This ISM device complies with Canadian ICES-001.
Cet appareil ISM est conforme a la norme NMB-001 du Canada.

Ordering information

N4968A clock and data demultiplexer 44 Gb/s.

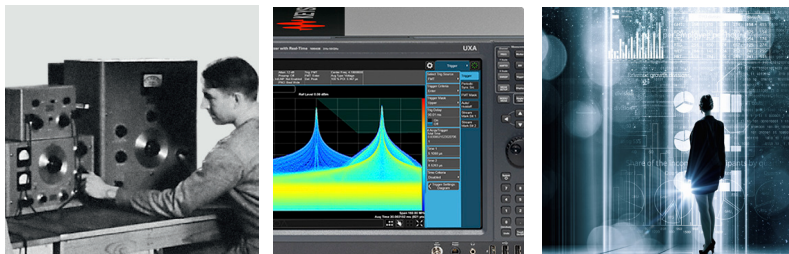
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