Highly cost effective solution for characterizing crosstalk susceptibility, backplanes and multi-lane serial data systems

Product Highlights

- Modular architecture supports 1 to 5 pattern generator or error detector heads
- Pattern generators with integrated two or four tap de-emphasis
- Transparent jitter pass-through from external clock source
- Swept aggressor channel delay for crosstalk characterization
- Single port remote control of all channels through USB or GPIB
- Compact size

A Better Solution When One Channel is Just Not Enough...

The N4965A multi-channel BERT is a modular, multi-channel signal integrity test system ideal for characterizing multi-lane serial data channels. By adding remotely mountable heads, each of its 5 channels can be configured as either a pattern generator, or error detector to form a bit error rate tester (BERT). Patterns available include various lengths of hardware generated PRBS, clock patterns, and DC logic 0 and logic 1. All heads can operate with differential or single ended signal connections. Output parameters in the pattern generator heads and input parameters in the error detector heads can be independently programmed, or ganged together for convenience. Presets for common logic families simplify user set up.

Integrated De-Emphasis

Pattern generator heads include integrated two-tap or four-tap de-emphasis conditioning. Commonly used in higher data rate systems to open eyes by counteracting high frequency loss in the channel, applying de-emphasis to the test signal is required for receiver testing. Other vendors' generators require additional dedicated external signal processors. The internal de-emphasis conditioning in the N4955A pattern generator heads eliminates the expense of additional signal processors, as well as the associated signal degradation resulting from the extra cables used to connect them.

Independent Generator and Detector Heads

Each remote head connects to the N4965A multi-channel BERT controller through a 1 m control cable. This allows the remote head to be located near the signal connection points in the device under test, minimizing cable loss, and maintaining signal integrity.
Control Interface and Analysis Software

Controlling multiple pattern generators or signal sources for characterizing multi-lane devices or cross talk is cumbersome and confusing. In addition to the need to address multiple instruments, the command syntax or user interface usually differs. The N4980A multi-instrument BERT software application provides users the ability to control multiple Keysight Technologies, Inc. instruments through a graphical user interface (GUI).

Set up is easy using the N4980A multi-instrument BERT software application. For repetitive testing, setups can be stored and recalled at a later time.

The base software is free of charge and in addition to instrument control, also allows you to perform measurements such as single-channel BER, multi-channel BER (with an unlimited number of channels), and bathtub measurements.

The N4980A–JTS jitter tolerance software package can be added to the base software. This package includes multi-channel jitter tolerance testing and has a built-in template editor for creating templates to meet the testing criteria of the most common standards. This package requires a license to use.

The multi-channel BER results view shows composite BER along with the performance of the individual lanes. Bar graphs give a quick indication of any lane specific problems without the need to look at the individual BER numbers.
Characterizing Crosstalk Susceptibility

Characterizing your system or backplane for crosstalk susceptibility has been a difficult challenge in the past. Serial BERTs are often used for this purpose, utilizing a full rate or 2X multiplied clock output for the adjacent channel aggressor signal. But does this really stress your DUT adequately?

Generally the receiver is only susceptible to crosstalk induced errors when the transitions occur in the sampling window of the detector. The use of a double rate clock as the aggressor does not assure that the transitions will occur in the detector decision time window, as the clock to data skew in the BERT, the skew in the signal path lengths, and the receivers clock recovery latency all combined, rarely results in signal alignment.

The N4965A multi-channel BERT configured with multiple pattern generator heads to be used as aggressors, overcomes this problem by independently sweeping the phase delay of each of the aggressor generators up to ± 2 UI relative to the reference generator. The delay sweep modulation signal is a low frequency triangular wave, assuring adequate dwell time in the sensitive detector decision time window.

For multi-lane systems and backplanes, multiple generator heads can be programmed to independently sweep multiple aggressor paths. Each channel uses a different low modulation frequency.

Figure 5. Sweeping multiple aggressor paths.

Figure 6. Fixed delay aggressors – Testing with fixed delay aggressors can result in induced interference outside of the critical receiver sampling time window, which is the center of the eye.

Figure 7. Slewing delay of aggressors – Slewing the delay of the aggressor assures impairment will occur during the sampling window.
Multi-lane device testing timing diagram

Multi-lane devices and SERDES are best characterized with live traffic on all lanes. The N4965A Multi-Channel BERT provides a convenient source of up to 5 lanes of non-synchronized PRBS patterns. The phase delay of all lanes relative to the reference lane can be adjusted independently, or even swept to test for framing errors.

Parallel testing single lane devices

100% or batch sample testing single lane devices in a production environment can be expensive in capital costs of the instruments, and test times.

Systems based on the N4965A multi-channel BERT for parallel testing of multiple devices are cost effective and simple to implement.

Configurations based on a single system allow implementation of two independent channels of serial BERT, up to five independent pattern generators, or single shared pattern source with four independent error detectors.
N4965A Multiple Clock Domains

The N4965A multi-channel BERT controller has two clock domains, Ref and Aux. The default condition is that all 5 channels and the divided clock outputs operate from the external clock connected to the Ref Clock input. Alternatively, the controller can be configured to operate Channels 1 through 4 from the Aux Clock input. This is useful in applications such as crosstalk testing with multiple pattern generators, where a victim generator, connected to Channel 0, operates from an external reference clock, while the aggressor generators, connected to channels 1 through 4, can operate asynchronously from an external auxiliary clock. Another crosstalk application for the two clock domains is to apply jitter injection stress to the victim while maintaining a clean clock for the aggressor channels. This can be done synchronously with an external clock source such as the N4960A or N4963A which provide both stress and unstressed clock outputs.

Figure 11. Asynchronous clocking example.

Figure 12. Stressed/unstressed clocking example.
## N4965A Controller Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input clock frequency</strong></td>
<td>1.0 to 12.5 GHz</td>
</tr>
<tr>
<td><strong>Input clock amplitude</strong></td>
<td></td>
</tr>
<tr>
<td>Reference input</td>
<td>-5 to +10 dBm (350 mV to 2 V p–p) for frequencies &lt; 6.5 GHz</td>
</tr>
<tr>
<td>Auxiliary input</td>
<td>0 to +10 dBm (630 mV to 2 V p–p) for frequencies ≥ 6.5 GHz</td>
</tr>
<tr>
<td></td>
<td>-10 to +10 dBm (200 mV to 2 V p–p) at all frequencies</td>
</tr>
<tr>
<td><strong>Residual jitter</strong></td>
<td>1.2 ps rms typical</td>
</tr>
<tr>
<td><strong>Divided clock output</strong></td>
<td></td>
</tr>
<tr>
<td>Divider ratio</td>
<td>1, 2, 4, 8 to 512 in steps of 1</td>
</tr>
<tr>
<td></td>
<td>514 to 1024 in steps of 2</td>
</tr>
<tr>
<td></td>
<td>1028 to 2048 in steps of 4</td>
</tr>
<tr>
<td></td>
<td>2056 to 4096 in steps of 8</td>
</tr>
<tr>
<td></td>
<td>Waveshape of divided clock slower than ~1 MHz will be differentiated</td>
</tr>
<tr>
<td><strong>Configuration</strong></td>
<td>Differential; will operate in single ended mode</td>
</tr>
<tr>
<td><strong>Amplitude</strong></td>
<td>0.3 to 0.7 V in 5 mV steps, single ended</td>
</tr>
<tr>
<td><strong>Output offset</strong></td>
<td>-2.0 to +2.0 V in 5 mV steps</td>
</tr>
<tr>
<td><strong>Termination voltage</strong></td>
<td>-2.0 to +2.0 V in 5 mV steps</td>
</tr>
<tr>
<td><strong>Rise/fall time (20% to 80%)</strong></td>
<td>25 ps maximum</td>
</tr>
<tr>
<td><strong>Clock input/output connectors</strong></td>
<td>SMA female</td>
</tr>
</tbody>
</table>

### Notes:

1. From 1.5 to 12.5 GHz, using N4960A clock/controller as the external clock source.
2. At 12.5 GHz, amplitude = 0.7 V, division ratio = 1
N4955A 12.5 Gb/s Pattern Generator Remote Head Specifications

**Signal configuration**
- Differential; will operate in single-ended mode

**Data line coding**
- Non-return to zero (NRZ)

**Output data rate**
- 1.0 to 12.5 Gb/s (timing parameter determined by N4965A controller)

**Patterns**
- PRBS $2^n - 1, n = 7, 10, 15, 23, 31$

**Divided clock patterns**
- **N4955A–P12**
  - Divide by 2, 4 e.g. $\div 2 = 1010$ pattern, $\div 4 = 1100$ pattern
- **N4955A–D12**
  - Divide by 2, 4, 8, 16, 32, 64
  - e.g. $\div 2 = 1010$ pattern, $\div 4 = 1100$ pattern; $\div 64 = 32 \times '1's$ followed by $32 \times '0's$

**Pattern invert**
- Available on all patterns except divided clock patterns

**Output amplitude**
- **N4955A–P12**
  - 0.2 to 2.0 V p-p single-ended, 5 mV resolution
- **N4955A–D12**
  - 0.6 to 1.2 V p-p single-ended, 5 mV resolution

**Rise/fall times (20% to 80%)**
- **N4955A–P12**
  - 30 ps maximum, 24 ps typical
- **N4955A–D12**
  - 25 ps maximum, 20 ps typical

**Additive jitter**
- 2.5 ps rms typical for data rates < 1.5 Gb/s
- 1.2 ps rms typical for data rates ≥ 1.5 Gb/s

**Output offset**
- $-1.8$ to $+1.8$ V in 5 mV steps

**Termination voltage**
- $-2.0$ to $+2.0$ V in 5 mV steps

**Cross over**
- 20 to 80% in 1% steps

**De-emphasis**
- **N4955A–P12, 2-tap (1 post cursor)**
  - Pre-cursor $0$ to $+8$ dB in 0.1 dB steps
  - Post1 cursor $0$ to $-10$ dB in 0.1 dB steps
- **N4955A–D12, 4-tap (1 pre-cursor, 2 post-cursor)**
  - Pre-cursor $0$ to $+8$ dB in 0.1 dB steps
  - Post2 cursor $0$ to $-8$ dB in 0.1 dB steps (Combination of post1 and post2 limited to $-10$ dB)

**Error injection (N4955A–D12 only)**
- Single error injection or injection rates with BER = $10^{-N}$, $N = 3, 4, 5, 6, 7, 8, 9$

**Delay range**
- $\pm 1,000$ UI, 1 mUI steps (timing parameter determined by N4965A controller)

**Skew range**
- $\pm 99.999$ UI, 1 mUI steps (timing parameter determined by N4965A controller)

**Delay sweep**
- 0, 1, 2, 4 UI p-p (timing parameter determined by N4965A controller)

**Data connectors**
- 2.92 mm female

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N4956A 12.5 Gb/s Error Detector Remote Head Specifications

**Signal configuration**
- Differential; will operate in single-ended mode

**Data line coding**
- Non-return to zero (NRZ)

**Output data rate**
- 1.0 to 12.5 Gb/s (timing parameter determined by N4965A controller)

**Patterns**
- PRBS $2^n - 1, n = 7, 10, 15, 23, 31$

**Maximum input amplitude**
- 2.0 V p-p single-ended

**Input sensitivity**
- < 0.1 V p-p single-ended

**Threshold adjustment**
- – 1.0 to $+1.0$ V in 1 mV steps

**Termination voltage**
- – 2.0 to $+2.0$ V in 5 mV steps

**Delay range**
- $\pm 1,000$ UI, 1 mUI steps (timing parameter determined by N4965A controller)

**Autoalign**
- Set optimum 0/1 threshold and data delay

**Threshold**
- 5 to 20 mV in 1 mV steps

**Delay**
- 5 to 20 mUI in 1 mUI steps

**BER measurement period**
- 0 to 99,999,999 seconds in 1 msec steps

**BER results**
- Bit error rate, error count, bit count, measurement seconds

**Phase margin**
- > 0.6 UI typical @ 10 Gb/s, 2$^{31}$-1 PRBS

**Data connectors**
- 2.92 mm female

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1. From 1.5 to 12.5 Gb/s, at 1 V p-p amplitude
2. At 0.7 V p-p amplitude
3. Using N4960A clock/controller as the external clock source.
### Physical and Environmental

<table>
<thead>
<tr>
<th>Remote control interface</th>
<th>USB2.0 and IEEE-488 (GPIB)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power requirements</strong></td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>100 to 240 VAC, auto-ranging</td>
</tr>
<tr>
<td>Frequency</td>
<td>50 to 60 Hz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>170 W maximum</td>
</tr>
<tr>
<td>Temperature, operating</td>
<td>+10 to +40 °C</td>
</tr>
<tr>
<td>Temperature, non-operating</td>
<td>-40 to +70 °C</td>
</tr>
<tr>
<td><strong>Dimensions (height, width, and depth)</strong></td>
<td></td>
</tr>
<tr>
<td>N4965A</td>
<td>100 mm (3.9 in) x 214 mm (8.4 in) x 425 mm (16.7 in)</td>
</tr>
<tr>
<td>N4955A–P12</td>
<td>33 mm (1.3 in) x 72 mm (2.8 in) x 130 mm (5.1 in)</td>
</tr>
<tr>
<td>N4955A–D12</td>
<td>33 mm (1.3 in) x 72 mm (2.8 in) x 130 mm (5.1 in)</td>
</tr>
<tr>
<td>N4956A–E12</td>
<td>33 mm (1.3 in) x 72 mm (2.8 in) x 130 mm (5.1 in)</td>
</tr>
<tr>
<td><strong>Weight</strong></td>
<td></td>
</tr>
<tr>
<td>N4965A</td>
<td>3.3 kg (7.1 lbs)</td>
</tr>
<tr>
<td>N4955A–P12</td>
<td>0.38 kg (13.4 oz)</td>
</tr>
<tr>
<td>N4955A–D12</td>
<td>0.38 kg (13.4 oz)</td>
</tr>
<tr>
<td>N4956A–E12</td>
<td>0.38 kg (13.4 oz)</td>
</tr>
</tbody>
</table>

Table 4.

### Regulatory Standards

**EMC**
- CISPR Pub 11 Group 1, Class A
- AS/NZS CISPR 11
- ICES/NMB–001
- This ISM device complies with Canadian ECES–001.
  - Cet appareil ISM est conforme à la norme NMB–001 du Canada.

**Safety**
- Complies with European Low Voltage Directive 2006/95/EC
  - Canada: CSA C22.2 No. 61010–1
  - USA: UL std no. 61010–1, 2nd Edition

**German Acoustic statement**
- Acoustic noise emission
  - LpA < 70 dB
- Operator position
  - Am Arbeitsplatz
- Normal position
  - Normaler Betrieb
- Per ISO 7779
  - Nach DIN 45635 t.19

Table 5.
Configuration Guide

Step 1. Select a clock synthesizer

<table>
<thead>
<tr>
<th>Description</th>
<th>N4963A</th>
<th>N4963A-101</th>
<th>N4960A-CJ0</th>
<th>N4960A-CJ1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency, 13.5 GHz</td>
<td>•</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency, 16 GHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single tone sinusoidal jitter</td>
<td>•</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multi-tone sinusoidal jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Random jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Periodic jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spread spectrum clock</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 6.

Step 2. Select the controller

<table>
<thead>
<tr>
<th>Description</th>
<th>N4965A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-channel BERT controller</td>
<td></td>
</tr>
</tbody>
</table>

Table 7.

Step 3. Select the pattern generator(s)

<table>
<thead>
<tr>
<th>Description</th>
<th>N4955A-P12</th>
<th>N4955A-D12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate, 12.5 Gb/s</td>
<td>•</td>
<td></td>
</tr>
<tr>
<td>Patterns, PRBS $2^n - 1$, n = 7, 10, 15, 23, 31</td>
<td>•</td>
<td></td>
</tr>
<tr>
<td>Patterns, divided clock (divide by 2/4)</td>
<td>•</td>
<td></td>
</tr>
<tr>
<td>Patterns, divided clock (divide by 8/16/32/64)</td>
<td>•</td>
<td></td>
</tr>
<tr>
<td>Output amplitude, 0.2 to 2.0 V, single ended</td>
<td>•</td>
<td></td>
</tr>
<tr>
<td>Output amplitude, 0.6 to 1.2 V, single ended</td>
<td>•</td>
<td></td>
</tr>
<tr>
<td>4-tap de-emphasis</td>
<td>•</td>
<td></td>
</tr>
<tr>
<td>2-tap de-emphasis</td>
<td>•</td>
<td></td>
</tr>
<tr>
<td>Error injection</td>
<td>•</td>
<td></td>
</tr>
</tbody>
</table>

Table 8.

Step 4. Select the error detector(s)

<table>
<thead>
<tr>
<th>Description</th>
<th>N4956A-E12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate, 12.5 Gb/s</td>
<td>•</td>
</tr>
</tbody>
</table>

Table 9.

Step 5. Select software (optional)

<table>
<thead>
<tr>
<th>Description</th>
<th>Model Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-instrument BERT software</td>
<td>N4980A</td>
</tr>
<tr>
<td>Jitter tolerance software package</td>
<td>N4980A-JTS</td>
</tr>
</tbody>
</table>

Table 10.

1. N4965A may be configured with up to five pattern generators.
2. The N4965A may be configured with up to five error detectors.
### Ordering Information

<table>
<thead>
<tr>
<th>Model number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>N4965A</td>
<td>Multi-channel BERT controller</td>
</tr>
<tr>
<td>N4955A-P12</td>
<td>12.5 Gb/s 2-tap pattern generator remote head 1</td>
</tr>
<tr>
<td>N4955A-D12</td>
<td>12.5 Gb/s 4-tap pattern generator remote head 1</td>
</tr>
<tr>
<td>N4956A-E12</td>
<td>12.5 Gb/s error detector remote head 1</td>
</tr>
</tbody>
</table>

Table 11.

### Recommended clock sources

<table>
<thead>
<tr>
<th>Model number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>N4960A-CJ0</td>
<td>Clock Synthesizer 16 GHz/Serial BERT Controller with single tone jitter injection</td>
</tr>
<tr>
<td>N4960A-CJ1</td>
<td>Clock Synthesizer 16 GHz/Serial BERT Controller with multi-tone jitter injection</td>
</tr>
<tr>
<td>N4963A</td>
<td>Clock Synthesizer 13.5 GHz</td>
</tr>
<tr>
<td>N4963A-101</td>
<td>Clock Synthesizer 13.5 GHz with single tone jitter injection</td>
</tr>
</tbody>
</table>

Table 12.

### Software

<table>
<thead>
<tr>
<th>Model number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>N4980A</td>
<td>Multi-instrument BERT software</td>
</tr>
<tr>
<td>N4980A-JTS</td>
<td>Jitter tolerance software package</td>
</tr>
</tbody>
</table>

Table 13.

1. The N4965A controller may be configured with up to 5x remote heads, any combination of N4955A-P12, N4955A-D12, and N4956A-E12.

### Calibration Service

For calibration service information, contact your local authorized Keysight distributor or Keysight sales department.

### More Information

For additional information, to schedule a product demonstration, or to request a quote, contact your local authorized Keysight Technologies distributor.
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Korea 080 769 0800
Malaysia 1 800 888 848
Singapore 1 800 375 8100
Taiwan 0800 047 866
Other AP Countries (65) 6375 8100

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