Keysight Technologies
MIPI D-PHY Protocol Test Solutions
N4851A/B MIPI D-PHY Acquisition Probe
N4861A/B MIPI D-PHY Stimulus Probe

Data Sheet
Accelerate your MIPI D-PHY test development

Simplify your MIPI D-PHY test environment by combining stimulus and analysis

Applications

- MIPI D-PHY hardware prototype turn-on and debug
- System integration of embedded controller with MIPI D-PHY display and camera devices
- Troubleshooting interoperability issues
- Robustness test with error injection
- Software debug of MIPI D-PHY-based systems

Key features

- Combined MIPI D-PHY real-time analysis and stimulus test solution
- Real-time trace of MIPI D-PHY bus modes
- Decoding and visualization of CSI-2 and DSI protocols
- Easy trigger setup with predefined pattern library
- Hierarchical trace display capabilities
- Automatic stimulus generation from bitmap picture
- Full custom traffic generation
- Capture and replay capabilities
- Link layer test with parametric control of voltages and timing
- Based on a modular, scalable, logic analyzer platform for multi-bus, system-level measurements
- Multilevel trigger sequencer to trigger the analyzer on complex event conditions
MIPI D-PHY is a packet-based interconnect standard defined for use in wireless mobile devices as the communication bus between the main components such as the embedded controller (BB-IC) and cameras and displays.

When you adopt the MIPI D-PHY standard in your designs, you will face new test challenges during the debug, integration and system validation phases of the development process.

To ensure your design operates according to the MIPI D-PHY link and CSI-2 or DSI protocol specification, you need real-time insight on the DUT’s behavior at various protocol levels, and you need to be able to trigger on protocol-specific patterns or error conditions.

To reproduce system problems or run non-regression tests, you often need to create traffic conditions that may be difficult to reproduce with real devices. The MIPI D-PHY stimulus solution can accelerate your design/debug/test cycle by reproducing these conditions.

The specific nature and operation modes of the MIPI D-PHY serial interconnect makes it extremely difficult to analyze or to stimulate with general-purpose test instruments.

Now you can get the capabilities you need with the N4851A/B and N4861A/B analysis and stimulus solution.

The Keysight Technologies, Inc. N4851A/B acquisition probe and the N4861A/B stimulus probe operate in conjunction with Keysight 16800 and 16900 Series logic analyzers to provide the digital serial stimulus and acquisition capabilities required to independently debug and test a MIPI D-PHY component, or integrate your MIPI D-PHY-based mobile designs.

Thanks to the modular and scalable architecture of Keysight 16800 and 16900 logic analyzers, the MIPI D-PHY analysis and stimulus measurements can be time-correlated with other measurements (control logic, other serial buses, memory) on the device under test, helping you perform system-level measurements.

Cross triggering capabilities help you observe the activity on a bus when a specific event happens on another bus, helping you find the root cause of complex system-level problems.

With this versatile architecture, you can use the same platform from the bus design phase to system-level test, so you reduce your expenditure on test equipment.

This common, scalable system for protocol analysis and traffic generation protects your financial investment for years to come.

Combine custom traffic generation and real-time analysis to diagnose and characterize your system faster.
Typical Configurations

MIPI D-PHY analysis configuration

- In analysis-only mode, the N4851A/B transparently captures traffic between two devices.
- Link activity and protocol operation (CSI, DSI) is captured through various probing solutions, from flying leads to soft-touch connectors.
- The analyzer includes a multilevel sequencer to trigger the analyzer on complex event conditions.
- Multiple analyzers can be synchronized and cross triggered for system-level measurements.

MIPI D-PHY stimulus and analysis solution

- In active test mode (stimulus + analysis), a customizable stimulus is sent to the DUT, with simultaneous analysis of the response.
- The stimulus solution can be used to test peripherals, such as display devices, by simulating a system controller.
- Stimulus patterns can be defined in multiple ways:
  - File-based stimulus
  - GUI-based stimulus
  - Record and play pattern
  - Bitmap-based Stimulus

Flying leads signal probing solution

N4851A/B MIPI D-PHY acquisition probe

N4861A/B MIPI D-PHY stimulus probe

Soft touch connectorless probes reduce cost and shorten your design cycle by eliminating probing connectors
N4851A/B Protocol Analysis Gives You Fast Insight into Your System

Flexible GUI gives you easy visibility into MIPI D-PHY activity and system operation
- Bus mode operation, CSI-2 and DSI traffic, and trigger status are simultaneously displayed

Hierarchical trace display speeds your debug process
- Avoid constant scrollings with the hierarchical display that maximizes information density on the screen
- DSI and CSI-2 decoding capabilities for camera and display traffic analysis
- Compare frames details and easily find bit-level differences
- Easily retrieve information with embedded markers
- Quickly find problems with automatic error detection

Powerful triggering, easy setup
- Easy trigger setup by using and editing predefined patterns from the pattern library

Multi-bus display for better insight into your system
- Traces captured from multiple buses are displayed with time-correlated time-stamps and common markers
- Multiple analyzers can share events for sophisticated cross triggering
Image Inserter and Image Extractor Applications

Quickly build MIPI DSI stimulus from bitmap files with the Image Inserter application

- Save hours of development and editing
- Configurable formats, bitmap encoding
- Multiframe generation
- Virtual channel support
- Supports burst mode, non-burst mode, command mode
- Supports initialization commands

Visualize bitmaps from real time trace files with the Image Extractor application

- Reconstruct picture from DSI trace
- Virtual channel support
- Multiple frame support

DSI Image Inserter

DSI Image Extractor
### Electrical characteristics

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage level support</td>
<td>D-PHY compliant</td>
</tr>
<tr>
<td>LPV&lt;sub&gt;high&lt;/sub&gt;</td>
<td>800 mV to 3.3 V</td>
</tr>
<tr>
<td>Voltage sensitivity</td>
<td>100 mV typical</td>
</tr>
<tr>
<td>Track changes in speed mode</td>
<td>Yes - Mode changes displayed on trace</td>
</tr>
<tr>
<td>Termination</td>
<td>Analyzer probe snoops the bus (is not an endpoint on the bus) Termination is dependent on the actual endpoint device</td>
</tr>
<tr>
<td>Lane width</td>
<td>2 channels (N4851A), 4 channels (N4851B)</td>
</tr>
<tr>
<td>Maximum bit rate (high-speed mode)</td>
<td>800 Mbps (N4851A), 940 Mbps (N4851B)</td>
</tr>
<tr>
<td>Minimum bit rate (high-speed mode)</td>
<td>80 Mbps, per D-PHY specification</td>
</tr>
<tr>
<td>Maximum bit rate (low-power mode)</td>
<td>10 Mbps, per D-PHY specification</td>
</tr>
<tr>
<td>Minimum bit rate (low-power mode)</td>
<td>N/A (no specification)</td>
</tr>
<tr>
<td>Protocol version support and decoding</td>
<td></td>
</tr>
<tr>
<td>MIPI D-PHY DSI 1.01</td>
<td>Yes</td>
</tr>
<tr>
<td>MIPI D-PHY DSI 1.00</td>
<td>No</td>
</tr>
<tr>
<td>MIPI D-PHY CSI-2 1.00</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Protocol viewing

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Protocol viewer</td>
<td>Hierarchical packet-level display</td>
</tr>
<tr>
<td>Protocol decoder</td>
<td></td>
</tr>
<tr>
<td>HS and LP data support</td>
<td>Yes</td>
</tr>
<tr>
<td>Short and long packet decode</td>
<td>Yes</td>
</tr>
<tr>
<td>CSI and DSI decode</td>
<td>Yes</td>
</tr>
<tr>
<td>Decode speed changes</td>
<td>Yes</td>
</tr>
<tr>
<td>Payload viewing</td>
<td>Yes</td>
</tr>
<tr>
<td>Error decode</td>
<td></td>
</tr>
<tr>
<td>SOT error display</td>
<td>Yes</td>
</tr>
<tr>
<td>EOT error display</td>
<td>Yes</td>
</tr>
<tr>
<td>Escape error display</td>
<td>Yes</td>
</tr>
<tr>
<td>Sequence error display</td>
<td>Yes</td>
</tr>
<tr>
<td>Turnaround error display</td>
<td>Yes</td>
</tr>
<tr>
<td>ECC, CRC error display</td>
<td>Yes</td>
</tr>
<tr>
<td>Contention detection</td>
<td>No</td>
</tr>
</tbody>
</table>
### Triggering capabilities

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trigger on protocol patterns</td>
<td>Yes, on both DSI and CSI long and short patterns</td>
</tr>
<tr>
<td>Protocol pattern customization</td>
<td>Yes, with bit-level editing</td>
</tr>
<tr>
<td>Real-time error detection</td>
<td></td>
</tr>
<tr>
<td>SOT error trigger</td>
<td>Yes, on a per lane basis</td>
</tr>
<tr>
<td>EOT error trigger</td>
<td>Yes, on a per lane basis</td>
</tr>
<tr>
<td>Escape error trigger</td>
<td>Yes, on a per lane basis</td>
</tr>
<tr>
<td>Sequence error trigger</td>
<td>Yes, on a per lane basis</td>
</tr>
<tr>
<td>Turnaround error trigger</td>
<td>Yes, on a per lane basis</td>
</tr>
</tbody>
</table>

### Display

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low power state of data transmission</td>
<td>Yes</td>
</tr>
<tr>
<td>Ultra-low power state</td>
<td>Not visible in the trace</td>
</tr>
<tr>
<td>Stopped</td>
<td>Yes</td>
</tr>
</tbody>
</table>
N4861A/B Stimulus Probe Helps You Characterize Your System’s Operation under Multiple Traffic Conditions

Increase test coverage with configurable traffic generation

- Configurable traffic can be generated from the GUI, or from CSV files and bitmap files
- Deterministic D-PHY, DSI, CSI-2 pattern generation
- Customize the initialization sequence independently from the main test sequence
- Repetitive events
- 1, 2 or 3 channels support
- Stimulus up to 1 Gbps

Test your device’s link layer and protocol layer

- Custom D-PHY bus mode transitions and link event generation
- Test low-power bus mode
- Custom DSI, CSI-2 traffic generation

Validate boundary conditions of your devices and components

- Timing control of MIPI D-PHY link layer events within or outside specifications
- Voltage control of MIPI D-PHY signals
- Manual control of error generation helps you test robustness and error recovery mechanisms

Record and play capabilities help you reproduce test scenarios from captured traces

- Use a wide range of specific real-world traffic conditions
- Save trace captured on a real target and replay it as many times as you want

Increase test coverage with configurable traffic generation

- Generate traffic for multiple ports and correlate the test results across time for comprehensive system testing

Timing and voltage control of MIPI D-PHY stimulus
### Electrical characteristics

<table>
<thead>
<tr>
<th>Feature</th>
<th>LSR features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lane width</td>
<td>2 channels (N4861A), 3 channels (N4861B)</td>
</tr>
<tr>
<td>Voltage level support</td>
<td>D-PHY compliant</td>
</tr>
<tr>
<td>Low-power voltage high adjustment</td>
<td>800 mV -&gt; 3.3 V</td>
</tr>
<tr>
<td>Low-power voltage low adjustment</td>
<td>–100 mV -&gt; +100 mV</td>
</tr>
<tr>
<td>High-speed voltage high adjustment</td>
<td>+150 mV -&gt; +450 mV</td>
</tr>
<tr>
<td>High-speed voltage low adjustment</td>
<td>Not adjusted independently (changes with LPVlow or HSVhigh)</td>
</tr>
</tbody>
</table>
| Slew rate control            | Meets D-PHY specification in fast mode                                       
|                              | Fast, medium, slow, slowest                                               |
| Mode change support          | Yes                                                                          |
| Waveform timing control      | Yes, automatic or manual settings                                          |
| CLK-POST timing control      | Yes, automatic or manual settings                                          |
| CLK-PRE timing control       | Yes, automatic or manual settings                                          |
| CLK-PREPARE timing control   | Yes, automatic or manual settings                                          |
| CLK-TRAIL timing control     | Yes, automatic or manual settings                                          |
| CLK-ZERO timing control      | Yes, automatic or manual settings                                          |
| HS-EXIT timing control       | Yes, automatic or manual settings                                          |
| HS-PREPARE timing control    | Yes, automatic or manual settings                                          |
| HS-Zero                      | Yes, automatic or manual settings                                          |
| HS-TRAIL                     | Yes, automatic or manual settings                                          |
| LPX                          | Yes, automatic or manual settings                                          |
| TA_Get                       | Yes, automatic or manual settings                                          |
| TA_GO                        | Yes, automatic or manual settings                                          |
| CLK lane and data lane skew adjust | No, under investigation                                                  |
| Device under test termination| 100-ohm differential termination                                            |
| Expected DUT HS termination  | None                                                                         |
| Expected DUT LP termination  | None                                                                         |
| Stimulus probe termination   | Either driver or tri-state (master only)                                    |
| (no termination switching     |                                                                             |
| provided)                    |                                                                             |
| Clock input                  | Required for stimulus probe operation                                       |
| Data rate below 200 Mbps     | Clock input = 1/2 bit rate                                                 |
| Data rate at or above 200 Mbps | Clock input = 1/10 bit rate                                               |
### Performance – the numbers below are guaranteed to comply to D-PHY’s specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum bit rate (high-speed mode)</td>
<td>500 Mbps (N4861A), 1 Gbps (N4861B)</td>
</tr>
<tr>
<td>Minimum bit rate (high-speed mode)</td>
<td>80 Mbps (per the D-PHY specification)</td>
</tr>
<tr>
<td>Maximum bit rate (low-power mode)</td>
<td>10 Mbps (per the D-PHY specification)</td>
</tr>
<tr>
<td>Minimum bit rate (low-power mode)</td>
<td>800 Kbps (based on timers)</td>
</tr>
</tbody>
</table>

#### Version support

MIPI D-PHY 0.89, 0.90, 1.00

Complete, except support for slave mode operation. Only operates as a master on the bus.

Probe not limited to CSI or DSI, supports D-PHY

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### Stimulus Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet generation</td>
<td>Yes</td>
</tr>
<tr>
<td>ECC/CRC automatic calculation</td>
<td>Yes, done by software</td>
</tr>
<tr>
<td>DSI video modes</td>
<td>Burst mode, non-burst mode, command mode</td>
</tr>
</tbody>
</table>

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### Error injection

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSDT request error generation</td>
<td>Yes, with timing control to violate specs</td>
</tr>
<tr>
<td>SOT synch error generation</td>
<td>No</td>
</tr>
<tr>
<td>End of HSDT error generation</td>
<td>Yes, with timing control to violate specs</td>
</tr>
<tr>
<td>LPD transmission error generation</td>
<td>Yes, with waveform timing control and direct control of data transmitted on the link</td>
</tr>
<tr>
<td>Protocol errors</td>
<td>Yes</td>
</tr>
<tr>
<td>Turnaround error generation</td>
<td>No (does not operate in slave mode)</td>
</tr>
<tr>
<td>ECC, CRC error generation</td>
<td>Manual</td>
</tr>
</tbody>
</table>

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N4851A/B and N4861A/B Physical Characteristics

**Dimensions**

N4851A/B exterior dimensions

![Dimensions](image)

- Folded cable length is approx. 15"
- Unfolded cable length is approx. 48"

N4851A/B front panel, rear panel and top view

![Front View](image)

![Top View](image)

- SMA connectors. Refer to Users Guide or online help
- Status LEDs
- Cable for connecting to device under test
- Logic analyzer connection via Samtec probes
- DC Power
- Option connector to N4861A/B
- Power switch

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N4851A/B and N4861A/B Physical Characteristics (continued)

Dimensions

N4861A/B exterior dimensions

N4861A/B front panel, rear panel, and top view
When you configure your MIPI D-PHY measurement system, consider the following:

**Ability to provide MIPI D-PHY stimulus**
- For comprehensive stimulus and response testing of your MIPI D-PHY device or system, select a logic analyzer with digital pattern generation capability (16822A, 16823A, or a 16900 modular logic analysis system with a 16720A pattern generator module).

**Flexibility to grow as your measurement needs evolve:**
- A modular 16900 Series logic analyzer addresses your measurement needs today and allows you to grow as your needs evolve.

**Modification of the logic analyzer’s MIPI D-PHY protocol decoder**
- The MIPI D-PHY standard provides the flexibility to customize your control structure and data packets for your specific application. With the B4641A protocol development kit, you can modify the logic analyzer’s MIPI D-PHY protocol decoder to track your custom solution.

**DUT requirements for use with N4861A/B stimulus probe:**
- SMA (m-m) connectors on the target. The number of SMA connectors depends on your test scenario: turn on, validation, or system integration.

**N4851U upgrade kit**
If you own an N4851A MIPI D-PHY analysis probe or an N4861A MIPI D-PHY stimulus probe, the N4851U upgrade kit will extend the capabilities of your test system:
- With the N4851U-004, your N4851A analysis probe can support up to 4 lanes.
- With the N4851U-004, your N4861A stimulus probe will support up to 3 lanes.
- One N4851U-004 is required for each logic analyzer connected to MIPI D-PHY analysis and stimulus probes.
Ordering Information: Analysis and Stimulus Solution

To configure a complete MIPI D-PHY digital acquisition and stimulus system, you will need to order or have the following items:

1. MIPI D-PHY probes
   - N4861A/B digital stimulus probe
     - N4861A-040: Two sets of four 40-inch SMA cables
   - N4851A digital acquisition probe
     - -010 for node-locked license
     - -020 for floating (server) license
   - N4851B digital acquisition probe

2. Method to create data
   - Convert captured logic analyzer trace to stimulus
   - Custom programmatic generation

3. Logic analyzer with 48-channel pattern generator
   - 16800 Series portables
     - 16822A – 68 ch
     - 16823A – 102 ch
   - 16900 Series modular mainframe with at least one each of the following:
     - 16900 Series module(s)
     - 16720A pattern generator module

4. Device under test
   - E5381A differential flying lead probe
   - E5405A differential pro series soft touch probe
   - E5387A differential soft touch probe
   - E5385A for logic analyzers with a 40-pin cable connection (16822A, 16823A, 16910/11A)
   - E5378A for logic analyzers with a 90-pin cable connection (1695X modules)

5. Logic analyzer (Two Samtec probes per N4851A/B – one for Tx and one for Rx. Select probe that is compatible with your logic analyzer.)

Notes:
1. N4861A/B digital stimulus probe requires an N4851A/B digital acquisition probe to operate and a clock generator, such as the Keysight 33250A.
2. Compatible with 16800 or 16900 Series logic analyzers with 68 channels or more.
Ordering Information: Analysis Solution

To configure a complete MIPI D-PHY digital acquisition system, you will need to order or have the following items:

1. MIPI probes
   - (One per Tx/Rx pair)

2. Logic analyzer
   - (One of the following for each N4851A/B)

3. Device under test
   - (One of the following for each N4851A/B)

4. Logic analyzer
   - (Two Samtec probes per N4851A/B – one for Tx and one for Rx. Select probe that is compatible with your logic analyzer)

- **N4851A digital acquisition probe**
  - -010 for node-locked license
  - -020 for floating (server) license

- **N4851B digital acquisition probe**

- **16800 Series portables**
  - 16802A – 68 ch
  - 16803A – 102 ch
  - 16804A – 136 ch
  - 16806A – 204 ch
  - 16822A – 68 ch
  - 16823A – 102 ch

- **16900 Series modular mainframe with at least one 16900 Series module**

- **Probes between the N4851A/B and the...**

  - **E5381A differential flying lead probe**
  - **E5405A differential probe**
  - **E5387A differential soft touch probe**

- **Related Keysight literature**

<table>
<thead>
<tr>
<th>Publication title</th>
<th>Pub number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Keysight 16800 Series Portable Logic Analyzers Data Sheet</td>
<td>5989-5063EN</td>
</tr>
<tr>
<td>Keysight 16900 Series Logic Analysis Mainframes Data Sheet</td>
<td>5989-0421EN</td>
</tr>
<tr>
<td>Probing Solutions for Keysight Technologies Logic Analyzers Catalog</td>
<td>5968-4632E</td>
</tr>
</tbody>
</table>

- **Product Web site**

  For the most up-to-date and complete application and product information, please visit our product Web site at: www.keysight.com/find/MIPI
myKeysight
www.keysight.com/find/mykeysight
A personalized view into the information most relevant to you.

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Hong Kong 800 938 693
India 1 800 112 929
Japan 0120 (421) 345
Korea 080-769 0800
Malaysia 1 800 888 848
Singapore 1 800 375 8100
Taiwan 0800 047 866
Other AP Countries (65) 6375 8100

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Germany 0800 6270999
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(BP-09-23-14)