PCB Impedance and Loss Control Test Software Solution

Simulation Software for Rigid, Flexible, and Hybrid PCB Impedance and Loss Control

Introduction

High-speed digital standards have tightened the margin for Printed Circuit Board (PCB) signal integrity. Interfaces such as DDR5 and PCIe Gen5 require impedance tolerances of ±10%, while PCIe Gen6 further tightens the tolerance to ±7%. Insertion-loss budgets on demanding channels have dropped below 1 dB per inch, and PCIe Gen6 caps total channel loss at 32 dB. Stackup complexity has increased with the use of hybrid PCB stackups, fine-pitch traces, and mixed prepreg constructions.

Conventional impedance calculators rely on simplified models and estimate parameters rather than physical material behavior. They do not account for post-lamination prepreg compression, composite Dielectric Constant (Dk) resulting from stacked prepreg materials, or changes in effective Dk experienced by the propagating signal. In practice, these calculators can deviate by 5% to 15% from measured impedance and insertion-loss results, even with industry-standard ultra-low-loss laminates.

Design teams need a simulator that reflects measured results and supports a continuous workflow, from stack-up definition to impedance and insertion-loss analysis, across rigid, flexible, and hybrid PCB constructions.

KEYSIGHT

Solution Overview

The Keysight PCB Impedance and Loss Control Test Software Solution is simulation software for PCB impedance and insertion-loss control on rigid and flexible substrates. A stackup model predicts the post-lamination microsection based on material behavior and process effects rather than assumed values. The electromagnetic field solver then computes the field distribution using this predicted physical structure. Simulated impedance and insertion-loss results have been shown to correlate with measurements within approximately 5%, based on customer evaluations using industry-standard low-loss PCB materials.

Stackup definition, impedance analysis, and insertion-loss analysis run within a single tool. The stackup editor defines multilayer constructions: core, prepreg, and copper foil layers, with material types and parameters drawn from a built-in material database. The solver then calculates impedance and insertion loss directly from the defined stackup without re-entering parameters.

The solution ships as ZA0129AS with two substrate-specific software components:

Software Component	Description
XA5129PCA PCB Impedance and Loss Simulation Software	For rigid PCB substrates. Covers stackup design, impedance and insertion-loss simulation, automated optimization, with Enterprise Resource Planning (ERP) and Excel integration.
XA5129FPA Flexible Printed Circuit (FPC) Impedance Simulation Software	For flexible printed circuits. Covers impedance modeling with FPC-specific physics, including mesh reference layers, electromagnetic shielding films, polyimide and adhesive coverlays, and adhesive-versus-adhesiveless laminate constructions.

Key Capabilities

Multi-Layer Stackup Design with Built-In Material Database

The stackup editor defines multi-layer PCB constructions using core, prepreg, and copper foil layers. Material properties[1] such as Dielectric Constant (Dk), Dissipation Factor (Df), and nominal thickness populate automatically from the built-in material database, so changes to the stackup propagate through all impedance and insertion-loss results in a single operation.

The database includes commonly used PCB material vendors and material families across multiple resin contents and glass weave styles, including 1055, 1080, and 2116. Mixed-Dk modeling computes the composite dielectric constant for traces spanning multiple prepregs, rather than averaging values that do not exist in the build.

Final dielectric thickness is calculated by modeling prepreg compression during the lamination press cycle, based on copper density on adjacent layers. Butter coat modeling is used to estimate the local resin thickness after lamination and identifies regions where insufficient resin fill may lead to resin starvation.

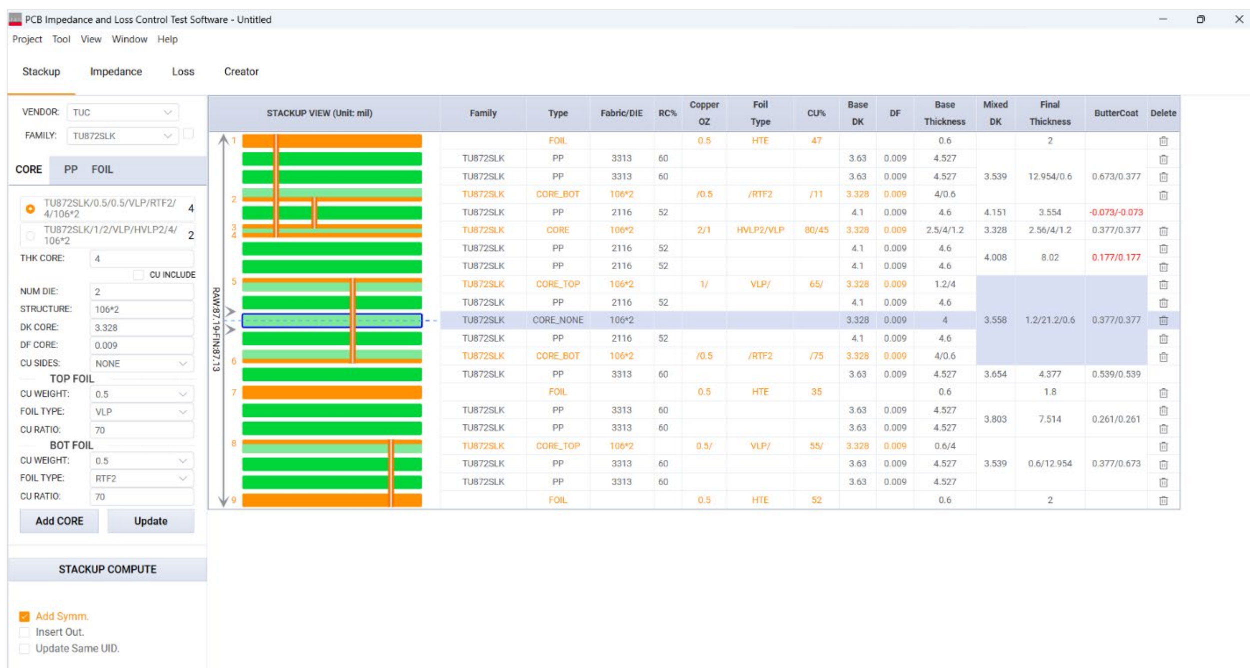

Figure 1. Stackup editor with per-layer material control. Dk, Df, and thickness.

1 Dielectric Constant (Dk) and Dissipation Factor (Df) prediction models have been correlated with measurement data obtained using Split-Cylinder Resonator (SCR) and Split-Post Dielectric Resonator (SPDR) methods.

Field-Solver-Based Impedance Analysis

The impedance solver uses a Boundary Element Method (BEM) field solver for fast, accurate PCB cross-sectional impedance analysis. It supports microstrip, stripline, coplanar, and embedded structures in both single-ended and differential-pair configurations.

Stackup definitions feed directly into the analysis, with material and geometry parameters transferred from the selected layers without re-entry. The solver accounts for trapezoidal conductor geometry and effective dielectric constant derived from the field distribution. Post-lamination geometry defined in the stackup editor flows through to the impedance calculation.

For each impedance profile, you can target an impedance value and allow the solver to converge automatically on the trace width and spacing that meet the specification. The resulting geometry and calculated parameters are stored within the Impedance Profile List for reuse and retrieval across designs.

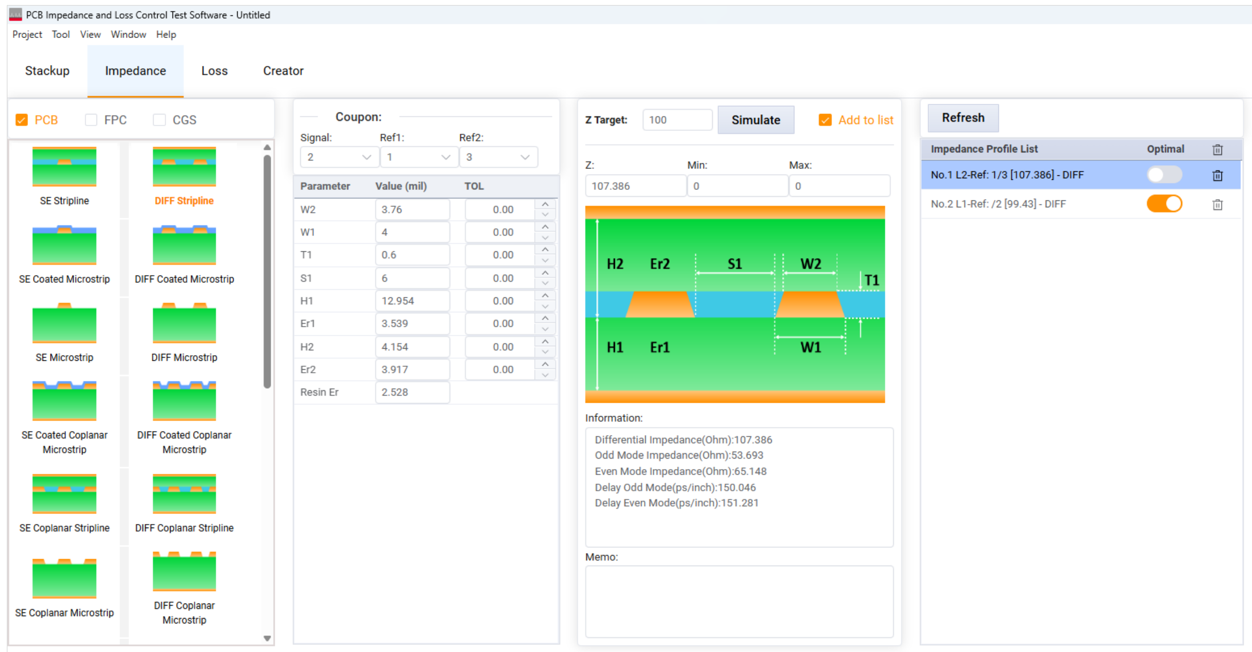

Figure 2. Differential impedance parameter panel: W1, W2, S1, H1, Er1 controls and computed odd-mode and even-mode results.

Field-Solver-Based Insertion-Loss Analysis (Rigid PCB)

For rigid substrates, the insertion-loss solver uses field-solver-derived transmission-line models. It shares the same stackup editor inputs as the impedance analysis, which ensures loss calculations are based on the same physical geometry and material definitions.

Microstrip and stripline structures common to high-speed PCB designs are supported up to 110 GHz. The solver computes conductor loss, dielectric loss, and total loss as separate components. Foil-type definitions model copper surface roughness for High-Temperature Elongation (HTE), Hyper-Very-Low-Profile (HVLP), and related foil families. Post-lamination dielectric geometry feeds directly into the loss calculation for closer correlation with manufactured boards.

Reusable impedance profile libraries allow previously calculated structures to be recalled into the loss workflow without re-entering parameters, enabling efficient iteration on materials, geometry, or copper roughness in one workflow. Copper surface treatment layers, including low-loss adhesion treatments, are represented in the loss model.

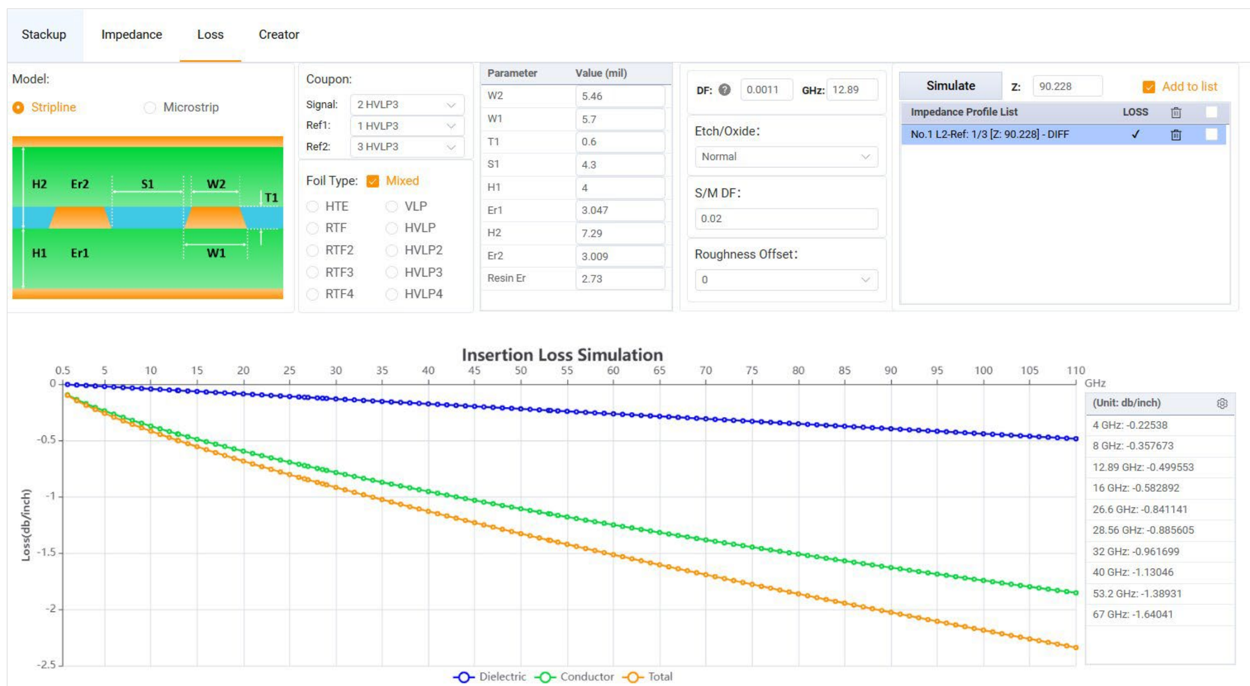

Figure 3. Insertion-loss simulation showing dielectric, conductor, and total loss across the design frequency range.

Flexible PCB Impedance Analysis with FPC-Specific Physics

The XA5129FPA supports impedance analysis for flexible printed circuits using parameters that reflect actual FPC construction. The mesh reference layer is modeled directly, with copper line width, opening size, and grid-filled-region Dk used to compute the equivalent reference plane.

Electromagnetic shielding films used for Electromagnetic Interference (EMI) suppression or impedance control are modeled with dedicated dielectric and loss parameters rather than approximated as continuous planes. Polyimide and adhesive coverlay layers are represented with their distinct dielectric properties. An adhesive-versus-adhesiveless laminate parameter selects the construction type, reflecting measurable differences in local dielectric behavior.

Impedance mode presents both substrates within the same user interface. A substrate tab switches between PCB and FPC coupon libraries, allowing a consistent workflow across rigid and flexible designs.

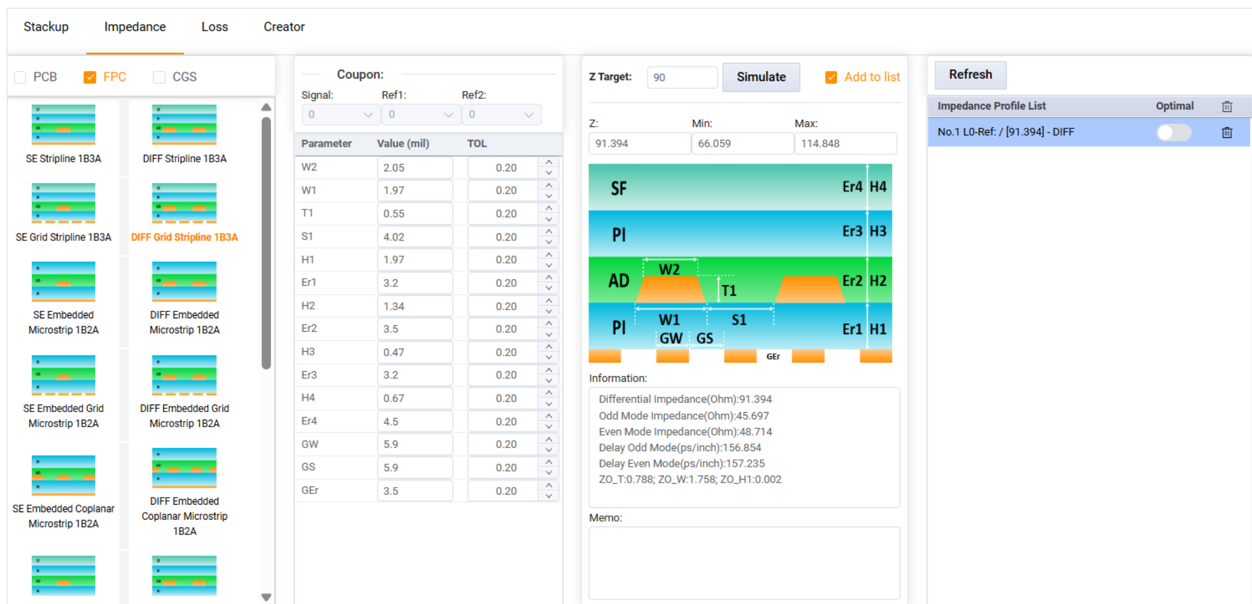

Figure 4. Impedance mode with FPC coupon libraries.

Automated Design Optimization

Auto-seek converges on trace width and spacing values that meet a target impedance, removing manual iteration from impedance qualification. Batch calculation evaluates multiple impedance configurations in a single run and returns target impedance, calculated impedance, and normalized geometry for comparison.

ERP and Excel integration enables data exchange with enterprise systems. Width and spacing values for each layer can be imported from Excel, calculated and adjusted, and exported back to the production planning system. The same interfaces support direct ERP integration for production deployment.

Parameter	Value
W2	5.3
W1	5.6
T1	1.2
S1	7.45
H1	5
Er1	3.783
H2	6.608
Er2	3.475

Z: 89.904

No	Sig	Ref	Model	Ztarget	Ztol	W	S	D	Zcalc	Wn	Sn	Dn	Zn	Znsm	Del
1	8	7/9	2	90	0	6.3	6.75	0	83.977	5.6	7.45	0	89.904	0	

Figure 5. Creator tab: target-driven impedance calculation with per-profile results table (Ztarget, Zcalc, and normalized W/S).

Key Capabilities

Category	Description
Supported Trace Configurations	• Impedance Analysis: Microstrip, stripline, coplanar, embedded, single-ended, and differential-pair structures. • Insertion-Loss Analysis: Differential stripline and differential microstrip structures.
Physical-Based Modeling	• Boundary Element Method (BEM) field solver. • Copper foil roughness modeling. • Resin-rich region impedance modeling. • Laminated thickness estimation based on material stack-up configuration. • Butter coat modeling for resin starvation risk indication and margin estimation.
Material and Conductor Libraries	• Validated Dk and Df values for commonly used rigid PCB laminate families, including standard, low-loss, and ultra-low-loss materials. • Multiple foil-type profiles (HTE, HVLP, and related families).
Accuracy	• Typical correlation within approximately 5% to measured impedance and insertion-loss data.
Automation	• Automatic trace width and spacing optimization, batch calculation across impedance profiles, and ERP and Excel integration.

Ordering Information

Software	Description	Notes
ZA0129AS	Keysight PCB Impedance and Loss Control Test Software Solution	Parent model
XA5129PCA	PCB Impedance and Loss Simulation Software[1]	Select one or both
XA5129FPA	FPC Impedance Solver Software[2]	

1. For rigid PCB substrates.
2. For flexible printed circuits.

Conclusion

The **ZA0129AS** is a simulation environment for PCB impedance and insertion-loss analysis across rigid and flexible substrates, with substrate-specific physics for each.

- The **XA5129PCA** supports rigid PCB workflows from stackup definition through impedance and insertion-loss analysis, including mixed-Dk, post-lamination, and foil-type modeling.
- The **XA5129FPA** supports flexible printed circuits with mesh reference layers, shielding films, coverlays, and adhesive-construction parameters.

Across both substrates, simulated results correlate with measured impedance and insertion loss within approximately 5% on industry-standard low-loss PCB materials.

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