

Pushing Power Amplifiers into the V Band with III-V Materials

End-to-End Research Project Delivers High-Performance GaN HEMTs on MMIC Validated in Flip Chip Packaging

SMART3: From GaN MMIC to Board Layout

Organization

- III-V Lab

Challenges

- Creating gallium nitride HEMTs operating in a power amplifier at 60 GHz or higher
- Co-design MMIC and package to enhance real-world performance
- Modeling accurate end-to-end, high-frequency behavior of chip, chip in package, package on circuit board

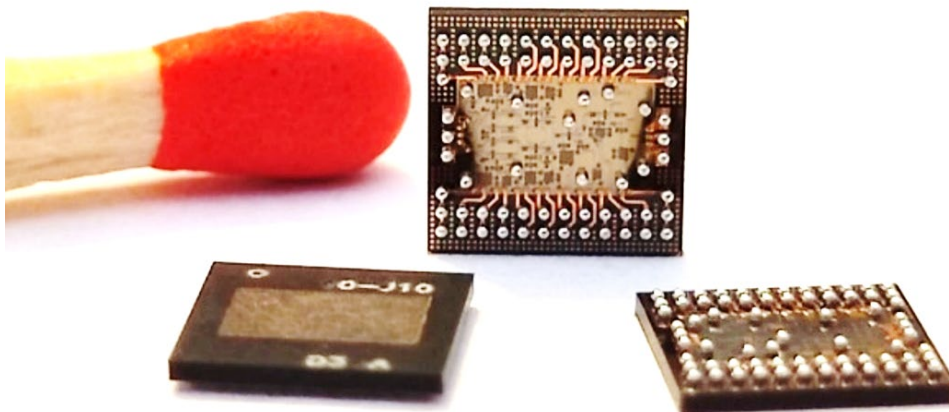
Solutions

- Use InAlN barrier layer for higher spontaneous polarization effects and reduced epitaxial strain
- Dissipate heat efficiently and optimize grounding using flip chip mounting in an FOWLP approach
- Merge foundry PDK and FOWLP packaging layers into a layer map for simulations
- Simulate interconnects between MMIC, package, and board, and optimize for low parasitics

Results

- RF transitions between MMIC and board show losses of less than 0.6 dB up to 65 GHz
- Gain of over 20 dB and output power of 27-30 dBm in a 55-68 GHz operating range

III-V Lab, headquartered in Palaiseau, France, is a joint laboratory operated by Thales, Nokia, and CEA-Leti, at the forefront of III-V semiconductor materials research, including Gallium Nitride (GaN), as well as their integration with III-V and silicon substrate materials. The recent SMART3 project took an additional step by creating a Monolithic Microwave IC (MMIC) power amplifier using InAlN/GaN/SiC HEMTs and integrating the chip in Fan-Out Wafer Level Packaging (FOWLP) technology supplied by Fraunhofer IZM.



Over the course of a four-year effort, III-V Lab design engineers collaborated on various aspects of the SMART3 project. RF design engineers utilized a suite of EDA tools in their workflow, including Keysight Advanced Design System (ADS) for layout and non-linear circuit simulation, as well as RFPro and EMPro for various stages of Electromagnetic (EM) simulations. Finally, system-level thermal analysis used a third-party thermal modeling and simulation tool. Fabricated parts show outstanding performance characteristics and a strong match between simulated values and measured results.

Challenge: Co-Designing an MMIC and its Package

At millimeter-wave (mmWave) frequencies and above, real-world effects have a significant impact on chip design. It's easy to overlook that even small amounts of parasitic resistance, capacitance, and inductance common to all package and board designs can alter performance, reducing margins and possibly causing an RF component to fall out of specification. Developing realistic models and providing accurate simulations of these effects requires EDA tools designed for the challenge.

III-V Lab recognized this early on, understanding that the SMART3 MMIC would require more robust packaging to achieve its performance goals when mounted on a Printed Circuit Board (PCB). The project settled on three motivational pillars:

- Innovative III-V-based HEMTs, giving the MMIC a foundation of high performance,
- Co-design of the MMIC and advanced FOWLP technology, synergistically tuning both designs for an optimized solution,
- Deeper analysis of the system-level stack with a packaged device deployed on a PCB, again optimizing parameters that designers working with mmWave RF devices are likely to encounter.

HEMT design is a stock-in-trade for III-V Lab, and the team was confident that it could apply advanced GaN materials to create a high-performance V band power amplifier – the question was how high they could push the frequency. However, the team wanted an end-to-end packaged solution as an outcome, and would be applying FOWLP for the first time.

"Packaging development is new for us," says Stéphane Piotrowicz, Senior Research Engineer at III-V Lab. "Our idea was to put a GaN power amplifier face down in a flip chip configuration, capable of dissipating a few watts in a small area, saving routing space, reducing insertion loss, and improving ground integrity." Figure 1 illustrates the packaging elements schematically, with the MMIC facing down and positioned close to the package's solder balls, and the heat spreader on the top side.

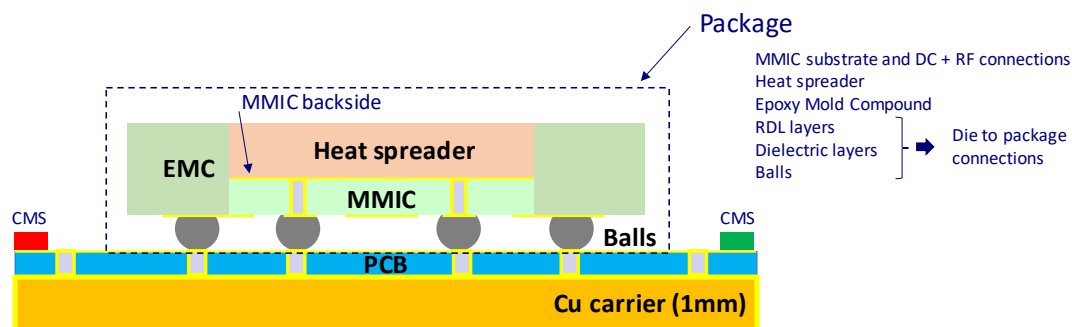


Figure 1. Flip chip mounting of the MMIC in an FOWLP optimizes interconnects and heat removal

The team aimed to stay within a single EM workflow, minimizing the need for back-and-forth format conversions. "We had little experience with 3D EM simulation," continues Piotrowicz. "Soon, brute-force simulations of the chip, package, and PCB became too long and memory-bound. We needed to separate issues and create models allowing for multiple, shorter simulation runs without sacrificing accuracy."

Solutions: InAlN Barrier, Integrated Tools, Smart Mount

Based on prior research, the III-V Lab team turned to a unique semiconductor composition centered on GaN for 4x50µm elementary transistors in its four-stage power amplifier. Fabrication of the MMIC shared process steps between III-V Lab and their foundry partner, United Monolithic Semiconductors (UMS).

III-V Lab handled layout in Keysight ADS and front-end processing up to device passivation. A crucial decision was to use indium aluminum nitride, or InAlN, as a barrier layer. InAlN offers high spontaneous polarization at a lower epitaxial strain, as it more closely matches the lattice of the GaN channel. Passive layers and back-end processing were performed by UMS, utilizing their Process Design Kit (PDK) for GaN HEMTs on SiC substrates. Figure 2 shows the 3.93 mm × 2.6 mm chip.

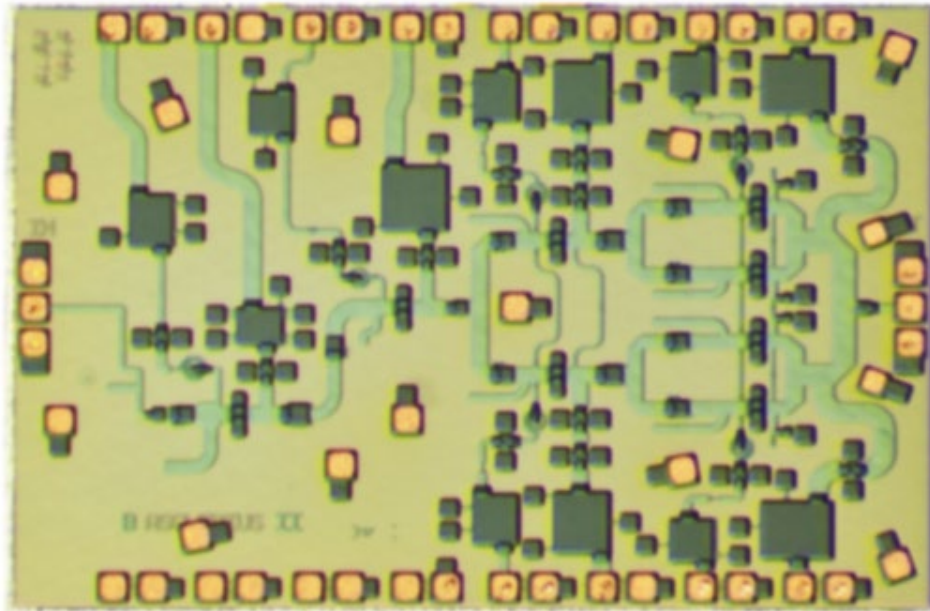


Figure 2. III-V Lab four-stage, 55-68 GHz power amplifier

Multi-tiered simulation, separating objects by technology and utilizing integrated Keysight RF EDA tools along with a creative layer map approach to a system-level model, reduced simulation times and resources, allowing for iterative use in the design workflow.

- ADS handled transistor modeling and non-linear circuit simulations, including harmonic balance and stability analysis, directly from layout views with no manual conversion steps.
- RFPPro provided 3D EM analysis of the package and board, enabling the extraction of S-parameters. Momentum, a feature in RFPPro, ran 2½ D planar EM simulations of structures in the MMIC.
- EMPro, again integrated with ADS, was explicitly used for EM analysis around dielectric structures.

ADS also provided a crucial layout capability for implementing the flip chip configuration. Smart Mount automatically maps interfaces between different design technologies when placed together, including the ability to flip an MMIC face down for insertion into the FOWLP, and then mount the FOWLP on the PCB. It frees designers to create objects independently, then integrate them without tedious format conversions, complicated by different structures, scales, and changing orientations. A concern in the III-V Lab MMIC design was the extremely thin layers used for making capacitors, which required a considerable increase in mesh size; however, this did not affect simulation accuracy.

Smart Mount is more than a mechanical time-saver. It also automatically merges electrical properties from separate design elements into a new model of the combined stack, making simulations far more accurate with coupling and parasitics fully taken into account. Mohamed Bouslama, RF Design Engineer at III-V Lab, poses the question, "Except for the RF input and output transitions with the package, can an MMIC be designed separately from its package?" For example, how do additional connections (or too few) between an MMIC and a PCB ground plane change performance? Figure 3 shows a layer map with the corresponding layers of the FOWLP and PCB added to the MMIC's EM stack (from the foundry PDK) for simulation purposes.

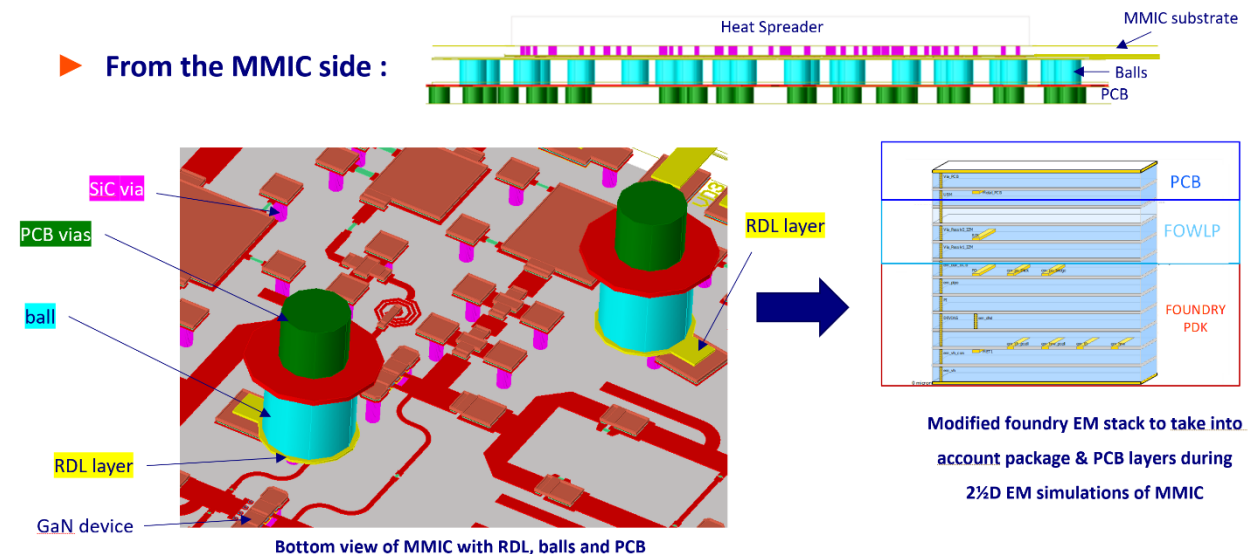


Figure 3. Diverse structures from three separate modules merged into a single stack for 2½D EM analysis

This EDA workflow also simplified collaboration with external III-V Lab partners. Package design files were sent to Fraunhofer, and PCB layouts were sent to a board fabrication house, both as direct exports from ADS at the end of the simulation and optimization efforts.

Results: Enhanced Package, Strong S-parameter Match

"Electromagnetic simulation allowed us to 'design the package', meaning we could optimize the location of the connections between the back side of the MMIC and the ground plane of the circuit board," Piotrowicz observes. "We also optimized the RF connections between the printed circuit board and the MMIC – changing positions, shapes, and distances in structures in the MMIC, the FOWLP, and the board." Measurements indicate only 0.6 dB of loss in RF transitions at frequencies up to 65 GHz.

"We were able to minimize losses further at very high frequencies with the FOWLP approach, by improving the RF transition design," adds Bouslama. "My objective was to find an RF transition configuration adaptable to numerous package sizes and applications, and RFPro, with its 3D EM simulation capability, provided valuable assistance in achieving that."

A final 36-hour simulation on the assembled PCB measured 100 ports (Figure 4), encompassing the package, decoupling capacitors, and DC and RF connections. Shorter simulation runs on MMIC in the FOWLP were in the range of three hours, which is much more tolerable in an iterative design workflow.

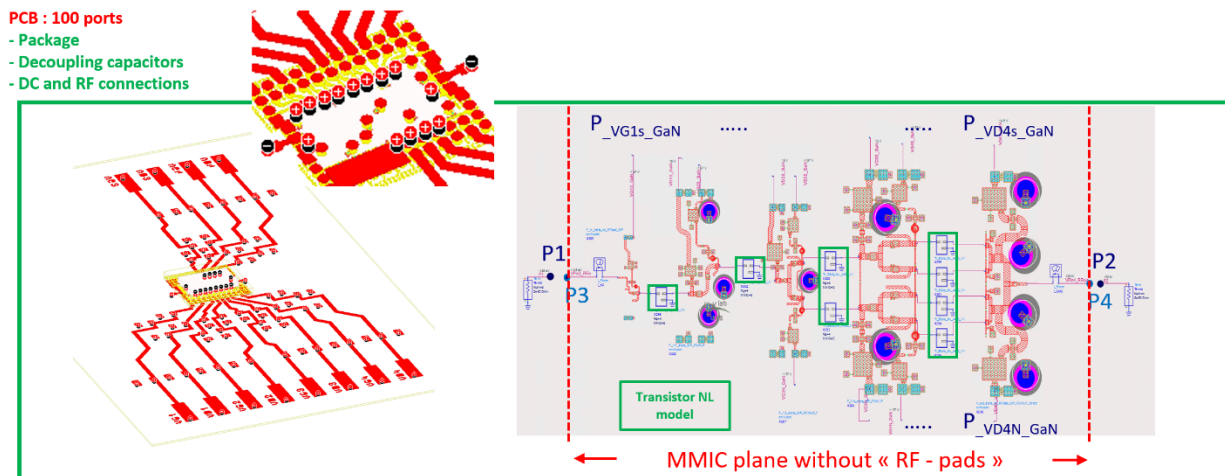


Figure 4. Final end-to-end simulation from the MMIC through the PCB with 100 ports of interest

ADS was the core of the EDA environment, but Piotrowicz also notes that RFPro made a significant contribution to this project. "RFPro allowed us to see electromagnetic fields inside the package, enabling us to check dominant propagation modes, like coplanar and microstrip, and the distribution of the electric field in critical areas such as RF transitions." This capability led to a strong match between the simulated and measured S-parameters, as shown in Figure 5. "Our accuracy was excellent given the high frequency and complexity of the MMIC and package," concludes Piotrowicz.

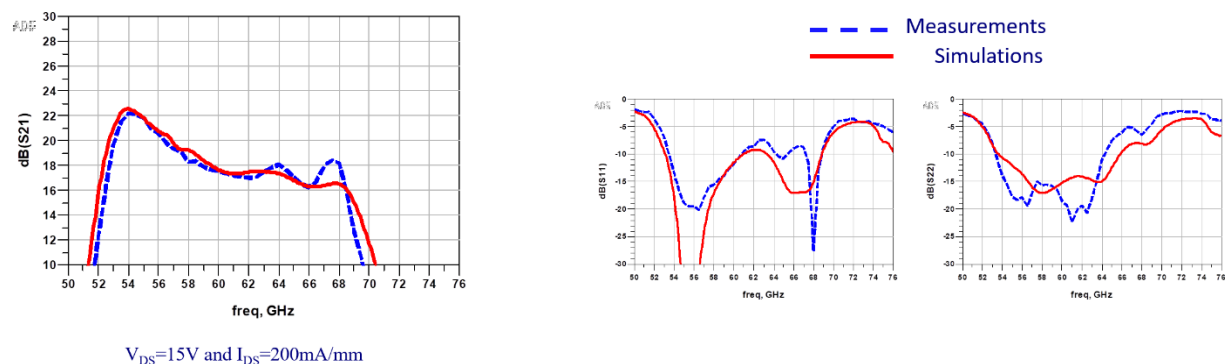


Figure 5. Match between simulated (red lines) and measured (blue lines) S-parameters in ADS plots

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Piotrowicz and Bouslama hint that it was likely possible to push the GaN power amplifier design alone to higher frequencies but are quite satisfied with the 55-68 GHz operating range achieved in SMART3.

Looking Ahead: Next Designs, More Visualization

Experience in realizable FOWLP technology may prove extremely valuable. The insertion loss in RF transitions through the FOWLP is so good that III-V Lab is applying for a patent on their SMART3 design methodology – and their thinking is it can be lower, perhaps 0.5 dB up to 80 GHz, in their next project.

III-V notes that the visualization capability in their earlier versions of ADS and RFPro could improve, and they actually used EMPro to visualize some RFPro results. (Significant visualization enhancements are featured in the latest ADS 2025 release, not used by III-V Lab for this project.) As first time users, they found RFPro easy to configure and well-integrated within the ADS environment. The local hands-on Keysight engineering assistance was another essential element in their success.

Learn more at the [III-V Lab website](#).

For more information on Keysight EDA solutions for advanced RF design, please visit:

[Keysight Advanced Design System \(ADS\)](#)

[Keysight RFPro](#)

All figures courtesy of G.I.E. III-V Lab

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