

M5302A PXIe LVDS Digital I/O

28 LVDS Channels, 8 Trigger Channels



Description

M5302A is a single-slot Digital IO PXIe module with 28 programmable LVDS channels and 8 single-ended channels. The LVDS channels can be used to communicate to the device under test or can be used to control other devices by emulating protocols such as Camera Link. The single-ended channels are suitable for event triggers or other general-purpose IO applications.

Key features

- Single PXIe slot
- Kintex UltraScale+ FPGA with PathWave FPGA support
- 28 bidirectional LVDS IO channels
- 4 General Purpose IO channels
- 8 Single-ended SMB IO channels
- PathWave Test Sync Executive support



M5302A Hardware Overview

Block diagram

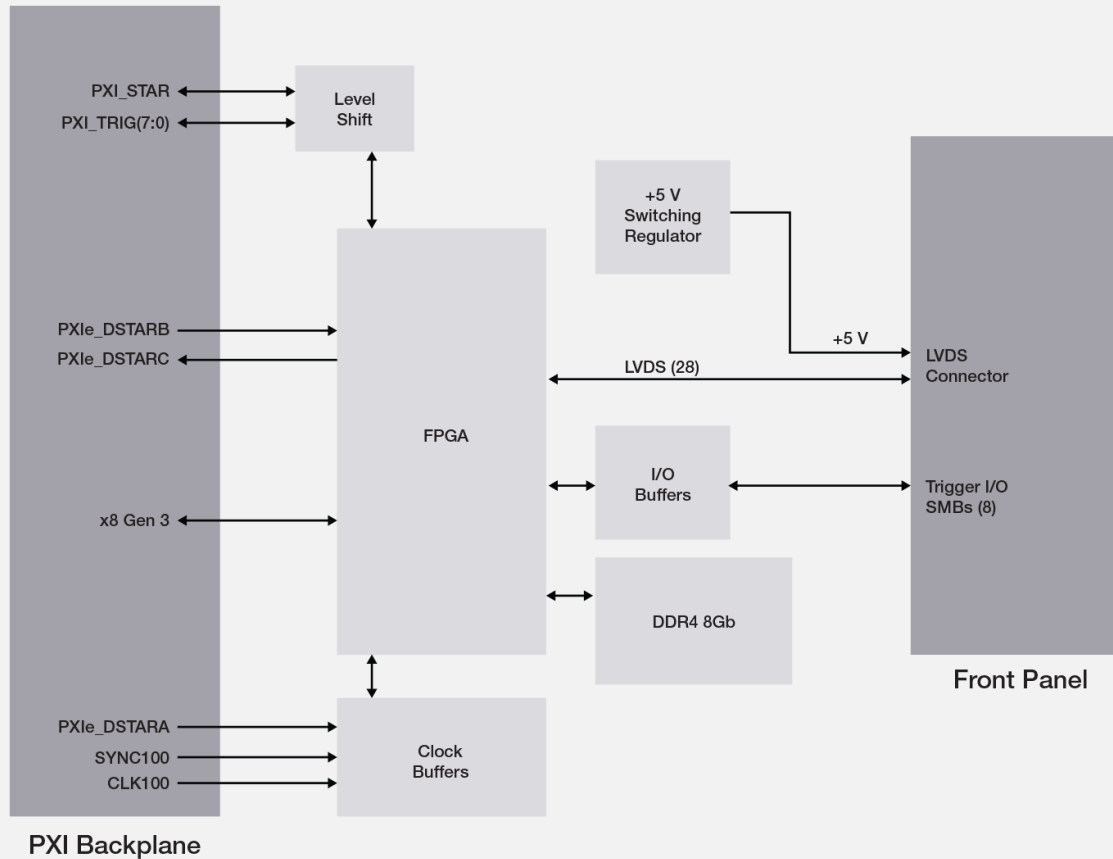


Figure 1. M5302A block diagram

LVDS connector

There are 28 bidirectional differential channels included on a 100-pin, front panel connector. These differential signals are LVDS (meant to drive 100-ohm differential load) and have a 1.2 Gbps maximum toggle rate. The Dig connector also includes +5 V power that is available to the user to power external interface circuitry (maximum current load is 0.5 A).

Trigger channels

Eight SMBs are available for instrument triggers or other general purpose I/O signals. These channels are single-ended with a voltage swing of 0 – 3.3 V when driving High Impedance loads (the voltage levels at the DUT are halved when connected to a 50 Ω load). These signals can toggle up to 1000 MHz.

FPGA

The M5302A is based upon the Kintex Ultrascale+ FPGA from Xilinx with 8 GB of DDR4. It includes an optional FPGA sandbox area where the user can add custom logic and algorithms that run at the clock speed of the FPGA. One of the typical uses of this capability is to implement advanced protocols such as Camera Link. Development of the custom FPGA code requires a PathWave development license (KF9000B).

M5302A Software Overview

Soft front panel

The M5302A has a Soft Front Panel (SFP) provides a simple interface to the digital IO module. It covers basic operation of the instrument and is especially useful for initially getting acquainted with the instrument before software programming is started. It also gives the user the ability to debug their system and to monitor driver calls.

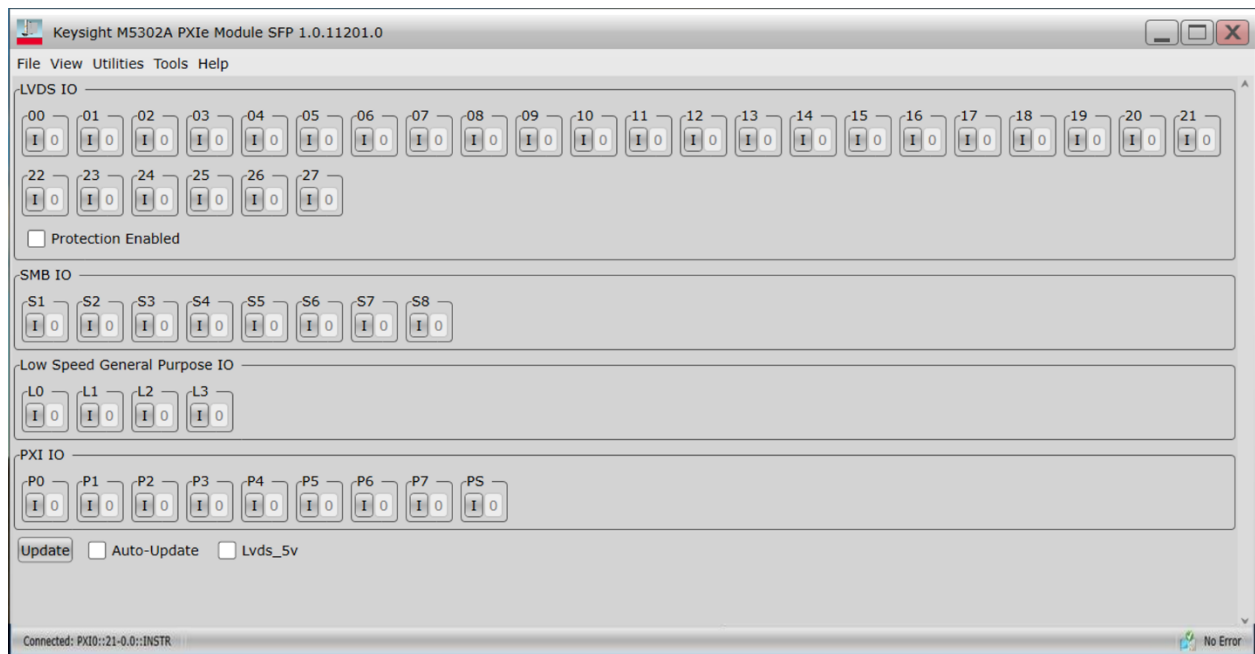


Figure 2. M5302A Soft Front Panel

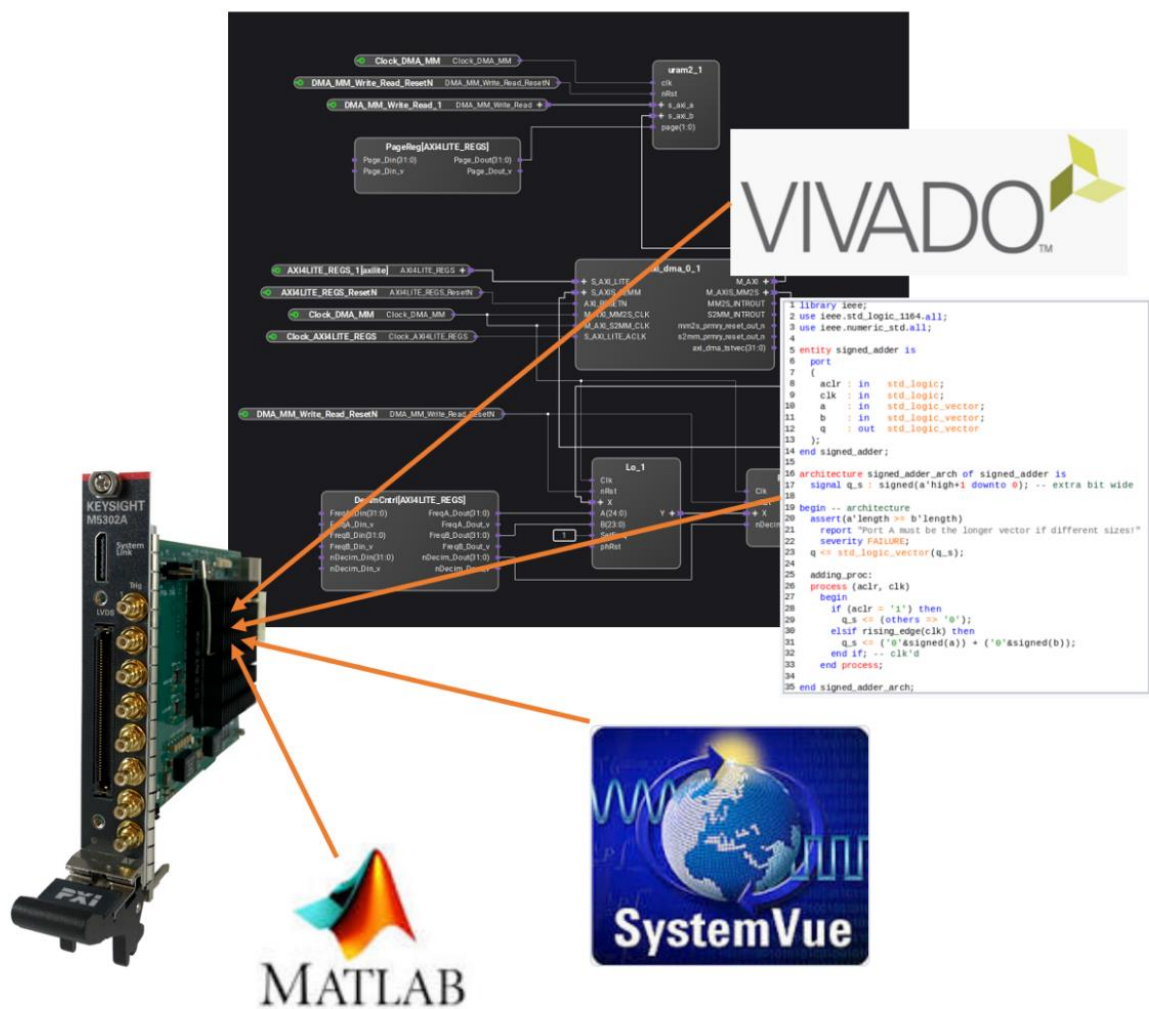
Drivers

The M5302A comes with IVI.NET, IVI-C, and IVI-COM drivers to enable easy integration into common test development environments. In addition, a Python interface will also be provided with the module.

PathWave FPGA

PathWave FPGA is a system-level FPGA development environment which enables you to open and customize the M5302A. When used with a PathWave FPGA license (KF9000B), you now have access to the user-programmable FPGA and can insert your custom logic into the instrument. You can begin from HDL or a design in the included library and add or import Vivado, SystemVue and MATLAB components. Key benefits:

- Process signals in real time or accelerate bottleneck operations by running as hardware-in-the-loop
- Achieve your test requirements by inserting your own IP into the instrument.
- Scale-up designs or channel counts by adding multiple M5302As



PathWave Test Sync Executive

The PathWave Test Sync Executive enables rapid development of high performance, multi-channel, real-time synchronous solutions. It is enabled on the M5302A with a KS2201A license and has seamless interaction with PathWave FPGA. The Sync Executive features:

- Transparent multi-module synchronization by precisely time aligning multiple M5302A channels in the same module or across several modules
- Real-time synchronous execution including sequencing, branching, and looping
- Time-deterministic hardware-based execution

Technical Specifications and Characteristics

General characteristics

Module characteristics	
Bus interface and compatibility	PXle peripheral module (x8 Gen 3)
Number of slots	1
Volatile Module memory	8 GB (DDR4)
Non-volatile flash memory	1 Gb
Front panel connectors	
LVDS	ERF8-050
Trigger Channels	SMB male (8)
System Sync	Reserved for future use
Mechanical (nom)	
Size	3U/1-slot PXle standard 130.1 x 21.7 x 210 mm; includes connectors and handle extensions
Weight	365 g (0.8 lbs)

Module power requirements

Description	Value	
Total Power Dissipation	42 W	
Supply Voltage	+3.3 V	+12 V
Supply Current	1.8 A	3 A

LVDS connector characteristics

LVDS channels	
Functionality	LVDS plus auxiliary DUT power supply
Channel type	Differential, Bidirectional
Number of channels	28
Channel impedance	100 Ω differential (nominal)
LVDS output characteristics (typical)	
Output voltage range	1.25 V $\pm$ 175 mV (100 Ω differential termination)
Maximum output short circuit current	20 mA
Maximum output channel toggle rate	1.2 Gbps
LVDS input characteristics (typical)	
Differential input voltage range	0.3 - 1.425 V (DC coupled) 0.6 – 1.1 V (AC coupled)
Input common mode voltage threshold	0.1 – 0.6 V
Maximum input toggle rate	1.2 Gbps

LVDS channel skew characteristics (typical) ¹	
Maximum skew adjustment range	± 1667 ps (user) + ± 1667 ps (system) = ± 3333 ps (total)
Maximum skew adjustment resolution	50 ps
Maximum edge polarity skew	± 50 ps
Maximum uncalibrated inter-channel skew error ^{2,3}	± 150 ps
Maximum inter-channel skew drift ($\pm 5^\circ\text{C}$)	± 200 ps
Performance with option HV2	
Max uncalibrated inter-module skew error ^{4,5}	± 250 ps
Maximum inter-module skew drift ($\pm 5^\circ\text{C}$)	± 300 ps
HVI action/event time resolution	3.33 ns

DUT power supply (typical)	
Output voltage	5 V $\pm$ 5%
Maximum output current	0.5 A

¹ Note that a 1.2 Gbps data valid window = 833 ps

² Total uncalibrated skew error between any two channels on same module over $\pm 5^\circ\text{C} \leq 2 \times (\text{Max Uncalibrated Inter-Channel Skew Error} + \text{Max Inter-Channel Skew Drift} + \text{Max Edge Polarity Skew}) = 800$ ps

³ Total user-calibrated skew error between any two channels on same module over $\pm 5^\circ\text{C} \leq 2 \times (\text{Max Skew Adjustment Resolution} / 2 + \text{Max Inter-Channel Skew Drift} + \text{Max Edge Polarity Skew}) = 550$ ps

⁴ Total uncalibrated skew error between any two channels across separate modules over $\pm 5^\circ\text{C} \leq 2 \times (\text{Max Uncalibrated Inter-Module Skew Error} + \text{Max Inter-Module Skew Drift} + \text{Max Edge Polarity Skew}) = 1200$ ps

⁵ Total user-calibrated skew error between any two channels across separate modules over $\pm 5^\circ\text{C} \leq 2 \times (\text{Max Skew Adjustment Resolution} / 2 + \text{Max Inter-Module Skew Drift} + \text{Max Edge Polarity Skew}) = 750$ ps

General purpose trigger channel characteristics

Trigger channel characteristics	
Number of channels	8
Channel type	Single-ended, bidirectional, ground reference
Default state	1 M Ω nominal
Output characteristics (typical)	
Output voltage	
50 Ω load	50 mV – 1.676 V
High impedance load	28 mV – 3.264 V
Output impedance	50 Ω nominal
Maximum output channel toggle rate	150 MHz
Input characteristics (typical)	
Input voltage range	0 – 5 V
Minimum low voltage threshold	0.8 V
Maximum high voltage threshold	2 V
Load impedance	100 M Ω
Maximum input channel toggle rate	75 MHz

Trigger channel skew characteristics (typical) ⁶	
Maximum skew adjustment range	± 1667 ps (user) + ± 1667 ps (system) = ± 3333 ps (total)
Maximum skew adjustment resolution	50 ps
Maximum edge polarity skew	± 500 ps
Maximum uncalibrated inter-channel skew error ^{7,8}	± 500 ps
Maximum inter-channel skew drift ($\pm 5^\circ\text{C}$)	± 500 ps
Performance with option HV2	
Max uncalibrated inter-module skew error ^{9,10}	± 750 ps
Maximum inter-module skew drift ($\pm 5^\circ\text{C}$)	± 750 ps
HVI action/event time resolution	3.33 ns

⁶ Note that a 300 Mbs Gbps data valid window = 3333 ps

⁷ Total uncalibrated skew error between any two channels on same module over $\pm 5^\circ\text{C} \leq 2 \times (\text{Max Uncalibrated Inter-Channel Skew Error} + \text{Max Inter-Channel Skew Drift} + \text{Max Edge Polarity Skew}) = 3000$ ps

⁸ Total user-calibrated skew error between any two channels on same module over $\pm 5^\circ\text{C} \leq 2 \times (\text{Max Skew Adjustment Resolution} / 2 + \text{Max Inter-Channel Skew Drift} + \text{Max Edge Polarity Skew}) = 2050$ ps

⁹ Total uncalibrated skew error between any two channels across separate modules over $\pm 5^\circ\text{C} \leq 2 \times (\text{Max Uncalibrated Inter-Module Skew Error} + \text{Max Inter-Module Skew Drift} + \text{Max Edge Polarity Skew}) = 4000$ ps

¹⁰ Total user-calibrated skew error between any two channels across separate modules over $\pm 5^\circ\text{C} \leq 2 \times (\text{Max Skew Adjustment Resolution} / 2 + \text{Max Inter-Module Skew Drift} + \text{Max Edge Polarity Skew}) = 2550$ ps

Module timing and trigger characteristics

Module reference clock	
Frequency	100 MHz
Reference clock source	PXI_CLK100
Accuracy	Chassis dependent

Input/Output triggers	
Trigger sources	Software, PXI_TRIG, PXI_STAR, and front panel I/O
Trigger destinations	PXI_TRIG and front panel I/O
Trigger polarity	Active high or active low (programmable)

Reconfigurable FPGA Characteristics

FPGA characteristics	
FPGA Type	Xilinx Kintex UltraScale+ KU15P
Timebase	300 MHz (phase-locked to 100 MHz chassis clock)
Timebase source	PXI_CLK100
Available FPGA resources	
CLB registers	502320
CLB LUTs	251160
Block RAM Tiles (Mb)	480
UltraRAM (Mb)	80
DSP blocks	960

Environmental characteristics^{11,12}

Operating and storage conditions	Operating	Storage
Temperature	0°C to 45°C	-40°C to 70°C
Altitude	Up to 10,000 ft (3048 m)	Up to 15,000 ft (4572 m)
Humidity	Type tested, 95% RH up to 40°C, decreases linearly to 40% RH at 45°C (non-condensing)	
Warm-up time	30 minutes	
Vibration		
Operating random vibration: type-tested at 5 to 500 Hz, 0.21 g rms		
Survival random vibration: type-tested at 5 to 500 Hz, 2.09 g rms		

¹¹ Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions.

¹² Test methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3

Regulatory characteristics

Safety
Complies with the current versions of the following standards (dates and editions are cited in the Declaration of Conformity): – IEC/EN 61010-1 – Canada: CSA C22.2 No. 61010-1 – USA: UL std no. 61010-1
EMC
Complies with the essential requirements of the European EMC Directive as well as the current editions of the following standards (dates and editions are cited in the Declaration of Conformity): – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A – AS/NZS CISPR 11 – ICES/NMB-001 This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme la norme NMB-001 du Canada
South Korean class A EMC declaration
Information to the user: This equipment has been conformity assessed for use in business environments. In a residential environment this equipment may cause radio interference. – This EMC statement applies to the equipment only for use in business environment.
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Definitions and conditions

Specification (spec)
Describes the performance of parameters covered by the product warranty and are valid for the unit's operation within the stated environmental range unless otherwise noted. Specifications include production guardbands to account for the expected statistical performance distribution, measurement uncertainties, and changes in performance due to environmental conditions. Standard calibration services offered by Keysight will ensure all these specifications are measured and a related statement of compliance with specification provided in the resulting calibration report.
Typical characteristic (typ)
Intended to provide additional information including the expected performance of an average unit that is not covered by the product warranty. These characteristics are shown in italics or labeled as 'typical'. Performance of a customer unit to typical specifications may or may not be measured during a calibration service.
Nominal characteristic (nom)
A general, descriptive term that does not imply a level of performance. It is not covered by the product warranty. Represents the value of a parameter that is most likely to occur; the expected mean or mode of all instruments at room temperature (approximately 23 °C). These characteristics are shown in italics or labeled as 'nominal'. Performance of a customer unit to nominal specifications may or may not be measured during a calibration service.
Additional information
The data contained in this document is subject to change.

Ordering Information

Product	Description
M5302A	PXIe Digital IO Module, 28 LVDS Channels, 1.2 Gbps
Related software	Description
KS2201A	PathWave Test Sync Executive development license
KF9000B	PathWave FPGA design environment license

Learn more at: www.keysight.com

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