Wafer Prober Plug-in for Test Automation on PathWave

Workflow Automation for Silicon Photonics Wafer Probing

The Keysight Test Automation on PathWave (TAP) software provides powerful, flexible and extensible test sequence and test plan creation with additional capabilities that optimize your test software development and overall performance. The Wafer Prober Plug-in supports your workflow automation for integrated and Silicon Photonics wafer probing and test.

Keysight TAP is a modern Microsoft .NET-based application that can be used stand-alone or in combination with higher-level test executive software environments. Leveraging C# and the power of Microsoft Visual Studio, TAP is not just another programming language. It’s a platform upon which you can build your test solutions, maximizing your team’s productivity by using your existing software development tools and infrastructure.
Architecture

Included with Keysight TAP is the core sequencing engine, tools and plug-ins to minimize your test system development time and test execution speed. Instrument plug-ins provide test steps that can be added to work-flow sequences without needing to use instrument level programming commands.

The N7700210C Wafer Prober Plug-in further simplifies automation by handling the interface to the Formfactor semi-automated probe station hardware and Formfactor Velox and Silicon Photonics Tools software. Test steps realize wafer chuck movement and probe positioning and alignment tasks within a test plan and can be combined with instrument test execution steps. The wafer prober settings needed for positioning and RF and optical probe configuration are provided in the test steps for easy configuration.

![Diagram of TAP architecture](image)

Figure 1. KS8400A Pathwave Test Automation Features

**N7700210C Product Overview**

![Diagram of N7700210C Wafer Prober TAP Plug-In feature overview](image)

Figure 2. N7700210C Wafer Prober TAP Plug-In Feature Overview
Features

The Keysight Wafer Prober TAP Plug-In supports integrated photonics test workflow for both wafer and singularized die testing by:

1. Data ingress for wafer structure, device coordinates, device parameters and test conditions based on .csv and .xml files
2. Prober hardware setup for configuring the probe station for array & single fiber probes, edge & surface coupling, RF & DC electrical probes and probe orientations
3. Test steps that combine common probe station commands for prober and probe control and prober status inquiry
4. Communication to probe station and to other instrument plug-ins for test execution, test set-up and instrument conditioning, and result management

The N7700210C Wafer Prober TAP Plug-in simplifies automation by providing easy-to-use measurement steps for the Formfactor probe station that handle all the details for configuring the CM300xi silicon photonics probe station and Formfactor Velox and Silicon Photonics Tools software.

Operation

An example test setup for integrated photonics is shown below:

Figure 3. Example Test Setup for Optical and Electro-optical DC & RF Test
Tunable lasers, Lightwave Component Analyzer and optical power meters are connected to the device input and output ports via polarization synthesizers and optical switches. The optical switches route the optical test signals to and from different ports of the fiber array the test instruments. The detector connected to the LogAmp serves for the active alignment of the optical fibers to the device under test (DUT). RF and DC probes connect to the electrical ports of the integrated photonics device.

An integrated photonics test plan typically consists of a combination of test execution steps for:

- Controlling the probe station for moving the wafer chuck and the optical and electrical probes to the device to be tested on the wafer or die.
- Configuring signal routes between the instruments and the optical and electrical probes to device I/O ports.
- Performing measurements by first stepping the wafer and probes to the device IO ports, performing automated alignment for optimum coupling and then triggering a measurement.
- Measurement steps automatically pull geometric and position information about the optical and electrical device ports on wafer or die from the wafer and device data base and the corresponding test conditions from the measurement plan.

Configuring the workflow with sequences of steps and coordination with other instruments and resources using TAP is a powerful contribution to enhancing efficiency in test development and throughput.

The sequence of test steps for configuring signal routes, controlling the probe station and performing measurements can be flexibly arranged in a test recipe. The TAP user interface allows you to easily adapt, test and modify this recipe. It is also possible to create several device type or application specific test recipes. Figure 4 shows an example test recipe for optical and electro-optical DC & RF test.

![Figure 4. Example Test Recipe for Optical and Electro-optical DC & RF Test](image-url)
This test recipe is realized by a test plan in the TAP software as described in chapter “Measurement steps and test plan”. Test plans can be generated independent of individual wafers. The above example in Figure 4 would serve wafers with CWDM receivers where detector structures are coupled to drop filters that would need wavelength dependent responsivity measurements over an optical channel window and an opto-electrical S-parameter measurement at the channel center wavelength. In a Measurement plan the user can select which devices will be tested for a particular wafer. In the measurement plan the user can also specify several different measurements on a particular element, like bandwidth measurement under different detector bias conditions. Each measurement has an individual measurement ID that is used by the measurement steps for saving measurement results.
Installation

The details needed to install and use the TAP software are given in the plug-in help file. Briefly this entails the following steps.

- Installing Formfactor Velox and SiPh-Tools SW on the measurement PC
- Downloading and installing TAP (KS8400A) and the wafer prober plug-in (N7700210C)
- Optionally installing other SW and plug-ins like N7700100C Photonic Application Suite incl. TAP plug-in, N4370P01A (LCA plug-in) or KS8105A (Switch Manager)
- Installing the purchased or temporary evaluation TAP licenses.
- Then starting Velox and SiPh-Tools SW
- Starting TAP and adding the Velox software as Instrument
- Adding TAP Results Listeners as needed: SQLite for display in Results Viewer and CSV for file storage

Using the Wafer Prober Plug-in

Plug-in Structure and Workflow

The wafer prober plug-in uses the following sets of data and settings:

- Wafer Definition contains all information and geometrical data about the wafer or chip under test, reticle / die and subdie structure, down to individual elements on the subdie.
- Wafer Prober Settings with:
  - Basic prober settings:
    - Definition of chuck and probe home positions
    - Optical and electrical probe configuration
  - Measurement plan:
    - The measurement plan contains the list of silicon photonics elements on the wafer or chip under test that is going to be probed. Additionally, it provides supplementary information for the conditioning and execution of measurement test recipes.
  - Optical path settings:
    - The optical path settings contain a list of customer definable optical routes which can later be used in the test plan for routing and signal conditioning.
Wafer Definition

The wafer prober plug-in uses 4 hierarchies to store data about the wafer under test: wafer, reticle or die, subdie and subdie elements.

In the KS8400A test automation platform the wafer is treated as a DUT. Various definitions can be imported from csv and xml files and edited in the user interface.
Figure 6. Wafer Data Input Window

Figure 7 shows the list of subdies within a reticle / die on a wafer, including their dimensions and reference position with respect to the reticle / die origin. This information can be imported from CSV file and edited in subdie map mask. Subdies in the map can be selected for test.

Figure 7. SubDie Map with Geometrical Information

Figure 8 shows the subdie elements map that includes the list of elements on a selected subdie. The insert shows the element optical IO port characteristics for the element with ID E001.
Figure 8. List of Device Elements and Example of Element Optical IO Port Characteristics

For better visibility, elements can be labeled and assigned to user defined device classes. The subdie elements map table contains further useful data:

- Center wavelengths used for alignment.
- Device port numbers. These are used indicate input (stimulus) and output (response) interfaces.
- Coupling direction (e.g. West) for arrays as well as the array pitch and IO type (e.g. surface or edge).
- Incident angle and polarization of operation for grating couplers.

Similar information can be entered for device electrical ports.

**Wafer prober settings**

**Basic prober settings**

The “Basic Prober Settings” contain all basic settings to align the wafer prober plug-in with the actual prober setup. This includes (among others):

- Definition of chuck and probe home positions
- Optical and electrical probe configuration
Figure 9. Wafer Prober Settings

Selecting and setting home locations is an essential step in the preparation of an automated measurement. Home locations for optical or electrical ports can be specified by position information w.r.t. the subdie origin or by “Selecting by device” from the list of individual subdie elements. This list is populated from the element definition file that is loaded in the “Wafer Data Input Window” (see Figure 6).

Before starting the test script, the optical and electrical probes need to be positioned at these home locations in a manual process using the user interface of the wafer prober control SW (e.g. Velox and SiPh-Tools).

**Optical path settings**

In the “Optical Path Settings” optical routes can be set up between instrument ports and the fiber probes across multiple optical switches. These routes can be named individually and addressed directly in the test plan by the “switch optical path” test steps. Measurement plan

The “Measurement Plan” allows the user to specify individual measurements on a device. This is useful for performing measurements on multiport devices with multiple input and output ports. Examples are ring filter structures with input, add, drop and thru ports, simple 2x2 couplers or balanced detectors connected to optical 2x2 splitters. Other examples include detector or modulator measurements under various bias conditions. Each measurement has an individual measurement ID that is used by the measurement steps. for saving measurement results.
Measurement steps and test plan

The plug-in provides a set of measurement steps that can be added to an automated test plan in TAP. The desired function can be chosen from the “Steps” panel.

![Steps Panel of Wafer Prober Plug-in (Selection)](image)

The steps can then be configured in TAP with the necessary details for the desired measurement. A typical test plan might look like this:
A full list of test steps is provided in the table in “Appendix A: List of Available Steps”.

Once a test plan has been set up, it can be run from the Test Automation Software. A log of the process is recorded, and flow timing is also displayed (see lower part of Figure 11.).

TAP also provides information of the execution duration of each individual step. This is useful for optimizing the measurement throughput.

**Supported Probe Stations**

The N7700210C Wafer Prober TAP Plug-in provides automation for the following Probe Station:

- Formfactor CM300xi with Velox rev.2.5 and Silicon Photonics Tools rev.2.0
### Ordering Information

The N7700210C Plug-in is used with the KS8400A TAP software, which requires a separate license. The system prerequisites for KS8400A apply to use of the plug-in.

- Choose your software product.
- Choose your license term: perpetual or subscription.
- Choose your license type: node-locked, transportable, USB portable, or floating.
- Depending on the license term, choose your support subscription duration.

### Products

- N7700210C Wafer Prober TAP Plug-in
- KS8400A Test Automation Platform, Developer’s System

### License type and terms

<table>
<thead>
<tr>
<th>Product</th>
<th>License type</th>
<th>License</th>
<th>Perpetual Support subscription</th>
<th>Subscription License &amp; support subscription</th>
</tr>
</thead>
<tbody>
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<td>Node-locked (fixed)</td>
<td>R-x5y-001-A</td>
<td>+ R-x6y-001-z</td>
<td>R-x4y-001-z</td>
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<td>+ R-x6y-004-z</td>
<td>R-x4y-004-z</td>
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<td>USB Portable</td>
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<td>+ R-x6y-005-z</td>
<td>R-x4y-005-z</td>
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<td>Floating (single region)</td>
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<td>+ R-x6y-006-z</td>
<td>R-x4y-006-z</td>
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<td>Floating (worldwide)</td>
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<td>R-x4y-010-z</td>
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<td>KS8400A</td>
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</table>

**Subscription Duration**

- L 12 months (default)
- X 24 months
- Y 36 months
- Z 60 months

**License Terms**

- + perpetual
- Z subscription

1 USB portable license requires a certified USB dongle (available for additional purchase, Keysight part number E8900-D10)
## Appendix A: List of Available Steps

<table>
<thead>
<tr>
<th>Group</th>
<th>Step Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Configuration Commands</strong></td>
<td>Call Velox script</td>
<td>Loads a Velox script file in the Scripting Console and executes it.</td>
</tr>
<tr>
<td></td>
<td>Velox command</td>
<td>Sends a user-defined command to the Velox software.</td>
</tr>
<tr>
<td></td>
<td>Import wafer map definition</td>
<td>Imports the wafer map definition from Velox and updates the wafer under test properties.</td>
</tr>
<tr>
<td></td>
<td>Open wafer map file in Velox</td>
<td>Opens the specified wafer map file in Velox.</td>
</tr>
<tr>
<td></td>
<td>Save Velox wafer map to file</td>
<td>Saves the current wafer map in Velox as native MAP file.</td>
</tr>
<tr>
<td><strong>Prober Commands</strong></td>
<td>Move chuck to contact height</td>
<td>Moves the chuck to contact height.</td>
</tr>
<tr>
<td></td>
<td>Move chuck to separation height</td>
<td>Moves the chuck to separation height (save height for X/Y movements).</td>
</tr>
<tr>
<td></td>
<td>Move optical probe(s) to alignment height</td>
<td>Moves the optical probes(s) to alignment height.</td>
</tr>
<tr>
<td></td>
<td>Move optical probe(s) to probe height</td>
<td>Moves the optical probe(s) to probe height.</td>
</tr>
<tr>
<td></td>
<td>Move optical probe(s) to separation height</td>
<td>Moves the optical probe(s) to separation height.</td>
</tr>
<tr>
<td></td>
<td>Move positioners to contact height</td>
<td>Moves the selected electrical positioners Z-axes to preset contact heights.</td>
</tr>
<tr>
<td></td>
<td>Move positioners to separation height</td>
<td>Moves the selected electrical positioners Z-axes to preset separation heights (save height for X/Y movements).</td>
</tr>
<tr>
<td><strong>Stepping</strong></td>
<td>Step to first die</td>
<td>Moves the chuck to the first die on the wafer map.</td>
</tr>
<tr>
<td></td>
<td>Step to next die</td>
<td>Moves the chuck to the specified die location. If all parameters are &quot;-1&quot;, the chuck will automatically step to the next logical die location.</td>
</tr>
<tr>
<td></td>
<td>Step to next subdie</td>
<td>Moves the chuck to the specified subdie location. If the subdie index is empty, the chuck will automatically step to the next logical subdie location.</td>
</tr>
<tr>
<td></td>
<td>Step to subdie element</td>
<td>Moves the optical probes to the specified subdie element location.</td>
</tr>
<tr>
<td><strong>Test Execution Commands</strong></td>
<td>Align optical probes</td>
<td>Runs an alignment on the current subdie element and returns the coupling power.</td>
</tr>
<tr>
<td></td>
<td>Check probing configuration</td>
<td>Checks the integrity and consistency of the current probing test plan. In case any conflicts or errors are found, the current test plan will be aborted.</td>
</tr>
<tr>
<td>Device Definition</td>
<td>Set optical parameters</td>
<td>Adds the defined subdies for the selected die at the current wafer prober die.</td>
</tr>
<tr>
<td>-------------------</td>
<td>------------------------</td>
<td>--------------------------------------------------------------------------------</td>
</tr>
<tr>
<td></td>
<td>Add subdies</td>
<td>Adds the defined subdies for the selected die at the current wafer prober die.</td>
</tr>
<tr>
<td></td>
<td>Add subdie elements</td>
<td>Adds the defined subdies elements for the selected die and subdie in SiPh-Tools.</td>
</tr>
<tr>
<td></td>
<td>Delete all subdies</td>
<td>Deletes all subdies from all dies.</td>
</tr>
<tr>
<td></td>
<td>Delete all subdie elements</td>
<td>Deletes all subdie elements defined in SiPh-Tools.</td>
</tr>
<tr>
<td>Signal Conditioning</td>
<td>Switch optical path</td>
<td>Switches an optical path according to the definitions in the optical path definitions.</td>
</tr>
<tr>
<td>Iteration</td>
<td>Wafer item loop</td>
<td>Iterates over the selected wafer item.</td>
</tr>
<tr>
<td></td>
<td>Measurement loop</td>
<td>Iterates over the current measurement plan.</td>
</tr>
<tr>
<td>Output Variables</td>
<td>Output center wavelength</td>
<td>Creates an output variable with the current center wavelength to be used in other test steps.</td>
</tr>
<tr>
<td></td>
<td>Output comment info</td>
<td>Creates an output variable with the current comment info to be used in other test steps.</td>
</tr>
<tr>
<td></td>
<td>Output element class ID</td>
<td>Creates an output variable with the class ID of the current loop element to be used in other test steps.</td>
</tr>
<tr>
<td></td>
<td>Output element ID</td>
<td>Creates an output variable with the ID of the current loop element to be used in other test steps.</td>
</tr>
<tr>
<td></td>
<td>Output extended settings</td>
<td>Creates an output variable with the current extended settings to be used in other test steps.</td>
</tr>
<tr>
<td></td>
<td>Output receive channels</td>
<td>Creates an output variable with the current optical receive channels to be used in other test steps.</td>
</tr>
<tr>
<td></td>
<td>Output test recipe</td>
<td>Creates an output variable with the test recipe information of the current loop element to be used in other test steps.</td>
</tr>
</tbody>
</table>
Related Literature

- PDL Measurement using the Keysight Polarization Controller
- Measuring Polarization Dependent Loss of Passive Optical Components
- Polarization-Resolved Measurements using Mueller Matrix Analysis
- Polarization Alignment Methods
- All-States Method for PDL or PER
- State of the Art characterization of optical components for DWDM applications
- IL and PDL spectra with the N7786B Polarization Synthesizer and the N7700A Photonic Application Suite
- Programming Keysight Technologies Continuous-Sweep Tunable Lasers
- On-Wafer Testing of Opto-Electronic Components Using the Lightwave Component Analyzers
- FormFactor’s Autonomous Silicon Photonics Measurement Assistant
- Integrated Photonics Test Brochure

More Information

www.keysight.com/find/N7700210C