Leti-UTSOI2: A compact model for Ultra-Thin Body and BOX FDSOI technology accounting for back interface inversion

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Outline

- FDSOI technology
  - Advantages of UTBB-FDSOI technology
  - Main device physics specificities with respect to bulk
- FDSOI transistor models
  - Limits of proposed solutions
  - Motivations for development of Leti-UTSOI2
  - Leti-UTSOI2 in compact model landscape
- Leti-UTSOI2 description
  - Original solutions
    - Surface potential calculation
    - Drain current compact expression
    - Quantum confinement
    - Short channel effects
    - Ground-plane depletion
    - Intrinsic charge model
  - A complete and available model
- Conclusions
Advantages of UTBB-FDSOI technology

- Fully-depleted device technologies required for sub-20nm node
  - Better scalability than bulk transistors
  - Improved variability thanks to undoped / low-doped channels

- Among these technologies, UTBB-FDSOI has several advantages
  - Simplest process (planar device, close to bulk)
  - Possibility to use back-bias to dynamically tune speed/power trade-off at circuit level

- Ability to apply large back-bias is a powerful extra performance enabler for UTBB-FDSOI technologies

Fig. 3: Dual ARM A9 Frequency vs. Vdd in FDSOI for various BB conditions compared to BULK 28LP technology

*From D. Jacquet et al., VLSI, 2013*
Main device physics specificities wrt bulk

- 2D electrostatics

Improved 2D electrostatics (i.e. less short channel effects) thanks to reduced junction depth ($X_j$ is limited to $t_{Si}$)

Removed channel random dopant fluctuations, thanks to undoped channel (buried oxide suppresses punchthrough current path)
Main device physics specificities wrt bulk

- Source/drain junctions

No source/bulk and drain/bulk area junctions
⇒ No junction currents
⇒ Junction capacitance replaced by (small) $C_{BOX} \times A_{source/drain}$ capa.
Main device physics specificities wrt bulk

- GIDL current

GIDL flows between source and drain and not between bulk and drain
Main device physics specificities wrt bulk

- Thermal behavior

Larger body to bulk thermal resistance, because oxide thermal conductivity is about 100x smaller than silicon one

⇒ At circuit level, $R_{th,BOX}$ negligible. FDSOI cooler thanks to reduced dynamic consumption

⇒ At device level, self-heating effect (a few tens of K)
Main device physics specificities wrt bulk

- Back bias effect: From bulk...

![Diagram of device physics](image-url)
Main device physics specificities wrt bulk

- … to FDSOI

In subthreshold regime, FDSOI 1D electrostatics is simpler than bulk one (all is linear), but conduction can take place at front or back interface.
Main device physics specificities wrt bulk

- Back bias effect: Two slopes on $V_{th}(V_{bs})$ curve
Main device physics specificities wrt bulk

• Where does conduction take place?
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Limits of proposed compact models

- Existing solutions for FDSOI assume back interface always depleted
  - Suitable up to moderate FBB (~Vdd)
  - For large FBB, accuracy is progressively lost e.g. on C(V) characteristics
  - **Predictability is limited in FBB mode** since semi-empirical parameters have to be used to compensate the effect of inadequate assumption

Limit of predictability
Long channel C(V)
\( T_{ox}=1\text{nm}, T_{Si}=6\text{nm}, T_{BOX}=20\text{nm} \)
Motivations for development of Leti-UTSOI2

- Enlarge the physically-described range of back plane polarizations with respect to existing solutions
- Improve the overall predictability of the model over technological parameters
- While benefiting from UTSOI1 maturity
Leti-UTSOI2 in compact model landscape

- 1990: BSIM3
- 1995: \( V_{th} \) (BSIM4)
- 2000: BSIM SOI (Partially and fully-depleted)
- 2005: Charge (EKV)
- 2010: Surface potential (HiSIM, HV, SOI, ...)
- 2015: Surface potential
  - Local / global
  - BSIM CMG/IMG
  - BSIM6
  - HiSIM
  - PSP
  - UTSOI
  - UTSOI2
Leti-UTSOI2 in compact model landscape

- Model structure

Leti-UTSOI2 is a surface potential model featuring local / global scale levels, as PSP and Leti-UTSOI1
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Original solutions: Interface potentials calc.

- **Challenge**
  - Find a sequence of analytical calculations that gives the solution for 1D Poisson’s equation + boundary conditions in all regimes!
  - Many papers in literature on this topic but need for a simpler solution

<table>
<thead>
<tr>
<th>Reference</th>
<th>Interpolation functions</th>
<th>Approx. on potential vertical profile</th>
<th>Numerical resolution</th>
<th>Comput. of boundaries between modes</th>
<th>Use of Lambert functions</th>
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<tbody>
<tr>
<td>H. Lu et al. IEEE TED 2006</td>
<td>No</td>
<td>No</td>
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<td>A.S. Roy et al. SSE 2006</td>
<td>Yes</td>
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<td>Z. Zhu et al. JJAP 2007</td>
<td>Yes</td>
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<td>F. Liu et al. IEEE TED 2008</td>
<td>No</td>
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<td>H. Abebe et al. Jour. Semi. Tech. Sc. 2009</td>
<td>No</td>
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<td>A. Sahoo et al. TED 2010</td>
<td>No</td>
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<td>S. Jandhyala et al. TED 2011</td>
<td>No</td>
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<td>A. Abraham et al. IEEE TED 2012</td>
<td>No</td>
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<td><strong>Our objective</strong></td>
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G.Dessai, G.Gildenblat, SSE, 2010
Original solutions: Interface potentials calc.

- Developed solution
  - Re-arranging the starting set of 3 equations allows to define a unique equation to be solved with front surface potential as unique variable
  - Usual procedure, based on initial guess + few error corrections based on Taylor expansion of the equation, is carried out
  - Surface potential calculation is (almost) as simple as in PSP or UTSOI1

Accuracy is <10feV for UTBB as well as IDG MOSFETs

*T. Poiroux et al., IEDM, 2013*
Original solutions: Drain current model

- **Challenge**
  - Usual linearization of inversion charge wrt front surface potential along the channel not suitable for UTBB with possible back inversion

- **Developed solution**
  - Definition of an effective electrostatic potential, whose gradient governs the drift component whatever the position of the inversion charge in the film
  - Generalization of the inversion charge linearization concept

  \[ \Rightarrow \text{Compact expression of the drain current, very accurate in all regimes} \]
Original solutions: Quantum confinement

- Developed solution
  - Bias dependent effective geometry prior to surface potentials calculation
  - 2nd order correction on drain current and charges

⇒ Consistent description of DC and AC models

Excellent predictability of AC core model
(same parameters in TCAD and model)
Original solutions: Short channel effects

- Developed solution
  - Equivalent geometry and biases defined prior to surface potential calculation in such a way that 1D calculation gives 2D result
  - Model predictability further improved in UTSOI 2.1.0 by linking 2D electrostatic model to device geometry
  
  \[ \text{Consistent description of DC and AC models} \]

Short channel effects – Physical basis
(subthreshold slope, roll-off, DIBL)
Original solutions: Backplane depletion

- Developed solution
  - Effective back bias calculated prior to surface potential calculation
  ⇒ Consistent description of DC and AC models
Original solutions: Charge model

- **Challenge**
  - Partitioning of the inversion charge between source and drain is usually based on front interface potential: not relevant in our case

- **Solution adapted from G. Dessai et al, TED, 2010**
  - Solution based on the effective charge concept, obtained in a straightforward way from our drain current calculations
# A complete and available model

<table>
<thead>
<tr>
<th>Physical effect</th>
<th>UTSOI1</th>
<th>UTSOI2</th>
</tr>
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<tbody>
<tr>
<td>Interface coupling</td>
<td>YES</td>
<td>YES</td>
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<td>Back interface inversion / dual channel operation</td>
<td>NO</td>
<td>YES</td>
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<td>Ground-plane depletion</td>
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<td>Quantum confinement</td>
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<td>Velocity saturation</td>
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<td>Short channel effects</td>
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<td>Channel length modulation</td>
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<td>Series resistance with gate voltage dependence</td>
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<td>Parasitic currents: Gate current, GIDL/GISL</td>
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<td>Parasitic capacitances: overlap, fringe</td>
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<td>Self-heating effect</td>
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<td>Stress model</td>
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<tr>
<td>Noise model: Flicker, thermal, induced gate, shot</td>
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<td>YES</td>
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<td>Source/drain junction asymmetry</td>
<td>NO</td>
<td>YES</td>
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</tbody>
</table>
A complete and available model

- Leti-UTSOI2 fulfills standard requirements from quality assurance and convergence tests for circuit design
- Accuracy against hardware data has been extensively checked (T. Poiroux et al., MOS-AK, Dec 2013)
- 1st release available in SPICE simulators since end of 2013

Example of circuit simulation
Conclusions

- Leti-UTSOI2 is the **first** and **unique** complete compact model accounting for back interface inversion in UTBB transistors
  - A formal symmetry between front and back interface has been respected in all equations of the core model
  - Model core is valid for all Independent Double Gate MOSFETs
- Predictability has been extensively checked against TCAD simulations
- Accuracy has been checked against silicon data
- Standard Quality and Robustness tests are successfully met for circuit design applications

- **UTSOI 2.0.0** is available since end 2013
- **UTSOI 2.1.0** will be available in Q4 2014
Acknowledgements

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- Authors would like to thank

- For more information about UTSOI, please visit http://www-leti.cea.fr/en/How-to-collaborate/Collaborating-with-Leti/UTSOI
Thank you for your attention