Maximising Serial Bandwidth And Signal Integrity In FPGAs

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Agenda

➤ Overview
  – Our transceivers
  – Serial Protocol Landscape

➤ Features to meet requirements
  – PLLs
  – Jitter Generation
  – Equalization

➤ Validation methods
  – Eye Scan
  – IBIS AMI and PDN modeling

➤ 3D IC advantage

➤ Summary
7 series offers a full transceiver portfolio for variant customer needs

- Ultra-high performance GTZ: **28.05Gb/s X 16**
- High-end Low-power GTH: **13.1Gb/s X 96**
- Mid-Range GTX: **12.5Gb/s X 32**
- High-Volume Low-Power GTP: **6.6Gb/s X 16**

- Virtex-7 HT has up to **2.802Tbps** total transceiver bandwidth
  - 16 GTZ and 72 GTH transceivers
Xilinx 7 Series: 4 Transceivers with superior performance

- **GTP @ 6.6Gb/s**
- **GTX @ 12.5Gb/s**
- **GTH @ 13.1Gb/s**
- **GTZ @ 28Gb/s**
How can we group serial protocols?

- PCIe Gen1
- PCIe Gen2
- PCIe Gen3
- SATA Gen1
- SATA Gen2
- SATA Gen3
- USB 3.0
- SDI
- HD-SDI
- 3G-SDI
- Vby1
- DisplayPort
- PCIe Gen1
- PCIe Gen2
- PCIe Gen3
- SATA Gen1
- SATA Gen2
- SATA Gen3
- DisplayPort
- USB 3.0
- CPRI
- CPRI
- CPRI
- XAUI
- HiGig2
- Fibre Channel
- Interlaken
- JESD204a
- CEI-6G LR/SR
- CPRI
- JESD204b
- CEI-11G
- CPRI
- CAUI/XLAUI
- nPPI
- 10GBASE-CR
- 10GBASE-KR
- SFI-Linear
- SFI-Limiting
- 10G-SDI
- Fibre Channel
- Interlaken
- CAUI-4
- CPPI-4
- CEI-28G
- OTU2/3/4
- CEI-11G
- JESD204b
7 Series GTH has the best equalization capability in the FPGA industry
- Compensates for reflection in long channels to support tough 10G backplanes

7 Series GTX equalization is second only to 7-GTH in the FPGA industry
- Industry’s only Fully auto-adaptive DFE for ease of use
PLLs: The source of all good things

➤ **GTX/GTH:**
  - 4 Ring and 1 LC per Quad

➤ **GTP:**
  - 2 Ring per Quad

➤ **GTZ:**
  - 8 LC tanks per octal for minimum jitter

➤ **Architecture optimized**
  - Low jitter
  - Low system power
TX PLL + Driver: Best in class jitter output

- **GTP/GTX/GTH/GTZ**
  - All use 3-tap setup: reduce DJ
  - Do not want to inject extra power into inconsistencies, better to rely on RX DFE

- **PLL**
  - Lowest RJ possible at all line rates.
Decision Feedback Equalization (DFE)

- A nonlinear equalizer that uses previous symbols to eliminate the Inter-Symbol-Interference (ISI) on current symbol.
  - The ISI on current symbol, caused by previous symbols, is subtracted by DFE.

\[ y(t) = u(t) + \sum_{i=1}^{n} w[i] \ast y_d(t - i \ast UI) \]
CTLE vs DFE:

- GTX
  - Auto-adapting DFE makes difficult links easy to tune

- GTH:
  - +2 fixed, +4 sliding taps = better tuning on harder channels
  - Auto-adapting CTLE in DFE path

- GTP/GTZ
  - Auto-Adapting CTLE

- So what? Auto-Adaptation.
  - Hand tuning a DFE is HARD WORK, takes time and is unreliable.
Several DFE taps compensate reflections in short distance
- 5 tap @ 10Gbps => ~1.5 inch

Virtex-7 GTH with DFE + XARC compensates reflections further in the channel
- XARC = Xilinx Advanced Reflection Cancellation
- Compensates 10x distance of reflection with auto adaptation (up to 64UI)
2D Eye Scan

- Parallel scan sampler in PMA
  - Post CTLE and DFE
- Non destructive
  - Full in service BER link margin
- Advanced PCS error measurement
  - Pattern analysis
Backplanes Support with 7 Series Transceiver

- 7-GTX is designed to support 10GBase-KR (well-designed high confidence channels)
- 7-GTH will provide enhanced 10GBase-KR support
- 7-GTP will support custom backplane up to 3.125Gbps
- 7-GTZ will support CEI-28G VSR but not backplane applications

### 7 Series GT Backplane?

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<th>Backplane?</th>
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Driving 10G Backplanes

Challenges

– Understanding your backplane impairments
– Maximizing signal quality and reducing impact due to loss, reflection and crosstalk
– Optimizing transceiver parameters to ensure robust receiver operation

Z-Pack TinMan System

– Low cost Tyco connector for KR
– 2 Daughter Cards: 5 inch Nelco 4000-6; 0.125” thickness & 0.005” trace width
– Backplane: 4”/8”/16”/24” Nelco 4000-13; 0.2” thickness & 0.007” trace width

Total ~30dB loss @ 5.6GHz
Proven Optical Interoperability

**Challenges**
- Access to lowest jitter transceivers
- Interoperability with optical vendors
- Accurately and efficiently check links

**7 Series Solution**
- Low Transmit Jitter (frequently < 0.28UI)
- High Jitter Tolerance for maximized margin
- 10G Optical interoperation without re-timers is achieved
  - SFP+ without re-timers
- System tuning easy with ChipScope 2-D eye scan
High Bandwidth Chip to Chip Interfaces

**Challenges**
- Need readily available proven IP
- High bandwidth operating at any data rate
- Low latency

**7 Series Chip to Chip Solution**
- Aurora core available through CoreGen as part of standard Xilinx tool flow
- Lightweight Serial Protocol
- Supports all GT variants at all line rates
- Extremely Flexible
  - Embedded clock enables long traces
  - Elastic buffers provide high skew tolerance
Proven PCI Express x8 Gen3

**Challenges**
- Out of the box IP Solution
- Compliant to Industry Specifications
- DMA to maximize bandwidth
- Scalable solution

**7 Series PCIe Solution**
- Complete Soft and Hard Gen3 Solutions
- Interoperable with Intel Sandy Bridge
- Full x8 Gen3 bandwidth
- Up to 1866 DDR3
- Scalable from x1-8 Gen1-3
Demo Setup
12.5 Gbit/s Backplane
Advanced Tools and IP to Accelerate and Simplify

➤ ChipScope Pro Serial Toolkit
  – Analyze Physical Environment
  – Auto Adapt and Optimize
  – Measure and “See” Eye in the Chip
    • Additional solution to “probing signals” challenge

➤ Xilinx and Third Party Serial IP
  – Industry Specific IP (Interlaken, OTU…..)
  – Common Protocol IP (PCIe, CPRI,…..)

➤ References and Resources
  – Characterization Reports
  – IBIS- AMI models and S-Parameter files
  – Interoperability Reports
  – Evaluation and Characterization Boards
Advanced Tools and IP to Accelerate and Simplify

Agilent FPGA Probe

- Access up to 128 internal signals per external dedicated debug pin.
- FPGA timing remains unchanged when selecting new sets of internal signals.
Xilinx Transceiver IBIS-AMI modeling with ADS
Simulating FPGA Power Integrity Using S-Parameter Models


The purpose of a Power Distribution Network (PDN) is to provide power to electrical devices in a system. Each device in a system not only has its own power requirements for its internal operation, but also a requirement for the input voltage fluctuation of the power rail. For Xilinx Kintex™-7 and Virtex®-7 FPGAs, the analog power rails have an input voltage fluctuation requirement of not more than 10 mV peak-to-peak from the 10 kHz to the 80 MHz frequency range. The self-generated voltage fluctuation on the power rails is a function of frequency and can be described by Ohm’s Law: Voltage (frequency) = Current (frequency) x Self-Impedance (frequency).

Thus, if the user determines the self-impedance (frequency) and knows the current (frequency) of the PDN, then the voltage (frequency) can be determined. The self-impedance (frequency) can easily be determined by simulating the frequency domain self-impedance profile of the PDN and is, thus, the subject of this white paper.
Benefits of Heterogeneous Integration

▶ Highest levels of integration
▶ Form-fit-function die for varying design requirements
▶ Electrically isolated 28G transceivers for optimal signal integrity

![Diagram showing benefits of heterogeneous integration](image)
28nm FPGA with 28Gbps GTZ Transceiver: 7VH580T

Heterogeneous VH580T

VH580T GTZ TX
Eye Diagram: 28.05Gb/s

7VH580T Demo Video

RX Eye Scan: 28.05Gb/s,
Thru 12.5dB Trace
28nm FPGA with 28Gbps GTZ Transceiver: 7VH580T

Heterogeneous 3DIC VH580T
Delivering Customer Value with 28nm Transceivers

**Programmable Systems Integration**
Industry’s highest level of serdes integration
Stacked silicon 3D IC and VCXO integration

**Increased System Performance**
>1.9 Tbps performance via 13G - 28G Serdes and Channel Optimization

**BOM Cost Reduction**
Eliminate multiple FPGAs and Transceiver Costs

**Total Power Reduction**
High integration & 28nm HPL process → low power

**Accelerated Design Productivity**
TTM and TIM advantage through programmability
Tools, IP and Targeted Design Platforms

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Questions? Questions!

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