What's new in J-BERT N4903B software release 7.61?

Other:

- Added USB 3.1 pattern files
- Added CEI patterns files

Known defects in version 7.61

No.	Defect #	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings.
2	SAD00415423	SER != 0 or BER != 0 after a stop/start
3	SAD00454108	N4903B does not work with Agilent IO-Library 16.2. Users should not install IO lib 16.2 to J-BERT
4	SAD00454493	Pressing "Output off" does not turn off outputs of connected N4916B and N4876A

Software History

J-BERT N4903B software release 7.60

Analysis of 128b/132b coded patterns (Option A03)

The analysis of 128b/132b coded patterns enables receiver testing of USB 3.1 ports.
The BERT error detector ignores the 128b/132b coded Skip Ordered Sets during error counting. It is able to handle the variable length of these SKPOS. The maximum bit rate for this mode is 10.35 Gb/s. SW 7.60 is required.

Other:

- N4903B: Updated user documentation
- M8061A: Updated Getting Started Guide

Defects fixed in version 7.60

No.	Defect #	Description
1	SAD00457221	M8061A Multiplexer connection diagram is incorrect
2	SAD00456065	N4903B is missing PCIe 1.0 patterns
3	SAD00457342	After loading the settings file, the sequence does not run correctly
4	SAD00457336	Update of the lower left data rate display no longer works after loading a setting
5	SAD00457313	Switching the error detector between BER and SER/FER mode causes the pattern generator to pause
6	SAD00457337	Audio server error message 80110, PG only unit

Known defects in version 7.60

No.	Defect #	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings.
2	SAD00415423	SER != 0 or BER != 0 after a stop/start
3	SAD00454108	N4903B does not work with Agilent IO-Library 16.2. Users should not install IO lib 16.2 to J-BERT
4	SAD00454493	Pressing "Output off" does not turn off outputs of connected N4916B and N4876A

J-BERT N4903B software release 7.50

New extension to 28.4 Gb/s with 8-tap de-emphasis (M8061A support)
With SW 7.50 the N4903B can control the M8061A 28.4 Gb/s multiplexer 2:1 with de-emphasis option. M8061A offers 8-tap de-emphasis, f/2 jitter injection capabilities and internal superposition of level interference (common-mode and differential mode). M8061A can be controlled from J-BERT N4903B user interface when SW 7.50 or later is installed. The N4903B requires a second output channel (opt 002). The connection is via USB to the AXIe chassis of M8061A.

Other:

- **N4916B:** new SW revision for stand-alone operation (zip file rev. 1.1.16.0) enhancement to allow injecting f/2 jitter. Pre-requisite is N4916B with options -STD and -001. In addition the N4916AB requires a return-to-factory re-calibration to use the f/2 jitter (case-by-case).
- N4876A: new SW revision for stand-alone operation (zip file rev. 1.0.0.9)
- N4903B: user documentation updated
- M8061A: getting started guide
- Agilent End-use-license agreement updated

Defects fixed in version 7.50

No.	Defect #	Description
1	SAD00455990	J-BERT jitter tolerance number of points reverts to default
2	SAD00455562	Self-test reports "failed" but details do not show any failure
3	SAD00456080	Eye diagram measurement stopped accumulating waveforms
4	SAD00456823	J-BERT accumulated results bug
5	SAD00456212	Error when switching between setting files
6	SAD00456900	SER, FER and cBER incorrect with cBER calculated based on SER
7	SAD00456944	SSC configuration was wrong
8	SAD00455946, SAD00455591	N4903B user documentation fixes (opt. 002 pattern set-up information in UG, ventilation requirements in GSG)

Known defects in version 7.50

No.	Defect #	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings.
2	SAD00415423	SER != 0 or BER != 0 after a stop/start
3	SAD00454108	N4903B does not work with Agilent IO-Library 16.2. Users should not install IO lib 16.2 to J-BERT
4	SAD00454493	Pressing "Output off" does not turn off outputs of connected N4916B and N4876A

J-BERT N4903B software release 7.40

PCIe® 3.0 handling of SKPOS: when the SER/FER analysis option (N4903B-A02/-UA2) is installed the error counter ignores changes in the number or length of 128b/130b coded PCIe symbols, the so-called Skip Ordered Sets (SKPOS).

Error Detector Trigger Output: activated whenever a filler symbol or SKPOS is recognized by the error detector. This allows the J-BERT pattern sequencer to react on trigger patterns from a device under test. Requires SER/FER analysis option (N4903B-A02/UA2).

MIPI M-PHY: in case of synch-loss no errors are counted.

Other:

- N4916B de-emphasis signal converter: updated user manuals (zip file rev. 1.1.15.0)
- N4876A 28.4 Gb/s multiplexer: updated user manuals (zip file rev. 1.0.0.9)

Defects fixed in version 7.40

No.	Defect #	Description
1	SAD00449745	RJ reported wrong value in jitter tolerance compliance
2	SAD00449746	Number of steps is not set back to default setting in jitter tolerance compliance
3	SAD00454710	Create SCPI command to close pop-up dialog boxes
4	SAD 00449864, SAD 00452509, SAD 00454106	User documentation corrections

Known defects in version 7.40

No.	Defect #	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings.
2	SAD00415423	SER != 0 or BER != 0 after a stop/start
3	SAD00454108	N4903B does not work with Agilent IO-Library 16.2. Users should not install IO lib 16.2 to J-BERT
4	SAD00454493	Pressing "Output off" does not turn off outputs of connected N4916B and N4876A

J-BERT N4903B software release 7.31

Defects fixed in version 7.31

No.	Defect #	Description
1	SAD00452788	Jitter sources accidentally turned off during jitter tolerance measurement

J-BERT N4903B software release 7.30

Error detector bit rate: display of data rate measured by CDR

Support of N4903B-L01/L0x: special option

Other:

- N4916B de-emphasis signal converter: updated user manuals (zip file rev. 1.1.13.0)
- N4876A 28.4 Gb/s multiplexer: updated user manuals (zip file rev. 1.0.0.7)

Defects fixed in version 7.30

No.	Defect #	Description
1	SAD00448020	Double and missing points in jitter tolerance compliance measurement for USB3, PCIe3.0
2	SAD00449006	SER accumulated results not saved in the text file
3	SAD00449667	Reduce intrinsic jitter of disabled BUJ source on certain instruments

Known defects in version 7.30

No.	Defect #	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings.
2	SAD00415423	SER != 0 or BER != 0 after a stop/start

J-BERT N4903B software release 7.20

Support of Microsoft Windows XP FES:

- Software is now Windows® XP FES (XP For Embedded Systems) compliant

New USB3 compliance patterns added

- New USB3 Pattern with unique position of detect symbol for faster synchronization of error detector: CP0_2SKP_for_SER_ED.ptrn
- New USB3 Pattern with unique position of detect symbol for faster synchronization of error detector: CP0_4SKP_for_SER_ED.ptrn

New N4916B De-Emphasis firmware version 1.1.8.0 released

- Bugfix: Amplitude setting below 12.5mV leads to too big amplitude.
- Reliability improvement by enhanced power-up/down sequencing.

Defects fixed in version 7.20

No.	Defect #	Description
1	SAD00441279	GUI does no longer allow use of 2^31-1 PRBS in sequences
2	SAD00442285	Jitter Tolerance Characterization Doesn't Work in USB Compliance (SER) Mode.

Known defects in version 7.20

No.	Defect #	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings.
2	SAD00415423	SER != 0 or BER != 0 after a stop/start

J-BERT N4903B software release 7.10

PCIe 3.0 receiver test support:

- PJ jitter sweep curve according to PCIe 3.0 added (requires opt. J10)
- Added a new type of PRBS 2^23-1 with the polynomial X^23 + X^21 + X^16 + X^8 + X^5 + X^2 + 1 (same as PCIe 3.0 scrambler); named PRBS23P (:SOURce1::PATTern:: [SELect][?] …,PRBS23P,... ; and sequence language by a new keyword (PRBS23P) expanded correspondingly)
- Added demo patterns for PCIe 3.0
    - 8x compliance pattern (for lane 0..7 and 8..15)
    - 8x modified compliance pattern (for lane 0..7 and 8..15)

Pattern editor improvements:

- New dynamic insert mode to automatically increase/reduce the pattern length while editing.
- Indicate illegal pattern length that cannot be rolled out to pattern length granularity within the maximum pattern length.
- 8b/10b editing
    - Indicate running disparity errors for 8b/10b applications.
    - Indicate that the pattern will cause running disparity errors when being looped.
    - 8b/10b symbols can now be used together with SATA OOB(out-of-band signaling) mode, this allows entry of Z symbols for OOB application using external channel addition of data out and auy data out.
    - Define running disparity at the start of the pattern.
    - Optional automatic correction of running disparity while editing.
- Export even/odd bits to generate Error Detector expected pattern files to be used in half-rate under-sampling applications.
- Added conversion options that allow to easily convert Standard to Alternate patterns and vice versa.
    - Assign standard pattern to A or B.
    - De-multiplexing standard pattern to A and B.
    - Multiplex alternate pattern to a standard pattern.
    - Discard either A or B part on conversion of an alternate pattern to a standard pattern.
- New and improved Block Edit functionality
    - Same Block Edit capabilities in pattern editor and sequence pattern editor.
    - Swap, Copy, Reverse traces
    - Rotate pattern left/right
    - Rotate pattern to align at an user defined bit sequence or 8b/10b symbol.
    - Invert running disparity in 8b/10b mode.
    - Correct running disparity in 8b/10b mode.
- Find and Replace functionality for binary, hex, 8b/10b, OOB and PAM4 modes.

Others:

- Added demo patterns for USB3.0
- New sequences for DisplayPort added

- De-emphasis signal converter N4916B Software update (N4916B zip1.1.4.0)
- 28 Gb/s Multiplexer N4876A Software update (N4876A zip 1.0.0.4)

Notes:

- IVI-COM driver version 1.2.7.0 does not yet support Win7 64bit OS.

Known defects in version 7.10

No.	Defect #	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings.
2	SAD00415423	SER != 0 or BER != 0 after a stop/start

Defects fixed in version 7.10

No.	Defect #	Description
1	SAD00439923	Manual Error Insertion on Aux-Data Out in Dual-Channel Mode
2	SAD00439001	Self test always shows "Failed" with N4916B connected
3	SAD00435465	USB CP0 for SER Pattern are wrong.
4	SAD00434860	Aux Data - Output Blanking
5	SAD00434422	GUI crashes
6	SAD00430619	N4903B GUI crashes during remote programming

J-BERT N4903B software release 7.00:

Fully independent PRBS and patterns on AUX data output (second channel mode):

- Sequence extension to support two channels (with independent patterns but same sequence)
- Sequence editor supports second channel
- New type of pattern editor to support two bit streams
- De-emphasis mode: support of external connected power divider to add two bit streams
- Cross-talk simulation by generating a PRBS with independent starting phase
- Out-Of-Band (OOB) signaling: pattern of second channel controls the electrical state of DATA OUT

Other:

- Jitter tolerance characterization measurement: ability to enter MIN/MAX curves are not bonded to option J12 (automated jitter compliance suite) anymore
- Support of 14G version of de-emphasis signal converter N4916B (N4916B zip1.1.0.0)
- Manual input timing adjustment for 28 Gb/s multiplexer N4876A with stand-alone software (N4876A zip1.0.0.3)
- Added bit rate presets for Fibre Channel, 100GbE-LR4, UHS-II, MIPI M-PHY, DisplayPort
- Added demo patterns for MIPI M-PHY

Notes:

- Software license N4903B-002 is required to use the second data channel capabilities
- IVI-COM driver version 1.2.7.0 does not yet support all commands necessary to support the De-emphasis Signal Converter N4916B.
- IVI-COM driver version 1.2.7.0 does not yet support 8B/10B Symbol Comparison functionality.

Known defects in version 7.00

No.	Defect #	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings.
2	SAD00415423	SER != 0 or BER != 0 after a stop/start

Defects fixed in version 7.00

No.	Defect #	Description
1	SAD00425933	J-BERT N4903B operation with MUX: wrong jitter display in ps.
2	SAD00421925	Jitter Tolerance Remote Programming; (bug in the N4903B remote programming interface when performing a jitter tolerance measurement).
3	SAD00422222	Sequencer "Start" button does not appear.

J-BERT N4903B Software Release 6.80:

Support of 8B/10B Frame Error Ratio (FER), Symbol Counters, and Symbol Pattern Editing which includes:

Enhanced Pattern Editor capabilities:

- Patterns can be viewed and edited in symbol format. This functionality is provided by Bin/Hex/Symbol Configuration dialog.
- Running disparity and invalid symbols can be viewed and edited in pattern editor in Symbol format.
- The "Find Pattern" dialog is enhanced to search for symbol pattern.
- Pattern files can be viewed and saved in a new file format "symbol format".

The following new error ratios are available besides BER, SER and cBER:

- FER (Frame Error Ratio)
- FSR (Filler Symbol Ratio)
- DER (Disparity Error Ratio)
- ISR (Illegal Symbol Ratio)

The "Accumulated Results" window now displays additional results, such as:

- Calculated Bit/Error count
- Compared/Received/Error Symbol count
- Received/Error Frame count
- Filler Symbol count
- Illegal Disparity Change count
- Illegal Symbol count
- Expected Symbol count
- SER (Symbol Error Ratio)
- cBER (Calculated BER)
- FER (Frame Error Ratio)
- FSR (Filler Symbol Ratio)
- DER (Disparity Error Ratio)
- ISR (Illegal Symbol Ratio)
- Data Rate Ratio
- Auto Resync count

A new cBER setup dialog is introduced which provides the following options:

- To select cBER results based on SER, FER, FSR, DER, ISR.
- To select Automatic or User defined mode for cBER conversion factor.
- Auto align with CDR enabled now supported above 11.5 Gb/s. Does data centre with appropriate threshold settings. Message dialog will pop up.
- Wild card for filler primitives.

- Support for masking high error counts prior to re-synchronization of the error detector. This option is available in the Error Detector's Pattern Sync Setup dialog.
- Jitter characterization and compliance measurement: if DUT loses 8B/10B alignment, now also in BER mode it is tried to re-establish alignment when sequence supports it.

Better cursor accuracy of N4916B De-emphasis signal converter

- To improve cursor accuracy calibration of N4916B a calibration table is added. This is only usefull for N4916B's shipped after the release of J-BERT N4903B SW 6.8 or N4916B's that have been returned for factory recalibration.

Notes:

- Software license N4903B-A02 (or UA2) is required to use the 8B/10B SER capabilities
- IVI-COM driver version 1.2.7.0 does not yet support all commands necessary to support the De-emphasis Signal Converter N4916B.
- IVI-COM driver version 1.2.7.0 does not yet support 8B/10B Symbol Comparison functionality.

Known defects in version 6.80

No.	Defect #	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings
2	SAD00415423	SER != 0 or BER != 0 after a stop/start.
3	SAD00421925	N4903B Jitter Tolerance Remote Programming; (bug in the N4903B remote programming interface when performing a jitter tolerance measurement).
4	SAD00422222	Sequencer "Start" button does not appear.
5	SAD00425933	J-BERT with MUX: wrong jitter display in ps.

Defects fixed in version 6.80

No.	Defect #	Description
1	SAD00419580	Programming Guide: SCPI command must not contain spaces.
2	SAD00422787	User Guide: N4093B User's Guide do not provide directions which applies for the N4916B to connect the Pattern Generator and DUT.
3	SAD00415322	GUI crash on opening the instrument state after running the jitter tolerance measurement.
4	SAD00422503	Auto align in CDR Mode modifies "Fine Adjust" value but does not display the change.
5	na	N5990A test automation software issue in which an error message "Specified type of lock could not be obtained" was launched.
6	na	N4916B De-Emphasis improvement: calibration table for improved cursor accuracy by droop compensation

J-BERT N4903B Software Release 6.70:

Multiplexer Control, Second Output Channel (Option 002)

- The N4903B supports the Agilent N4876A 28 Gb/s Multiplexer 2:1. All Multiplexer output parameters can be controlled via J-BERT UI. J-BERT's AUX output provides pattern and PRBS to drive the multiplexer.

  This allows expanding the pattern generator bit rate of J-BERT up to 28.4 Gb/s and of ParBERT up to 27 Gb/s. N4876A offers excellent output signal performance for accurate characterization up to 28 Gb/s. For more information to setup the N4876A see START - N4900 Series Documents - N4876A Getting Started.

- License for Opt. 002 "PRBS and pattern on AUX data" is required for using N4876A

Faster automated jitter characterization

- Reduce the number of measurements points with the ability to enter jitter start values under Jitter Characterization-Properties-Search

Notes:

- Power Cycle of N4876A is mandatory after updating its software.

Version 6.60:

Symbol Error Ratio Analysis (Option A02)

- Integrated receiver tolerance testing capability for USB3, SATA, SAS, MIPI M-Phy by analyzing coded, packetized data and filters filler symbols;
- Presets for filler and align symbols for USB3, SATA, MIPI,
- Filtering of up to four user-definable filler symbols,
- Filtering of consecutive occurrences up to 12.5 Gb/s without dead time;
- Display of calculated bit error or symbol error ratio in real-time;
- Ability to enter and monitor sent and received patterns in 8B/10B coded or uncoded bit or symbol format;
- Handles running disparity automatically,
- Supports Block Masking in SER mode.

Sequences / Patterns

- A sequence now can consist of up to 120 blocks. It depends on the number and the kind of loops used.
- Updated USB3/SATA loopback sequence/patterns.

Notes:

- IVI-COM driver version 1.2.7.0 does not yet support all commands necessary to support the De-emphasis Signal Converter N4916B.
- IVI-COM driver version 1.2.7.0 does not yet support SER functionality.

Known defects in version 6.50 and 6.60

S. No.	Parameter	Description
1	SAD00397466	"Preset Instrument State" button does not reset the various Jitter Tolerance settings

Defects fixed in version 6.60

. No.	Parameter	Description
1	SAD00412975	Programming Guide: SOURce8:CONFigure:DISTribution OFF does not work
2	SAD00412976	Programming Guide: SOURce8:CONFigure:DISTribution OFF Resolved
3	SAD00412977	Programming Guide: SOURce2:DIVider8
4	SAD00412756	N4916B remote control sometimes doesn't update post

Version 6.51:

- Optimize hardware driver for option D14

Version 6.50:

- The N4903B supports the De-emphasis Signal Converter N4916B. Accurately characterize your multi-gigabit serial interface with the 4-tap de-emphasis signal converter with optional clock multiplier. For more information see START→ N4900 Series Documents → N4916B ReadMe.
- Trigger pulses at AUX IN input are detected down to a pulse width of 5 ns typ. when used as sequence trigger

Defects fixed in version 6.50

- SAD00397013 eye-diagram measurement fails to autoscale correctly
- SAD00397463 eye-diagram measurement fails to autoscale correctly
- SAD00408298 Delay Control Input can't be enabled without option J10 installed
- SAD00395370 Support for PRBS2^9

Version 6.10:

- The GUI mainframe design has been changed to improve usability of the instrument.
  - The list bar on the left hand side of the GUI has been replaced by a menu, which is opened by pressing the menu button in the upper left corner.
  - The complete Pattern Generator and Error Detector status information is displayed at the bottom of the GUI.
- The Spread Spectrum Clocking has been enhanced:
  - SSC and SJ can now be activated and used simultaneously
  - In addition to downspread, also up- and centerspread are available now
  - Non-triangular SSC-profile has been added, which can be specified using a simple text-file
  - The SSC deviation reset value changed from **BOTH** to **DATA.**
- The Jitter Tolerance Measurement has been adapted to the new jitter capabilities
  - The Jitter Tolerance Measurements no longer automatically activates PJ-1 and SJ.
  - The user must setup all jitter parameters on the jitter setup page before starting the test
  - The Firmware performs a plausibility check on the jitter setup before starting the measurement

New key capabilities of J-BERT N4903B (initial release):

- Supports testing of forwarded clock devices:
  - Half-rate clock with variable duty-cycle
  - Jitter on clock and data
  - Delay of jitter between clock and data
- PCIe 2.0 compliant jitter injection:
  - LF-RJ and HF-RJ
  - Dual-tone PJ
  - Residual SSC
  - Electrical idle
- Variable output levels on trigger and aux data outputs
- Wider PJ range of up to 300MHz
- Built-in tunable CDR is always included
- Pattern sequencer with up to 60 blocks

Operating and Programming Hints

- The following must be taken into account for all differential outputs of the PG and differential inputs of the ED: if only the normal or complement port is used in your test setup, the unused output ports **must be terminated with 50Ω**.
- The N4900 Series Family comprises of several products, which require different application software. If a software update is required, please make sure your device is updated with the correct software version released for your instrument. Installing software intended for a different device may result in unpredictable issues, and may even permanently damage it. Agilent does not cover such damages under warranty.

- If a new Microsoft Windows user login is created, the user must have administrator privileges to run the instrument firmware. Otherwise the firmware cannot access the instrument hardware.

- In order to access the instrument from another computer, e.g. by a remote program, the *Windows Firewall* must be configured to allow remote access to the Agilent Firmware Server (due to security considerations, this access is disabled by default). To allow remote access to the firmware server, use the *Windows Firewall* applet from *Control Panel*: in the *Exceptions* tab, click on the *Add program* button, and browse for *C:\Program Files\Agilent\N4903A\FirmwareServer\n490xfw.exe*. To minimize risk, we recommend enabling access just from your subnet (use the *Change scope* button, from the same dialog box). Please note that some dialog boxes are taller than the height of the screen of the instrument, and the Ok and Cancel buttons might not be visible. You can move the dialogs upper on the screen, by dragging their title bar (using a mouse makes this much easier; simply plug an USB mouse in the front panel of the instrument).

- Alternate Pattern Trigger Level requires minimum pattern length:
  When the trigger is configured to be level sensitive (i.e. high for Pattern B) there is a latency from start of pattern B until the trigger goes high. To see the trigger going high, a minimum pattern length of 1024 bits is required.

- Performing Jitter Tolerance Measurements
  The automated jitter tolerance measurements makes use of both, SJ and PJ, to sweep the modulation frequency of the jitter. Which one is used is selected automatically depending on the required jitter amplitude, its frequency and the capability of the jitter source.
  To avoid unnecessary restarts of the pattern generator and to provide continuous data and clock to the device under test during a Jitter Tolerance Measurement, the following workflow is recommended:

  1. Turn off Spread Spectrum Clocking (SSC) and residual Spread Spectrum Clocking (rSSC)
  2. Set all jitter sources (RJ, PJ1/2, SJ and BUJ) to 0mUI
  3. Turn on global jitter switch
  4. Setup and turn on RJ, PJ2 and BUJ, if required
  5. Turn on PJ
  6. Turn on SJ
  7. Restart pattern sequence (if required to synchronize DUT)
  8. Perform an auto alignment to adjust the sampling point of the error detector
  9. Start the measurement

- If the N4916A is connected via USB to a N4903B instrument, while the N4916A is powered off, it is possible that the N4916A is not recognized by Windows as a valid USB device, not even after switching it on. If this happens, remove and reinsert the USB cable **without powering off the N4916A**. If this still doesn't solve the problem, restart N4903A without powering off the N4916A.

Output protection when operating into open or wrongly adjusted external termination voltage

The generator module offers a huge flexibility for external termination schemes and external termination voltage levels to address common technologies. For details, please refer to the Technical Data Sheet.

An internal protection circuit continuously monitors the voltage levels of clock, data, aux data and trigger output. It becomes active if the termination voltage is wrongly adjusted. The output protection circuit may become active if the output voltage Vout becomes higher than Vhi+0.5V or lower than Vlo-0.5V.

The output protection circuit is shared among two output drivers each. Data Out and Clock Out as well as Aux Data Out and Trigger/Ref Clock Out are supervised by one circuit together. As a consequence, if an output voltage violation occurs, both outputs are disabled together for a short period of time.

If an output voltage violation occurs, the output voltages Vhi, Vlo and Vterm are re-programmed to safe values, typically to the externally measured termination voltage:

Vhi = Vlo = Vterm = externally measured termination voltage.

Afterwards the output drivers are reenabled.

How to avoid an open condition in an automated test environment like IC or wafer test?

The monitoring of an open condition is based on 100ms intervals. Earliest detection of missing termination is 200ms after setting the output levels. Earliest detection of correct termination will be 100ms after detecting unterminated operation. To optimize the test throughput by avoiding the protection circuit to become active, it is recommended to perform the DUT change in the following manner:

1. End of previous test. DUT is ready to be exchanged.
2. Adjust a High Level, which is less than 1V above Vterm. This will avoid the protection circuit to be activated. If Vterm is above 1.5V, the levels do not have to be changed.
3. Remove the tested DUT.
4. Insert next DUT.
5. Adjust new user levels.
6. Start test of next DUT.