



*A Whitepaper:*

# Using Boundary Scan to Link Design and Manufacturing Test

By

Raymond J. Balzer  
Agilent Technologies  
Loveland, CO, USA  
[Ray\\_Balzer@agilent.com](mailto:Ray_Balzer@agilent.com)

and

Adam W. Ley  
ASSET InterTech, Inc.  
Richardson, TX, USA  
[aley@asset-intertech.com](mailto:aley@asset-intertech.com)

## **Executive Summary**

In recent years, many in the electronic test industry have begun to realize that the value of boundary-scan test technology can be leveraged across the various phases in a product's life cycle. In particular, boundary-scan can provide a link between design test with manufacturing test, producing long-term benefits in terms of greater efficiencies and higher quality products. Such a link between design and manufacturing test will enable the benefits of standardizing and re-using design verification tests and PLD programming algorithms in manufacturing.

Of course, certain steps must be taken to allow for this linking. This paper will discuss the hardware and software infrastructure needed to achieve efficient test portability. In addition, design-for-test (DFT) guidelines and recommendations that improve the linkages among product design, prototype verification and high-volume manufacturing test will be highlighted. And, to demonstrate how some of these concepts can be applied, several case studies demonstrating effective boundary-scan test strategies will be described.

## **Introduction**

In some industries, boundary scan is used extensively as a means for testing printed circuit boards (PCB) and assemblies. Boundary scan provides many advantages for achieving high quality products and reducing time to market. Because of its simple interfacing requirements, several benchtop boundary scan tools have been developed and these are commonly used by board and system designers.

There are many benefits to re-using tests from design and prototype testing in production and field repair. Faster time to market, lower test costs and higher quality are just some of the critical benefits.

Some might argue that the portability of the benchtop environment allows it to be directly, physically ported to manufacturing test. For example, this could be attempted by simply placing the benchtop tools alongside a production in-circuit test (ICT) system. While this can certainly work in some instances, it will mostly fail. There are simply too many benefits from a higher level of hardware and software integration.

In order to achieve the benefits of re-using tests, integrated circuits (ICs), boards, and systems must be designed correctly to support boundary scan. In addition, there are a number of best practices that have been identified to aid the transition from design and prototype testing into production.

In addition, some results from several cases will be presented in this paper to indicate how well the theory can be put into practice.

## **Why Boundary Scan?**

A number of factors have contributed to the recent explosion in the implementation of boundary scan (IEEE Std 1149.1) for PCB assembly test and on-board programming. Clearly, one factor is the ubiquitous availability and deployment of FPGAs, CPLDs, ASICs, and other "off-the-shelf" boundary-scan devices. As more boundary-scan-enabled devices are placed on PCBs, test departments are more likely to use the built-in scan technology.

Driving the adoption of scan-based test even further are the dramatic changes in the board-test environment itself, such as higher package densities, smaller traces, high-frequency-interconnect requirements, and the resulting loss of traditional node access. ASICs and VLSI digital-device complexity make coverage from traditional digital in-circuit test much more difficult and costly. Board node count is also rising in many environments and is breaking the limits for ICT and ICT fixturing, as well as the limits for prototype-test techniques, such as flying-probe testers.

Boundary scan provides an ideal combination of ease of test generation, potentially high fault coverage, effective diagnostics, and simple interfacing. Such a combination has spurred the adoption of boundary scan by original equipment manufacturers (OEM) and electronic manufacturing services (EMS) firms that value high quality products, fast time to market, and lower product development and production test costs.

Firms have discovered that with the availability of benchtop boundary-scan tools, product design, debug, and prototype turn-on are all much faster and easier if the boards are designed with boundary scan.

Other benefits to both design and production are that boundary scan is extensible and can also be used in scales ranging from Multi-Chip Modules (MCMs) and daughterboards up to card-cage and system level. And not only

does boundary scan provide testing at any of these levels, it also can program Flash memory and other in-system programmable devices that are devices accessible by boundary scan.

In this new environment, stand-alone boundary-scan tools for PCB design and prototype verification has become extremely common. Now, many test engineers and technicians would like to link more effectively the early phases of prototype test and programming to the manufacturing test processes.

### **Leveraging the Test Advantages of Boundary Scan**

While boundary scan offers significant test-development automation, the fact remains that test engineering is still required to achieve desirable levels of test coverage and reliability. Once this engineering has been completed, it is not efficient to repeat it for manufacturing test. Further, if the board/system designer does the initial test development, then there is no confusion about how the board works or how it should properly operate during test. The test department can leverage the designer's insight if the designer's tests can be re-used. This is how high-quality tests are leveraged. High-quality tests lead to high-quality manufactured products.

Once the design team's efforts can be leveraged into production, the importance of effectively implementing boundary scan will be even more apparent. This leads management to exert added pressure for more pervasive and better utilization of boundary scan on succeeding projects.

More pervasive and more effective utilization of boundary scan will facilitate reducing ICT test-pad access on PCBs. This simplifies and speeds up board layout. For ICT, reduced physical access means fewer fixture probes and wires; thus, fixtures are cheaper and perhaps they can be delivered a few days sooner. At the same time, the effective utilization of boundary scan means that high test coverage is maintained.

Leveraging boundary scan tests from design into manufacturing reduces the time spent developing tests for production at ICT, for example. By reducing total test development, the ICT department should be able to produce a working program and fixture with targeted fault coverage in a shorter period of time. And ICT development is usually in the critical path for a product's release. Thus, any reduction in effort for ICT development leads directly to improved time to market (TTM). In many markets, the suppliers with the shortest TTM are able to gain critical market share and maximize profits.

A shared set of tests improves the control and management of the test suite as well as the actual quality of the tests themselves. Different departments can leverage the work of others and, in turn, make improvements that are subsequently shared with other departments. For example, production ICT might refine tests to gain additional test coverage or diagnostic resolution for commonly occurring faults. Not only can this be shared with a final test or field test/repair station, but also it can usefully be shared with the company's design group.

Most designs go through several revisions. With cross-departmental sharing of tests, the design team can take advantage of the improved suite of tests developed by production. Design can benefit from the improved fault coverage and diagnostics resolution developed by the production department when a new design is in debug or during prototype turn-on. Again, the net benefits are less time spent development tests, lower costs, and faster TTM.

ICT and functional repair stations also benefit from a common suite of tests. For boards with intense usage of boundary scan, many high-volume production sites have installed benchtop boundary-scan test on their ICT systems and functional repair stations. Typically, these benchtop tests are completely different from the tests at ICT. Not only that, the fault coverage and even the test results were often different. This caused much confusion and finger pointing. By being able to run a common set of tests, these problems are eliminated.

Other production sites may realize the value from benchtop test at ICT repair because of the matching of test results and leveraged test development. For "dog boards", the benchtop test environment can offer many tools for advanced diagnosis. Single stepping of tests is one such tool. Single stepping with technician diagnosis is not practical or economical at ICT. But with leveraged tests, it is easy to implement such techniques off line.

Many have been tempted to set up a new production test/programming station in the production line using a benchtop system. The argument is that the benchtop system has a lower operating cost than an expensive ICT system or a functional test station. In addition, a boundary-scan benchtop test station and can offer significant test coverage and also be used for Flash and/or in-system programming (ISP), both of which can be time consuming .

These advantages often are more than offset by cost increases from additional handling, which increases direct costs, floor space, and increased damage from the increased handling.

By leveraging the tests and programming from the benchtop systems cleanly at ICT, the benefits that ICT brings to production can be shared with the boundary-scan test and programming suite. ICT brings many features required for robust production usage. This includes the ability to support automation in many dimensions.

First, benchtop boundary-scan testing usually requires that a technician attach a ribbon cable connector to a test header on the board-under-test. The ribbon cable and connector and operator intervention are all problematic for high-volume production and unskilled operators. In addition, some production lines are truly automated. Traditional ICT has a longer history of providing test automation.

Some other features that ICT brings are common failure-reporting mechanisms and data logging and interconnection with management data systems. When benchtop tests are properly integrated with ICT, benchtop test can share the same reporting systems with ICT. In addition, the combined system would produce a combined fault-coverage report. This allows easy insight into production test coverage.

Leveraged tests can be shared among the following test/repair stages:

- Design verification
- Prototype test
- Environmental test
- ICT
- ICT repair
- Functional test and repair
- Field re-programming and repair

#### **Features Needed to Effectively Leverage Boundary-Scan Tests in Production**

First, the requirements for production will be described, then the requirements for production test engineering. Then the actual hardware and software features to support these requirements will be described.

##### *Production Requirements*

- High throughput
- High, known fault coverage
- Precise, automated diagnostics
- Minimal operator intervention
- Support of conveyor automation
- Automated support of multi-TAP boards
- Test stability and portability
- Support for panelized boards
- High system reliability and uptime
- System self-test and self-diagnosis

In addition, some practical requirements are considered, such as the need for compatibility with existing ICT configurations so that the company's investments in fixtures/programs and test systems is not rendered obsolete. Also, the on-going value of ICT cannot be compromised. That is, shorts and opens testing, and other ICT features must not be degraded.

##### *Test Engineering Requirements*

- Fast, easy integration into the existing processes
- Robust solution
- Easily supported Engineering Changes to the board-under-test (BUT)
- Effective support for transferring improved tests back to design
- Fault coverage reports
- Effectively support multiple versions of the board
- Work with multiple logic families on the same board
- Support all tests with all I/O configurations used by design on the benchtop
- Have an ability to use quasi-static digital lines to condition the board and its ICs for testing

- Allow test improvement and debug while an ICT fixture is being produced

The hardware and software features that address these requirements are discussed below.

*Hardware Features*

High-speed boundary-scan test requires a high-speed PCI interface in the host PC controller to support high data rates, high test clock (TCK) rates up to 50 MHz, and high throughput. The design, using just a single interface pod, supports four boundary-scan TAP channels. This supports both multiple TAPs on a board and panel testing of as many as four board panels. The design is extensible to an additional pod per PCI card and multiple PCI cards.

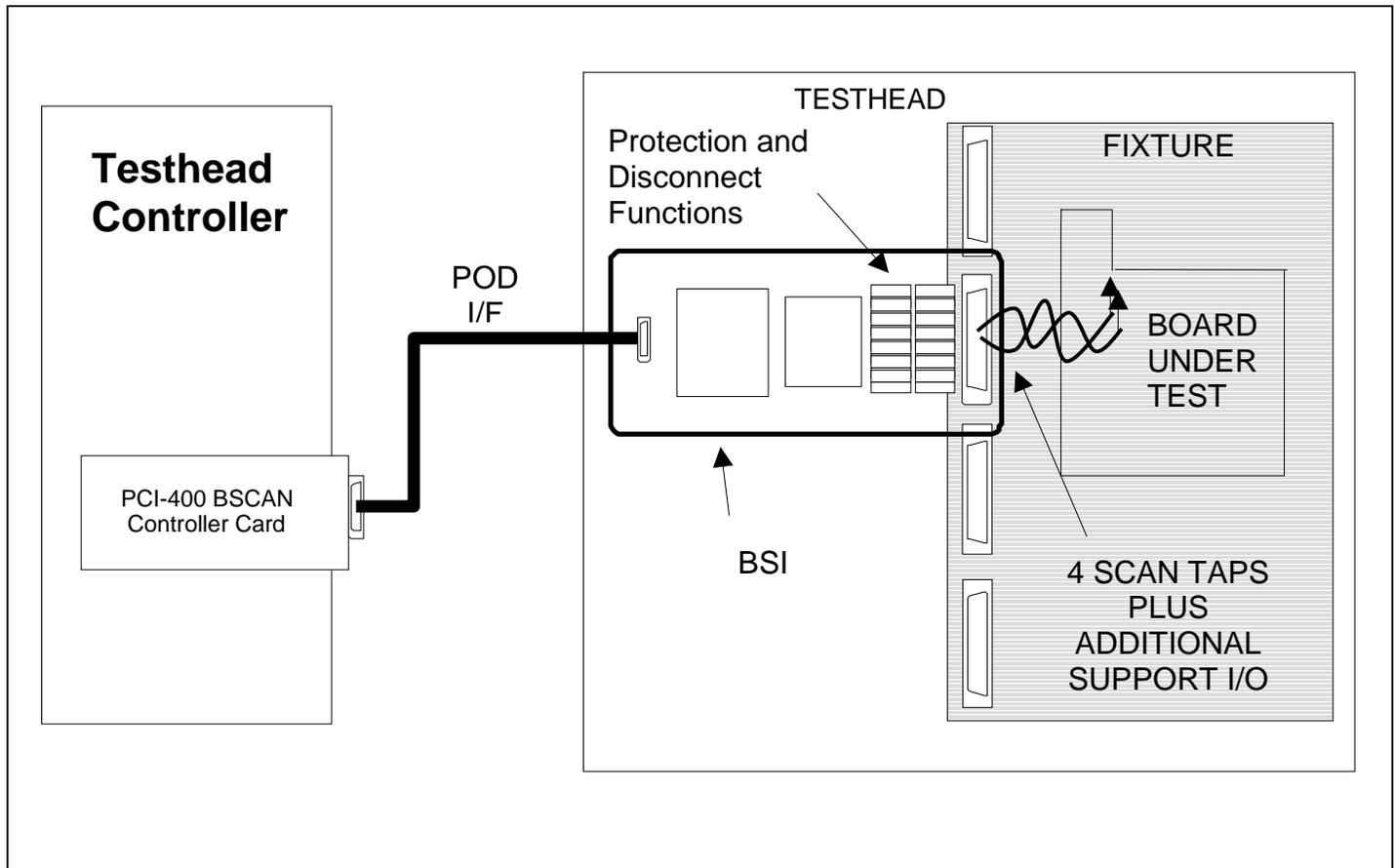
The interface between the PCI card and pod uses differential signals to allow reliable operation up to 12 feet. This allows for good cabling flexibility.

The pod itself is a modified version of the pod used in the benchtop boundary-scan system. It is augmented and optimized for use in the ICT system while retaining compatibility and interoperability of tests in either environment.

The pod in the tester is called a Boundary-Scan Interface card (BSI). The BSI is packaged much differently than a conventional benchtop pod. The BSI is designed for insertion into the ICT system and is shrouded by the ICT's sheet metal enclosure. As a result, no housing is needed.

The BSI uses a completely different interface to the BUT. Whereas the traditional pod is manually connected to a TAP header with a ribbon cable, the BSI has a 100-pin connector with spring-loaded probes to interface automatically with the ICT fixture. The BSI has the electrical contact reliability of locking a fixture to the testhead.

This manner of integration means that conveyor operation is fully supported. It also means that physical access to the BUT to connect to the TAP header is not required. This is quite important, since most modern ICT board tests require gated fixtures do not provide access to the top side of the BUT.



**Figure 1 -- Hardware Configuration**

The BSI, unlike the pod, contains electrical-disconnect relays that allow immediate and complete isolation of the BSI electronics, including ground, from the BUT. Opto-isolation electronics are used to control the disconnect relays. These methods are essential for supporting ICT's electrical isolation requirements for unpowered test modes, such as the testing of shorts and opens.

Taking steps to ensure signal integrity is quite important for TCK rates to 50 MHz in an ICT-fixture environment. The BSI, as well as the pod, are designed with termination options. Direct drive is effective for nodes with low-impedance input termination. Otherwise, the backmatch mode uses series termination to match the expected wiring impedance. The ICT fixture from the BSI will use twisted-pair wires, rather than ribbon cable typically used with a pod. In addition, the twisted-pair wires in the ICT fixture will typically be much longer than the ribbon-cable length connecting the benchtop pod to the TAP header. The BSI uses slightly different series terminations to adjust to these subtle electrical differences.

So that reliable testing at 50 MHz can be achieved, the BSI uses retiming compensation to account for buffer and wire length delays. Still, the particular implementation of retiming also supports testing at any available frequency setting down to a low of 160 kHz.

Each TAP can be for the common logic families from 1.8-volt through 5-volt logic. This can be programmed for each BUT. Further, each TAP can be programmed differently. Thus, multiple TAPs with differing logic levels are supported. In total, the BSI has 12 independently programmable voltage regulators. This supports the four TAPs, four sets of four digital I/Os, and four additional digital I/Os.

The digital I/Os (DIOs) are designed to support quasi-static digital setup and are bidirectional. One DIO per TAP is further optimized to support high-speed write-enable signals to accelerate Flash programming. Another DIO per TAP is optimized to support Ready/Busy signals from Flash. These DIO lines map precisely the functionality of the benchtop pod.

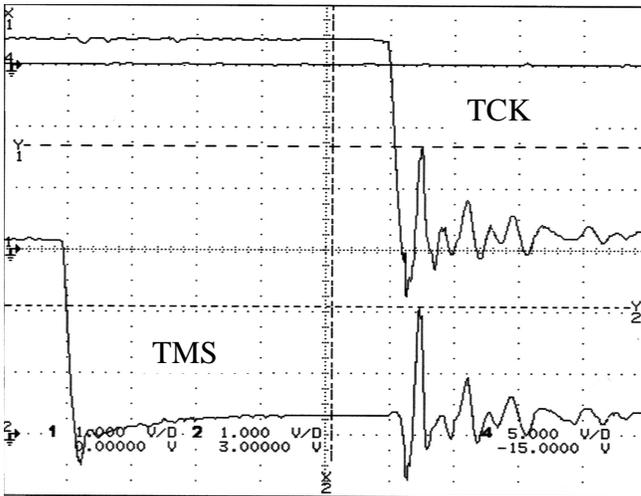
Software can place all I/O pins in a three-state condition to both protect the BSI electronics and allow powered ICT to proceed without interference. Protection and isolation can also be achieved by configuring relay control over the BSI disconnect relays and disconnecting the BSI during the powered ICT tests.

In order to support reliable testing at frequencies up to 50 MHz, certain practices should be followed. The user should use twisted-pair wiring for all the TAP signals and optimize the board placement on the fixture to minimize the TAP wire length from the BSI to the probe locations.

TCK requires even more care. In order to preserve the ICT features of unpowered and powered tests using the TCK node, it must be double wired to an ICT pin card. This creates a stub that will cause reflections and the possibility of an unintended double clock edge. While no such cases have been observed in practice, it is recommended that a disconnect relay be implemented in the fixture to keep stub length below two inches when the BSI is used for boundary-scan testing.

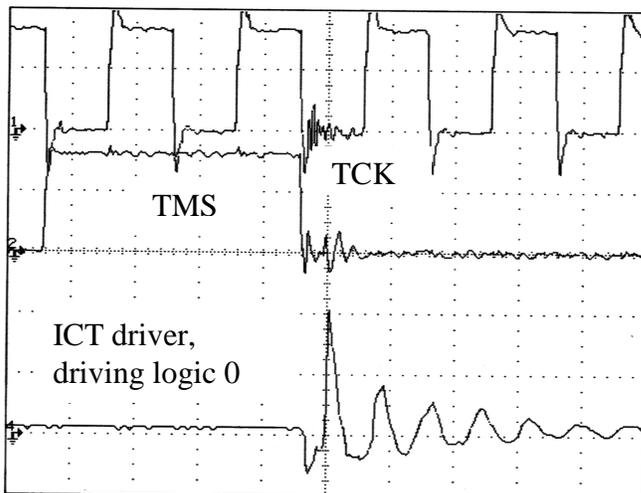
The BSI also has multiple provisions for self testing and diagnosis. The connection from the PCI card to the BSI can be tested. BSI functionality can be tested with loop-back features supported by the on-board ASIC and surrounding circuitry. Finally, an external fixture provides signal loop back to test signal and ground continuity and operation through the 100-pin connector.

Failures induced by ground bounce and instability have plagued traditional boundary-scan testing on ICT systems. The loading of bed-of-nails fixtures with a large number of simultaneously switching nodes can create transient currents summed on the ground wiring between the BUT and the test system. Ground wiring inductance combined with a large transient voltage could also lead to a transient voltage on ground. This is then reflected in the signal lines as a glitch with respect to ground. See Figure 2 for an example. These voltage levels are sufficient to cause undesired state changes and test failures.



**Figure 2 – Ground bounce with traditional ICT**

The BSI takes its TAP ground reference from the BUT ground, not the ICT ground. This is a critical difference during transitions that induce large current transients in the ground path between the ICT system and the BUT. There is little loading between the BSI and the BUT; thus, current flow and any ground voltage transients are minimized.



**Figure 3 – TAP from BSI displays immunity to ICT loading and bounce**

Figure 3 illustrates a dramatic improvement. To start with, an unacceptable level of ground-bounce was created. A four-volt transient is created between the ICT system and the BUT, yet the BSI signals, TCK and TMS, show remarkably little noise. The test ran without failure at a high TCK rate for hundreds of thousands of test iterations. One can conclude that this new test-electronics interface will have far better test stability because of its ground-bounce immunity.

Another benefit of using the BSI approach instead of an ICT pin card is that the BSI hardware interface has no impact on the conventional ICT pin-card configuration. Thus an ICT system can be upgraded to support leveraged tests without affecting the firm's investment in existing test systems, fixtures, and programs.

#### *Software Features*

The software has been optimized on both the benchtop system and the ICT system to facilitate easy and automatic porting, and efficient integration of the tests.

On the benchtop side, a number of optional settings and some implementation constraints at the benchtop are required for effective use in production. Thus, a new feature was added that checks the project for compatibility with porting to an ICT system.

One simple constraint requires that the benchtop project must target board-level test and not card-cage or system testing. Checks are done both on the benchtop and at ICT.

In production and depending upon the mix, a variety of test fixtures may cycle onto the ICT system. It is vital that the project contains all the information for configuring the hardware, such as the TCK rate, terminations, voltages, and other factors. These settings are often just tweaked at the base hardware level at the benchtop. This would not be satisfactory for manufacturing and so project-level settings are enforced.

For the physical interface, the benchtop user must have a customized cable for the TAP header. The software does not need to understand the low-level details, just the chain. However, to support ICT's automatic generation of fixture-wiring files, explicit mapping of signals to nets must be provided.

In order to run the benchtop tests transparently to the ICT operator, the benchtop GUI cannot intrude. As a result, a customized application programming interface (API) was implemented.

At ICT, the existing test-development process was extended so that the benchtop project could be imported as seamlessly as possible. A simple construct was added in the test configuration file to specify the presence, location, and usage of the BSI. With this, the software knows whether to look for a project and operate on it or not. The test engineer just needs to drop the project file into a new, dedicated directory associated with the BUT, specify the desired probe locations for the TAP resources, and the rest of the test generation process is automatic. The software automatically imports and reads the project files, does many error checks and outputs a complete set of files, tests, test sequences, and fixture-wiring information. The error checks include enforcing a maximum of three inches separation of the ground termination of the twisted pair from the signal probe. This ensures consistent impedance, clean signals and stable tests.

Another aspect of the test-development coordination between the two systems is the name cross-reference feature. For various reasons, net, device, and pin names can be slightly altered from the original CAD data when this data is imported into either the ICT or the boundary-scan benchtop test systems. Rather than requiring identical names for the two systems, a name cross-reference system was established. Thus, the leveraged tests are able to run with original data, including names, and produce normal failure reports. However, the ICT system software translates these names to those used in the ICT environment. Thus, one consistent representation of the board is presented to the ICT system, repair operators, and the data logging and management information systems.

The ICT debug GUI was augmented to support running the leveraged tests for evaluation, as well as allowing the benchtop GUI to be used for advanced debug or just to simply modify or enhance existing tests.

At run time, the software executes new, native test-executive commands targeting the BSI and associated test hardware:

```
test scanworks "mybrd.chain1.interconnect"
```

This automatically invokes the various API calls necessary for test execution and retrieval of test results with any diagnostics. All system flags (e.g. boardfailed) are automatically set as if they were native tests. Similarly, data logging is fully integrated.

The test sequence was automatically generated to run the tests in a logical, progressive sequence. This resulted in the leveraged tests being interleaved with the traditional powered ICT tests. The automatically generated sequence enforces some electrical isolation and protection of the two sets of test hardware. In particular, the BSI is programmed to a three-state condition while conventional ICT is running. Further, the programmer is encouraged to open the BSI relays, as well.

Yet, the software was also designed to allow concurrent operation of the ICT system's digital and powered analog subsystems with the BSI. The programmer merely removes or comments some of the code that does the isolation of the two systems and runs consecutive commands that initiate the ICT subsystems and then execute the BSI. So the ICT programmer gets automatic isolation and protection, yet an easy ability to override this and implement more complex, coordinated-resource tests.

The software supports the various levels of hardware self testing, both at runtime and as part of system self tests, using loop-back connectors in the augmented diagnostics fixture.

## **DFT Guidelines**

For the concept of boundary-scan test re-use to work, several guidelines are recommended. First, boundary scan must be successfully implemented on the board. Second, the benchtop tests should be optimized before they are re-used in production.

Obviously, this strategy suggests a thorough and ongoing adoption of boundary-scan ICs on PCBs. Ideally, the ICs have been verified as compliant to IEEE Std 1149.1 and the BSDL files that describe the parts have been verified both as having standards-compliant syntax and matching the functionality of the parts they describe. These points are very critical to project success.

At the board design level, the number of boundary-scan chains should be minimized. Fewer and longer chains provide far higher test coverage and simplify test fixturing. The TAP signals should be interconnected "normally" as indicated in the IEEE Std 1149.1 specification. Any TRST pins should be tied together to a common node and pulled high. The TCK line should be laid out as if it were a high-speed clock signal, which it is. All of the TAP signals should be brought to a test header or connector that follows a standardized layout and has matching grounds for each signal pin.

At the benchtop, tests should be developed targeting individual boards, not just systems. All resource definition for ICT compatibility checks should be done. Of course, the developed tests should maximize fault coverage while providing good diagnostics resolution. The tests must be stable and reliable. Flash and ISP programming should be implemented to complete the suite.

To further aid production, name tests meaningfully, such as "U15\_memory" rather than "Memory\_test1". Also, it is better to create several simpler actions than one large one where production might need finer control. For example, when programming a PLD, rather than developing one programming action that includes blank checking, programming, and verifying together, make separate actions for each separate task. That gives the ICT engineer the ability to easily optimize task sequences, depending on the needs of the test environment. For example, production may re-test boards with chips already programmed and may not want to spend time erasing and re-programming them.

## **Case Studies**

A small simple 140-node demo board is routinely used in training classes for test-development exercises. The benchtop export process only takes about 20 minutes. The ICT total test-development-process lab takes about 70 minutes, with an additional 10 to 15 minutes of incremental work for the leveraged tests. The test plan needs several minutes to add four lines of code for relay control for isolation and TCK-stub optimization at the start and end of BSI tests. The fixture vendor had some difficulty understanding how to wire the extra six twisted-pair wires, but, once completed, the tests ran with no debug. This was a simple, single-stage, un-gated vacuum fixture. The tests were stable up to 44 MHz using direct-drive mode.

A major Contract Manufacturer did a trial for evaluation purposes. The selected board had about 850 nodes, with four boundary-scan devices in one chain and four adjacent memory devices, flash memory and an ISP device (one of the scan devices).

Benchtop export for ICT took approximately 30 minutes. The ICT test development required several hours, while adding the benchtop tests took less than 30 minutes. The benchtop tests included a chain integrity test, a chain interconnect test, four memory interconnect tests, a flash programming action via boundary scan, and one ISP programming action.

By inspection, it was readily noted that the BSI wires had been done improperly by the fixture vendor, who subsequently fixed these eight twisted pairs. The fixture was a single-stage, gated vacuum fixture and used a TCK disconnect relay to optimize the stub.

The tests ran immediately at ICT. However, during the course of several hours testing and experimenting, some intermittencies (false failures) were observed and debugged. Total debug effort was less than 30 minutes during that time. All that was needed was a small reduction in test frequency (from 16 MHz to 14 MHz) and the addition of a small settling delay at the start of BSI tests. 42 production boards were successfully tested without mishap. The ISP and flash programming were verified at a system self-test station. A known-good board was cycled 100 times, running the leveraged tests without a single false failure. Selected failures were inserted and all were found and correctly diagnosed and the diagnoses were reported to the standard ICT ticket printer. The evaluating engineer

estimated that using leveraged tests would save 25 percent on the total costs for ICT development, debug, and fixturing.

### **Summary**

Boundary-scan tests have a unique set of qualities that make them usable across a wide range of test and programming locations. The high coverage combined with the simple fixturing interface led to the development of benchtop boundary-scan testers. Once these were used for design verification and prototype testing, it became apparent that leveraging these tests in all manufacturing, field test and programming stations made economic sense.

The advantages associated with leveraging these tests in manufacturing are many and varied. However, a few are especially notable, including lower costs, faster time-to-market (with associated increased profits), and higher quality.

Many hardware and software features were implemented to satisfy the many needs of production and production test engineering. This provides significantly more value than by simply placing two independent testers adjacent to one another.

For efficient operations, boundary scan should be designed into printed circuit boards. Benchtop test development should follow a few guidelines to optimize for test re-use in production.

This is more than theory. Several boards have been done as trials. The tests do port to the ICT fixture and run. The integration is thorough and clean, thus little time is spent adding them in. The diagnostics are accurate and follow the ICT paradigm. One manufacturer of PCB assemblies estimates that using leveraged tests would save 25 percent on the total cost of ICT.