USB 3.0: Facing the Challenges of SuperSpeed USB Product Development

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Presentation Goals

• Help you understand market need for USB 3.0

• Provide progress update and schedule of development activities

• Provide high level overview of USB 3.0 architecture

• Compare and contrast to USB 2.0: what has changed and what is the same

• Disclaimer: The material and content that describes specific details of the USB 3.0 specification belongs to the USB 3.0 Promoters. Agilent is not speaking or presenting on behalf of the USB 3.0 Promoters.
Agenda

USB Market Overview
Physical Layer Overview
Cable/Connector challenges
Hubs
Frequently Asked Questions
Summary
Background

Hi-Speed USB (480 Mbps) is now inadequate for many products
Emerging applications will benefit from higher performance
* USB 1.0 – 1996, USB 2.0 - 2000

Most other aspects of SuperSpeed USB will remain the same:
• Backward compatibility with USB 2.0
• Maintain the extensive device driver infrastructure
• Preserve USB ease of use expectations for Users
In 2008 HS products exceeded FS/LS for the first time
SS products will start at 0.5% in 2009 growing to >10% by 2012

The USB Market is HUGE and growing

Source: In-Stat, 3/08
USB 2.0 is now a performance bottleneck

High speed USB 2.0 = 480 Mbps signaling rate
- Real throughput is typically much less at around ½ this data rate (< 240Mbps)
- Additional limitations due to IO performance limitations
  - Approximately 35 MB/s maximum usable application data rate

Something faster is needed for large digital multi-media files

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<th>Song / Pic</th>
<th>256 Flash</th>
<th>USB Flash</th>
<th>SD-Movie</th>
<th>USB Flash</th>
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<td>5.7 min</td>
<td>22 min</td>
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<td>3.3 sec</td>
<td>20 sec</td>
<td>53.3 sec</td>
<td>70 sec</td>
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SuperSpeed USB Applications

Solid State/Flash Storage Market in 2010
USB 3.0 Promoter Group Announcement

INDUSTRY LEADERS DEVELOPING SUPERSPEED USB INTERCONNECT

Popular USB Computer Connection Technology Expands to 5 Gigabits per second with Proposed USB 3.0 Specification

INTEL DEVELOPER FORUM, San Francisco, Sept. 18, 2007 – Intel Corporation together with HP, NEC Corporation, NXP Semiconductors and Texas Instruments Incorporated have formed the USB 3.0 Promoter Group to create a SuperSpeed USB personal interconnect that can deliver 5 Gbps speed – ten times the speed of today’s connection. The technology will target fast sync-and-go transfer applications in the PC, consumer, and mobile segments that are necessary as digital media becomes ubiquitous and file sizes increase up to and beyond 25 Giga-Bytes.

- 5 Gbps data rate
- Fast Sync-N-Go
  - Minimizes User Wait-Time
  - Download 27 GB HD movie in 70 sec
- Optimized Power Efficiency
  - No polling
  - Lower active & idle power requirements
- Backward compatible with USB 2.0
USB Implementers Forum (USB-IF)

USB-IF Promoter Board of Directors
Hewlett-Packard, Intel Corporation, LSI Corporation, Microsoft Corporation, NEC Corporation, NXP Semiconductors

- Compliance Committee
- Marketing Committee
- On-The-Go (OTG) Working group
- Device Working group

USB Compliance Workshops
USB compliance test development

Agilent Technologies
SuperSpeed USB Timeline

- **Initial Deployment**
- **Product Development**
- **STDs Development**
- **Broad Deployment**

**USB 3.0 Specification Complete Nov 12, 2008**

**Compliance Program/Industry Enabling Development**

**USB 3.0 Developers Conference**

**Compliance Testing**

**2008** | **2009** | **2010** | **2011**
USB 3.0 Industry Events Update

• USB 3.0 Promoter and Contributor Groups formed in 2007
• Compliance test requirements and enabling work underway
• USB-IF will continue to manage Logos, test plugfest events and marketing/promotion
• Agilent demonstrated USB 3.0 compliance test solution and test fixture prototype at USB 3.0 developers conference in November.

• Final specification available at http://www.usb.org/developers/docs/
  – adopters agreement
USB 3.0 Specification now available

http://www.usb.org/developers/docs/

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USB 3.0 Specification

Universal Serial Bus Revision 3.0 Specification (zip file format, size 2.97 MB) provides the technical details to understand USB 3.0 requirements and design USB 3.0 compatible products. Modifications to the USB 3.0 specification are made through Engineering Change Notices (ECNs).

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USB 3.0 Adopters Agreement

USB 3.0 Adopters Agreement (pdf file format, size 56k)

The USB 3.0 Adopters Agreement allows a signing company to participate in a reciprocal, royalty-free licensing arrangement for compliant products. Any USB 3.0 Adopters Agreement shall only be effective if received within one (1) year after first sale of products that include ‘Compliant Products’. See the USB 3.0 Adopters Agreement for details.
Extensible Host Controller Interface (xHCI) Draft Specification for USB 3.0

Universal Serial Bus 3.0

The eXtended Host Controller Interface (xHCI) draft specification describes the register-level host controller interface for Universal Serial Bus (USB) Revision 2.0 and above. The specification includes a description of the hardware/software interface between system software and the host controller hardware.

This specification is intended for hardware component designers, system builders and device driver (software) developers. The reader is expected to be familiar with the current Universal Serial Bus Specification revisions. Note: In case of conflicts between the xHCI and the USB specifications, the USB specifications take precedence and must be followed.

The specification is primarily targeted to host controller developers and system OEMs, but provides valuable information for platform operating system and BIOS device driver developers, adapter IHVs/ISVs, and platform/adapter controller vendors. This specification can be used for developing new products and associated software.

* xHCI Contributor agreement is required

How to become an xHCI contributor:

Thank you for your interest in becoming a contributor to the xHCI Specification. To become a contributor to the xHCI specification, please complete the steps listed below:

Step 1. Print and execute the xHCI Contributor agreement. Note: The agreement must be executed by a corporate officer.
Agilent Technologies Announces USB 3.0 SuperSpeed Physical Layer Compliance Test Application

SANTA CLARA, Calif., Nov. 24, 2008

Agilent Technologies Inc. (NYSE: A) today announced a comprehensive solution for testing SuperSpeed USB 3.0 devices to ensure compliance with the newly published standards.

At the first USB 3.0 Developers Conference in San Jose, Calif., Agilent demonstrated its new USB 3.0 transmitter and USB 3.0 receiver compliance test solutions. This demonstration included the industry’s first USB 3.0 signal quality test fixture. The complete solution enables engineers to quickly and accurately test their USB 3.0 designs.

Agilent’s solution will incorporate the final USB 3.0 specification announced by the USB-IF on Nov. 14. USB 3.0, known as “SuperSpeed USB” will deliver 10 times the data transfer rate of USB 2.0 and make power usage more efficient. SuperSpeed USB will be necessary for data-storage devices transferring more than 25 Gbps. Industry experts expect manufacturers to adopt SuperSpeed USB by the end of 2009 and to have consumer products widely available in 2010. However, until the actual silicon is available for testing, no USB solution will be ready for official certification.

“We are working closely with the developers of the SuperSpeed USB technology to make sure our solution completely meets the needs of engineers testing for USB 3.0 compliance,” said Scott Sampi, general manager of Agilent’s oscilloscope business. “To further improve the Agilent SuperSpeed USB 3.0 solution, we are collaborating with beta partners.”
Market Requirements Summary

• Performance 10X USB2 - PHY signal rate of 5 Gbps
  – data throughput > 200 MB/s

• Optimize for power efficiency

• Connector & Cable backward compatible with USB 2.0

• Protocol scalable to provide extension beyond 5Gbps

• Minimize SW impact
  – Same Programming and Device models as USB 2.0

• Support Virtualization for Devices
What is different for USB 3.0

### USB 2.0 High-Speed
- 480Mbps
- NRZI, Half Duplex
  (1 bi-directional link)
- 4 signals
  - D+, D-
  - VCC, GND
- Cable Lmax= 5meter
- $I_{\text{configLP/FP}} = 100\text{mA} / 500\text{mA}$
- No SSC

### USB 3.0 SuperSpeed
- 5 Gbps
- 8B/10B PRBS, Full Simplex
  (2 uni-directional links)
- 8 signals
  - 4 USB2 (D+,D-,Vcc,Gnd)
  - 4 SS Signals
- Cable $L_{\text{max}} = 3$ meters
- $I_{\text{configLP/FP}} = 150\text{mA} / 900\text{mA}$
- SSC
SuperSpeed Measurement Requirements

- Transmitter Compliance Testing:
  
  Still being defined - will reflect many of the same requirements as PCI Express 2.0 (5GT/s) and SATA compliance testing

  - Compliance will be measured at the end of the “compliance channel”
  - SMA termination for TX signals, phase matched SMA cable
  - Terminate link under test with high speed oscilloscope
  - Measure transmitted waveform with high speed oscilloscope
  - Use compliance pattern
  - 1M UI of data
  - Compute:
    - eye diagram,
    - Rj, Dj, Tj@10^-12 BER,
    - average data rate,
    - rise/fall time,
  - Test requirement for SSC Slew Rate
Transmitter Test Setup

Minimum bandwidth 12GHz
USB 3.0 Jitter Transfer Function

Figure 6-8. For information on the golden PLL measurement refer to the latest version of INCITS TR-35-2004, INCITS Technical Report for Information Technology – Fibre Channel – Methodologies for Jitter and Signal Quality Specification (FC-MJSQ).

Agilent USB 3.0 Transmitter Testing

Agilent USB2 Compliance application

Agilent USB3 Compliance application

DSA91304A Oscilloscope

Agilent USB3 Test Fixture

USB 3.0 Superspeed PHY Test Report

Overall Results: 2 of 12 Tests Failed
Polling.LFPS to compliance mode

Better power efficiency: low frequency periodic signal (LFPS) over polling

When receiver termination is present but no signaling is occurring on the differential link, it is considered to be in the electrical idle state. When in this state, low frequency periodic signaling (LFPS) is used to signal initialization and power management information. The LFPS is relatively simple to generate and detect and uses very little power.
Agilent USB 3.0 Receiver Test
Addresses Super Speed Requirements

- Based on N4903A J-BERT and N4915A-005 switch
- Complete solution for stress pattern generation with integrated jitter sources and error count
- Supports compliance testing and product characterization

At 5Gbps, USB 3.0 will require more stringent TX and RX testing:
- BER testing will mandatory part of compliance requirement
- Agilent N4903A J-BERT can create stressed USB 3.0 signaling

150 Mb/s-12.5 Gb/s Pattern Generator and Error Detector.
Includes built-in CDR
Jitter sources for RJ, PJ/SJ, BUJ
Interference channel ISI and Sinusoidal interference
SSC (spread spectrum clocks)
Receiver Test setup

Pattern Generator and Error Detector
RX Testing State Diagram
Achieve Success at 5GT/s with Good designs and Agilent Tools

- Cable, connector and channel characterization and testing will be crucial to ensuring links are reliable and meet performance requirements
  - TDR/TDT measurements will be essential to ensuring designs meet differential impedance targets
  - VNA measurements will allow verification of return loss, insertion loss and near/far end cross talk requirements
- Those same S-parameter measurements will allow de-embed of fixture and cabling to characterized your transmitter design to package/die.
- Signal BW and channel length will result in closed eye measurements

Equalization will also be needed to open eye at RX
Cable and Connector Challenges

- Deliver low cost
- Backward compatibility with USB 2.0
- Minimize connector types
- Meet performance reqts for 5Gbps
- Ease of use
- EMI/ESD

Cable/Connector Cost
And complexity will increase
USB 3.0 SS Standard Connectors

USB 3.0

USB 3.0 Standard-A Plug Pin No

USB 3.0 Standard-A Receptacle Pin No

USB 3.0 Standard-A Receptacle Footprint

USB 3.0 Standard-A Plug Pin No

USB 3.0 Standard-A Receptacle Pin No

USB 3.0 Standard-A Receptacle Footprint

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USB 3.0 Technical Review
Dec. 2008
Link Layer Improvements

USB 2 Transactions

OUT

host

token

data
•••

hndsh

device

token

data
•••

hndsh

IN

Bus turnaround times require 100s of bit times

USB 3 Transactions

Host

SSTX

data
•••

hndsh

Device

SSTX

data
•••

SSRX

hndsh

Full Simplex bus topology greatly improves bus utilization
Hubs

Provide fan out for USB3 connectivity

Two separate logical controllers

USB 2.0 Speeds

SuperSpeed

Upstream Connection supports both

Supports up to 128 devices
Frequently Asked Questions

1. Does USB 3.0 define or require an optical connection?
   • NO, this was discussed during the initial phases of the investigation but was ruled out due to cost. USB 3.0 will be wired only.

2. Is USB 3.0 going to be backward compatible with USB 2.0?
   • Yes, USB 3.0 requires that the host port is compatible with all USB 2.0 supported speeds: Low speed, Full speed and High speed.

3. Why does SuperSpeed require 4 new signals, SSTXP, SSTXN, SSRXP, SSRXN?
   • Backwards compatibility requires support for Low and Full-Speed USB. These run at 3.3V signal levels which is not compatible with IO buffers designed to run at 5Gbps

4. How will users know that a USB port supports SuperSpeed?
   • USB 3.0 ports will be color-coded Blue to make them recognizable.
Summary

SuperSpeed USB addresses USB 2.0 performance bottleneck and retains attributes that made USB so successful

• Maintains backward compatibility

• 10x performance

• Same programming and device models as USB 2.0

• Optimized for power efficiency

• Protocol scalable to 20Gb/s

USB 3.0 will deliver Performance and Power Efficiency

Agilent has the tools and expertise to help you succeed with USB 3.0