Tips to debug DDR parametric and protocol measurement with Mixed Signal Oscilloscope

Ai-Lee Kuan
Product Marketing Engineer
(Memory Solutions)
Agenda

• Memory system development cycle.

• Get the most out of your debug tool - MSO
  • Parametric testing with DDR compliance tool
  • Timing relationship across multiple digital channels.
  • Protocol decode

• Tips using the MSO to validate and troubleshoot DDR signals.
  • Probing with MSO
  • DDR Parametric Compliance Testing
  • DDR Protocol Decode
  • DDR Analog and Digital Signals Time Correlation
  • Trigger functions on DDR bus.
  • Create User Defined App for controller testing
# Memory System Development Cycle

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<td>Tools</td>
<td>Simulation software (ADS)</td>
<td>Oscilloscope, Logic Analyzer, Mix Signal Oscilloscope</td>
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<td>Tasks</td>
<td>Device and Interconnect Characterization</td>
<td>Design for Test</td>
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<td>Optimization of transmitter, receiver, and channel for most reliable data transfer</td>
<td>Prototype Characterization &amp; Validation</td>
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<td>Increased design complexity and smaller timing margins</td>
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<td>System Integration &amp; Functional Validation</td>
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**Typical Challenges**
- Signal Integrity
- Read/Write Separation
- Probing
- Elusive, intermittent failures
- Data Corruption
- Interoperability across a broad range of devices & system configurations

**Tools**
- Simulation software (ADS)
- Oscilloscope, Logic Analyzer, Mix Signal Oscilloscope
- Agilent Restricted
Memory System Development Cycle

**Project Phase**

- **Tools**
  - Simulation software (ADS)
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- **Tasks**
  - Design for Test
  - Bring-Up Test
  - System Integration & Functional Validation
  - Prototype Characterization & Validation
  - Signal Integrity
  - Read/Write Separation
  - Probing
  - Elusive, Intermittent failures
  - Data Corruption
  - Interoperability across a broad range of devices & system configurations
  - Increased design complexity and smaller timing margins
  - Co-design of IC/package/connectors/channel
  - Typical Challenges

- **Typical Challenges**
  - Data Corruption
  - Probing
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Advanced Design System for Design Simulations

Physical Design Verification

Interconnect Modeling

DDR channel simulation

DDR Toolkit in ADS

DDR Simulation to meet Compliance Specifications

Package Simulation for SI and PI

Driver/Receiver Design Integration

Prefer Agilent Technologies

Preparing for Memory Technology Advances

December 16, 2008
Memory System Development Cycle

**Project Phase**
- **Design Simulation**
  - Simulation Software (ADS)
  - Device and Interconnect Characterization
  - Optimization of transmitter, receiver, and channel for more reliable data transfer
  - Co-design of IC/package/connectors/channel
- **Device, Board and System Test**
  - Oscilloscope, Logic Analyzer, Mix Signal Oscilloscope
  - Design for Test
  - Prototype Characterization & Validation
  - Bring-Up Test
  - System Integration & Functional Validation
  - Signal Integrity
  - Read/Write Separation
  - Probing
  - Elusive, intermittent failures
  - Data Corruption
- **Typical Challenges**
  - Interoperability across a broad range of devices & system configurations

**Tasks**
- Increased design complexity and smaller timing margins

**Tools**
- Tools include simulation software (ADS), oscilloscopes, logic analyzers, and mix signal oscilloscopes.

**Agilent Restricted**

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Device, Board and System Test

**Tool:** Oscilloscope  
**Challenges:**  
✓ Signal integrity  
Reliable data transfer at speed - cross talk, impedance, transmitter, receiver, power distribution, interconnect  
✓ Read/Write Separation  
Trace failures to root cause for signal integrity analysis

**Tool:** Logic Analyzer  
**Challenges:**  
✓ Data Corruption  
Read or Write errors, read/write leveling, bad address and protocol violations  
✓ Interoperability across a broad range of devices and system configurations

**Tool:** Mix Signal Oscilloscope  
**Challenges:**  
✓ Signal integrity  
✓ Read/Write Separation  
✓ Data corruption  
✓ Interoperability across devices and system configurations  
✓ Elusive, intermittent failures
Agenda

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  • Parametric testing with DDR compliance tool
  • Timing relationship across multiple digital channels.
  • Protocol decode

• Tips using the MSO to validate and troubleshoot DDR signals.
  • Probing with MSO
  • DDR Parametric Compliance Testing
  • DDR Protocol Decode
  • DDR Analog and Digital Signals Time Correlation
  • Trigger functions on DDR bus.
  • Create User Defined App for controller testing
Get the MOST out of your MSO

It’s THREE instruments in ONE

**Analog view** enables DDR clock and electrical testing for compliance to JEDEC spec.

**Timing Waveform** enables viewing of timing relationships across multiple DDR buses (data, strobes, clock, command).

**Listing** enables viewing of state information

**Protocol Decode** enables decoding of Command, Bank Address, Address, Data.
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Probing with MSO

A MSO has 4 analog channels and 16 digital channels that are time correlated for both DDR analog and protocol debug.

- **16 digital channels** for probing with flying leads, soft touch or etc.
- **4 analog channels** for probing with scope probe.
- Logic analyzer flying lead set to connect to DQ and Command.
- Scope probe board adapter/probe head to connect to DQS, DQ and CK.
DDR Probing Options for Scopes/Logic Analyzer

Soft touch probe

NEW InfiniiMax to Soft touch pro adapter

DDR BGA probes

NEW LPDDR BGA probe
MSO for DDR Parametric Measurement

MSO with DDR compliance test software provides automatic parametric testing capability on your DDR signals for compliance as per JEDEC specification:
- Clock (tCK, tJIT(cc), tERR.. etc)
- Electrical (Vih, Vil, Vid, Vix... etc)
- Timing (tDQSQ, tDSS, tWPRE, tWPST)

Eye-Diagram Analysis

DQ Setup Time

Write Preamble Width
MSO for DDR Eye-Diagram Analysis

Troubleshoot an eye-diagram failure when it violates the DDR mask

Unfold the eye-diagram to see the waveform exactly where the violation occurred. You can then perform more failure analysis such as measuring the timing relationships between signals or look at DQ pattern for inter-symbol interference (ISI) related failures.
Debugging clock jitter failures with EZJIT tool (time interval error jitter measurement)

- Clock signal
- Histogram of the Clock TIE
- Measurement trend of the Clock TIE
- Jitter spectrum of the Clock TIE
MSO for DDR Timing

Digital channels provides timing information across multiple DDR buses for timing measurement.

Example 1: Making Power-Down modes timing measurement in timing mode with the logic analyzer channels.
Example 2: MRS Command to Power-Down Entry
MSO for DDR Protocol Decode – Step 1

Easy setup for decoding the DDR protocol with the digital channels.

Example:
Set up 8 bit DATA (DQ0-7) with Command (RAS, CAS, WE) bus.
Group the buses:

**Bus 1 - DATA (DQ0-7)**

**Bus 2 - Command (RAS, CAS, WE)**
Group the buses:

Bus 1 - DATA (DQ0-7)

Bus 2 - Command (RAS, CAS, WE)
MSO for DDR Protocol Decode – Step 3

Create a symbol file as per JEDEC command truth table:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>WE</th>
<th>CAS</th>
<th>RAS</th>
<th>HEX value</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>ACT</td>
<td>Bank Activate</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>READ</td>
<td>Read Operation</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>REF</td>
<td>Refresh</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>BURST</td>
<td>Burst Operation</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>PRE</td>
<td>Precharge Bank</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>WRITE</td>
<td>Write Operation</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>LOAD</td>
<td>Mode Register Set</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

At C:\Documents and Settings\All Users\Documents\Infiniium\Config directory, you will see a text file named bus2.txt
Format:
Symbol .. Bus value.. Format
(binary, decimal or hexadecimal).
MSO for DDR Protocol Decode

DDR Protocol Decode view with waveform and listing window
DDR Analog/Digital Bus Time Correlation

Setup command and data bus to use state clock:
CK is connected to Channel 2
DQS is connected to Channel 1

COMMAND bus needs to use the state clock from CK (Channel 2) and set to sample at rising edge only.

DATA bus needs to use the state clock from DQS (Channel 1) and set to sample at both rising and falling edges.
DDR Analog/Digital Bus Time Correlation

Start of a Burst (Burst length = 4)  End of back to back bursts (Burst length = 4)
Trigger Function - Pattern/State Trigger

Trigger on a known data pattern, DQ = x10 (Sequence data pattern: x10, x30, x50, x70..)

At Trigger Setup, select Pattern/State trigger and trigger on Bus 1 (DQ) = 10.
Trigger Function - State/Pattern Trigger

Trigger found: DQ = x10 (start of a data pattern sequence = x10, x30, x50, x70)
Trigger Function – Pattern/State Trigger

Trigger on 2 bus patterns: Bank Address and Command

Command = READ

Bank Address = 3
Trigger Function - InfiniiScan

Use InfiniiScan “Zone Qualify” to trigger on Read or Write burst.

- **Zone 1** is drawn on the DQS waveform to discard the normal bits or idle state signals.
- **Zone 2** is drawn on one of the distinctive waveform of the Read and Write bursts patterns.

There are 2 distinctive Read and Write burst patterns.
Trigger Function - InfiniiScan

Trigger on READ burst only

Read operation on the bus issued by the memory controller.
Trigger Function - InfiniiScan

Trigger on Write burst only.

Write operation on the bus issued by the memory controller.
Memory Controller Debug

User Defined Application (UDA) – Measure tDS and tDH READ cycle at the memory controller

Test sequence:
1. Setup trigger on a read cycle on command bus.
2. Write a test sequence to measure setup and hold time with DQS and DQ.
3. Build and Launch the Application
Memory Controller Debug – Step 1

Create a set up file – Trigger on command READ
Write a test sequence to measure setup and hold time with DQS and DQ using SCPI commands.
Memory Controller Debug – Step 3

Build and Launch application

- Measure Read hold time, tDH
- Measure Read setup time, tDS
Memory Controller Debug

HTML report

- Read hold time, tDH
- Read setup time, tDS
Memory Controller Debug

Integrate InfiniiScan and Eye Diagram features into UDA:

The ISCan subsystem commands:

- DELay
- MEASurement
- MODE (selects the type of InfiniiScan trigger mode)
- NONMonotonic
- SERial
- ZONE (placement of zones and trigger mode)

The Serial Data Equalization subsystem commands:

- FFEQualizer:DISPlay (display real-time eye diagram on or off.)
- FFEQualizer:SOURce
- FFEQualizer:NTAPs
- FFEQualizer:TAP
- FFEQualizer:TAP:PLENgth
- FFEQualizer:TAP:WIDTh
- FFEQualizer:TAP:DELay
- FFEQualizer:TAP:AUTomatic
- FFEQualizer:BANDwidth
Summary

The MSO series scope has sufficient bandwidth to validate and troubleshoot DDR signals with the powerful capability:

- **DDR Parametric Compliance Testing**
  - Automatic clock, electrical and timing test as per JEDEC specification.
- **DDR Protocol Decode**
  - Listing window with protocol and data information.
- **DDR Analog and Digital Signals Time Correlation**
  - Variety of Probing options for best measurement accuracy
  - State clocking with DDR data and command bus.
  - View both analog and digital bus at the same time.
- **Trigger functions on DDR bus**
  - Pattern trigger on command, BA, Addr, Data..etc
  - InfiniiScan to separate Read and Write operations
- **Memory Controller Debug with UDA**
# Product Information

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<tr>
<td><strong>Mix Signal Oscilloscope</strong></td>
<td></td>
</tr>
<tr>
<td>MS09254A</td>
<td>2.5 GHz, 4 analog plus 16 digital channels</td>
</tr>
<tr>
<td>MS09404A</td>
<td>4 GHz, 4 analog plus 16 digital channels</td>
</tr>
<tr>
<td><strong>DDR BGA Probes</strong></td>
<td></td>
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<tr>
<td>W2637/8A</td>
<td>LPDDR BGA probes</td>
</tr>
<tr>
<td>W2631/2/3/4A</td>
<td>DDR2 BGA probes</td>
</tr>
<tr>
<td>W3631/3A</td>
<td>DDR3 BGA probes</td>
</tr>
<tr>
<td><strong>DDR Compliance Software</strong></td>
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<td>U7233A</td>
<td>LPDDR / DDR Compliance Software</td>
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## DDR Protocol Solution with Logic Analyzer

### Our Customers
- Embedded Applications
  - Computer / Server

### Data Acquisition
- 2GHz Sata / 8GHz Timing High Speed Logic Analysis Module

### Probing
- DDR2 & 3 BGA Probes
- DDR2&3 Slot DIMM Interposer

### Analysis Tool
- Protocol Compliance and Performance Analysis tool