Testing DisplayPort Over the Type-C Connector

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Topics Today

– Overview
– TX/RX Testing Requirements
– Cable Test
– Questions
USB Type-C Interface and DP Alt Mode Overview
What is the USB Type-C Connector?
“One connector to rule them all”

<table>
<thead>
<tr>
<th>Original USB Industry Drivers</th>
<th>Type-C Industry Drivers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single connector type/Expandability</td>
<td>Broad application in standards</td>
</tr>
<tr>
<td>Performance/Speed</td>
<td>20 Gb/s with path to 80 Gb/s</td>
</tr>
<tr>
<td>Power</td>
<td>Can handle 5 amps at 20 volts</td>
</tr>
<tr>
<td>Ease of Use for End-User</td>
<td>Reversible (can be flipped)</td>
</tr>
</tbody>
</table>

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Where does USB-C fit?
Why Does It Matter?
Simplicity and Capability to consumer…. 
……Complexity to Designers, Integrators, and Validators

Speed
Speeds of the Future and Backwards Compatibility

Power
Up to 100 W
Power direction no longer fixed

Standards Integration

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USB Type C Signal Plan

High Speed Lanes

- 4 High Speed Lanes: Up to 20Gbs each
- 4 GND & 4 Supply Pins To handle up to 5 amps
- USB2 lines: -USB2 operation -Link Communication
- SBU lines: -Extra lines for alternate use

Port 1

Port 2
USB Type C Signal Plan

CC Pins

CC lines for:
- Orientation
- Configuration Channel
- Supply Power to Cable
- Power Delivery
- Communication
USB Type C Port Function

USB 3.1 & USB 2.0

USB3.1 Operation

Alt
STD

STD Mux

Port Mux

USB 3.1

USB2.0 Operation

D+
D−

D−
D−

USB 2.0

V_{BUS}
SBU2
CC1

V_{BUS}
SBU1

TX2
RX2

TX2
RX2

Product

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USB Type C Port Function
Alternate Mode: DisplayPort

Downstream Facing Port (Video Output)
- DP
- STD Mux
- Port Mux
  - USB 3.1
  - Power Supply

Upstream Facing Port (Display)
- Provider/Consumer
- Power (V_BUS) Control
- Port Mux
- Cable
  - GND
  - TX2, TX1
  - V_BUS
  - SBU2, CC1
  - D-, D+
  - TX3, TX0
  - V_BUS
  - CC2
  - RX0, RX3
  - V_BUS
  - SBU2, CC1
  - D-, D+
  - CC2
  - RX1, RX2
  - V_BUS
  - GND
Testing DisplayPort over the Type-C Connector: TX and RX Phy Layer Validation

**Disclaimer:** The DisplayPort AltMode compliance test requirements are not final. Therefore, all opinions, judgments, recommendations, etc. that are presented herein are the opinions of the presenter of the material and do not necessarily reflect the opinions of VESA, or other member companies.

Brian Fetz
Marketing Engineer
Oscilloscope and Protocol Division
Review of DisplayPort Interface

Main Link
- Up to 4 differential lanes: 4 possible bit rates
- TX:
  - 4 possible level settings
  - 4 possible pre-emphasis settings
  - Spread Spectrum Clocking (optional)
  - Dual Mode optional
- RX:
  - Receiver individual clock recovery
  - Receiver Tolerance curve specified.
  - Receiver Sensitivity = 50mV

AUX Channel
- Phy Layer
  - Bit rate at 1Mbs
  - Manchester II encoded
- Purpose
  - Link Management
  - Test Mode control
DisplayPort TX w/USB Type-C connector
TX Test Setup for DP over USB Type-C

Fixtures

Keysight TPAs
N7015A
N7016A

Connector: Type C

High Speed Phy test
AUX Phy test
USB C to DP cable

Unigraf DPR-100
AUX Automation

Power Delivery Controller

AUX Automation

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DisplayPort 1.3/1.4

- New DisplayPort 1.3/1.4 Specification: Phy Layer Implications

**DP TX Testing**
- **DP TX**
  - RBR, HBR, HBR2, HBR3
- **De-Embed Fixture**
- **Embed Cable Model**
- **CTLE**
- **DFE**
- **Measurement**
  - **Eye Diagram**
  - **Jitter**
  - **Level, PE, SSC**

**Mathematical Processing**
- **Acq**

**DP RX Testing**
- **Level Control, Jitter Addition**
- **Crosstalk Addition**
- **Add Channel Loss**
- **DP RX**
  - RBR, HBR, HBR2, HBR3
- **Calibration**
- **Test**
DP Transmitter Testing: Whole Channel

**DUT** → **Cable Model** → **Sink**

- **Data**
- **Level**
- **Tx**
- **PE**
- **Ck**
- **Driver**
- **Logic Decode**

**DisplayPort Source**

- Standard DP
- mDP
- USB Type C

**Cable Loss Model**

**CTLE**

**DFE (50mv max)**

**TP2** → **TP3** → **TP3EQ** → **TP3EQ’**

**REFERENCE EQUALIZER**

Math performed on oscilloscope on TP2 acquisition

**Eye**
## DisplayPort Tests: Patterns and Test Point

<table>
<thead>
<tr>
<th>Test</th>
<th>RBR</th>
<th>HBR</th>
<th>HBR2</th>
<th>HBR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-1 Eye Diagram</td>
<td>PRBS7</td>
<td>PRBS7/HBR2CPAT</td>
<td>HBR2CPAT TP3EQ</td>
<td>Arbitrary TP3EQ</td>
</tr>
<tr>
<td>3-2 Non PreEmphasis Level</td>
<td>PRBS7</td>
<td>PRBS7</td>
<td>PRBS7</td>
<td>Arbitrary</td>
</tr>
<tr>
<td>3-3 Pre-Emphasis Level</td>
<td>PRBS7</td>
<td>PRBS7</td>
<td>PLTPAT</td>
<td>Arbitrary</td>
</tr>
<tr>
<td>3-4 Inter Pair Skew</td>
<td>D10.2</td>
<td>D10.2</td>
<td>D10.2</td>
<td>Arbitrary</td>
</tr>
<tr>
<td>3-11 Non ISI Jitter</td>
<td>PRBS7</td>
<td>PRBS7</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>3-11 Deterministic Jitter</td>
<td>NA</td>
<td>NA/HBR2CPAT</td>
<td>HBR2CPAT TP3EQ</td>
<td>Arbitrary TP3EQ</td>
</tr>
<tr>
<td>3-12 Total Jitter</td>
<td>PRBS7</td>
<td>PRBS7/HBR2CPAT/D10.2</td>
<td>CP2520/D10.2 TP3EQ</td>
<td>Arbitrary TP3EQ</td>
</tr>
<tr>
<td>3-14 Main Link Frequency</td>
<td>D10.2</td>
<td>D10.2</td>
<td>D10.2</td>
<td>Arbitrary</td>
</tr>
<tr>
<td>3-15 Spread Spectrum Modulation Frequency</td>
<td>D10.2</td>
<td>D10.2</td>
<td>D10.2</td>
<td>Arbitrary</td>
</tr>
<tr>
<td>3-16 Spread Spectrum Deviation Accuracy</td>
<td>D10.2</td>
<td>D10.2</td>
<td>D10.2</td>
<td>Arbitrary</td>
</tr>
<tr>
<td>3-18 Dual Mode TMDS Clock</td>
<td>All appropriate Data Rates/Random Pattern</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-19 Dual Mode TMDS Eye Test</td>
<td>All appropriate Data Rates/Random Pattern</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## DisplayPort Tests and Levels & Pre-Emphasis

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<thead>
<tr>
<th>Test</th>
<th>Levels</th>
<th>Pre-Emphasis</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-1 Eye Diagram</td>
<td>RBR/HBR: Setting 2 HBR2/3: User Choice</td>
<td>RBR/HBR: Setting 0 HBR2/3: User Choice</td>
</tr>
<tr>
<td>3-2 Non PreEmphasis Level</td>
<td>All Settings</td>
<td>Setting 0</td>
</tr>
<tr>
<td>3-3 Pre-Emphasis Level</td>
<td>All Settings</td>
<td>All Valid Settings</td>
</tr>
<tr>
<td>3-4 Inter Pair Skew</td>
<td>Setting 2</td>
<td>Setting 0</td>
</tr>
<tr>
<td>3-11 Non ISI Jitter</td>
<td>RBR/HBR: All settings</td>
<td>RBR/HBR: Setting 0</td>
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<tr>
<td>3-14 Main Link Frequency</td>
<td>Setting 2</td>
<td>Setting 0</td>
</tr>
<tr>
<td>3-15 SSC Modulation Frequency</td>
<td>Setting 2</td>
<td>Setting 0</td>
</tr>
<tr>
<td>3-16 SSC Deviation Accuracy</td>
<td>Setting 2</td>
<td>Setting 0</td>
</tr>
<tr>
<td>3-18 Dual Mode TMDS Clock</td>
<td>No choice</td>
<td></td>
</tr>
<tr>
<td>3-19 Dual Mode TMDS Eye Test</td>
<td>No choice</td>
<td></td>
</tr>
</tbody>
</table>
RX Test Setup for DP over USB Type-C

InterSymbol Interference

High Speed Phy test

USB C to DP cable

AUX Automation

Unigraf DPT-200

N7015A

N7016A
Keysight DisplayPort 1.3 Solutions and Solution Elements

Source Test Solution
- Computer Motherboards, ICs, Graphic Cards
  - DSO V series Infinium Real Time Oscilloscopes
  - Unigraf DPR-100 For automation
  - U7232D DisplayPort Compliance Test SW

Media Testing
- Cables, PC Boards, Connectors
  - E5071C VNA

Sink Test Solution
- PC Monitors
  - N4915A-006 DP ISI Generation
  - Unigraf DPT-200 for Automation

Link Layer & General Solutions
- Protocol Debug solution
  - Granite River Labs GRL-DP-DEC

Source Test Solution
- Wilder TPA
- N7015A TPA
- BIT-DP-CBL-0002
- Luxshare Rec

Media Testing
- STD/mDP
- USB C

Sink Test Solution
- STD/mDP
- USB C
- BIT-DP-RTF-0002
- Luxshare Rec

Link Layer & General Solutions
- STD/mDP
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Testing DisplayPort over the Type-C Connector: Cable Test Challenges

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Supported Cable Types

USB Type-C to USB Type-C
• Type-C to Type-C will re-use USB Type-C electrical specifications and will require proper documentation from USB-IF to prove compliance

USB Type-C to DisplayPort
• Specification based on USB Type-C to USB Type-C Passive Cable Assemblies (Section 3.7.3) specification methodology

USB Type-C to Protocol Converter (e.g. DVI, HDMI)

USB Type-C to Multi-function Dock
DisplayPort Alt Mode Cable Measurement Challenges

Tighter device margins (1UI is ~120 ps @ 8.1 Gbps)

Managing the different impedance environments of USB Type-C (85Ω) and DisplayPort (100Ω)

Significant loss at higher frequencies require more rigorous approach to removing fixture effects, to measure the true performance of the device

Channel response affected by many features in channel (loss, reflection, crosstalk, mode conversion)
Managing the Different Impedance Environments

4.2.3 USB Type-C to DisplayPort Cable Electrical Properties
Insertion loss and Return loss are to be tested relative to an 85Ω differential environment at the USB Type-C connector and relative to a 100Ω differential environment at the DisplayPort connector.

How to perform measurements when the impedance targets are different on each end?

Recommendations:
• Design fixtures in 50 ohm SE (100 ohm DIFF)
• Calibrate in 50 ohm SE (100 ohm DIFF)
• Measure in 50 ohm SE (100 ohm DIFF)
• Renormalize S-parameters of USB port to 85 ohm, using port reference impedance conversion function
S-parameters and Reference Impedance

Reference impedance is an important concept to understand when using S-parameters.

Typically, S-parameters are stated as xx dB. However, to be exact, it should be stated as xx dB when yy Ω is used as the reference impedance. The reference impedance is typically 50 Ω and is omitted. But in principle, it may be an arbitrarily value.

It is important to keep in mind that the S-parameter is a relative (normalized) value. In other words, the S matrix values change depending on the reference impedance.

50 Ω is only a reference value, so it can be changed. Suppose the S-parameter S is already determined for 50 Ω, it is possible to transform it to S-parameter $S'$ for other reference impedances by using

$$S' = P^{-1}(S - \gamma)(I - \gamma S)^{-1}P$$
ENA Option TDR provides an integrated port reference impedance conversion feature.
Removing the Fixture Effects from Measurement

USB Example

• USB 3.1 CTS recommends **2x Thru de-embedding (AFR) and TRL calibration**
• Excellent correlation between the AFR and TRL methods
• Removing the effects of the fixture is critical to ensure sufficient yield
New Compliance Methodology

Traditional Method

- Interconnects have been characterized by measuring parametric characteristics such as insertion loss and impedance.
- The limitation of the traditional parametric measurement is that it does not allow tradeoffs among the various test parameters.

Sufficient margin on insertion loss, but fails several points on return loss. Will this spec violation really cause interoperability issues?
There are three signal integrity impairments that impact the end-to-end link performance: attenuation, reflection and crosstalk.

The channel metrics represents these three impairments:

- Insertion loss fit at Nyquist frequency (ILfitAtNq)
- Integrated multi-reflection (IMR)
- Integrated crosstalk (IXT)

The IMR and IRL limits have a dependency on ILFitAtNq. More IMR and IRL can be tolerated when ILFitAtNq decreases.
DisplayPort Alt Mode Cable Assembly Compliance Test

Typical Configuration

• ENA Mainframe
  • E5071C-4D5: 4-port, 300 kHz to 14 GHz
  • E5071C-4K5: 4-port, 300 kHz to 20 GHz
• Enhanced Time Domain Analysis Option (E5071C-TDR)
• ECal Module (N4433A)

(*) The list above includes the major equipment required. Please contact our local sales representative for configuration details.

• Method of Implementation (MOI) document and instrument setup file will be made available for download on Keysight.com

Test Fixtures
Fixtures are available for purchase through Luxshare-ICT.

ENA Option TDR is a authorized test tool for Cable PHY.
http://www.vesa.org/displayport-developer/certified-components/

www.keysight.com/find/ena-tdr_compliance
DisplayPort Alt Mode Cable Measurement Challenges

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Managing the different impedance environments of USB Type-C (85Ω) and DisplayPort (100Ω)
Renormalize S-parameters using port reference impedance conversion function

Significant loss at higher frequencies require more rigorous approach to removing fixture effects, to measure the true performance of the device
2x thru de-embedding using Automatic Fixture Removal (AFR)

Channel response affected by many features in channel (loss, reflection, crosstalk, mode conversion)
Paradigm shift from traditional parametric testing to channel metrics

Keysight has the tools and expertise to help you conquer USB 3.1 Physical Layer Test Challenges