Serial ATA Interoperability Program Revision 1.4
Agilent MOI for SATA SI Tests
Using Agilent E5071C ENA Network Analyzer Option TDR

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Serial ATA Logo Group
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1. Modification Record

<table>
<thead>
<tr>
<th>Revision</th>
<th>Comments</th>
<th>Issue Date</th>
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</tbody>
</table>

2. Acknowledgements

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Sho Okuyama             Agilent Technologies        sho_okuyama@agilent.com
3. Purpose

This test procedure was written to explain how to use the Agilent E5071C ENA Network Analyzer Option TDR to make the measurements required per the Serial ATA specification rev 3.0 for cable assemblies.

4. References

Serial ATA Revision 3.0

Serial ATA Interoperability Program Revision 1.4 Unified Test Document Version 1.01

5. Resource Requirements

1. E5071C Network Analyzer with option TDR and one of the following options
   4D5/4K5

2. Electronic Calibration Module N4433A

3. Four 3.5 mm cables and adapters of 20 GHz bandwidth or equivalent

4. 50 Ohm terminators to terminate unused channels (ex. Agilent 909D-301)

5. Two SATA plug fixtures. Recommended fixtures are listed below.
   - Crescent Heart Software P/N TF-SATA-FE-ZP
   - ICT Solutions P/N TF-1P21
   - Wilder Technologies P/N SATA-TPA-P 600-1013-000
6. Measurement Setup

6.1. Recalling State File

This section describes how to setup the instrument for SATA compliance testing. Using the state file distributed on www.agilent.com/find/ena-tdr_sata-si, the setup operation can be skipped. Download the file that matches the E5071C option, and extract the file. The zip file includes two state files for internal SATA and eSATA. If you use your local PC to download, save the state file to a USB mass storage device in order to move it to the E5071C. Connect the USB mass storage device into the USB port on the front panel of the E5071C. For manual measurement setup, refer to the section 8 Appendix.

Note: Hard Keys (Keys located on the Front panel of E5071C) are displayed in Blue color and Bold. (Example: Avg, Analysis)

Note: Soft keys (Keys on the screen) are displayed in Bold. (Example: S11, Real, Transform)

Note: Buttons (in the TDR) are displayed in Green color and Bold. (Example: Trace, Rise Time)

Note: Tabs (in the TDR) are displayed in Brown color and Bold. (Example: Setup, Trace Control)

1. If TDR setup wizard appears, click Close button on the wizard.
2. Open Setup tab (item1).
3. Click Advanced Mode (item2).
4. A dialog box appears requesting for confirmation. Then click Yes. (Clear the check box for “Use Advanced Calibration Methods”)
5. Click **File** (item3) and select **Recall State** to open the Recall State dialog box.

6. Specify a folder and a file name, and click **Open**.

6.2. **Measurement Configuration**

This Section describes the screen configuration of the E5071C and the cable connection.

![Figure 6-1: SATA SI compliance test setup](image)

Channel1 for time domain measurement is controlled by the TDR user interface at the bottom of the screen and Channel2 for frequency domain measurement is controlled by the softkey on the right-side of the screen or hardkey on the instrument front panel.
Figure 6-2: Cable and fixture connection

The cables and fixtures should be connected to the instrument as shown in the figure above. Table 4-1 shows the cable connection for each measurement item. The measurement items of the same cable connection can be done simultaneously.

Table 6-1: Cable and Fixture Connection

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mated Connector Impedance</td>
<td>A Tx+</td>
<td>A Tx-</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
<tr>
<td>Cable Absolute Impedance</td>
<td>B Tx+</td>
<td>B Tx-</td>
<td>A Rx+</td>
<td>A Rx-</td>
</tr>
<tr>
<td>Cable Pair Matching</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common Mode Impedance</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Insertion Loss</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Rise Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inter-Symbol Interference (Eye Diagram)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intra-Pair Skew</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential-to-Differential Crosstalk</td>
<td>A Tx+</td>
<td>A Tx-</td>
<td>A Rx+</td>
<td>A Rx-</td>
</tr>
<tr>
<td></td>
<td>B Tx+</td>
<td>B Tx-</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
</tbody>
</table>

Note: A and B represent each one of the test fixtures.
6.3. Calibration and Adjustment

6.3.1. SI-C1, SI-C2 Time Domain Calibration

1. Press **Channel Next** key to select Channel1.

2. Open **Setup** tab (item1).

3. Click **ECal** (item2) to launch TDR Setup Wizard.

4. Connect the test cables to the ECal module.

5. Click **Calibrate** button, then click **Next >**.
6. Disconnect the ECal module then connect the test fixtures and leave them at OPEN.

7. Click **Fixture Comp** (item1).

8. Click **Finish** (item2).
6.3.2.  SI-C3 Rise Time Adjustment

The system rise time is adjusted at the connector of the test fixture.

1.  Press Channel Next key to select Channel1.
2.  Press Channel Max key to enlarge Channel1.
3.  Connect the SMA cables from port 1 and 2 of the E5071C to the TX+ and TX- connectors of the SATA-to-SMA Test Fixture.  Leave the test fixture at OPEN.
5.  Open TDR/TDT tab.
6.  Select Tdd11.
7.  Click Run button.
8.  Adjust Rise Time so that the marker value on Trace 4 is as close as 70 psec, and note the input value (Input value #1).  Repeat the same procedure on Trace 4 for rise time as close as 35 psec and note the input value (Input value #2).
9.  Set measurement parameter on Trace 4 back to the original Tdd21.
10. Set the rise time to the input value #1 on the trace 1, 2, 3, 5, 6, 7, 9, 10, 13, 14 in Channel 1.
11. Set the rise time to the input value #2 on the trace 4, 8, 12 in Channel 1.
12. Press Channel Max key to get Channel1 back to the normal size.

6.3.3.  SI-C1, SI-C2, SI-C3 Frequency Domain Calibration

1.  Press Channel Next key to select channel 2.
2.  Connect SMA cables to the ECal module.
3.  Press Cal button on the instrument front panel.
4.  Press ECal > 4-Port Cal to perform calibration.
7. Measurement and Data Analysis

7.1. Introduction

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process. The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

This section specifies all reference material external to the MOI, including the specific subclauses references for the test in question, and any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by a bracketed number (e.g., [1]) when mentioned in the test description. Any other references in the test description that are not indicated in this manner refer to elements within the MOI document itself (e.g., “Appendix 8.1.”, or “Figure 7.1”).

Last Modification

This specifies the date of the last modification to this test.

Test Procedure

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

Observable Results

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.
7.2. Cable Assembly Requirement

7.2.1. SI-01 Mated Connector Impedance

**Purpose:** To verify that the mated connector impedance of the DUT is within the conformance limits.

**References:** [1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.8.1.

**Last Modification:** November 11, 2010 (Version 1.00RC)

**Test Procedure:**

Assuming the initial setup/calibration procedures in chapter 6 have been performed, the measurement for this test is as follows:

1. Connect the test fixture to the test cables according to the Table 7-1. Unused test ports should be terminated.

**Table 7-1: Cable Connection**

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fixture PIN Number</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A Tx+</td>
<td>A Tx-</td>
<td>B Rx+</td>
<td>B Rx-</td>
<td></td>
</tr>
<tr>
<td>B Tx+</td>
<td>B Tx-</td>
<td>A Rx+</td>
<td>A Rx-</td>
<td></td>
</tr>
</tbody>
</table>

Note: A and B represent each one of the test fixtures.

2. Connect SATA cable to the test fixture.

3. Press **Channel Next** key to select Channel1.

4. Press **Channel Max** key to enlarge Channel1.

5. Click **Stop Single** for Time Domain measurement.
Figure 7-1: Measurement example of SI-01, SI-02, SI-03, SI-04, SI-08, and SI-10.

**Observable Results:** Read Pass/Fail sign on Trace1 and Trace5 (item1 in Figure 7-1).

**Mated Connector Impedance Limit Line**

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max</td>
<td>-0.1 ns</td>
<td>0.3 ns</td>
<td>115 Ohm</td>
<td>115 Ohm</td>
</tr>
<tr>
<td>Min</td>
<td>-0.1 ns</td>
<td>0.3 ns</td>
<td>85 Ohm</td>
<td>85 Ohm</td>
</tr>
</tbody>
</table>
7.2.2. SI-02 Cable Absolute Impedance

**Purpose:** To verify that the cable absolute impedance of the DUT is within the conformance limits.

**References:** [1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.8.2.

**Last Modification:** November 11, 2010 (Version 1.00RC)

**Test Procedure:**
Assuming the initial setup/calibration procedures in chapter 6 have been performed, the measurement for this test is as follows:

1. Connect the test fixture to the test cables according to the Table 7-2. Unused test ports should be terminated.

**Table 7-2: Cable Connection**

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixture PIN Number</td>
<td>A Tx+</td>
<td>A Tx-</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
<tr>
<td></td>
<td>B Tx+</td>
<td>B Tx-</td>
<td>A Rx+</td>
<td>A Rx-</td>
</tr>
</tbody>
</table>

Note: A and B represent each one of the test fixtures.

2. Connect SATA cable to the test fixture.

3. Press **Channel Next** key to select Channel1.

4. Press **Channel Max** key to enlarge Channel1.

5. Click **Stop Single** for Time Domain measurement.

**Observable Results:** Read Pass/Fail sign on Trace9 and Trace13 (item 2 in Figure 7-1).

**Cable Absolute Impedance Limit Line**

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max</td>
<td>0.3 ns</td>
<td>0.9 ns</td>
<td>110 Ohm</td>
<td>110 Ohm</td>
</tr>
<tr>
<td>Min</td>
<td>0.3 ns</td>
<td>0.9 ns</td>
<td>90 Ohm</td>
<td>90 Ohm</td>
</tr>
</tbody>
</table>
7.2.3. SI-03 Cable Pair Matching

**Purpose:** To verify that the maximum and minimum cable impedance value of each single ended channel is matched within the conformance limits.

**References:** [1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.8.3.

**Last Modification:** November 11, 2010 (Version 1.00RC)

**Test Procedure:**

Assuming the initial setup/calibration procedures in chapter 6 have been performed, the measurement for this test is as follows:

1. Connect the test fixture to the test cables according to the Table 7-3. Unused test ports should be terminated.

   **Table 7-3: Cable Connection**

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixture PIN Number</td>
<td>A Tx+</td>
<td>A Tx-</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
<tr>
<td>B Tx+</td>
<td>B Tx-</td>
<td>A Rx+</td>
<td>A Rx-</td>
<td></td>
</tr>
</tbody>
</table>

   Note: A and B represent each one of the test fixtures.

2. Connect SATA cable to the test fixture.

3. Press **Channel Next** key to select Channel1.

4. Press **Channel Max** key to enlarge Channel1.

5. Click **Stop Single** for Time Domain measurement.

**Observable Results:**

Read the marker values on Trace2, Trace6, Trace10, and Trace14. (item3 in Figure 7-1)

If all conditions shown below are satisfied, then pass. Otherwise fail.

- \((\text{Marker1 on Trace2}) - (\text{Marker1 on Trace6}) < +5 \text{ Ohm,}\)
- \((\text{Marker2 on Trace2}) - (\text{Marker2 on Trace6}) < +5 \text{ Ohm,}\)
- \((\text{Marker1 on Trace10}) - (\text{Marker1 on Trace14}) < +5 \text{ Ohm,}\)
- \((\text{Marker2 on Trace10}) - (\text{Marker2 on Trace14}) < +5 \text{ Ohm.}\)
7.2.4. SI-04 Common Mode Impedance

Purpose: To verify that the common mode impedance of the DUT is within the conformance limits.


Last Modification: November 11, 2010 (Version 1.00RC)

Test Procedure:

Assuming the initial setup/calibration procedures in chapter 6 have been performed, the measurement for this test is as follows:

1. Connect the test fixture to the test cables according to the Table 7-4. Unused test ports should be terminated.

Table 7-4: Cable Connection

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixture PIN Number</td>
<td>A Tx+</td>
<td>A Tx-</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
<tr>
<td></td>
<td>B Tx+</td>
<td>B Tx-</td>
<td>A Rx+</td>
<td>A Rx-</td>
</tr>
</tbody>
</table>

Note: A and B represent each one of the test fixtures.

2. Connect SATA cable to the test fixture.

3. Press Channel Next key to select Channel1.

4. Press Channel Max key to enlarge Channel1.

5. Click Stop Single for Time Domain measurement.

Observable Results:

Read Pass/Fail sign on the Trace3 and Trace7. (item4 in Figure 7-1)

Common Mode Impedance Limit Line

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max</td>
<td>0.3 ns</td>
<td>0.9 ns</td>
<td>40 Ohm</td>
<td>40 Ohm</td>
</tr>
<tr>
<td>Min</td>
<td>0.3 ns</td>
<td>0.9 ns</td>
<td>25 Ohm</td>
<td>25 Ohm</td>
</tr>
</tbody>
</table>
7.2.5. SI-05 Differential Rise Time

**Purpose:** To verify that the differential rise time of the DUT is within the conformance limits.

**References:** [1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.8.5.

**Last Modification:** November 11, 2010 (Version 1.00RC)

**Test Procedure:**

Assuming the initial setup/calibration procedures in chapter 6 have been performed, the measurement for this test is as follows:

1. Connect the test fixture to the test cables according to the Table 7-5. Unused test ports should be terminated.

**Table 7-5: Cable Connection**

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixture PIN Number</td>
<td>A Tx+</td>
<td>A Txb-</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
<tr>
<td></td>
<td>B Tx+</td>
<td>B Txb-</td>
<td>A Rx+</td>
<td>A Rx-</td>
</tr>
</tbody>
</table>

Note: A and B represent each one of the test fixtures.

2. Connect SATA cable to the test fixture.

3. Press **Channel Next** key to select Channel1.

4. Press **Channel Max** key to enlarge Channel1.

5. Click **Stop Single** for Time Domain measurement.

**Observable Results:** Read the rise time on the Trace4. (item5 in Figure 7-1)

<table>
<thead>
<tr>
<th>Internal SATA cable</th>
<th>If the rise time &lt; 85 ps, then pass. Otherwise fail.</th>
</tr>
</thead>
<tbody>
<tr>
<td>eSATA cable</td>
<td>If the rise time &lt; 150 ps, then pass. Otherwise fail.</td>
</tr>
</tbody>
</table>
7.2.6. SI-06 Intra-Pair Skew

**Purpose:** To verify that the differential rise time of the DUT is within the conformance limits.

**References:** [1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.8.6.

**Last Modification:** November 11, 2010 (Version 1.00RC)

**Test Procedure:**

Assuming the initial setup/calibration procedures in chapter 6 have been performed, the measurement for this test is as follows:

1. Connect the test fixture to the test cables according to the Table 7-6. Unused test ports should be terminated.

**Table 7-6: Cable Connection**

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixture PIN Number</td>
<td>A Tx+</td>
<td>A Tx-</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
<tr>
<td></td>
<td>B Tx+</td>
<td>B Tx-</td>
<td>A Rx+</td>
<td>A Rx-</td>
</tr>
</tbody>
</table>

Note: A and B represent each one of the test fixtures.

2. Connect SATA cable to the test fixture.

3. Press **Channel Next** key to select Channel1.

4. Press **Channel Max** key to enlarge Channel1.

5. Click **Stop Single** for Time Domain measurement.

**Observable Results:** Read the delta time between Trace8 and Trace12. (item6 in Figure 7-1)

<table>
<thead>
<tr>
<th>Internal SATA cable</th>
<th>If the delta time &lt; 10 ps, then pass. Otherwise fail.</th>
</tr>
</thead>
<tbody>
<tr>
<td>eSATA cable</td>
<td>If the delta time &lt; 20 ps, then pass. Otherwise fail.</td>
</tr>
</tbody>
</table>
7.2.7. SI-07 Insertion Loss

**Purpose:** To verify that the insertion loss of the DUT is within the conformance limits.

**References:** [1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.8.7.

**Last Modification:** November 11, 2010 (Version 1.00RC)

**Test Procedure:**

Assuming the initial setup/calibration procedures in chapter 6 have been performed, the measurement for this test is as follows:

1. Connect the test fixture to the test cables according to the Table 7-7. Unused test ports should be terminated.

**Table 7-7: Cable Connection**

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixture PIN Number</td>
<td>A Tx+</td>
<td>A Tx-</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
<tr>
<td></td>
<td>B Tx+</td>
<td>B Tx-</td>
<td>A Rx+</td>
<td>A Rx-</td>
</tr>
</tbody>
</table>

Note: A and B represent each one of the test fixtures.

2. Connect SATA cable to the test fixture.

3. Press **Channel Next** key to activate Channel2.

4. Press **Trigger > Single** for Frequency Domain measurement.

![Figure 7-2: Measurement example of SI-07](image)

**Observable Results:** Read Pass/Fail sign on Trace1 (item1 in Figure 7-2).
**Insertion Loss Limit Line (Internal SATA)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>10 MHz</td>
<td>4.5 GHz</td>
<td>-6 dB</td>
<td>-6 dB</td>
</tr>
</tbody>
</table>

**Insertion Loss Limit Line (eSATA)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>10 MHz</td>
<td>4.5 GHz</td>
<td>-8 dB</td>
<td>-8 dB</td>
</tr>
</tbody>
</table>
7.2.8. SI-08 Differential to Differential Crosstalk: NEXT

**Purpose:** To verify that the differential to differential crosstalk the DUT is within the conformance limits.

**References:** [1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.8.8.

**Last Modification:** November 11, 2010 (Version 1.00RC)

**Test Procedure:**

Assuming the initial setup/calibration procedures in chapter 6 have been performed, the measurement for this test is as follows:

1. Connect the test fixture to the test port cables according to the Table 7-8: Cable Connection. Unused test ports should be terminated.

**Table 7-8: Cable Connection**

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixture PIN Number</td>
<td>A Tx+</td>
<td>A Tx-</td>
<td>A Rx+</td>
<td>A Rx-</td>
</tr>
<tr>
<td></td>
<td>B Tx+</td>
<td>B Tx-</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
</tbody>
</table>

Note: A and B are the fixture identifiers.

2. Connect SATA cable to the test fixture.


![Measurement Example of SI-08](image)

**Observable Results:** Read the pass/fail sign on Trace2 (item 1 in Figure 7-3).
## Differential to Differential Crosstalk: NEXT Limit Line

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max</td>
<td>10 MHz</td>
<td>4.5 GHz</td>
<td>-26 dB</td>
<td>-26 dB</td>
</tr>
</tbody>
</table>
7.2.9. SI-09 Inter-Symbol Interference

**Purpose:** To verify that the mated connector impedance of the DUT is within the conformance limits.

**References:** [1] SATA Interoperability Program Revision 1.4 Unified Test Document, Section 2.8.1.

**Last Modification:** November 11, 2010 (Version 1.00RC)

**Test Procedure:**

Eye diagram test is performed with the lone-bit pattern (LBP)\(^1\). The LBP bit pattern file can be downloaded from [www.agilent.com/find/ena-tdr_sata-si](http://www.agilent.com/find/ena-tdr_sata-si). Assuming the initial setup/calibration procedures in chapter 6 have been performed, the measurement for this test is as follows:

1. Connect the test fixture to the test cables according to the Table 7-9. Unused test ports should be terminated.

**Table 7-9: Cable Connection**

<table>
<thead>
<tr>
<th>ENA Port Number</th>
<th>Port1</th>
<th>Port2</th>
<th>Port3</th>
<th>Port4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixture PIN Number</td>
<td>A Tx+</td>
<td>A TxB</td>
<td>B Rx+</td>
<td>B Rx-</td>
</tr>
<tr>
<td></td>
<td>B Tx+</td>
<td>B TxB</td>
<td>A Rx+</td>
<td>A Rx-</td>
</tr>
</tbody>
</table>

Note: A and B represent each one of the test fixtures.

2. Connect SATA cable to the test fixture.

3. Press Channel Next key to select Channel1.

4. Press Channel Max key to enlarge Channel1.

5. Click Stop Single for Time Domain measurement.


7. Open Eye/Mask tab.

8. Click User Pattern button, then Bit Pattern Editor appears.

9. Click Load button and specify the LBP bit pattern file with the dialog box.

10. Click Close button.

11. Click Draw Eye button.

---

\(^1\) The LBP is comprised of the repetition of the following bit pattern, resulting in a bit length of 2048. 0011 0110 1111 0100 0010 0011 0110 1111 0011 0101 0011 0100 1101 0011 0101 0011 0100 1100
Figure 7-4: Measurement Example of SI-09

Observable Results:

Read Jitter p-p on the eye diagram (item1 in Figure 7-4). If Jitter p-p < 50 ps, then pass. Otherwise fail.
8. Appendix

7.5.1. Starting Setup
1. If TDR setup wizard was appeared, click Close button in the TDR setup wizard.
2. Open Setup tab (item1).
3. Click Preset (item2) under Basic to preset the E5071C.
4. A dialog box appears requesting for confirmation. Then click OK.
5. Set DUT Topology (item3) to “Single-Ended 4-Port”.
6. Click Advanced Mode (item4).
7. A dialog box appears requesting for confirmation. Then click Yes. (Clear the check box for “Use Advanced Calibration Methods”)

7.5.2. Mated Connector Impedance
1. Click Stop Single.
2. Open TDR/TDT tab.
3. Open Trace Control tab.
4. Clear Time and Marker check box under Coupling.
5. Select Trace1.
6. Open Parameters tab.
7. Set Measure to “Differential”.
8. Set Rise Time to 70 psec (20-80%).
9. Click the box below the left knob under Horizontal.
10. Input 100 psec/div with the Entry dialog box.
11. Click the box below the right knob under Horizontal.
12. Input -100 psec with the Entry dialog box.
13. Click the box below the left knob under Vertical.
14. Input 5 Ohm/div with the Entry dialog box
15. Click the box below the right knob under Vertical.
16. Input 75 Ohm with the Entry dialog box
17. Open Trace Control tab.
18. Click Trace Settings Copy button. Then Trace Settings Copy dialog box appears.
19. Select Trace1 in the From list.
20. Select Trace5 in the To list.
21. Click Copy.
22. Click Close.
23. Select Trace5.
24. Open Parameters tab.
25. Click Tdd22 in the table.

7.5.3. Cable Absolute Impedance
1. Open Trace Control tab.
2. Click Trace Settings Copy button. Then Trace Settings Copy dialog box appears.
3. Select Trace1 in the From list.
4. Select Trace9 in the To list.
5. Click Copy.
6. Select Trace5 in the From list.
7. Clear Trace9 and select Trace13 in the To list.
8. Click Close.

7.5.4. Cable Pair Matching

1. Select Trace2.
2. Open Parameters tab.
3. Set Measure to “Time Domain”.
4. Set Rise Time to 70 psec (20-80%).
5. Click the box below the left knob under Horizontal.
6. Input 50 psec/div with the Entry dialog box.
7. Click the box below the right knob under Horizontal.
8. Input 300 psec with the Entry dialog box.
9. Click the box below the left knob under Vertical.
10. Input 10 Ohm/div with the Entry dialog box.
11. Click the box below the right knob under Vertical.
12. Input 0 Ohm with the Entry dialog box.
13. Click Maker menu and select 1.
14. Click Maker Search menu and Select Max.
15. Click Maker menu and select 2.
16. Click Maker Search menu and Select Min.
17. Open Trace Control tab.
18. Click Trace Settings Copy button. Then Trace Settings Copy dialog box appears.
19. Select Trace2 in the From list.
20. Select Trace6, Trace10, and Trace14 in the To list.
21. Click Copy.
22. Click Close.
23. Open Parameters tab.
25. Click T22 in the table.
27. Click T33 in the table.
29. Click T44 in the table.

7.5.5. Common Mode Impedance

1. Select Trace3.
2. Set Measure to “Differential”.
3. Set Format to “Impedance”.
4. Select Tcc11 in the table.
5. Set Rise Time to 70 psec (20-80%).
6. Press Display > Equation Editor… > Enter an equation “CMI1= S11+S12”.
7. Check Equation Enabled check box.
8. Click Apply.
9. Click Close.
10. Click the box below the left knob under Horizontal.
11. Input 100 psec/div with the Entry dialog box.
12. Click the box below the right knob under Horizontal.
13. Input -100 psec with the Entry dialog box.
14. Click the box below the left knob under Vertical.
15. Input 5 Ohm/div with the Entry dialog box
16. Click the box below the right knob under Vertical.
17. Input 10 Ohm with the Entry dialog box
18. Open Trace Control tab.
19. Click Trace Settings Copy. Then Trace Settings Copy dialog box appears.
20. Select Trace3 in the From list.
21. Select Trace7, Trace11, Trace15 in the To list.
22. Click Copy.
23. Click Close.
25. Press Display > Equation Editor… > Enter an equation “CMI2= S22+S21”.
26. Repeat step7 to step9.
27. Select Trace11.
28. Press Display > Equation Editor… > Enter an equation “CMI3= S33+S34”.
29. Repeat step7 to step9.
30. Select Trace15.
31. Press Display > Equation Editor… > Enter an equation “CMI4= S44+S43”.
32. Repeat step7 to step9.

7.5.6. Differential Rise Time
1. Select Trace4.
2. Set Measure to “Time Domain” and “Differential”.
3. Set Format to “Volt”.
4. Select Tdd21 in the table.
5. Set Rise Time to 35 psec (20-80%).
6. Click the box below the left knob under Horizontal. Then Entry dialog box appears.
7. Input horizontal scale to 2 ns/div.
8. Click the box below the right knob under Horizontal. Then Entry dialog box appears.
9. Input horizontal position to -1 ns.
10. Click the box below the left knob under Vertical. Then Entry dialog box appears.
11. Input vertical scale to 100 mV/div.
12. Click the box below the right knob under Vertical. Then Entry dialog box appears.
13. Input vertical position to 200 mV.
14. Click Marker Search menu and select Rise Time (20-80%).
7.5.7. Intra-Pair Skew

1. Select **Trace8**.
2. Set **Measure** to “Time Domain”.
3. Set **Format** to “Volt”.
4. Select **T31** in the table.
5. Set **Rise Time** to 35 psec (20-80%).
6. Click the box below the left knob under Horizontal. Then Entry dialog box appears.
7. Input horizontal scale to 2 ns/div.
8. Click the box below the right knob under Horizontal. Then Entry dialog box appears.
9. Input horizontal position to -1 ns.
10. Click the box below the left knob under Vertical. Then Entry dialog box appears.
11. Input vertical scale to 50 mV/div.
12. Click the box below the right knob under Vertical. Then Entry dialog box appears.
13. Input vertical position to 100 mV.
14. Open **Trace Control** tab.
15. Click **Trace Settings Copy**. Then Trace Settings Copy dialog box appears.
16. Select the **Trace8** in the From list.
17. Select the **Trace12** in the To list.
18. Click **Copy**.
19. Click **Close**.
20. Select **Trace12**.
21. Open **Parameters** tab.
22. Select **T42** in the table.
23. Select **Trace8**.
24. Click **Marker Search** menu and select **Δ Time**. Then Delta Time dialog box appears.
25. Check **Δ Time** check box.
26. Set **Target (Stop)** to “Trace12 (T42)”.
27. Click **OK**.
28. Press **Display** > **Equation Editor**... > Enter an equation “\(\text{Intra} = S31-S32\)”.
29. Check **Equation Enabled** check box.
30. Click **Apply**.
31. Click **Close**.
32. Select **Trace12**.
33. Press **Display** > **Equation Editor**... > Enter an equation “\(\text{Intra} = S42-S41\)”.
34. Check **Equation Enabled** check box.
35. Click **Apply**.
36. Click **Close**.
37. Select **Trace16**.
38. Click **Data Mem** and select **Off**.

7.6. **Manual Setup for Eye Diagram Measurement**

1. Open **Eye/Mask** tab.
2. Set Bit Pattern **Data Rate** to 3 Gbps.
3. Set Bit Pattern **Rise Time** to 133 ps (20-80%).
4. Set Bit Pattern **Type** to “USER”.

7.7. **Manual Setup for Frequency Domain Measurement**

7.7.1. **Channel and Trace Settings**

1. Press **Display**.
2. Click **Allocate Channels** > 
3. Press **Channel Next**.
4. Click **Num of Traces** > 2.
5. Click **Allocate Traces** > 

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7.7.2. Common Settings

1. Press **Sweep Setup > Sweep Type > Lin Freq.**
2. Set **Points** to 201.
3. Press **Start > Set start value to 10 MHz.**
4. Press **Stop > Set stop value to 4.5 GHz.**
5. Press **Avg > Set IF Bandwidth to 10 kHz.**
6. Press **Analysis > Fixture Simulator > Fixture Simulator** and turn it ON.

7.7.3. Insertion Loss Measurements

1. Press **Trace Next** to select Trace1.
2. Click **Topology > Device > Bal-Bal.**
3. Click **Port1 (bal) > 1-2.**
4. Click **Port2 (bal) > 3-4.**
5. Click **Return.**
6. Click **BalUn** and turn it ON.
7. Click **Measurement > Sdd21.**
8. Press **Scale.**
9. Set **Scale/Div** to 5 dB/div.
10. Set **Reference position** to 9 Div.

7.7.4. Differential to Differential Crosstalk: NEXT

1. Press **Trace Next.**
2. Press **Analysis > Fixture Simulator > BalUn** and turn it ON.
3. Click **Measurement > Sdd21.**
4. Press **Scale.**
5. Set **Scale/Div** to 10 dB/div.
7.8. Limit Test Settings

7.8.1. Displaying Judgment Result of Test

If a channel has a judgment result of fail, the fail message appears on the screen. It will be judged as failed if one or more unsatisfactory trace exists within the channel.

Follow the procedure below.

1. Press Analysis > Limit Test > Fail Sign to switch the fail sign ON/OFF.

7.8.2. Setting the Warning Beeper

Beep sound that occurs when the judgment result is fail. Follow the procedure below.

1. Press System > Misc Setup > Beeper > Beep Warning to switch the warning beeper ON/OFF.

7.8.3. Defining the Limit Line

Set limit lines to perform pass/fail tests on the following measurement items.
- Mated Connector Impedance (Trace1, 5 in Channel1)
- Cable Absolute Impedance (Trace1, 5 in Channel1)
- Common Mode Impedance (Trace3, 7 in Channel1)
- Insertion Loss (Trace1 in Channel2)
- Differential to Differential Crosstalk: NEXT (Trace2 in Channel2).

1. Press Channel Next key and Trace Next key to activate the trace on which limit lines should be set.

2. Press Analysis > Limit Test > Edit Limit Line to display the limit table shown below (Initially, no segments are entered in the limit table). Using the limit table, create/edit a segment.

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0 s</td>
<td>600 ps</td>
<td>1.05 u</td>
<td>1.05 u</td>
</tr>
<tr>
<td>2</td>
<td>0 s</td>
<td>600 ps</td>
<td>75 u</td>
<td>75 u</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3. Enter the limit line data following the tables below.

4. Click **Return**.

5. Click **Limit Line** and turn it **ON**.

6. Click **Limit Test** and turn it **ON**.

7. Repeat 1 to 6 for each Measurement items.
### Mated Connector Impedance Limit Line

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max</td>
<td>-0.1 ns</td>
<td>0.3 ns</td>
<td>115 Ohm</td>
<td>115 Ohm</td>
</tr>
<tr>
<td>Min</td>
<td>-0.1 ns</td>
<td>0.3 ns</td>
<td>85 Ohm</td>
<td>85 Ohm</td>
</tr>
</tbody>
</table>

### Cable Absolute Impedance Limit Line

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max</td>
<td>0.3 ns</td>
<td>0.9 ns</td>
<td>110 Ohm</td>
<td>110 Ohm</td>
</tr>
<tr>
<td>Min</td>
<td>0.3 ns</td>
<td>0.9 ns</td>
<td>90 Ohm</td>
<td>90 Ohm</td>
</tr>
</tbody>
</table>

### Common Mode Impedance Limit Line

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max</td>
<td>0.3 ns</td>
<td>0.9 ns</td>
<td>40 Ohm</td>
<td>40 Ohm</td>
</tr>
<tr>
<td>Min</td>
<td>0.3 ns</td>
<td>0.9 ns</td>
<td>25 Ohm</td>
<td>25 Ohm</td>
</tr>
</tbody>
</table>

### Insertion Loss Limit Line (Internal SATA)

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>10 MHz</td>
<td>4.5 GHz</td>
<td>-6 dB</td>
<td>-6 dB</td>
</tr>
</tbody>
</table>

### Insertion Loss Limit Line (eSATA)

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
<td>10 MHz</td>
<td>4.5 GHz</td>
<td>-8 dB</td>
<td>-8 dB</td>
</tr>
</tbody>
</table>

### Differential to Differential Crosstalk: NEXT Limit Line

<table>
<thead>
<tr>
<th>Type</th>
<th>Begin Stimulus</th>
<th>End Stimulus</th>
<th>Begin Response</th>
<th>End Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max</td>
<td>10 MHz</td>
<td>4.5 GHz</td>
<td>-26 dB</td>
<td>-26 dB</td>
</tr>
</tbody>
</table>