ADS Interoperability for RFIC Design with ADS2016.01

Updated January 5, 2016
### Keysight EDA Silicon RFIC Design Solution

**Small-scale RFIC**

<table>
<thead>
<tr>
<th>LDMOS</th>
<th>IPD</th>
<th>SiGe</th>
<th>BiCMOS</th>
<th>CMOS-SOI</th>
<th>RF-CMOS</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25u</td>
<td></td>
<td></td>
<td>0.13u</td>
<td></td>
<td></td>
<td>14n</td>
</tr>
</tbody>
</table>

**Large-scale RFIC**

- **ADS**
  - ADS front-to-back
    - User performs complete circuit design to tape-out within ADS platform (using 3rd-party DRC sign-off tool)

- **Interoperable Flow & Solutions**
  - ADS front-end & EM for RFIC and beyond
    - User performs front-end and EM block design in ADS, but moves to Virtuoso for layout implementation

- **Virtuoso**
  - Virtuoso-based Flow
    - User runs (Keysight) RF circuit and EM simulation within the Virtuoso platform

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[Image of ADS front-to-back process]

[Image of Virtuoso-based Flow]

http://www.keysight.com/find/eosof-rfic-design
Solving complex SiRF IC design challenges while working seamlessly of a single ADS / Virtuoso OA library

- Schematic and layout design optimization in ADS on OA library (EM & ETH-cosim, module and system level).
- Improved design efficiency and faster time to market while using RF-centric design tools at a competitive cost.
Tight integration of ADS schematic interoperable PDK with Momentum substrate for seamless OA schematic design and EM-co-simulation on RF subsystems in the ADS/Virtuoso environment.

- Supported by 7 silicon foundries
- 16 PDKs available w/ coverage increasing in 2016
- New Momentum capabilities to support efficient simulation of silicon:
  - Via Simplification
  - Dummy Fill support
  - Substrate Parameterization
  - EM-co-simulation
  - iRCX import utility for TSMC processes
- New Si RFIC design flow improvements:
  - Improved DC annotation & Schematic Design Environment
  - Support of Config Views
  - SiRF-centric utility to generate dummy metal fill
- Momentum/FEM for true multi-technology and module simulation on interoperable designs

Typical Interoperability PDK Library:

Libraries w/ Virtuoso primitive symbols

ADS PDK
(AEL functions equivalent for Virtuoso PDK devices)

Momentum substrate
Improved Schematic Design Environment in ADS2016.01

ADS2016.01 Provides the DC annotation capability expected from RFIC designers to permit interactive debug of complex RFIC designs.

Virtuoso

ADS w/ Virtuoso look-alike DC annotation

Schematic Design Improvements:
- DC Annotation
- Enhanced analogLib
- Wire editing and schematic layer display
- Schematic area pin support
- VerilogA support
- Schematic Pcells
- Config Views

Display of DC annotation & CDF defined device parameters
Use Express Pcell function in Virtuoso to generate cached layout data from skill code layout pcells. This data can be read in ADS but not modified.

- ADS/Virtuoso schematic interoperable PDK
  Tech file, layer mapping and display setup through PDK

- ADS w/o PDK
  Create tech file using utility

Use “createTechnology” utility to create matching techfile for ADS!
EM Co-simulation in ADS2016.01

Improve accuracy and first time silicon success on RF block designs through Momentum EM Co-simulation. Account for interconnects between devices and replace inaccurate Spice models where needed with EM simulations to obtain an accurate S-parameter result on an integrated RF block.

Partition of inductors and MIM caps as circuit (Spice) devices and interconnect lines for EM simulation

- **blue/magenta** curve (Co-simulation on circuit / EM partition)
- **black** curve (schematic simulation, ignoring the interconnections)
The new substrate stack parameterization in Momentum allows the designer to explore the effect of process corners on devices and design. This approach is far superior to the classical Spice corner analysis which is only narrowly valid for the particular figure of merit that the corner case was optimized for.
MIM Cap Simulation in Momentum

Momentum offers the derived layer approach to model “short” vias. These vias use the same layout layer that connects inter metal, however stop short due to presence of a MIM electrode or gate poly silicon. Easy to use setup for Momentum simulation on layout data as is.

Derived layers setup to model short via to mimcap top electrode:

<table>
<thead>
<tr>
<th>Via</th>
<th>Layer</th>
<th>Conductor</th>
</tr>
</thead>
</table>
| via3_original | M3   | SBC1... meta3 via3_original meta3
| via3_mimcap | M4   | Conductor meta4 via3_mimcap topmm2 AND(via3, “topmm”) |
| via4_original | M4   | SBC1... meta4 via4_original meta4
| via4_mimcap | M5   | Conductor meta5 via4_mimcap topmm2 AND(via4, “topmm”) |
Via Simplification in ADS2016.01

The Momentum Preprocessor offers a choice of different via array simplifications to support an efficient simulation without the need of manual layout manipulation. Use Momentum 3D layout view to inspect the result and achieve the appropriate level of simplification. Maintain individual via shapes at “via limited” connections to guarantee uncompromised EM accuracy.

- OA via array: Envelop OA via array into single block
- Local via array: Envelop any via array into single block
- Local via stack: Envelop any via array into single block and extend for zero metal overlap

OA via arrays are merged, while pcell vias (non-OA vias) are left individually
Merge OA and non-OA via arrays
Via arrays blocks are extended for zero metal overlap
Momentum allows the designer to leave dummy metal fill in the
design and simulate the effect at no added simulation expense in
time through either choosing the “equivalent dielectric” model or
by ignoring the fill shapes.

- **Unrelated metal** = dummy metal fill
  - **blue/magenta** curve (remove unrelated metal)
  - **black** curve (keep unrelated metal via equivalent dielectric
    model in Momentum)

This design uses a “smart” placement of dummy fills via the new
dummy fill utility. Hence the effect on insertion loss and return loss
of diplexer is minimal.
Momentum iRCX Import Utility in ADS2016.01

Substrate Editor -> Import iRCX

Use substrate file either in ADS or in Virtuoso

Provide TSMC iRCX file & Cadence PDK tech file

Generate a Momentum stack-up on the fly for any TSMC process. No expert user required to setup EM simulations.

Video Tutorial Coming Soon!

Validated TSMC Technologies:

<table>
<thead>
<tr>
<th>TSMC Technology</th>
<th>Metal Variant</th>
</tr>
</thead>
<tbody>
<tr>
<td>28nm(CLN28HPM)</td>
<td>1P9M_5X3Z+UT_AIRDL</td>
</tr>
<tr>
<td></td>
<td>1P10M_5X2Y2Z+UT_AIRDL</td>
</tr>
<tr>
<td></td>
<td>1P8M_5X2Z+UT_AIRDL</td>
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<tr>
<td>28nm(CRN28HPL)</td>
<td>1P7M+UT-ALRDL_4X1Z1U</td>
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<tr>
<td>40nm(CRN40LP)</td>
<td>1P9M_6X1Z1U_AIRDL</td>
</tr>
<tr>
<td>55nm(CMN55ULP)</td>
<td>1P7M+UT-ALRDL_4X1Z1U</td>
</tr>
<tr>
<td>55nm(CMN55LP)</td>
<td>1P6M+UT-ALRDL_4X1U</td>
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<tr>
<td>65nm(CRN65LP)</td>
<td>1P9M_4X1Z1U_AIRDL</td>
</tr>
<tr>
<td>65nm(CLN65G)</td>
<td>1P7M_4X2Z_AIRDL</td>
</tr>
<tr>
<td>90nm(CRN90LP)</td>
<td>1P9M+ALRDL_6X1Z1U</td>
</tr>
<tr>
<td>180nm(CR018SOI)</td>
<td>1P4M+ALRDL_1X2U</td>
</tr>
</tbody>
</table>
**New Advanced Layout Feature ADS2016.01**

**Problem Statement:**

Meeting metal density requirements for small silicon RFIC chips with large keep-out regions for metal fills, in order to not affect RF performance, is a well-known challenge. The issue is exacerbated as the metal fill addition is usually accomplished at the very end of the layout design process prior to mask generation, when it is difficult to change the layout design. Hence a tool that is easily and interactively used during the design process, will significantly ease the pain of meeting the tape-out target for an silicon RFIC with required metal density.

**New Area Fill Utility:**

This new utility provides the designer and layout engineer an easy to use tool to generate dummy metal fills for silicon RFIC chips in ADS prior to tape-out. The designer can quickly generate the area metal fill in a circuit block or entire chip, tailor it to the required metal density requirements and validate its effects on the circuitry with Momentum early in the design process. Metal fill effects and potential degradation of the chip are recognized early by the designer, rather than experienced late in the stage or in the worst case after silicon ships. Furthermore, the layout fill data is generated hierarchically and is available through interoperability for use in other EDA platforms.

- Available as add-on utility to ADS 2016.01
- Requires Advanced Layout License (W2320)
- Works with any OA ADS native or ADS interoperable PDK / IPL iPDK
- Dummy fill layout is created hierarchically and available in ADS or Virtuoso through interoperability.
Metal Fill Example on SP9T Antenna Switch

Medium complexity RFIC of size 1.1 x 1.4mm

Total time needed to tailor and generate metal fills ~ 10 mins

Area Fill Utility

Metal Densities on all layers in spec, ranging between 25% - 36%

~ 70000 shapes of dummy metal fill added to the circuit

CMOS SOI SP9T Antenna Switch provided by TowerJazz

DRC Clean
Interoperability Design Example – Wifi Diplexer

Shared OA Library between ADS and Virtuoso

Video Tutorial Coming Soon!

Title: How to Optimize a SiRF Design for Tape-Out.
Interoperability Design Example – TowerJazz SPDT

Co-Simulation of Silicon, QFN package and wire bonds

Video Tutorial Coming Soon!
Title: How to Accurately Simulate Channel Isolation in SiRF Antenna Switches.

Gives accurate Insertion Loss and Linearity.

Gives accurate Insertion Loss, Linearity and Isolation.
New iPDK Support with ADS2016

- iPDKs are compatible with any OpenAccess-compliant EDA tool
- TCL callbacks
- PyCells for device layout Pcells
- Foundry iPDKs available from AMS, Xfab, Lfoundry, ST Microelectronics and TSMC

Advantages of iPDK in ADS

- Leveraging the interoperability concept beyond Virtuoso SKILL code PDKs
- Bringing ADS faster to processes supported with a foundry iPDK
- New processes, advanced TSMC tech nodes, power-management etc. available now in ADS
- Full suite of ADS tools available for designs using an iPDK.

White Paper Coming Soon!

Title: What is an ADS iPDK.
Foundry – Silicon PDK Support Roster

[Image of the Keysight Technologies website page showing Silicon Foundry PDKs]

http://www.keysight.com/find/eosof-silicon-foundry-pdks
Foundry - ADS/Virtuoso Interoperable PDKs

<table>
<thead>
<tr>
<th>Foundary</th>
<th>Interoperable PDKs with ADS 2015.01</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOWERJAZZ</td>
<td>SBC18HA, CS13/18, SBC18H3, SBCQE1</td>
</tr>
<tr>
<td>GLOBALFOUNDRIES</td>
<td>40nm LP-RF, 130nm SOI, 65nm LPe-RF</td>
</tr>
<tr>
<td>IBM</td>
<td>BiCMOS 5PAe, CSOI7SW</td>
</tr>
<tr>
<td>TSMC</td>
<td>SOI 180nm v0.5a, SOI 180nm v1.3a, CRN65GP</td>
</tr>
<tr>
<td>IBM</td>
<td>SGB25V, SG13S</td>
</tr>
<tr>
<td>FUJITSU</td>
<td>Fujitsu 55nm</td>
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<table>
<thead>
<tr>
<th>Platform Specific</th>
<th>Standard Virtuoso PDK</th>
<th>ADS/Virtuoso Interoperable PDK</th>
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<tbody>
<tr>
<td>Callbacks &amp; custom netlist procedures</td>
<td>Skill</td>
<td>Lisp</td>
</tr>
<tr>
<td>Layout Pcells</td>
<td>Skill</td>
<td>OA Express Pcell</td>
</tr>
</tbody>
</table>

Schematic interoperability with Virtuoso PDK to facilitate use of ADS in RFIC design flow. Read layout in ADS for EM or multi-technology co-simulation and design post processing (dummy metal fill, DRC).
# Foundry – ADS IPL Interoperable PDKs (iPDK)

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<th>ADS IPL iPDK</th>
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<tr>
<td>Callbacks &amp; custom netlist procedures</td>
<td>Skill</td>
<td>TCL + AEL</td>
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<tr>
<td>Layout Pcells</td>
<td>Skill</td>
<td>Python</td>
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## iPDKs with ADS 2016.01

<table>
<thead>
<tr>
<th>Foundry</th>
<th>IPDKs</th>
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<tbody>
<tr>
<td>TOWERJAZZ</td>
<td>TS018PM</td>
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<tr>
<td>amii</td>
<td>S35, HK410, C35, HK410, H35, HK410</td>
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<tr>
<td>ST</td>
<td>C28FDSOI</td>
</tr>
<tr>
<td>LFoundry</td>
<td>LF15A</td>
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<tr>
<td>X FAB</td>
<td>XP018</td>
</tr>
<tr>
<td>TSMC</td>
<td>CLN28HPC, TN40CM</td>
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</tbody>
</table>

Use IPL iPDK for schematic design, EM co-simulation and design post processing (dummy metal fill, DRC) in ADS. Enable co-simulation and multi-technology simulation of RF with power management / control chip.