Keysight D9050PCIC PCIe Gen5 Compliance Application

KEYSIGHT TECHNOLOGIES

Programmer's Reference

Notices

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In This Book

This book is your guide to programming the Keysight Technologies D9050PCIC PCIe Gen5 Compliance Application.

- Chapter 1, “Introduction to Programming,” starting on page 7 describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 17, and Chapter 4, “Instruments,” starting on page 33 provide information specific to programming the D9050PCIC PCIe Gen5 Compliance Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, and 4 for changes.

Contents

1 Introduction to Programming

Remote Programming Toolkit / 8

This chapter introduces the basics for remote programming a compliance application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The D9050PCIC PCIe Gen5 Compliance Application uses Remote Interface Revision 6.00. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

2 Configuration Variables and Values

The following table contains a description of each of the D9050PCIC PCIe Gen5 Compliance Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Configure	Compliance Signal Check	EnableSignalCheck	1.0, 0.0	When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Configure	Force New Waveform Acquisition	ForceNewWfmAcq	1.0, 0.0	When force new waveform acquisition is enabled, it will keep on re-acquire new waveform regardless of required waveform existed or not.
Configure	Noise Reduction BW, GHz	EBW_16G	0.0, 50.0E+9, 25.0E+9, 20.0E+9, 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9, 5.5E+9, 5.0E+9, 4.5E+9, 4.0E+9, 3.5E+9, 3.0E+9, 2.5E+9, 2.0E+9, 1.5E+9, 1.0E+9	(Limited availability*) Specify the noise reduction bandwidth to use for all tests.
Configure	Noise Reduction BW, GHz	EBW_32G	0.0, 50.0E+9, 25.0E+9, 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9	(Limited availability*) Specify the noise reduction bandwidth to use for all tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Noise Reduction BW, GHz	EBW_5G	0.0, 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9, 5.5E+9, 5.0E+9, 4.5E+9, 4.0E+9, 3.5E+9, 3.0E+9, 2.5E+9, 2.0E+9, 1.5E+9, 1.0E+9	(Limited availability*) Specify the noise reduction bandwidth to use for all tests.
Configure	Noise Reduction BW, GHz	EBW_8G	0.0, 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9, 5.5E+9, 5.0E+9, 4.5E+9, 4.0E+9, 3.5E+9, 3.0E+9, 2.5E+9, 2.0E+9, 1.5E+9, 1.0E+9	(Limited availability*) Specify the noise reduction bandwidth to use for all tests.
Configure	Number of UI	NumUI_16G	(Accepts user-defined text), 8.0E+6, 2.0E+6, 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Number of UI	NumUI_32G	(Accepts user-defined text), 8.0E+6, 2.0E+6, 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Number of UI	NumUI_5G	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Number of UI	NumUI_8G	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Sample Rate, GSa/s	SRate_16G	160.0E+9, 80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 256.0E+9, 128.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Configure	Sample Rate, GSa/s	SRate_32G	160.0E+9, 80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 256.0E+9, 128.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Configure	Sample Rate, GSa/s	SRate_5G	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 256.0E+9, 128.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Sample Rate, GSa/s	SRate_8G	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 256.0E+9, 128.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Configure	Sample rate, GSa/s	ClockSR	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 5.0E+9, 2.0E+9, 1.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9, 5.0E+9, 5.0E+9, 1.0E+9	Select the sample rate to acquire reference clock signal.
Configure	Show Jitter Filter Plot	ShowJitterFilterPlot	0, 2, 3, 4, 5	Select the clock jitter plot to display. Generating plots will increase test runtime.
Configure	SigTest Version	Base_SigTestVer16GT	3.2.0, 3.2.0.1, 4.0.37, 4.0.39, 4.0.41, 4.0.46	Specify the version of the SigTest for 16.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	SigTest Version	Base_SigTestVer32GT	3.2.0, 3.2.0.1, 4.0.37, 4.0.39, 4.0.41, 4.0.46	Specify the version of the SigTest for 32.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	SigTest Version	Base_SigTestVer8GT	3.2.0, 3.2.0.1, 4.0.37, 4.0.39, 4.0.41, 4.0.46	Specify the version of the SigTest for 8.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	SigTest Version	Preset_SigTestVer16GT	3.2.0, 3.2.0.1, 4.0.37, 4.0.39, 4.0.41, 4.0.46	Specify the version of the SigTest for 16.0 GT/s Base Transmitter Tests (Equalization Preset Test). Setting is defined according to Data Rate.
Configure	SigTest Version	Preset_SigTestVer32GT	3.2.0, 3.2.0.1, 4.0.37, 4.0.39, 4.0.41, 4.0.46	Specify the version of the SigTest for 32.0 GT/s Base Transmitter Tests (Equalization Preset Test). Setting is defined according to Data Rate.
Configure	SigTest Version	Preset_SigTestVer8GT	3.2.0, 3.2.0.1, 4.0.37, 4.0.39, 4.0.41, 4.0.46	Specify the version of the SigTest for 8.0 GT/s Base Transmitter Tests (Equalization Preset Test). Setting is defined according to Data Rate.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Sine(x)/x Interpolation	SineXInterpolation	ON, OFF, INT1, INT2, INT4, INT8	Sine(x)/x Interpolation.
Configure	Stitch Method	StitchMethod	Absolute, Dynamic	Select the method to stitch the waveform for reference clock phase jitter test. Absolute method stitches the waveform based on absolute data. Dynamic method aligns waveform data to have common offset before stitching. This option only applies when Spread Sprectrum Clocking is enabled.
Configure	Trigger Pulse Width, s	TrigPulseWidth16G	8.0E-9, 7.0E-9, 6.0E-9, 5.0E-9	(Limited availability*) Specify the width in second for the Pulse Width Trigger setup.
Configure	Trigger Pulse Width, s	TrigPulseWidth32G	8.0E-9, 7.0E-9, 6.0E-9, 5.0E-9, 3.0E-9	(Limited availability*) Specify the width in second for the Pulse Width Trigger setup.
Configure	Trigger Pulse Width, s	TrigPulseWidth8G	8.0E-9, 7.0E-9, 6.0E-9, 5.0E-9	(Limited availability*) Specify the width in second for the Pulse Width Trigger setup.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 99	Specify N using the 'Minimum required margin %' control.
Set Up	Apply Device Definition Changes	ApplyChangesConfigVar	0.0, 1.0	Apply Device Definition Changes Apply Device Definition Changes
Set Up	ConnectionType	OptConnectionType	Single-Ended	Select Connection Type
Set Up	Device Name	DeviceName	(Accepts user-defined text)	Name for the DUT in testing Name for the DUT in testing
Set Up	DeviceDirectory	OfflineDeviceDirectoryName	New Device1	

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Enable Collective Data Acquisition	PresetWfmCollectiveAcqConfigVar	0.0, 1.0	Enable Collective Data Acquisition Enable Collective Data Acquisition
Set Up	Enable DUT Automation	DUT Automation	0.0, 1.0	Enable DUT Automation Enable DUT Automation
Set Up	Enable Workshop Compliance Mode	Workshop Compliance Mode	0.0, 1.0	Enable Workshop Compliance Mode Enable Workshop Compliance Mode
Set Up	Saved Files Directory	SavedFilesDirectory	(Accepts user-defined text)	Directory to save output files from Workshop Mode Test Directory to save output files from Workshop Mode Test
Set Up	Select 16.0 GT/s related tests	16.0 GT/s	0.0, 1.0	Select 16.0 GT/s related tests Select 16.0 GT/s related tests
Set Up	Select 2.5 GT/s related tests	2.5 GT/s	0.0, 1.0	Select 2.5 GT/s related tests Select 2.5 GT/s related tests
Set Up	Select 32.0 GT/s related tests	32.0 GT/s	0.0, 1.0	Select 32.0 GT/s related tests Select 32.0 GT/s related tests
Set Up	Select 5.0 GT/s related tests	5.0 GT/s	0.0, 1.0	Select 5.0 GT/s related tests Select 5.0 GT/s related tests
Set Up	Select 8.0 GT/s related tests	8.0 GT/s	0.0, 1.0	Select 8.0 GT/s related tests Select 8.0 GT/s related tests
Set Up	Select clock channel +	SingleEndedClockChannelPConfigVar		Select clock channel + Select clock channel +
Set Up	Select clock channel -	SingleEndedClockChannelNConfigVar		Select clock channel - Select clock channel -
Set Up	Select data channel +	SingleEndedDataChannelPConfigVar	ChannelR-1, ChannelR-3	Select data channel + Select data channel +
Set Up	Select data channel -	SingleEndedDataChannelNConfigVar	ChannelR-1, ChannelR-3	Select data channel - Select data channel -
Set Up	Select preset for 16.0 GT/s related tests	Preset16GConfigVar	(Accepts user-defined text), P00, P01, P02, P03, P04, P05, P06, P07, P08, P09, P10	Select preset for 16.0 GT/s related tests Select preset for 16.0 GT/s related tests

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Select preset for 32.0 GT/s related tests	Preset32GConfigVar	(Accepts user-defined text), P00, P01, P02, P03, P04, P05, P06, P07, P08, P09, P10	Select preset for 32.0 GT/s related tests Select preset for 32.0 GT/s related tests
Set Up	Select preset for 8.0 GT/s related tests	Preset8GConfigVar	(Accepts user-defined text), P00, P01, P02, P03, P04, P05, P06, P07, P08, P09, P10	Select preset for 8.0 GT/s related tests Select preset for 8.0 GT/s related tests
Set Up	Select the Reference Clock Type.	RefClkConfigVar	Clean Clock, SSC	Select the Reference Clock Type.
Set Up	Select the SRIS type.	SRISEnabledConfigVar	None, Enabled	Select the SRIS type.
Set Up	TestMode	OptTestMode	Analyze Captured Waveforms, Capture and Analyze Stored Waveforms	Select the test mode to be tested.
Set Up	TestPoint	TestPoint	Base - Transmitter Tests, Base - Reference Clock Tests	Select the PCIExpress device test point to be tested.
Set Up	TestPointPresetTest	TestPointPresetTest	0.0, 1.0	Select to run Preset Tests (Gen 3 and 4 Only).
Set Up	User Comment	UserComments	(Accepts user-defined text)	Additional comments for the DUT in testing. Additional comments for the DUT in testing.
*Limited availability: Availability of this setting depends upon the oscilloscope model and installed license options.				

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name — The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID — The number to use with the RunTests method.
- Description — The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application:

NOTE The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
Base Reference Clock Test (Workshop) (16.0 GT/s)	49001	
Base Reference Clock Test (Workshop) (2.5 GT/s)	19001	
Base Reference Clock Test (Workshop) (32.0 GT/s)	59001	
Base Reference Clock Test (Workshop) (5.0 GT/s)	29001	
Base Reference Clock Test (Workshop) (8.0 GT/s)	39001	
Base Tx Test (Workshop) (2.5 GT/s)	19000	
Base Tx Test (Workshop) (5.0 GT/s)	29000	
Base Tx Test - Workshop Mode Test (16.0 GT/s)	49000	
Base Tx Test - Workshop Mode Test (32.0 GT/s)	59000	
Base Tx Test - Workshop Mode Test (8.0 GT/s)	39000	
Reference Clock, Absolute Crossing Point Voltage	14008	This test verifies that the absolute crossing point voltage of the reference clock single-ended waveforms is within the allowed range.
Reference Clock, Absolute Max Input Voltage	14014	This test verifies that the absolute maximum input voltage of the reference clock is within the allowed range.
Reference Clock, Absolute Min Input Voltage	14016	This test verifies that the absolute minimum input voltage of the reference clock is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Reference Clock, Average Clock Period	14004	The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100Hz. A requirement of +/- 300 PPM applies to systems that do NOT employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM.
Reference Clock, Average Clock Period (32.0GT/s)	54004	The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100Hz. A requirement of +/- 300 PPM applies to systems that do NOT employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM. This test is applicable for devices that support 32.0GT/s speed.
Reference Clock, Average Clock Period (32.0GT/s, SRIS)	54005	The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100Hz. A requirement of +/- 300 PPM applies to systems that do NOT employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM. This test is applicable for devices that support 32.0GT/s speed with SRIS mode.
Reference Clock, Differential Input High Voltage	14006	This test verifies that the high voltage of the reference clock differential waveform is greater than the minimum allowed value.
Reference Clock, Differential Input Low Voltage	14007	This test verifies that the low voltage of the reference clock differential waveform is greater than the maximum allowed value.
Reference Clock, Duty Cycle	14005	This test verifies that the duty cycle of the reference clock differential waveform is within the allowed range.
Reference Clock, Falling Edge Rate	14003	This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Reference Clock, RMS Jitter (Common Clk) (16.0 GT/s)	44011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (2.5 GT/s)	14011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (32.0 GT/s)	54011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (5.0 GT/s)	24011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)	34011	This test verifies that the measured RMS jitter, TREFCLK-RMS, is less than the maximum allowed value.
Reference Clock, Rise-Fall Matching	14018	This test verifies that the rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching is within the allowed range.
Reference Clock, Rising Edge Rate	14002	This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.
Reference Clock, Variation of VCross	14010	This test verifies that the variation of VCross over all rising clock edges is within the allowed range.
Tx, AC common mode voltage - 1.25GHz (LPF) (2.5 GT/s)	11026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 16GHz (LPF) (32.0 GT/s)	51026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 2.5GHz (LPF) (5.0 GT/s)	21026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (16.0 GT/s)	41027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (32.0 GT/s)	51027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (5.0 GT/s)	21027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 30kHz to 500MHz (BPF) (8.0 GT/s)	31027	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-AC-CM-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 4GHz (LPF) (8.0 GT/s)	31026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 8GHz (LPF) (16.0 GT/s)	41026	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (VTX-AC-CM-PP) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, Absolute delta of DC common mode voltage between D+ and D- (16.0 GT/s)	41028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (2.5 GT/s)	11028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (32.0 GT/s)	51028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Absolute delta of DC common mode voltage between D+ and D- (5.0 GT/s)	21028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (8.0 GT/s)	31028	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (16.0 GT/s)	41029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (2.5 GT/s)	11029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (32.0 GT/s)	51029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (5.0 GT/s)	21029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (8.0 GT/s)	31029	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE-IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, DC common mode voltage (16.0 GT/s)	41025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (2.5 GT/s)	11025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (32.0 GT/s)	51025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (5.0 GT/s)	21025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (8.0 GT/s)	31025	This test verify the DC common mode, VTX-DC-CM is within the allowed limit as specified in the PCI Express Base Specification.
Tx, Data dependent jitter (16.0 GT/s)	41016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (2.5 GT/s)	11016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (32.0 GT/s)	51016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (5.0 GT/s)	21016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (8.0 GT/s)	31016	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, De-emphasis Preset #0 (16.0 GT/s)	41100	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #0 (32.0 GT/s)	51100	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #0 (8.0 GT/s)	31100	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, De-emphasis Preset #1 (16.0 GT/s)	41101	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (32.0 GT/s)	51101	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (8.0 GT/s)	31101	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #10 (16.0 GT/s)	41111	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #10 (32.0 GT/s)	51111	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #10 (8.0 GT/s)	31111	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #2 (16.0 GT/s)	41102	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #2 (32.0 GT/s)	51102	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #2 (8.0 GT/s)	31102	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #3 (16.0 GT/s)	41103	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, De-emphasis Preset #3 (32.0 GT/s)	51103	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #3 (8.0 GT/s)	31103	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (16.0 GT/s)	41107	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (32.0 GT/s)	51107	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (8.0 GT/s)	31107	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (16.0 GT/s)	41109	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (32.0 GT/s)	51109	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (8.0 GT/s)	31109	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Deemphasized Voltage Ratio -3.5dB (2.5 GT/s)	11001	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. This measurement is for de-emphasis level settings of -3.5dB.
Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)	21001	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. This measurement is for de-emphasis level settings of -3.5dB.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)	21002	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. This measurement is for de-emphasis level settings of -6dB.
Tx, Deterministic DjDD uncorrelated PWJ (16.0 GT/s)	41015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (32.0 GT/s)	51015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (5.0 GT/s)	21015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s)	31015	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (16.0 GT/s)	41010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (2.5 GT/s)	11010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (32.0 GT/s)	51010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (5.0 GT/s)	21010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (8.0 GT/s)	31010	This test verifies that the full swing Tx voltage with no equalization VTX-DIFF-PP is within the allowed range.
Tx, Min swing during EIEOS for full swing (16.0 GT/s)	41019	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for full swing (32.0 GT/s)	51019	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for full swing (8.0 GT/s)	31019	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (16.0 GT/s, Low Power)	41020	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Min swing during EIEOS for reduced swing (32.0 GT/s, Low Power)	51020	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (8.0 GT/s, Low Power)	31020	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.
Tx, Preshoot Preset #5 (16.0 GT/s)	41104	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #5 (32.0 GT/s)	51104	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #5 (8.0 GT/s)	31104	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #6 (16.0 GT/s)	41105	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #6 (32.0 GT/s)	51105	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #6 (8.0 GT/s)	31105	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #7 (16.0 GT/s)	41106	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #7 (32.0 GT/s)	51106	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #7 (8.0 GT/s)	31106	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Preshoot Preset #8 (16.0 GT/s)	41108	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #8 (32.0 GT/s)	51108	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #8 (8.0 GT/s)	31108	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #9 (16.0 GT/s)	41110	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #9 (32.0 GT/s)	51110	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #9 (8.0 GT/s)	31110	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Pseudo package loss (16.0 GT/s)	41018	This test verifies that the maximum pseudo package loss, ps21TX is within the allowed range.
Tx, Pseudo package loss (32.0 GT/s)	51018	This test verifies that the maximum pseudo package loss, ps21TX is within the allowed range.
Tx, Pseudo package loss (8.0 GT/s)	31018	This test verifies that the maximum pseudo package loss, ps21TX is within the allowed range.
Tx, Random jitter (16.0 GT/s)	41017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (32.0 GT/s)	51017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (5.0 GT/s)	21017	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (8.0 GT/s)	31017	This test verifies that the random jitter, it is informative only.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Reduced swing Tx voltage with no TxEQ (16.0 GT/s, Low Power)	41011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (2.5 GT/s, Low Power)	11011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (32.0 GT/s, Low Power)	51011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (5.0 GT/s, Low Power)	21011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (8.0 GT/s, Low Power)	31011	This test verifies that the reduced swing Tx output voltage with no equalization VTX-DIFF-PP-LOW is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 5.0 16.0GT/s)	41024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 5.0 2.5GT/s)	11024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 5.0 32.0GT/s)	51024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 5.0 5.0GT/s)	21024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 5.0 8.0GT/s)	31024	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Modulation Frequency (PCIE 5.0 16.0GT/s)	41021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 5.0 2.5GT/s)	11021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 5.0 32.0GT/s)	51021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 5.0 5.0GT/s)	21021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 5.0 8.0GT/s)	31021	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Peak Deviation (Max) (PCIE 5.0 16.0GT/s)	41022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 5.0 2.5GT/s)	11022	This test verifies that the SSC maximum deviation within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, SSC Peak Deviation (Max) (PCIE 5.0 32.0GT/s)	51022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 5.0 5.0GT/s)	21022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 5.0 8.0GT/s)	31022	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 16.0GT/s)	41023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 2.5GT/s)	11023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 32.0GT/s)	51023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 5.0GT/s)	21023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 5.0 8.0GT/s)	31023	This test verifies that the SSC minimum deviation within the allowed range.
Tx, Total uncorrelated PWJ (16.0 GT/s)	41014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (32.0 GT/s)	51014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (5.0 GT/s)	21014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (8.0 GT/s)	31014	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Uncorrelated deterministic jitter (16.0 GT/s)	41013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (2.5 GT/s)	11013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (32.0 GT/s)	51013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (5.0 GT/s)	21013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (8.0 GT/s)	31013	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Uncorrelated total jitter (16.0 GT/s)	41012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (2.5 GT/s)	11012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (32.0 GT/s)	51012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (5.0 GT/s)	21012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (8.0 GT/s)	31012	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Unit interval (16.0 GT/s)	41000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification.
Tx, Unit interval (2.5 GT/s)	11000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 4-19 of the PCI Express Base Specification.
Tx, Unit interval (32.0 GT/s)	51000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification.
Tx, Unit interval (5.0 GT/s)	21000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 4-19 of the PCI Express Base Specification.
Tx, Unit interval (8.0 GT/s)	31000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 8-6 of the PCI Express Base Specification.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 6 Instrument Names

Instrument Name	Description
Infiniium	Infiniium

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